Application Note: SY6507

Half-Bridge Inverter for Inductive Coupling Wireless Power Transfer

General Description

The SY6507 is designed for WPC application. It integrates a mid-frequency half-bridge N-MOSFET inverter with extremely low $R_{DS(ON)}$ to achieve high transfer efficiency. It follows the switching control signal derived from the upstream device. If the over load happens, the SY6507 will trigger OCP and the STAT pin will be pulled low to indicate the fault condition to the host. EN control is available to turn off the chip. Freewheeling conduction mode is active for OCP and EN off control.

Features

- 4V to 22V Input Voltage Range
- Low $R_{DS(ON)}$ for Integrated N-channel MOSFET
- Acceptable WPC Switching Frequency Range: 80kHz ~ 300kHz
- Enhanced Acceptable Switching Frequency up to 1MHz
- OCP with Freewheeling Conduction Mode
- EN Control with Freewheeling Conduction Mode

Ordering Information

SY6507 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY6507TCC	QFN2×3-12	

Applications

- Smart Phones, Tablets, and Other Handhelds
- Custom Wireless Power Applications

Typical Application

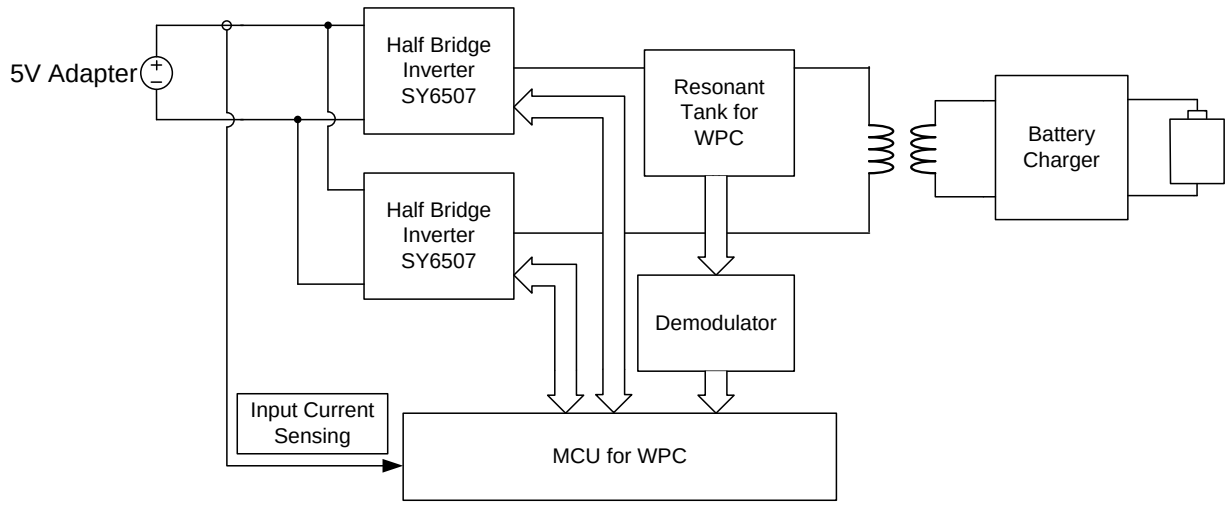


Figure1. Schematic Diagram

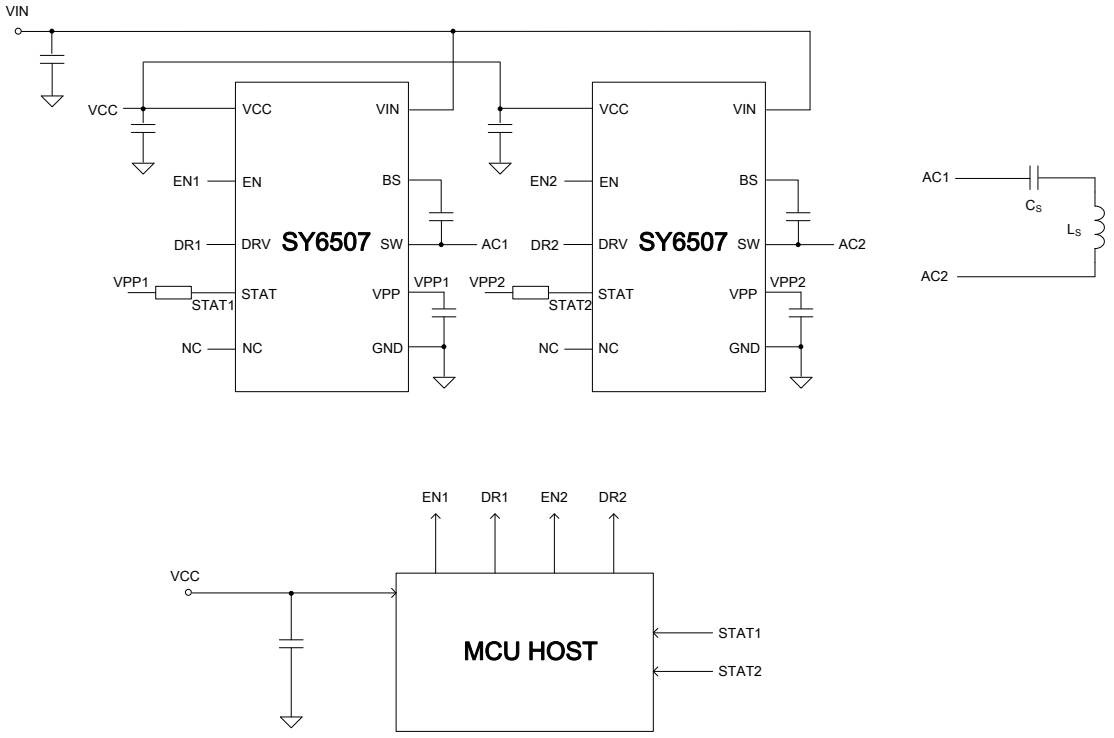


Figure2. Typical Application (For Full Bridge Application)

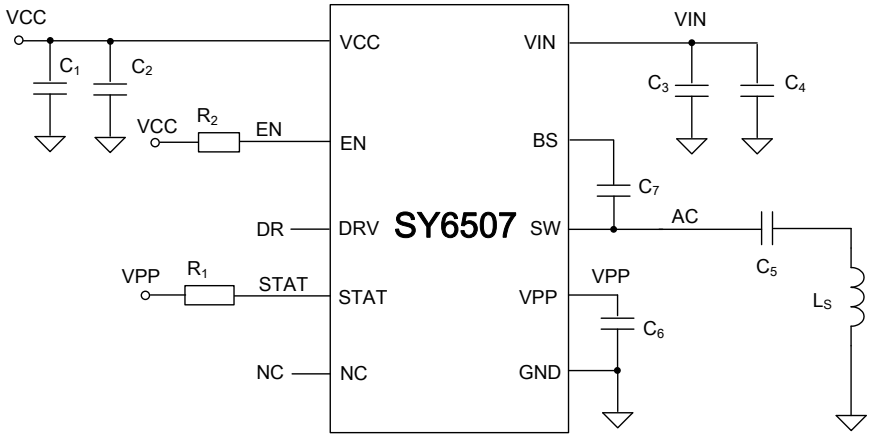
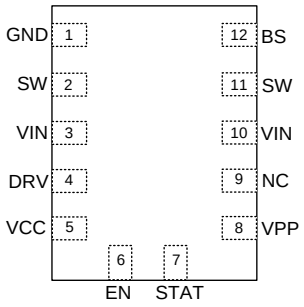


Figure3. Typical Application (For Half Bridge Application)

Pinout (Top View)



(QFN2×3-12**)**

Top Mark: BND*xyz* (device code: BND, ***x=year code, y=week code, z= lot number code)***

Name	Number	Description
GND	1	Ground pin.
SW	2,11	Half bridge inverter switching node pin.
VIN	3,10	BUS voltage input pin. Decouple this pin to ground with at least a 10μF MLCC capacitor.
DRV	4	PWM signal input pin.
VCC	5	The driver and control circuits power supply pin. Decouple this pin to GND with at least a 1μF MLCC capacitor.
EN	6	Enable control input. Pull high to enable the half-bridge inverter.
STAT	7	Fault indication signal. Pull low to indicate fault. Connect this pin to VPP with a 10kΩ resistor.
VPP	8	Bias output pin. Connect this pin to ground with a 1μF MLCC capacitor for internal stable LDO power supply.
NC	9	NC. Leave it floating.
BS	12	High side FET driver boot-strap pin. Connect at least a 100nF MLCC capacitor between this pin and SW pin.

Block Diagram

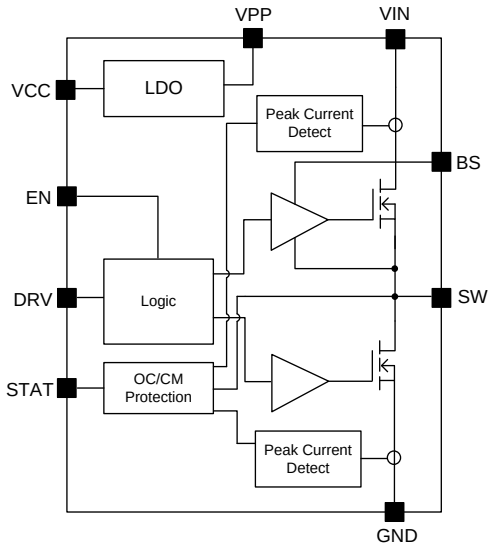


Figure4. Block Diagram

Absolute Maximum Ratings (Note1)

VIN, SW, EN, VCC (Note2) ---------- -0.3V to 25V
BS-SW, DRV, VPP, STAT ---------- -0.3 V to 4V
Power Dissipation, P_D @ T_A = 25℃, QFN2×3-12 ---------- 1.2W
Package Thermal Resistance (Note3)
Θ_{JA} ---------- 84℃/W
Θ_{JC} ---------- 52℃/W
Junction Temperature Range ---------- -40℃ to 150℃
Lead Temperature (Soldering, 10 sec.) ---------- 260℃
Storage Temperature Range ---------- -65℃ to 150℃

Recommended Operating Conditions (Note4)

VIN, SW, EN, VCC ---------- 4V to 22V
BS-SW, DRV, VPP, STAT ---------- 0 V to 3.3V
Junction Temperature Range ---------- -40℃ to 125℃
Ambient Temperature Range ---------- -40℃ to 85℃

Electrical Characteristics

(V_{IN}=12V, V_{CC}=5V, T_A= 25℃, unless otherwise specified)

Symbol Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Supply Input						
BUS Voltage Range	V_{IN}				22	V
Quiescent Current	I_Q	EN=0, T_A=25℃			6	μA
V_{CC} Voltage Range	V_{CC}		3.0		22	V
V_{CC} Under Voltage Lockout Threshold	V_{CCUVLO}	V_{CC} rising and measured from V_{CC} to GND	2.6	2.8	3.0	V
V_{CC} Under Voltage Lockout Hysteresis	ΔV_{CCUVLO}	Measured from V_{CC} to GND, T_A=25℃		120		mV
Bias Output Voltage	VPP	V_{CC}=5V	3.1	3.3	3.5	V
EN						
High Level Threshold	V_H				1.5	V
Low Level Threshold	V_L		0.5			V
DRV						
DRV Frequency Range	F_{DRV}	Follow external PWM signal and have the ability from 80kHz to 1MHz	80		1000	kHz
High Level Threshold	V_{DRVH}				2.6	V
Low Level Threshold	V_{DRVL}		0.8			V
MOSFET						
Top NFET on Resistance of Half bridge	$R_{DS(ON)\_TOP}$	T_A=25℃		40		mΩ
Bottom NFET on Resistance of Half Bridge	$R_{DS(ON)\_BOT}$	T_A=25℃		40		mΩ
Current Protect						
High Side Peak Current Threshold	I_{PK_HS}	T_A=25℃	7	8	9	A
Low Side Peak Current Threshold	I_{PK_LS}	T_A=25℃	7	8	9	A
Internal Timer						
Protection Auto Recovery Time	t_{REC}		90	130	170	ms
Low-side Switch Keeps on Time	t_{LON}	Before all the switches turn off		1		ms
Thermal Protect						
Thermal Shutdown Temperature	T_{SD}			150		℃
Thermal Recovery Hysteresis	T_{HYS}			15		℃

Note1: Stresses beyond the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note2: Because of the parasitic capacitance and inductance of the internal MOSFETs, a voltage spike will be produced at SW pin in the switching moment. To avoid potential damage on internal MOSFETs, the voltage spike should be no higher than 25V.

Note3: Θ_{JA} is measured in the natural convection at T_A= 25℃ on a high effective four-layer thermal conductivity test board of JEDEC 51-2 thermal measurement standard.

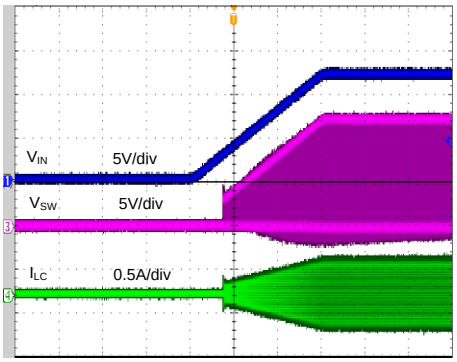
Note4: The device is not guarantee to function outside its operating conditions.

Typical Performance Characteristic

(For half bridge application)

Startup from V_{IN}

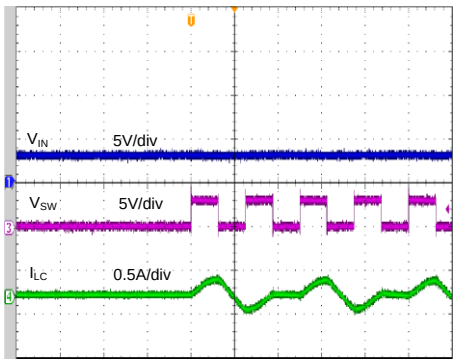
(V_{IN}=V_{CC}=12V)



Time (4ms/div)

Startup from V_{IN}(1)

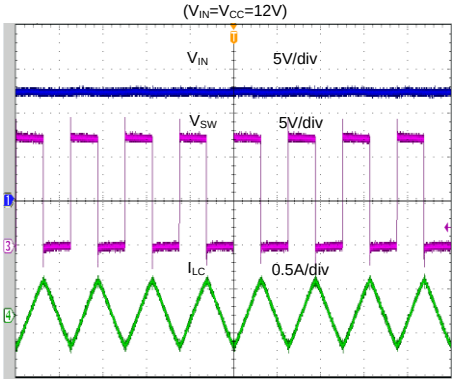
(V_{IN}=V_{CC}=12V)



Time (4μs/div)

Startup from V_{IN}(2)

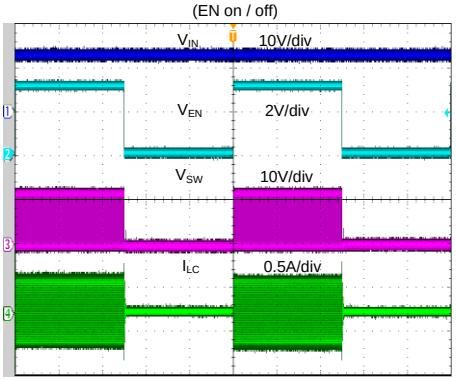
(V_{IN}=V_{CC}=12V)



Time (4μs/div)

EN Enable Control Test

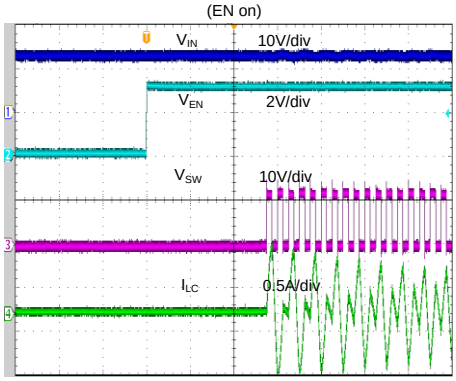
(EN on / off)



Time (20ms/div)

EN Enable Control Test

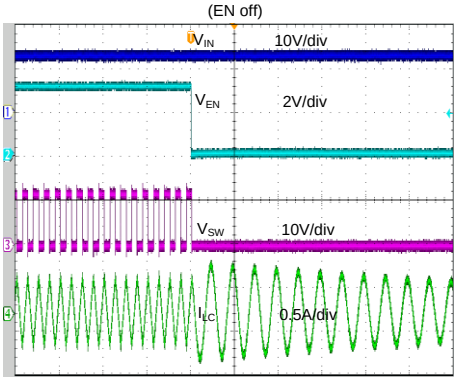
(EN on)



Time (20μs/div)

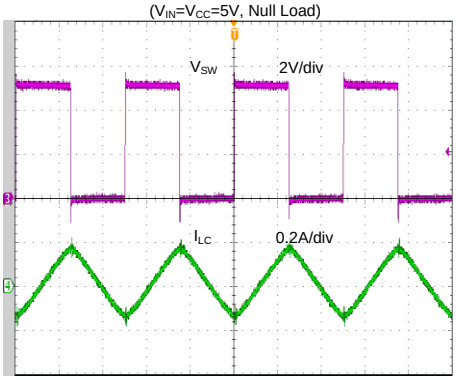
EN Enable Control Test

(EN off)



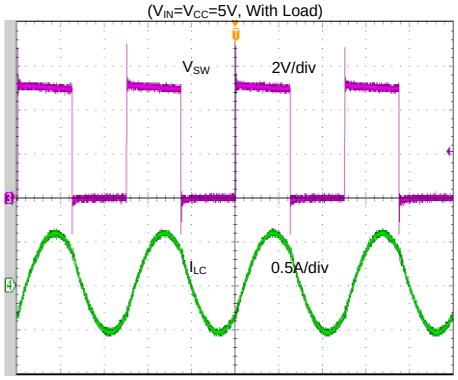
Time (20μs/div)

Normal Working
(V_{IN}=V_{CC}=5V, Null Load)



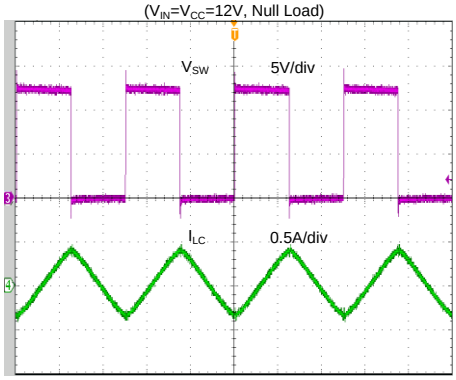
Time (2μs/div)

Normal Working
(V_{IN}=V_{CC}=5V, With Load)



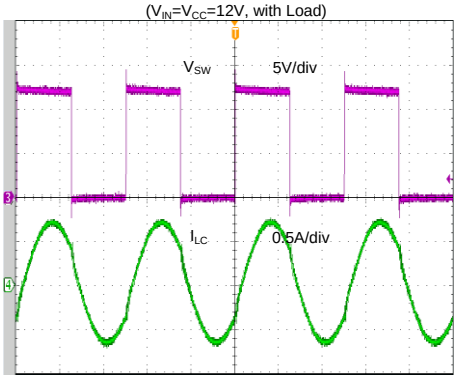
Time (2μs/div)

Normal Working
(V_{IN}=V_{CC}=12V, Null Load)



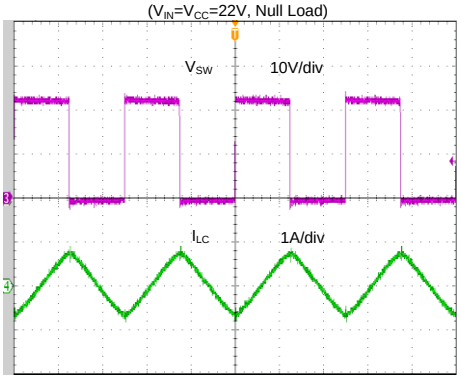
Time (2μs/div)

Normal Working
(V_{IN}=V_{CC}=12V, with Load)



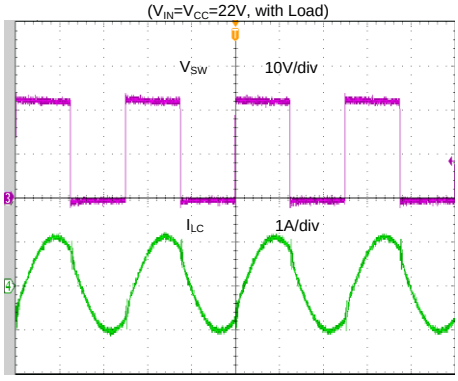
Time (2μs/div)

Normal Working
(V_{IN}=V_{CC}=22V, Null Load)



Time (2μs/div)

Normal Working
(V_{IN}=V_{CC}=22V, with Load)



Time (2μs/div)

Operation Principle Description

PWM input

The SY6507 has single PWM input pin and generates the complementary driving signal for the integrated half-bridge switches. Enough dead time is achieved between the driving signal of high-side MOSFET and low-side MOSFET to prevent from shoot through.

Tri-state Driving Control

If DRV pin is high level, high-side switch will turn on and low-side switch will turn off. If DRV pin is low level, high-side switch will turn off and low-side switch will turn on. If DRV pin is floating, both of them will turn off. However, before the switches turn off, the low-side switch would keep on for t_{LON} to let the resonant current drop to zero.

Over Current Protection

When the SY6507 detects the inverter's high-side or low-side switch peak current exceeding a pre-determined threshold, the low-side switch would be latched on for t_{LON} as the freewheeling time and the STAT pin would be pulled low till to the recovery. The recovery period of OCP is t_{REC}.

Capacitive Mode Protection

The SY6507 has capacitive mode protection. When the SY6507 detects that the switching node voltage is positive at low-side switch turn-on moment, capacitive mode protection would be triggered. The protection control logic is same as OCP.

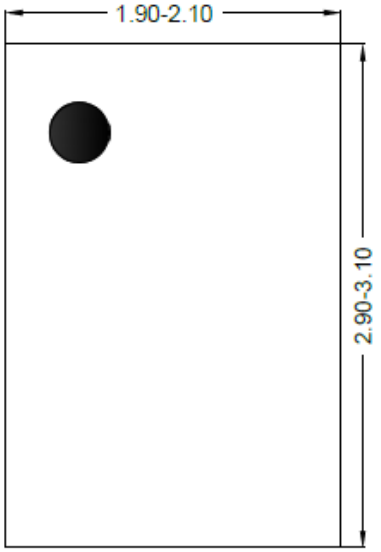
Thermal Shutdown Protection

When the junction temperature exceeds 150℃, the SY6507 will shut down and both of switches will turn off. Before the switches turn off, the low-side switch would keep on for t_{LON} as the freewheeling time. Once the temperature drops below 135℃ after t_{LON}, the SY6507 can be enable again.

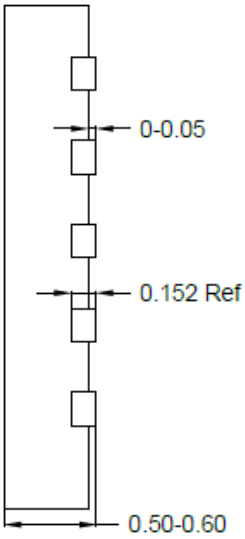
EN Control

The SY6507 has EN control function. Pull EN high to enable the chip working, pull EN low to disable the chip working. Before the chip enters into idle mode if EN is pulled low, the t_{LON} freewheeling conduction must be finished.

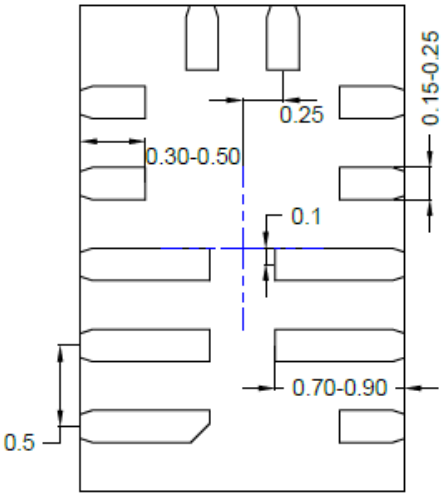
QFN2×3-12 Package Outline & PCB Layout



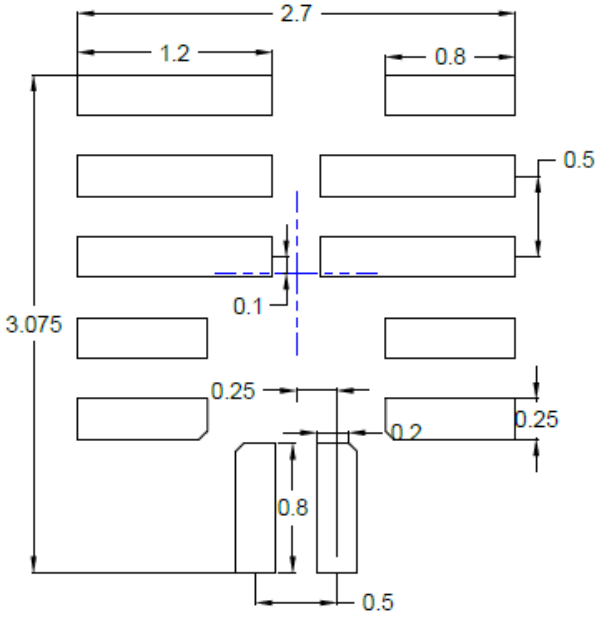
Top View



Side View



Bottom View

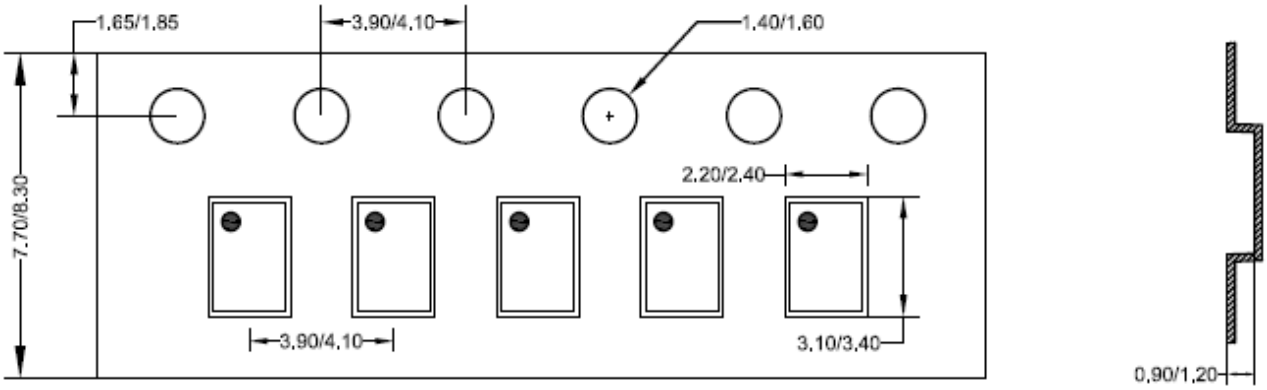


PCB Layout (Recommended)

Notes: 1. All dimensions in millimeter and exclude mold flash & metal burr;
2. The center of PCB diagram refers to chip center.

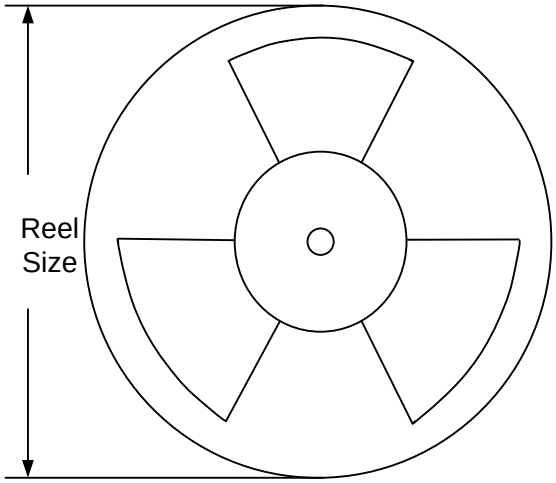
Taping & Reel Specification

1. QFN2×3-12 Taping Orientation



Feeding Direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN2×3	8	4	7"	400	160	3000

3. Others: NA

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