SY22661

Single Stage Flyback and PFC Controller with Primary Side Control for LED Lighting and integrated 0~10V transformer driver

General Description

The SY22661 is a single stage Flyback and PFC controller targeting at LED isolate dimming applications, which can achieve up to 5% dimming level and high precision for all loading range. It is a primary side controller without applying any secondary feedback circuit for low cost, and drives the converter in the quasi-resonant mode to achieve higher efficiency. It keeps the converter in constant on time operation to achieve high power factor. It integrates 0~10V transformer driver and simply the peripheral.

Ordering Information

SY22661□(□□□)

- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY22661FAC	SO8	----

Features

- Primary Side Control Eliminates the Opto-coupler.
- Dimming Range from 5% to100%
- 0~10V Dimming is Driver by Transformer.
- Valley Turn-on of the Primary MOSFET to Achieve Low Switching Losses
- High Voltage Start-up Function , Start-up Time<300ms
- Low Standby Power<500mW
- Reliable Short LED and Open LED Protection
- Power Factor >0.90
- Internal High Current MOSFET Driver: 0.19A Sourcing and 0.6A Sinking
- Compact Package: SO8

Applications

- LED Dimming

Typical Applications

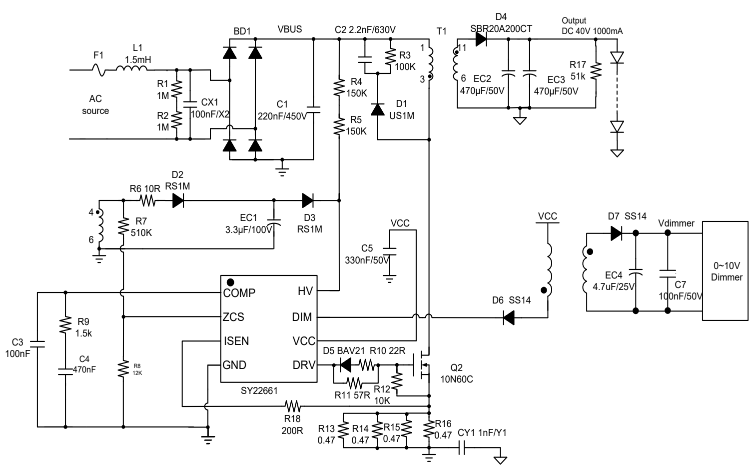


Figure.1 Typical application

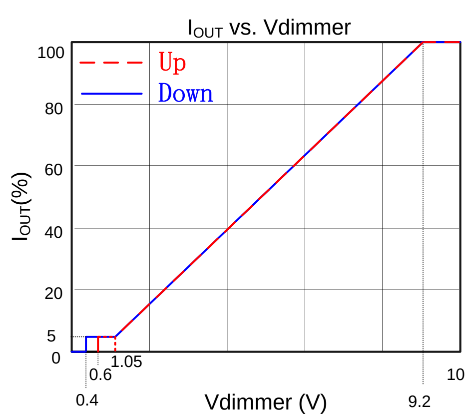
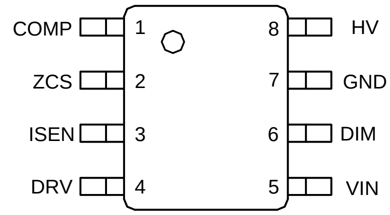


Figure.2 Iout vs. Vdimmer

Pinout (top view)



（SO8）

Top Mark: CTN *xyz* (device code: CTN, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin number	Pin Description
COMP	1	Loop compensation pin. Connect a RC network across this pin and ground to stabilize the control loop.
ZCS	2	Inductor current zero-crossing detection pin. This pin receives the auxiliary winding voltage by a resister divider and detects the inductor current zero crossing point. This pin also provides over voltage protection, line regulation modification function and CV detection simultaneously. If the voltage on this pin is above $V_{ZCS,OVP}$, the IC would enter over voltage protection mode. Good line regulation can be achieved by adjusting the upper resistor of the divider.
ISEN	3	Current sense pin. Connect this pin to the source of the primary switch. Connect the sense resistor across the source of the primary switch and the GND pin. (current sense resister R_S: $R_S = k\frac{V_{REF}\times N_{PS}}{I_{OUT}}$, k=0.167)
DRV	4	Gate driver pin. Connect this pin to the gate of primary MOSFET.
VIN	5	Power supply pin. 330nF ceramic cap is recommend between this pin to GND
DIM	6	Connect this pin to primary side of Dim transformer to achieve dimming signal.
GND	7	Ground pin
HV	8	High voltage Start-up pin.

Block Diagram

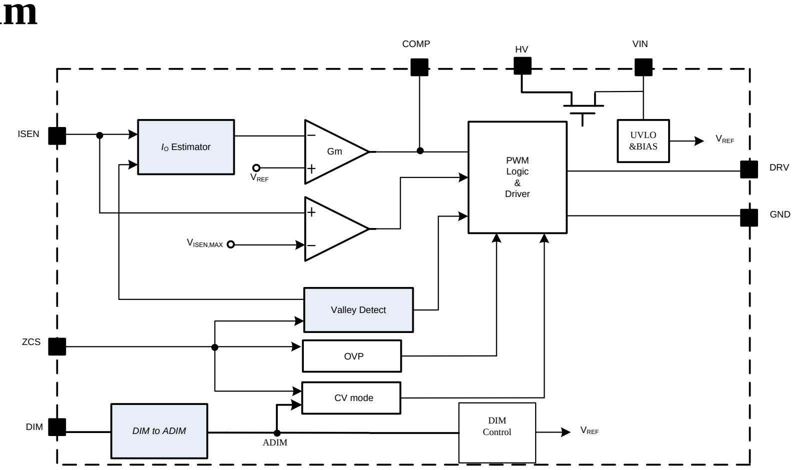


Figure.3 Block Diagram

Absolute Maximum Ratings (Note 1)

VIN, DRV -- -0.3V~18V
Supply current I_{VIN} -- 7mA
ZCS--- -0.3V~1.8V
DIM -- -0.3V~40V
ISEN, COMP --- -0.3~ 3.6V
HV---700V
Power Dissipation, @ T_A = 25°C SO8 -- 1.1W
Package Thermal Resistance (Note 2)
SO8, θ JA ---88°C/W
SO8, θ JC ---45°C/W
Junction Temperature Range -- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) -- 260°C
Storage Temperature Range -- -65°C to 150°C

Recommended Operating Conditions (Note 3)

Junction Temperature Range -- -40°C to 125°C

Electrical Characteristics

(V_{IN} = 12V (Note 3), T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
VIN Turn-on Threshold	V_{VIN_ON}		10.6	11.8	13	V
VIN Turn-off Threshold	V_{VIN_OFF}		6.6	7.3	8.2	V
VIN OVP Voltage	V_{VIN_OVP}			17		V
Start-up Current	I_{ST}	$V_{VIN}<V_{VIN\_OFF}$	130	180	230	µA
Discharge Current in OVP Mode	I_{VIN_OVP}	V_{VIN}=12V (Note 4)	5	7	10	mA
Error Amplifier Section						
Internal Reference Voltage	V_{REF}		275	280	285	mV
Current Sense Section						
Current Limit Reference Voltage	V_{ISEN_MAX}		0.4	0.45	0.5	V
ZCS Pin Section						
ZCS Pin OVP Voltage Threshold	V_{ZCS_OVP}		1.43	1.5	1.57	V
Gate Driver Section						
Gate Driver Voltage	V_{Gate}		9.5	12	14.5	V
Maximum Source Current	I_{SOURCE}		150	200	250	mA
Minimum Sink Current	I_{SINK}		500	650	800	mA
Max ON Time	T_{ON_MAX}	V_{COMP}=2.7V		22		µs
Min ON Time	T_{ON_MIN}			450		ns
Max OFF Time	T_{OFF_MAX}			50		µs
Min OFF Time	T_{OFF_MIN}			1.5		µs
Maximum Switching Frequency	F_{MAX}			120		kHz
DIM function Section						
Peak Current	I_pk		18	23	28	mA
HV Function Section						
BV	V_BV		700			V
Thermal Section						
Thermal Shut down Temperature	T_{SD}			150		°C

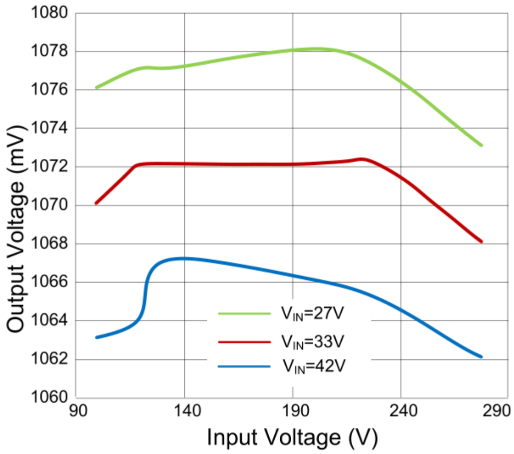
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: Increase VIN pin voltage gradually higher than V_{VIN_ON} voltage then turn down to 12V.

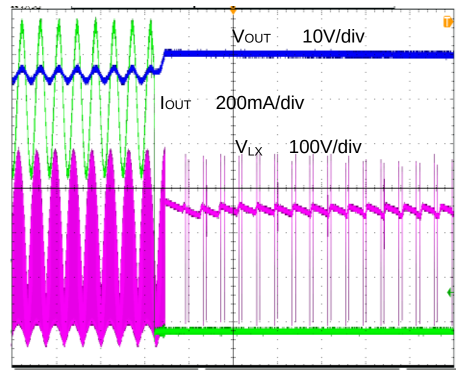
Note 4: Increase VIN pin voltage gradually higher than V_{VIN_OVP} voltage then turn down to 12V

Typical Performance Characteristic



Open LED Protection

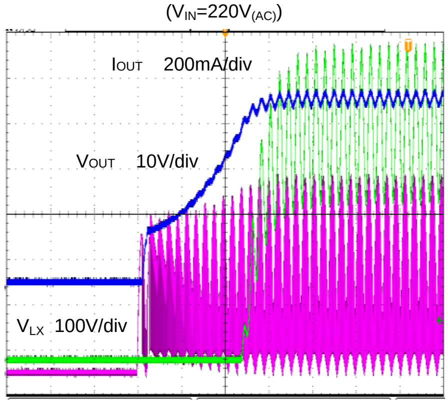
(V_{IN}=220$V_{(AC)}$)



Time (20ms/div)

Startup

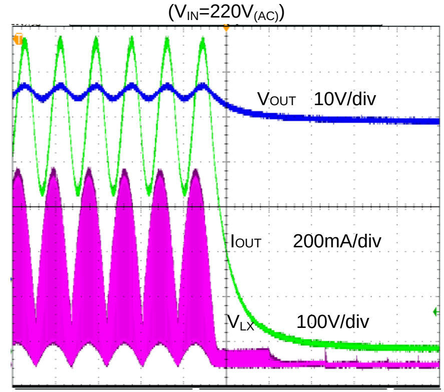
(V_{IN}=220$V_{(AC)}$)



Time (40ms/div)

Shutdown

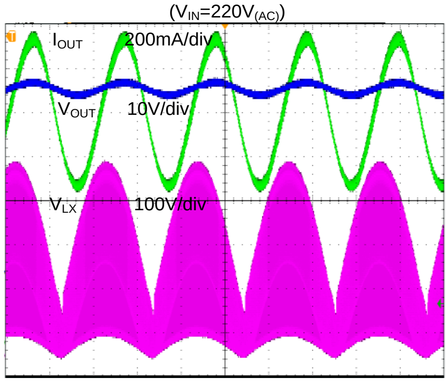
(V_{IN}=220$V_{(AC)}$)



Time (10ms/div)

Steady States

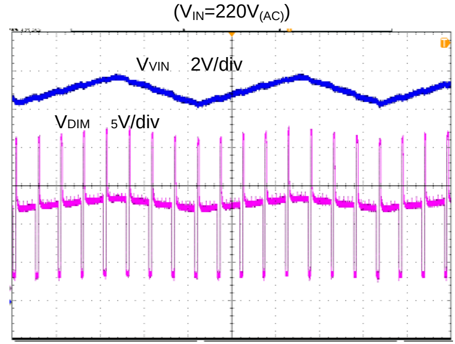
(V_{IN}=220$V_{(AC)}$)



Time (4ms/div)

Steady State

(V_{IN}=220$V_{(AC)}$)



Time (40ms/div)

Operation

The SY22661 is a single stage Flyback and PFC controller targeting at LED lighting applications with isolate dimming function.

SY22661 provides primary side control to eliminate the opto-couplers and the secondary feedback circuits, which can decrease the BOM cost of the system design.

High power factor is achieved by constant on time operation mode, with which both the control scheme and the circuit structure are simple.

In order to reduce the switching loss and improve EMI performance, Quasi-Resonant switching mode is applied. The maximum switching frequency is limited at 120KHz to reduce switching losses and improve EMI performance when the converter is operated at light load condition.

In order to meet isolate dimming applications， 0~10V transformer driver is integrated, the dimming circuit is simple.

SY22661 provides reliable protections such as Short Circuit Protection (SCP), Open LED Protection (OLP), Over Temperature Protection (OTP), etc.

SY22661 is available with SO8 package.

Applications Information

HV start up

After AC supply or DC BUS is powered on, the capacitor C_{VIN} between VIN and GND pin is charged up by BUS voltage through a start-up resistor R_{ST} and HV inner MOS. Once V_{VIN} rises up to V_{VIN_ON}, the internal blocks start to work. V_{VIN} will be pulled down by internal consumption of IC until the auxiliary winding of transformer could supply enough energy to HV to maintain V_{VIN} above V_{VIN_OFF}.

The whole start up procedure is divided into four sections shown in Fig.4. t_{STC} is the C_{VIN} charged up section, and t_{STO} is the output voltage build-up section. The start-up time t_{ST} is composed of t_{STC} and t_{STO}, and usually t_{STO} is much smaller than t_{STC}.

t_{STO} is fast start-up stage, which will help to create output voltage quickly. After t_{STO}, if V_{DIMMER} is less than V_{DIMMER_ON}, IC enters into CV mode. When V_{DIMMER} is larger than V_{DIMMER_ON}, IC works in constant on time mode.

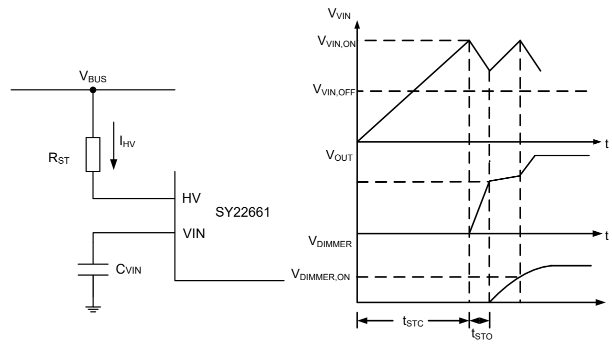


Fig.4 Start up

The start up resistor R_{ST} and C_{VIN} are designed by rules as below:

(a) Preset start-up resistor R_{ST}, make sure that the current through R_{ST} is larger than 0.35mA and smaller than 1mA.

$$\frac{V_{BUS}}{1mA} < R_{ST} < \frac{V_{BUS}}{0.35mA} \qquad (1)$$

Where V_{BUS} is the BUS line voltage

(b) Select C_{VIN} to obtain an ideal start up time $t_{ST,}$ and ensure the output voltage is built up at one time.

$$C_{VIN} = \frac{(\frac{V_{BUS}}{R_{ST}} - I_{ST}) \times t_{ST}}{V_{VIN\_ON}} \qquad (2)$$

Usually, 330nF-470nF/50V ceramic cap is recommend

(d) If the C_{VIN} is not big enough to build up the output voltage at one time, decrease R_{ST}, go back to step (a) and redo such design flow until the ideal start up procedure is obtained.

HV supply logic

In initial state, V_{VIN} =0, after AC supply or DC BUS is powered on, inner MOS of HV works, C_{VIN} is charged by I_{HV}, when V_{VIN} rise to V_{VIN_ON} ,inner MOS of HV turn off. When V_{VIN} is discharged to V_{VIN_ON} -1.5V, inner MOS of HV will works against, and also turn off when V_{VIN} rise to V_{VIN_ON}.

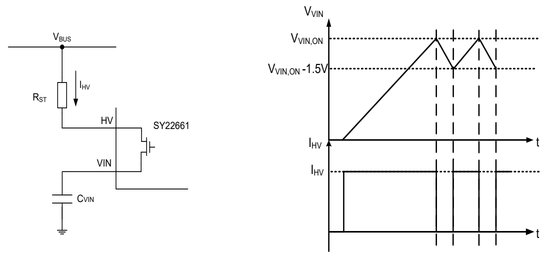


Fig.5 HV supply logic

Internal pre-charge design for quick start up

See as Fig.6, In P3, V_{COMP} is pre-charged by internal current source until it is over the initial voltage V_{COMP_IC}. V_{COMP_IC} can be programmed by R_{COMP}. Such design is meant to reduce the start-up time.

The voltage pre-charged V_{COMP_IC} in start-up procedure can be programmed by R_{COMP}:

$$V_{COMP\_IC} = 1.2V - 300\mu A \times R_{COMP} \quad (3)$$

Where V_{COMP_IC} is the pre-charged voltage of COMP pin.

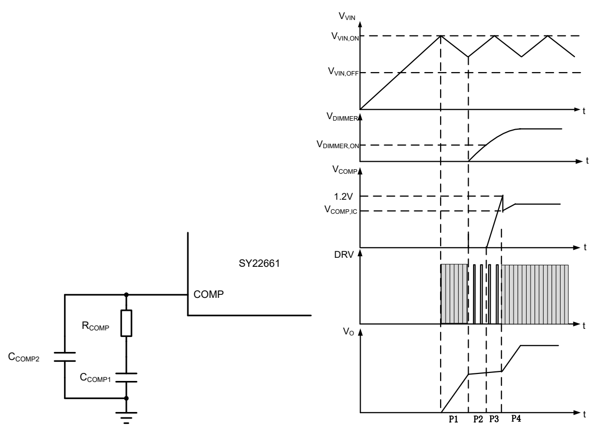


Fig.6 Pre-charge scheme in start up

Generally, a big capacitance of C_{COMP1} is necessary to achieve high power factor and stabilize the system loop (470nF~1μF is recommended).

The voltage pre-charged in start-up procedure can be programmed by R_{COMP}; On the other hand, larger R_{COMP} can provide larger phase margin for the control loop; A small ceramic capacitor is added to suppress high frequency interruption (100nF is recommended in C_{COMP2})

Shut down

After AC supply or DC BUS is powered off, the energy stored in the BUS capacitor will be discharged. When the auxiliary winding of the transformer cannot supply enough Voltage to HV pin, V_{VIN} will drop down. Once V_{VIN} is below V_{VIN_OFF}, the IC will stop working and V_{COMP} will be discharged to zero.

Primary side constant current control

Primary side control is applied to eliminate secondary feedback circuit and opto-coupler, which reduces the BOM cost. The switching waveforms are shown in Fig.7.

The output current I_{OUT} can be represented by,

$$I_{OUT} = \frac{I_{SP}}{2} \times \frac{t_{DIS}}{t_S} \quad (4)$$

Where I_{SP} is the peak current of the secondary side; t_{DIS} is the discharge time of the transformer; t_S is the switching period.

The secondary peak current is related with primary peak current, if the effect of the leakage inductor is neglected.

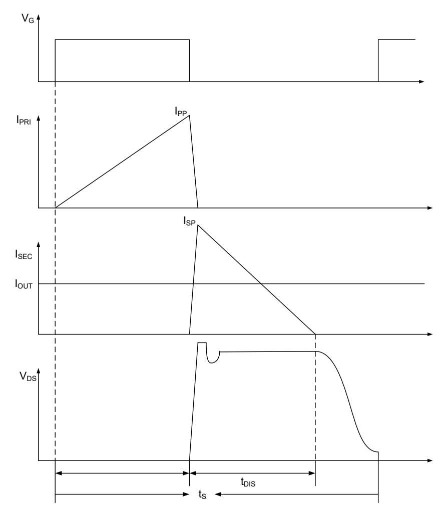


Fig.7 switching waveforms

$$I_{SP} = N_{PS} \times I_{PP} \quad (5)$$

Where N_{PS} is the turn ratio of primary to secondary of the transformer.

Thus, I_{OUT} can be represented by

$$I_{OUT} = \frac{N_{PS} \times I_{PP}}{2} \times \frac{t_{DIS}}{t_S} \quad (6)$$

The primary peak current I_{PP} and inductor current discharge time t_{DIS} can be detected by ISEN and ZCS pin, which is shown in Fig.8.These signals are processed and applied to the negative input of the gain modulator. In static state, the positive and negative inputs are equal.

$$V_{REF} = I_{PP} \times R_S \times \frac{t_{DIS}}{t_S} \times k_1 \quad (7)$$

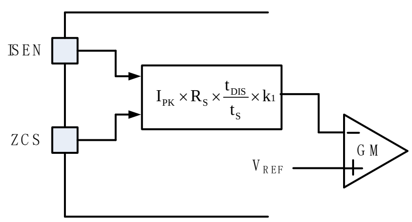


Fig.8 Output current detection diagram

Finally, the output current I_{OUT} can be represented by

$$I_{OUT} = \frac{V_{REF} \times N_{PS}}{R_S \times 2 \times k_1} \quad (8)$$

Where k_1 is the output current weight coefficient; V_{REF} is the internal reference voltage; R_S is the current sense resistor.

k_1 and V_{REF} are all internal constant parameters, I_{OUT} can be programmed by N_{PS} and R_S.

$$Rs = \frac{V_{REF} \times N_{PS}}{I_{OUT} \times 2 \times k_1} \quad (9)$$

Then

$$R_S = \frac{k \times V_{REF} \times N_{PS}}{I_{OUT}}, k = \frac{1}{2k_1} \quad (10)$$

Quasi-Resonant Operation

QR mode operation provides low turn-on switching losses for the converter.

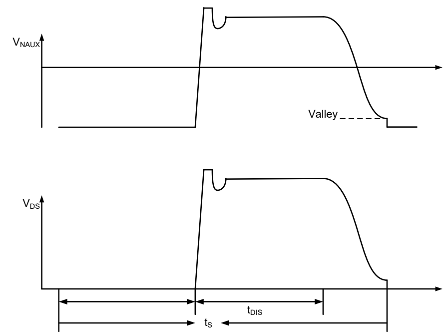


Fig.9 QR mode operation

The voltage across drain and source of the primary MOSFET is reflected by the auxiliary winding of the Flyback transformer. ZCS pin detects the voltage across the auxiliary winding by a resistor divider. When the voltage across drain and source of the primary MOSFET is at voltage valley, the MOSFET would be turned on.

CV Mode

When $V_{DIMMER} < V_{DIMMER\_OFF}$, IC still need bias power:

(1) If V_{DIMMER} voltage is greater than V_{DIMMER_ON}, IC always works at CC mode.

(2) If V_{DIMMER} voltage is lower than V_{DIMMER_OFF}, CV mode is triggered. IC works in CV mode to maintain V_{ZCS} nearby V_{ZCS_CV} (0.5V). N_P: N_{AUX} and R_{ZCS} can be adjusted to prevent LED flicker and keep bias supply enough at CV mode.

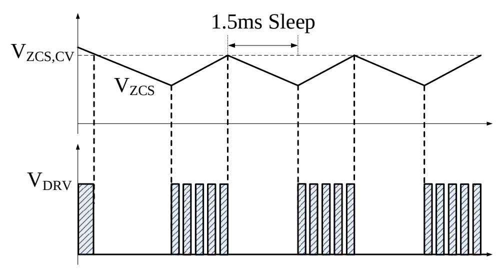


Figure.10 The working process of CV mode

In CV mode, which is shown in Fig.10.

(1) If V_{ZCS} is greater than V_{ZCS_CV} (0.5V), IC will sleep for 1.5ms.

(2) After 1.5mS sleep, if V_{ZCS} is smaller than V_{ZCS_CV}, IC will work until V_{ZCS} is greater than V_{ZCS_CV}. During this time, MOSFET turns on by QR and turns off until the ISEN voltage V_{RS} reach 50mV.

The output of CV can be calculated as below:

$$V_{OUT,CV} = 0.5V \times (\frac{R_{ZCSU} + R_{ZCSD}}{R_{ZCSD}}) \times \frac{N_S}{N_{AUX}} \quad (11)$$

Where, R_{ZCSU} is the upper resistor of ZCS pin; R_{ZCSD} is the down resistor of ZCS pin; N_S and N_{AUX} are the turns of secondary winding and auxiliary winding separately.

Dimming function

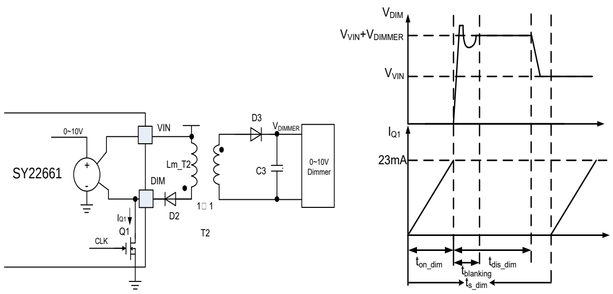


Figure.11 DIM working module

The dimming circuit is a Flyback converter. The inductor Lm_T2 store energy when Q1 turns on. Q1 works in constant peak current 23mA mode. After Q1 turning off, inductor release energy for 0~10V dimmer power supply. Simultaneously, the voltage between DIM pin and VCC pin is reflected the voltage of dimmer. (Set the turn ratio of primary to secondary of the dimming transformer is 1). It is shown in Fig.11.

$$V_{DIM} - V_{VIN} = V_{DIMMER} + (V_{D3} - V_{D2}) \quad (12)$$

In order to eliminate error between D2 and D3, the same type diode is needed in this circuit, SS14 is recommended.

In order to avoid sampling mistake, a blanking time $t_{blanking}$ is used to eliminate oscillation voltage of VDIM when Q1 turn off. So the t_{dis_dim} need to higher than $t_{blanking}$. So the inductance:

$$L_{m\_T2} > \frac{V_{DIMMER,max} \times t_{blanking}}{23mA} \quad (13)$$

Where $t_{blanking}$ is 1.5us.

If magnetic ring is used in this application, due to the u_i vary fast during low to high temperature. Normally, the inductance of magnetic ring is only half when transformer works in high temperature or low temperature （lower than -30℃）。So the magnetic ring inductance will be set as:

$$L_{m\_T2} > \frac{2 \times V_{DIMMER,max} \times t_{blanking}}{23mA} \quad (14)$$

Also, need to consider the ± 30% error of the μ_i .

Over Voltage Protection (OVP) & Open LED Protection (OLP)

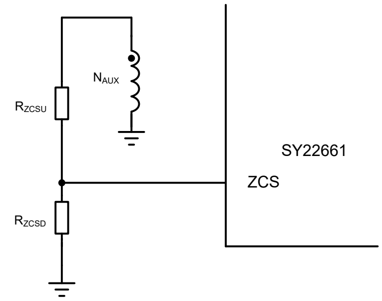


Fig.12 OVP&OLP

The output voltage is reflected by the auxiliary winding voltage of the Flyback transformer, and ZCS pin provides over voltage protection function. When the load is null or large transient happens, the output voltage will exceed the rated value. When V_{ZCS} exceeds V_{ZCS_OVP}, the over voltage protection is triggered and the IC will discharge V_{VIN} by an internal current source. Once V_{VIN} is below V_{VIN_OFF}, the IC will shut down and be charged again by HV voltage through start up resistor. If the over voltage condition still exists, the system will operate in hiccup mode.

Thus, the turns of the auxiliary winding N_{AUX} and the resistor divider is related with the OVP function.

$$\frac{V_{ZCS\_OVP}}{V_{OVP}} = \frac{N_{AUX}}{N_S} \times \frac{R_{ZCSD}}{R_{ZCSU} + R_{ZCSD}} \quad (15)$$

$$\frac{V_{VIN\_OVP}}{V_{OVP}} \geq \frac{N_{AUX}}{N_S} \quad (16)$$

Where V_{OVP} is the output over voltage specification; R_{ZCSU} and R_{ZCSD} compose the resistor divider. The turn ratio of N_S to N_{AUX} and the ratio of R_{ZCSU} to R_{ZCSD} could be induced from equation (15) and (16).

Short Circuit Protection (SCP)

When the output is shorted to ground, the output voltage is clamped to zero. The voltage of the auxiliary winding is proportional to the output winding, so valley signal cannot be detected by V_{ZCS} .Without valley detection, MOSFET cannot be turned ON until maximum off time t_{OFF_MAX} is matched. If MOSFET is turned ON by t_{OFF_MAX} 64 times continuously, IC will be shut down and enter into hiccup mode.

Line regulation modification

The IC provides line regulation improvement function by adjusting the external resistor.

Due to the sample delay of ISEN pin and other internal delay, the output current increases with the increasing of input BUS line voltage. A small compensation voltage ΔV_{ISEN_C} is added to ISEN pin during ON time to improve such performance. This ΔV_{ISEN_C} is adjusted by the upper resistor of the divider connected to ZCS pin and external resistor $R_{ISEN,C}$ on ISEN pin.

$$\Delta V_{ISEN,C}=V_{BUS}\times\frac{N_{AUX}}{N_P}\times\frac{1}{R_{ZCSU}}\times k_2\times(R_{k2}+R_{ISEN,C}) \quad (17)$$

Where R_{VSENU} is the upper resistor of the divider; k_2 is an internal constant as the modification coefficient; R_{k2} is an internal feed-forward resistor; auxiliary resistor $R_{ISEN,C}$ can be added to enhance feed-forward effects.

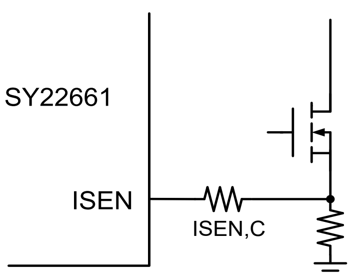


Fig.13 Feed-forward resistor

The compensation is mainly related with R_{ZCSU}, larger compensation is achieved with smaller R_{ZCSU}. Normally, R_{ZCS} ranges from 100kΩ~1MΩ.

Then R_{ZCSD} can be selected by,

$$V_{AUX\_CV}=\frac{0.5\cdot(R_{ZCSU}+R_{ZCSD})}{R_{ZCSD}}\geq 20 \quad (18)$$

12K is recommended to use in R_{ZCSD}.
R_{ZCSU} is the upper resistor of the divider; N_S and N_{AUX} are the turns of secondary winding and auxiliary winding separately.

Power Device Design

MOSFET and Diode

When the operation condition is with maximum input voltage and full load, the voltage stress of MOSFET and secondary power diode is maximized;

$$V_{MOS\_DS\_MAX}=\sqrt{2}V_{AC\_MAX}+N_{PS}\times(V_{OUT}+V_{D\_F})+\Delta V_S \quad (20)$$

$$V_{D\_R\_MAX}=\frac{\sqrt{2}V_{AC\_MAX}}{N_{PS}}+V_{OUT} \quad (21)$$

Where V_{AC_MAX} is the maximum input AC RMS voltage; N_{PS} is the turn ratio of the Flyback transformer; V_{OUT} is the rated output voltage; V_{D_F} is the forward voltage of secondary power diode; ΔV_S is the overshoot voltage clamped by RCD snubber during OFF time.

When the operation condition is with minimum input voltage and full load, the current stress of MOSFET and power diode is maximized.

$$I_{MOS\_PK\_MAX}=I_{P\_PK\_MAX} \quad (22)$$

$$I_{MOS\_RMS\_MAX}=I_{P\_RMS\_MAX} \quad (23)$$

$$I_{D\_PK\_MAX}=N_{PS}\times I_{P\_PK\_MAX} \quad (24)$$

$$I_{D\_AVG}=I_{OUT} \quad (25)$$

Where $I_{P\_PK\_MAX}$ and $I_{P\_RMS\_MAX}$ are maximum primary peak current and RMS current, which will be introduced later.

Transformer (N_{PS} and L_M)

N_{PS} is limited by the electrical stress of the power MOSFET:

$$N_{PS}\leq\frac{V_{MOS\_(BR)DS}\times 90\%-\sqrt{2}V_{AC\_MAX}-\Delta V_S}{V_{OUT}+V_{D\_F}} \quad (26)$$

Where $V_{MOS\_(BR)DS}$ is the breakdown voltage of the power MOSFET.

In Quasi-Resonant mode, each switching period cycle t_S consists of three parts: current rising time t_1, current falling time t_2 and quasi-resonant time t_3 are shown as Fig.14.

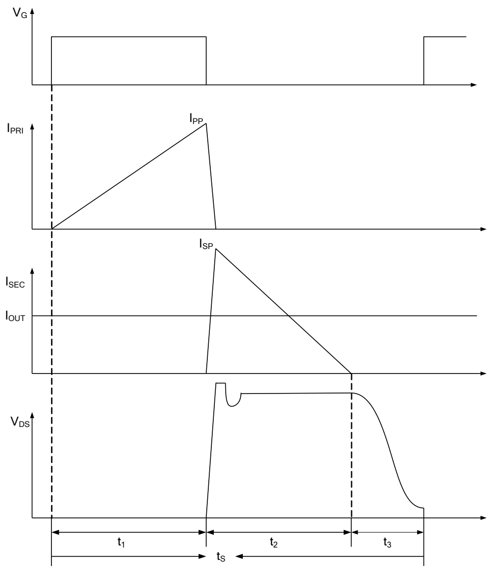


Fig.14 switching waveforms

The system operates in the constant on time mode to achieve high power factor. The ON time increases with the decreasing of input AC RMS voltage and the increasing of load. When the operation condition is with minimum input AC RMS voltage and full load, the ON time is maximized. On the other hand, when the input voltage is at the peak value, the OFF time is maximized. Thus, the minimum switching frequency f_{S_MIN} happens at the peak value of input voltage with minimum input AC RMS voltage and maximum load condition; meanwhile, the maximum peak current through MOSFET and the transformer happens.

Once the minimum frequency f_{S_MIN} is set, the inductance of the transformer could be induced. The design flow is shown as below:

(a) Select N_{PS}

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - \sqrt{2}V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \qquad (27)$$

(b) Preset minimum frequency f_{S_MIN}

(c) Compute relative t_S, t_1 (t_3 is omitted to simplify the design here)

$$t_S = \frac{1}{f_{S\_MIN}} \qquad (28)$$

$$t_1 = \frac{t_S \times N_{PS} \times (V_{OUT} + V_{D\_F})}{\sqrt{2}V_{AC\_MIN} + N_{PS} \times (V_{OUT} + V_{D\_F})} \qquad (29)$$

(d) Design inductance L_M

$$L_M = \frac{V_{AC\_MIN}^2 \times t_1^2 \times \eta}{2P_{OUT} \times t_S} \qquad (30)$$

(e) Compute t_3

$$t_3 = \pi \times \sqrt{L_M \times C_{Drain}} \qquad (31)$$

Where C_{Drain} is the parasitic capacitance at drain of MOSFET.

(f) Compute primary maximum peak current $I_{P\_PK\_MAX}$ and RMS current $I_{P\_RMS\_MAX}$ for the transformer fabrication.

$$I_{P\_PK\_MAX} = \frac{2P_{OUT} \times [\frac{L_M}{\sqrt{2}V_{AC\_MIN}} + \frac{L_M}{N_{PS} \times (V_{OUT} + V_{D\_F})}]}{L_M \times \eta} + \frac{\sqrt{4P_{OUT}^2 \times [\frac{L_M}{\sqrt{2}V_{AC\_MIN}} + \frac{L_M}{N_{PS} \times (V_{OUT} + V_{D\_F})}]^2 + 4L_M \times \eta \times P_{OUT} \times t_3}}{L_M \times \eta} \qquad (32)$$

Where η is the efficiency; P_{OUT} is rated full load power

Adjust t_1 and t_S to t_1' and t_S' considering the effect of t_3

$$t_S' = \frac{\eta \times L_M \times I_{P\_PK\_MAX}^2}{4P_{OUT}} \qquad (33)$$

$$t_1' = \frac{L_M \times I_{P\_PK\_MAX}}{\sqrt{2}V_{AC\_MIN}} \qquad (34)$$

$$I_{P\_RMS\_MAX} \approx \sqrt{\frac{t_1'}{6t_S'}} \times I_{P\_PK\_MAX} \qquad (35)$$

(g) Compute secondary maximum peak current $I_{S\_PK\_MAX}$ and RMS current $I_{S\_RMS\_MAX}$ for the transformer fabrication.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} \qquad (36)$$

$$t_2' = t_S' - t_1' - t_3 \qquad (37)$$

$$I_{S\_RMS\_MAX} \approx \sqrt{\frac{t_2'}{6t_S'}} \times I_{S\_PK\_MAX} \qquad (38)$$

Transformer design (N_P,N_S,N_{AUX})

The design of the transformer is similar with ordinary Flyback transformer. The parameters below are necessary:

Necessary parameters	
Turns ratio	N_{PS}
Inductance	L_M
Primary maximum current	$I_{P\_PK\_MAX}$
Primary maximum RMS current	$I_{P\_RMS\_MAX}$
Secondary maximum RMS current	$I_{S\_RMS\_MAX}$

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area A_e.

(b) Preset the maximum magnetic flux ΔB

ΔB=0.22~0.26T

(c) Compute primary turn N_P

$$N_P = \frac{L_M \times I_{P\_PK\_MAX}}{\Delta B \times A_e} \quad (39)$$

(d) Compute secondary turn N_S

$$N_S = \frac{N_P}{N_{PS}} \quad (40)$$

(e) Compute auxiliary turn N_{AUX}， For VCC is supplied by HV, and HV is supplied by $V_{AUX,MIN}$, in order to ensure the VCC works normally during CV mode. N_{AUX} can set:

$$N_{AUX} = N_S \times \frac{3 \times V_{AUX,CV}}{V_{OVP}} \quad (41)$$

Where V_{OVP} is the output over voltage protection point, and $V_{AUX,CV}$ is 20V.

(f) Select an appropriate wire diameter

With $I_{P\text{-}RMS\text{-}MAX}$ and $I_{S\text{-}RMS\text{-}MAX}$, select appropriate wire to make sure the current density ranges from 4A/mm^2 to 10A/mm^2.

(g) If the winding area of the core and bobbin is not enough, reselect the core style, go to **(a)** and redesign the transformer until the ideal transformer is achieved.

Output capacitor C_{OUT}

Preset the output current ripple ΔI_{OUT}, C_{OUT} is induced by

$$C_{OUT} = \frac{\sqrt{(\frac{2I_{OUT}}{\Delta I_{OUT}})^2 - 1}}{4\pi f_{AC} R_{LED}} \quad (42)$$

Where I_{OUT} is the rated output current; ΔI_{OUT} is the demanded current ripple; f_{AC} is the input AC supply frequency; R_{LED} is the equivalent series resistor of the LED load.

RCD snubber for MOSFET

The power loss of the snubber P_{RCD} is evaluated first

$$P_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{\Delta V_S} \times \frac{L_K}{L_M} \times P_{OUT} \quad (43)$$

Where N_{PS} is the turns ratio of the Flyback transformer; V_{OUT} is the output voltage; V_{D_F} is the forward voltage of the power diode; ΔV_S is the overshoot voltage clamped by RCD snubber; L_K is the leakage inductor; L_M is the inductance of the Flyback transformer; P_{OUT} is the output power.

The R_{RCD} is related with the power loss:

$$R_{RCD} = \frac{(N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S)^2}{P_{RCD}} \quad (44)$$

The C_{RCD} is related with the voltage ripple of the snubber ΔV_{C_RCD}:

$$C_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{R_{RCD} f_S \Delta V_{C\_RCD}} \quad (45)$$

Layout

(a) To achieve better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to the BUS line capacitor first, then to the switching circuit.

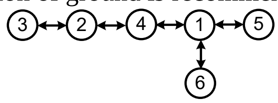
(b) The circuit loop of all switching circuit should be kept small: primary power loop, secondary loop and auxiliary power loop.

(c) Bias supply trace should be connected to the bias supply capacitor first instead of GND pin. The bias supply capacitor should be put beside the IC.

(d) Loop of 'Source pin – current sample resistor – GND pin' .should be kept as small as possible.

(e) The resistor divider is recommended to be put beside the IC.

(f) The connection of ground is recommended as:



Ground ①: ground of BUS line capacitor
Ground ②: ground of bias supply capacitor and GND pin
Ground ③: ground of signal trace except GND pin
Ground ④: ground of current sample resistor.
Ground ⑤: primary ground node of Y capacitor.
Ground ⑥: ground of auxiliary winding

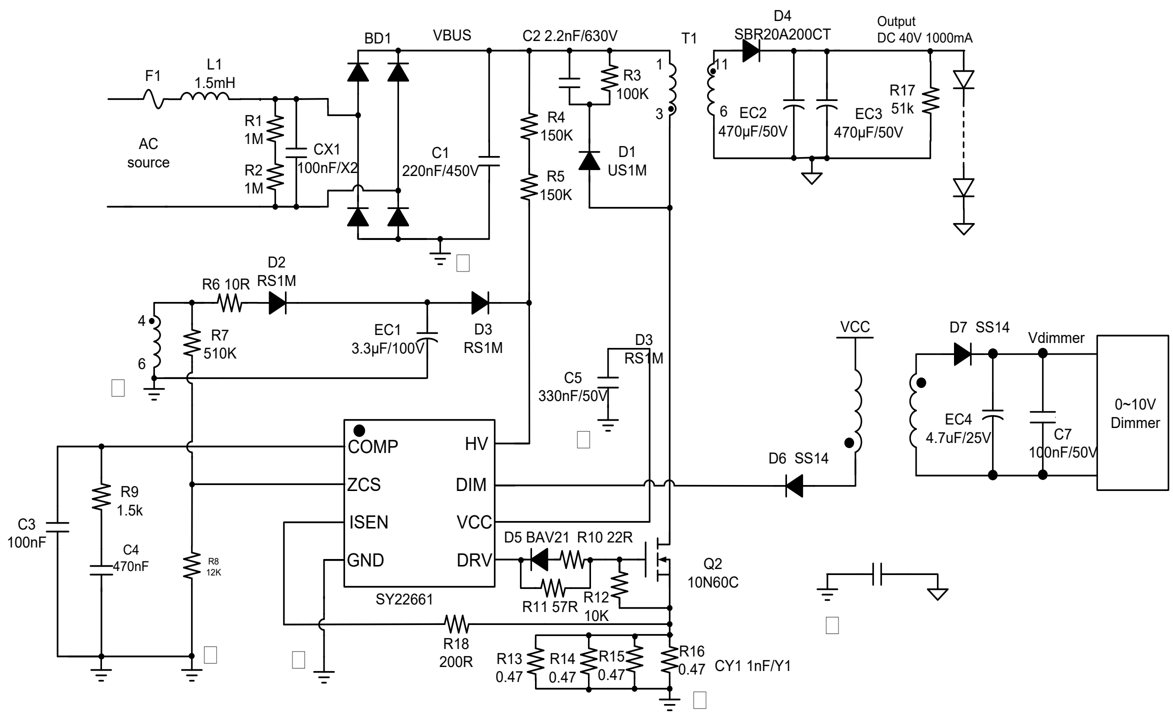


Fig.15 Ground Layout

Design Example

A design example of typical application is shown below step by step.

#1. Identify design specification

Design Specification			
V_{AC}(RMS)	90V~264V	V_{OUT}	42V
I_{OUT}	1000mA	η	89%

#2. Transformer design (N_{PS}, L_M)

Refer to Power Device Design

Conditions			
V_{AC_MIN}	90V	V_{AC_MAX}	264V
$\triangle V_S$	50V	$V_{MOS\_(BR)DS}$	600V
P_{OUT}	42W	$V_{D,F}$	1V
C_{Drain}	100pF	f_{S_MIN}	75kHz

(a) Compute turns ratio N_{PS} first

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - \sqrt{2} V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D,F}}$$
$$= \frac{600V \times 0.9 - \sqrt{2} \times 264V - 50V}{42V + 1V}$$
$$= 2.71$$

N_{PS} is set to

$$N_{PS} = 2.60$$

(b)f_{S_MIN} is preset

$$f_{S,MIN} = 42kHz$$

(c) Compute the switching period t_S and ON time t_1 at the peak of input voltage.

$$t_S = \frac{1}{f_{S\_MIN}} = 23.8\mu s$$

$$t_1 = \frac{t_S \times N_{PS} \times (V_{OUT} + V_{D\_F})}{\sqrt{2} V_{AC\_MIN} + N_{PS} \times (V_{OUT} + V_{D\_F})}$$
$$= \frac{23.8\mu s \times 2.60 \times (42V + 1V)}{\sqrt{2} \times 90V + 2.60 \times (42V + 1V)}$$
$$= 11.13\mu s$$

(d) Compute the inductance L_M

$$L_M=\frac{V_{AC\_MIN}^2\times t_1^2\times\eta}{2P_{OUT}\times t_S}=\frac{90V^2\times 11.13\mu s^2\times 0.89}{2\times 42W\times 23.8\mu s}=446.693\mu H$$

Set

$$L_M=440\mu H$$

(e) Compute the quasi-resonant time t_3

$$t_3=\pi\times\sqrt{L_M\times C_{Drain}}=\pi\times\sqrt{440\mu H\times 100pF}\approx 659ns$$

(f) Compute primary maximum peak current $I_{P\_PK\_MAX}$

$$I_{P\_PK\_MAX}=\frac{2P_{OUT}\times[\frac{L_M}{\sqrt{2}V_{AC\_MIN}}+\frac{L_M}{N_{PS}\times(V_{OUT}+V_{D\_F})}]}{L_M\times\eta}+\frac{\sqrt{4P_{OUT}^2\times[\frac{L_M}{\sqrt{2}V_{AC\_MIN}}+\frac{L_M}{N_{PS}\times(V_{OUT}+V_{D\_F})}]^2+4L_M\times\eta\times P_{OUT}\times t_3}}{L_M\times\eta}$$

$$=3.26A$$

Adjust switching period t_S and ON time t_1 to t_S' and t_1'.

$$t_S'=\frac{\eta\times L_M\times I_{P\_PK\_MAX}^2}{4P_{OUT}}=\frac{0.89\times 440\mu H\times 3.26A^2}{4\times 42W}=24.772\mu s$$

$$t_1'=\frac{L_M\times I_{P\_PK\_MAX}}{\sqrt{2}V_{AC\_MIN}}=\frac{440\mu H\times 3.26A}{\sqrt{2}\times 90V}=11.27\mu s$$

Compute primary maximum RMS current $I_{P\_RMS\_MAX}$

$$I_{P\_RMS\_MAX}\approx\sqrt{\frac{t_1'}{6t_S'}}\times I_{P\_PK\_MAX}=\sqrt{\frac{11.27\mu s}{6\times 24.772\mu s}}\times 3.26A=0.90A$$

(g) Compute secondary maximum peak current and the maximum RMS current.

$$I_{S\_PK\_MAX}=N_{PS}\times I_{P\_PK\_MAX}=2.60\times 3.26A=8.47A$$

$$t_2'=t_S'-t_1'-t_3=24.772\mu s-11.27\mu s-0.659\mu s=12.843\mu s$$

$$I_{S,RMS,MAX} \approx \sqrt{\frac{t_2'}{6t_S'}} \times I_{S\_PK\_MAX} = \sqrt{\frac{12.843\mu s}{6\times 24.772\mu s}} \times 8.47A = 2.55A$$

#3. Select power MOSFET and secondary power diode

Refer to Power Device Design

Known conditions at this step			
V_{AC_MAX}	264V	N_{PS}	2.60
V_{OUT}	42V	V_{D_F}	1V
ΔV_S	50V	η	89%

(a) Compute the voltage and the current stress of MOSFET:

$$\begin{aligned} V_{MOS\_DS\_MAX} &= \sqrt{2}V_{AC\_MAX} + N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S \\ &= \sqrt{2} \times 264V + 2.60 \times (42V + 1V) + 50V \\ &= 535V \end{aligned}$$

$$I_{MOS\_PK\_MAX} = I_{P\_PK\_MAX} = 3.26A$$

$$I_{MOS\_RMS\_MAX} = I_{P\_RMS\_MAX} = 0.90A$$

(b) Compute the voltage and the current stress of secondary power diode

$$\begin{aligned} V_{D\_R\_MAX} &= \frac{\sqrt{2}V_{AC\_MAX}}{N_{PS}} + V_{OUT} \\ &= \frac{\sqrt{2} \times 264V}{2.60} + 42V \\ &= 186V \end{aligned}$$

$$I_{D\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} = 2.60 \times 3.26A = 8.47A$$

$$I_{D\_AVG} = I_{OUT} = 1A$$

#4. Select the output capacitor C_{OUT}

Refer to Power Device Design

Conditions			
I_{OUT}	1000mA	ΔI_{OUT}	$0.3I_{OUT}$
f_{AC}	50Hz	R_{LED}	$12\times 1.6\Omega$

The output capacitor is

$$C_{OUT}=\frac{\sqrt{(\frac{2I_{OUT}}{\Delta I_{OUT}})^2-1}}{4\pi f_{AC}R_{LED}}$$
$$=\frac{\sqrt{(\frac{2\times 1A}{0.3\times 1A})^2-1}}{4\pi\times 50Hz\times 12\times 1.6\Omega}$$
$$=546\mu F$$

#5. Set VIN pin

Refer to **Start up**

Conditions			
V_{BUS_MIN}	90V × 1.414	V_{BUS_MAX}	264V × 1.414
I_{ST}	34μA (typical)	V_{IN_ON}	22V (typical)
		t_{ST}	300ms (designed by user)

(a) R_{ST} is preset

$$R_{ST}<\frac{V_{BUS}}{350\mu A}=\frac{90V\times 1.414}{350\mu A}=363k\Omega,$$
$$R_{ST}>\frac{V_{BUS}}{1mA}=\frac{90V\times 1.414}{1mA}=127k\Omega,$$

Set R_{ST}

$$R_{ST}=150k\Omega\times 2=300k\Omega$$

(b) Design C_{VIN}

Set C_{VIN}

$$C_{VIN}=330nF$$

#6 Set COMP pin

Refer to **Internal pre-charge design for quick start up**

Parameters designed	
R_{COMP}	1.5kΩ
C_{COMP1}	470nF
C_{COMP2}	100nF

#7 Set current sense resistor to achieve ideal output current

Refer to **Primary-side constant-current control**

Known conditions at this step			
k	0.167	N_{PS}	2.60
V_{REF}	0.28V	I_{OUT}	1A

The current sense resistor is

$$R_S = \frac{k \times V_{REF} \times N_{PS}}{I_{OUT}}$$
$$= \frac{0.167 \times 0.28V \times 2.60}{1A}$$
$$=0.12\Omega$$

#8 set ZCS pin

Refer to **Line regulation modification** and **Over Voltage Protection (OVP) & Open Loop Protection (OLP)**

First identify R_{ZCSU} need for line regulation.

Parameters Designed			
R_{ZCSU}	510kΩ		

Then compute R_{ZCSU} and N_{AUX}

Conditions			
V_{ZCS_OVP}	1.5V	V_{OVP}	48V
V_{OUT}	42V		
Parameters designed			
R_{ZCSU}	510kΩ		
N_S	12	N_{AUX}	

$$V_{AUX\_CV} = \frac{0.5 \cdot (R_{ZCSU} + R_{ZCSD})}{R_{ZCSD}} \geq 22$$

$$\frac{0.5}{21.5} \geq \frac{R_{ZCSD}}{R_{ZCSU}}$$

R_{ZCSUP}=510 kΩ

$$R_{ZCSD} \leq 11.8$$

R_{ZCSD} is set to

R_{ZCSD}=12kΩ

Then set the N_{AUX} to

$$N_{AUX} = N_S \times \frac{3 \times V_{AUX,CV}}{V_{OVP}}$$

N_{AUX}=16.5

N_{AUX} is set to17

#9 Set dimming Transformer inductance

Refer to **Dimming function**

Known conditions at this step			
$V_{DIMMER,MAX}$	12V	N_{PS_T2}	1

Magnetic ring is used in this application. Then $L_{m,T2}$ is set to

$$L_{m\_T2} > \frac{2\times V_{DIMMER,\max}\times t_{blanking}}{23mA} = \frac{2\times 12\times 1.5\mu}{23m}$$

$$L_{m\_T2} > 1.56mH$$

Consider the ± 30% error of the μ_i, L_{m_T2} can set:

$$L_{m\_T2} > \frac{1.56mH}{0.7} = 2.2mH$$

L_{m_T2} set 3mH.

#10 final result.

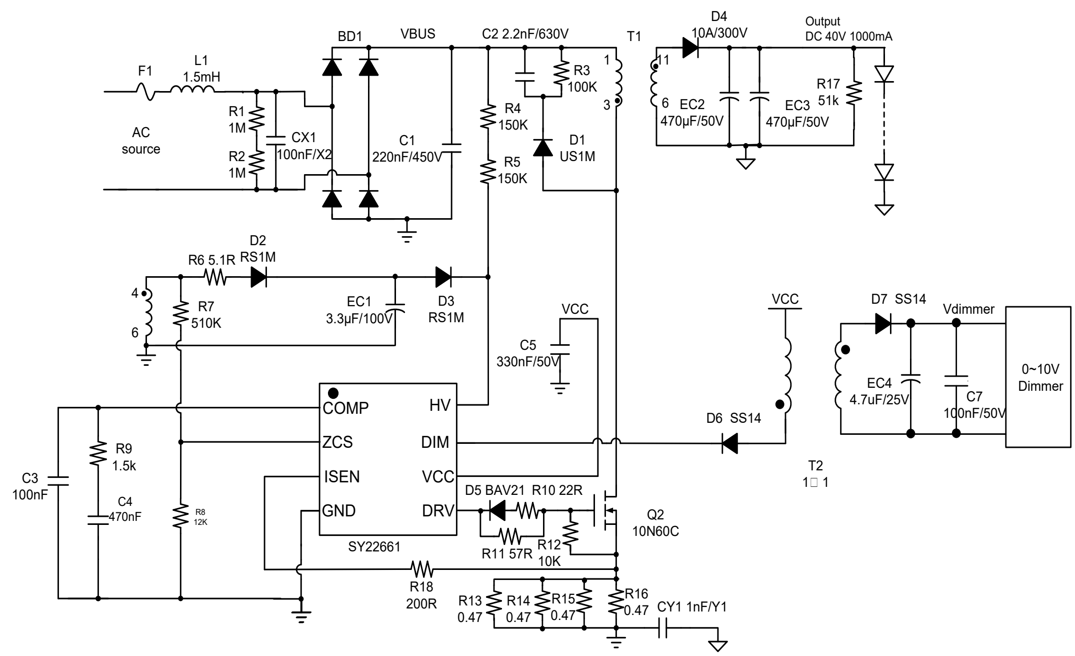
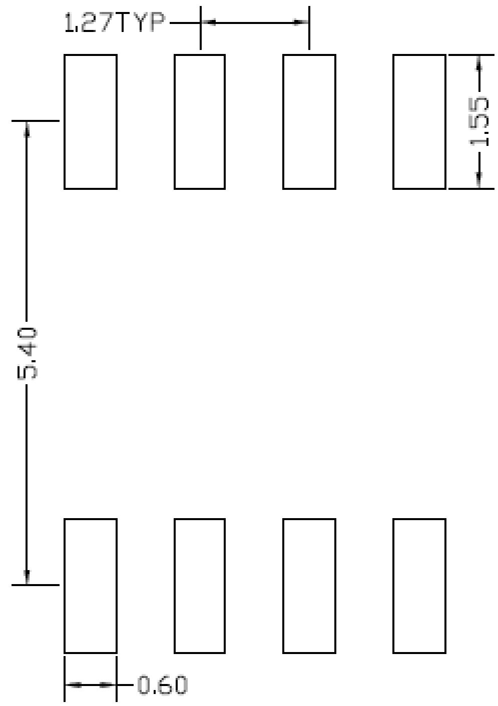
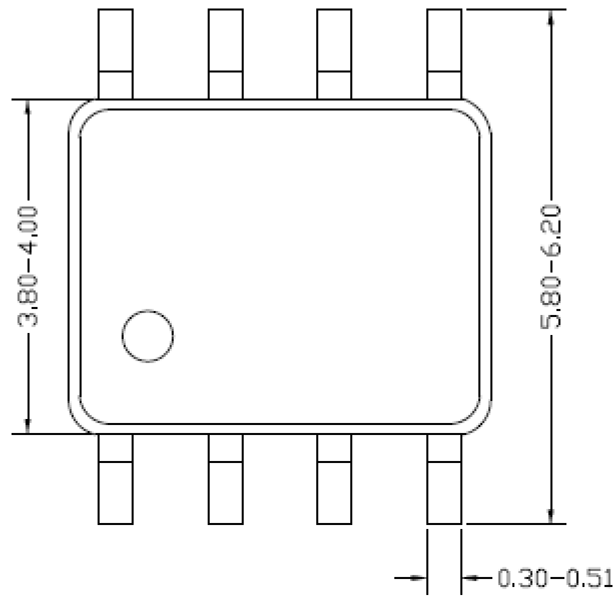


Fig.16 Final Design Result

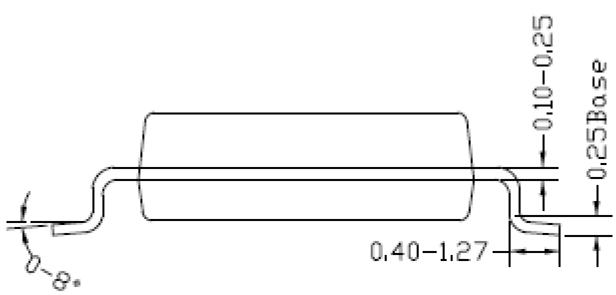
SO8 Package Outline & PCB Layout Design



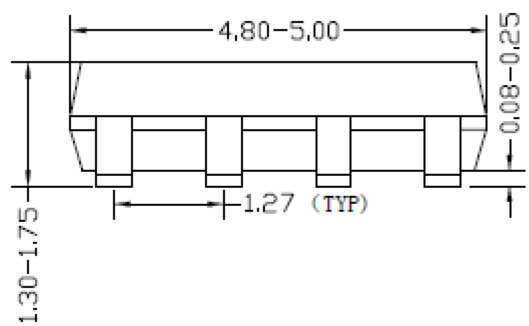
Recommended Pad Layout (Reference only)



Top view



Side view

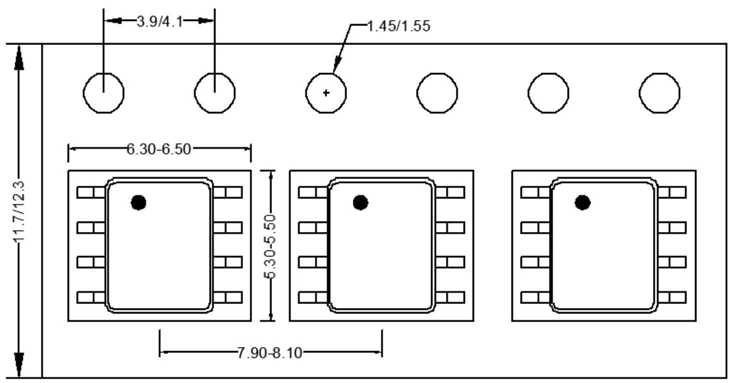


Front view

Notes: All dimensions are in millimeter and exclude mold flash & metal burr.

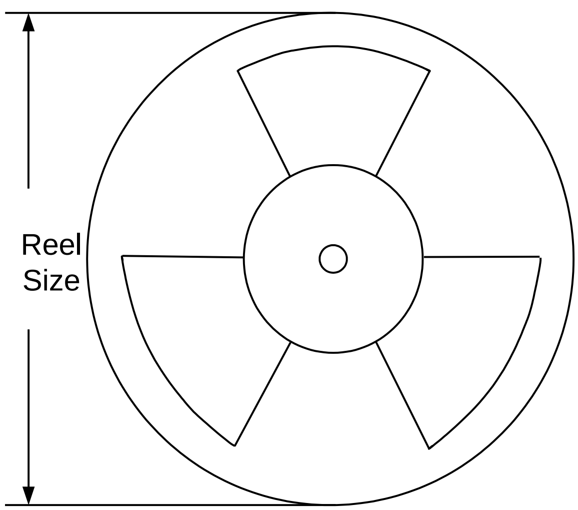
Taping & Reel Specification

1. Taping orientation for packages（SO8）



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SO8	12	8	13"	400	400	2500

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
December 4,2020	Revision 0.9	Initial Release

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