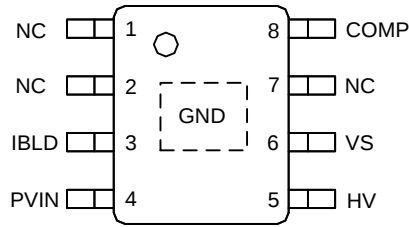


Pinout (top view)



(SO8E)

Top Mark: DLNxyz (device code: DLN, x=*year code*, y=*week code*, z=*lot number code*)

Pin	Name	Description
1,2,7	NC	No connect
3	IBLD	Bleeding current from BUS to achieve good compatibility.
4	PVIN	Drain of integrated power MOSFET.
5	HV	IC power supply.
6	VS	Source of integrated power MOSFET integrate, sense output current.
8	COMP	Loop compensation Pin.
Bottom	GND	GND of IC.

Block Diagram

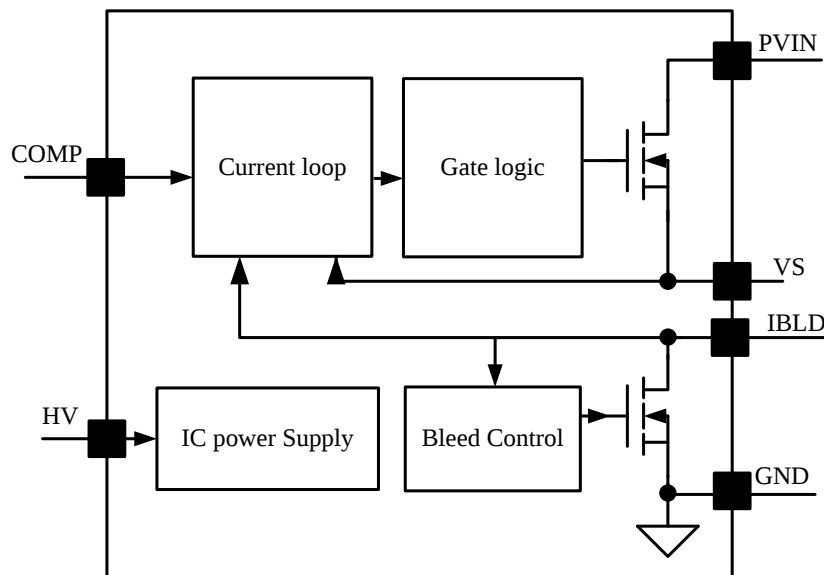


Fig2. IC block diagram

Absolute Maximum Ratings (Note 1)

PVIN-----	-0.3V to 350V
IBLD, HV-----	-0.3V to 500V
VS, COMP-----	-0.3V to 3.6V
Power Dissipation, @ T _A = 25°C SO8E-----	3.3W
Package Thermal Resistance (Note 2)	
SO8E, θ _{JA} -----	30°C/W
SO8E, θ _{JC} -----	10°C/W
Temperature Range -----	-40°C to 150°C
Lead Temperature (Soldering, 10 sec.) -----	260°C
Storage Temperature Range -----	-40°C to 150°C

Electrical Characteristics

(HV= 15V (Note 3), T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
HV Turn-on Threshold	HV_ON		9.3	11	12.7	V
HV Turn-off Threshold	HV_OFF		5.8	7.5	9.2	V
BV of HV MOSFET	BV_HV		500			V
Quiescent Current	I _Q			140		μA
Inter REF Section						
Inter current reference	V _{REF}		96	100	104	mV
Power MOSFET Section						
BV of Integrated PVIN MOSFET	V _{PVIN}		350			V
BV of Integrated IBLD MOSFET	V _{IBLD}		500			V
Thermal Section						
Thermal Fold Back Temperature	T _{FB}			148		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2” x 2” FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: Increase HV pin voltage gradually higher than HV_ON voltage then turn to 25V.

Operation

The SY22643P is a dimmable linear AC/DC driver with integrated 350V MOSFET for LED lighting.

It's compatible with Leading/Trailing edge dimmer.

With the constant current control, SY22643P can achieve good line regulation and load regulation.

The patented technique leads to high power efficiency and PF (>0.9).

SY22643P provides reliable protections such as over temperature protection (Thermal fold-back), etc.

SY22643P is available with SO8E package.

Applications Information

Start Up and IC Power Supply

After AC supply is powered on, IC is charged up by BUS voltage. Once HV reaches HV_ON, IC starts to work, BUS voltage and C_{OUT} voltage will supply the power IC need.

The startup and power supply procedure is shown in Fig.3.

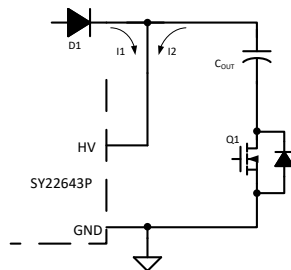


Fig.3 Start up

Shut Down

After AC supply is powered off, the energy stored in the output capacitor will be discharged. When HV is below HV_OFF, the IC will stop working.

Constant-Current Control

The output current I_{OUT} can be represented by

$$I_{OUT} = \frac{V_{REF}}{R_s}$$

Where V_{REF} is the internal reference voltage; R_s is the current sense resistor.

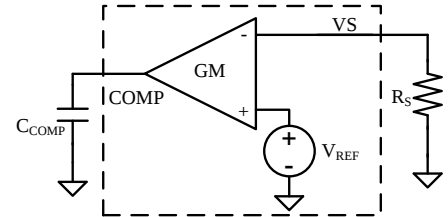


Fig.4 Closed loop

Output capacitor C_{COMP} needs to be big enough to keep average output current equal to V_{REF}.

Special Design for Current Compensation

To have a better efficiency, special design is integrated in SY22643P.

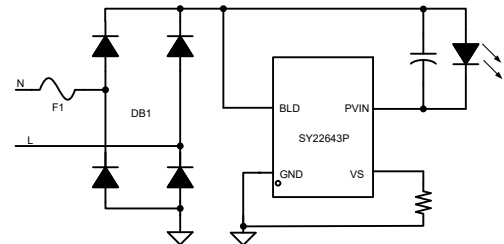


Fig.5 The patented technology of compensation

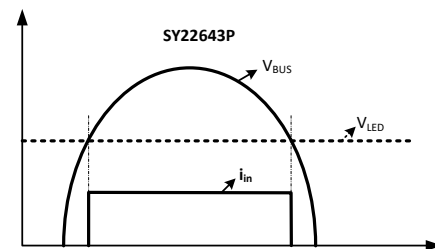


Fig.6 Shape of Input current for high PF

Input current of SY22643P is constant when V_{BUS} is higher than V_{LED}, set V_{LED} about 115V, it is just right for the requirement PF>0.9.

TRIAC Dimming

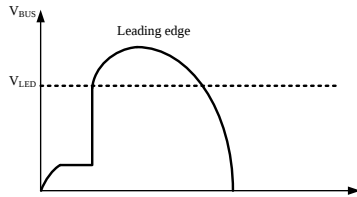


Fig.7 BUS voltage with TRIAC

When cooperate with dimmer, IC will provide enough latching current and holding to keep dimmer working normally.

Thermal Fold-back Function

SY22643P have thermal fold-back function.

Design Guide:

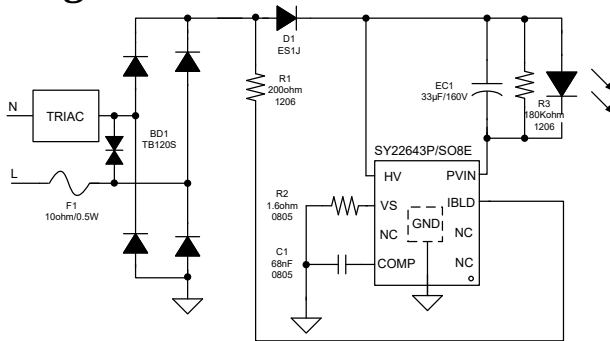


Fig.8 Schematic

1: F1 selection:

4.7ohm to 22ohm is recommended for F1, usually, the smaller F1 is, the better line regulation is

2: D1 selection:

Super-fast recovery diode like ES1J is suggested for D1, it will effectively prevent negative current flow from PVIN.

3: R1 selection:

R1 is used for current limit on IBLD, usually, 200ohm is recommended.

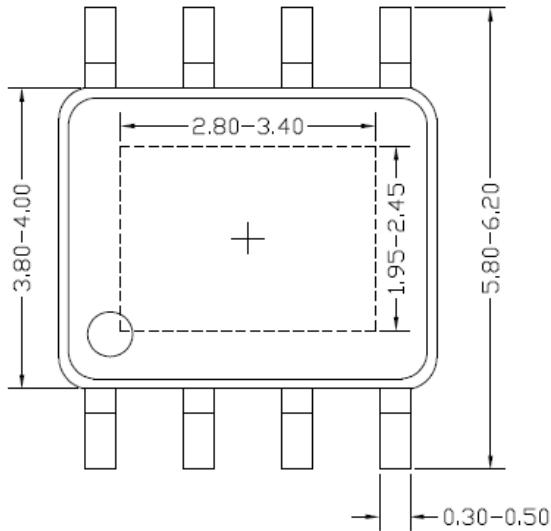
4: R2 selection:

R2 is used to sense output current. Inter Ref is 100mV, $R2 = 100\text{mV}/I_o$.

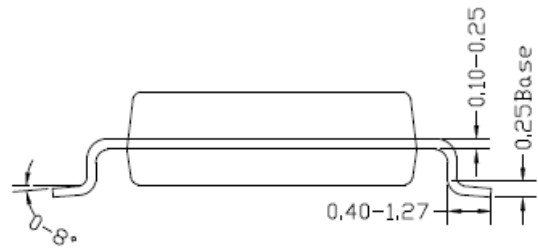
5: C1 selection:

Consider of PF and loop response speed, usually, C_{COMP} is suggested 68~100nF.

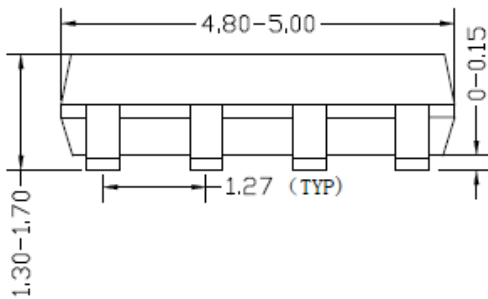
SO8E Package Outline & PCB layout



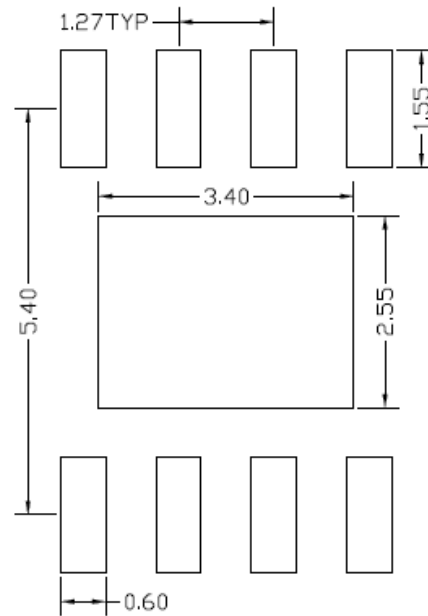
Top view



Side view



Front view



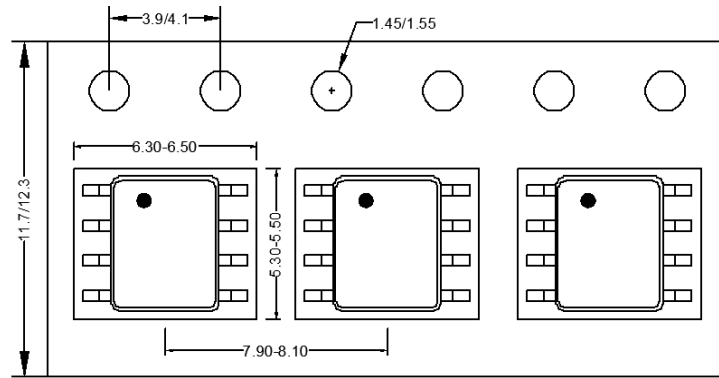
**Recommended PCB Layout
(Reference Only)**

Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

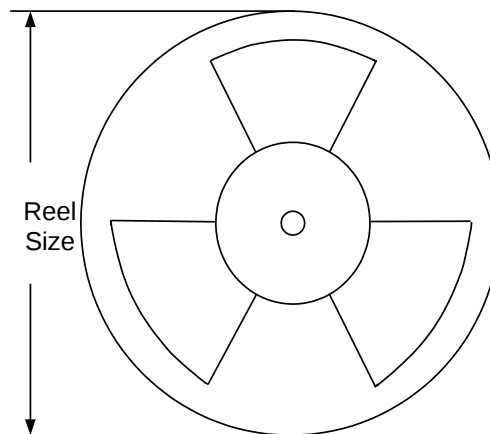
1. Taping orientation

SO8E



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
SO8E	12	8	13"	400	400	2500

Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
December 4, 2020	Revision 0.9	Initial Release

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