SY23215

Power-over-Ethernet and DC-DC Flyback Converter

General Description

The SY23215 is a combined Power-over-Ethernet (PoE) powered device (PD) interface and primary-side controller optimized specifically for isolated converter designs. The SY23215 supports the IEEE 802.3at and 802.3af standards, 25W powered device (PD). External resistors connected to the SY23215 provide the proper IEEE 802.3 signatures for the detection function and programming of the classification mode.

To achieve higher efficiency and better EMI performance, the SY23215 drives flyback converters in quasi-resonant mode and with adaptive PWM/PFM control.

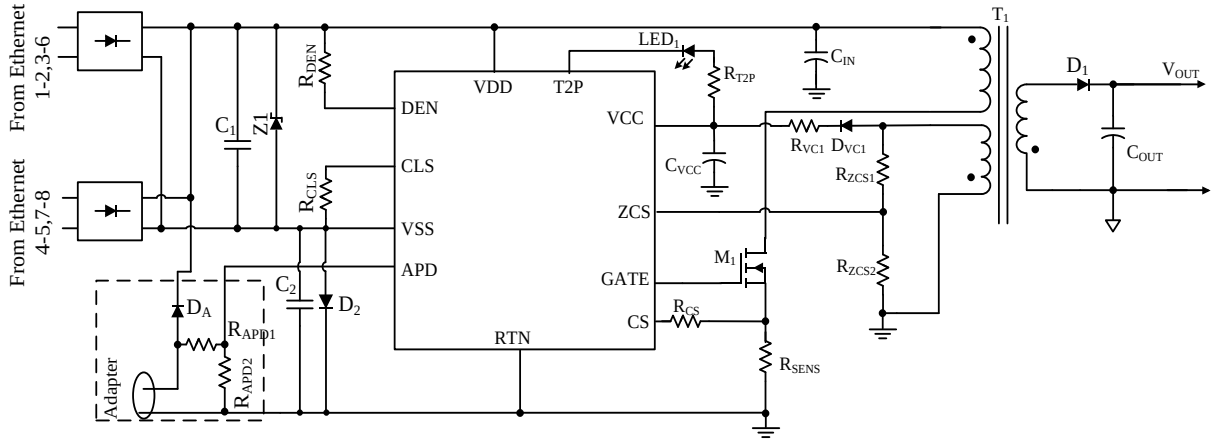
Features

- Power up to 25W
- Supports the IEEE 802.3at and 802.3af Standards
- Primary-Side Control for DC/DC Flyback Converter
- QR-Mode Operation for High Efficiency
- PWM/PFM Control for Higher Average Efficiency
- Adapter ORing Support
- 95V, 0.4Ω Hotswap MOSFET
- RoHS-Compliant and Halogen-Free
- Compact Package: QFN4*4-20

Applications

- IEEE 802.3at- and 802.3af-Compliant Devices
- Video and VoIP Telephones
- RFID Readers
- Multiband Access Points
- Security Cameras

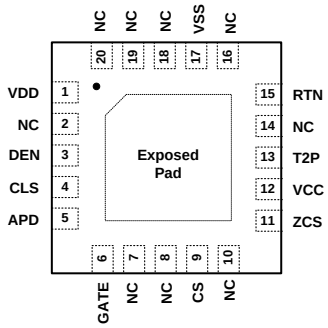
Typical Applications



Ordering Information

Ordering Part Number	Package type	Top Mark
SY23215QYC	QFN4x4-20 RoHS Compliant and Halogen Free	CKZ*xyz*

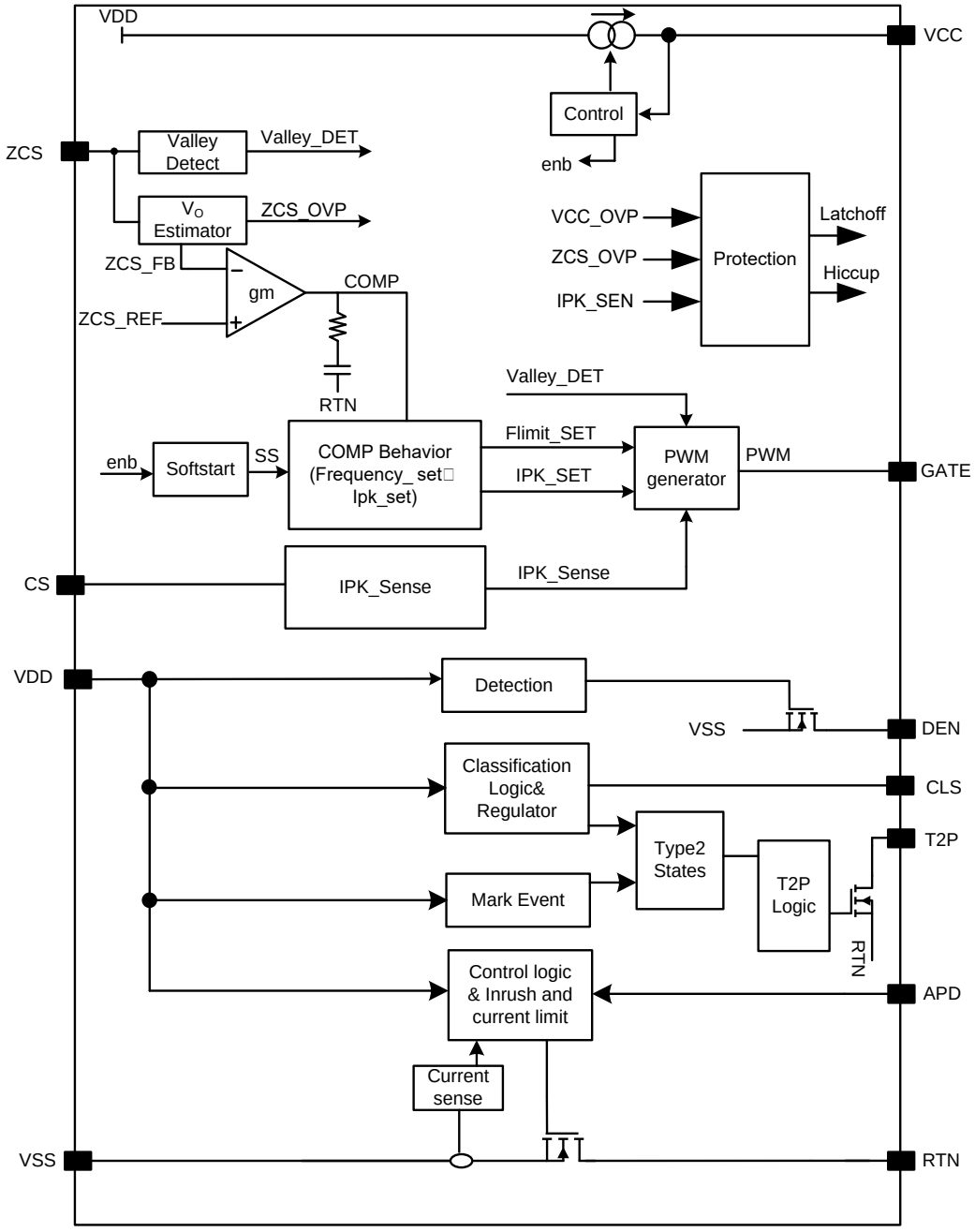
Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	VDD	Connect to the positive PoE input power rail. V_{DD} powers the PoE interface circuits. Bypass with a 0.1µF capacitor and protect with a TVS.
3	DEN	Connect a 24.9kΩ resistor from DEN to V_{DD} to provide the PoE detection signature. Pulling this pin to V_{SS} during powered operation causes the internal hotswap MOSFET to turn off.
4	CLS	Connect a resistor from CLS to V_{SS} to program classification current. 2.5V is applied to the program resistor during classification to set class current.
5	APD	Pull APD above 1.5V to disable the internal hotswap switch and force power to come from an external adapter. Connect APD to RTN when not used.
6	GATE	Gate-drive pin.
9	CS	Current-sense pin.
11	ZCS	Inductor current zero-crossing detection pin. This pin receives the auxiliary winding voltage using a resistor-divider and detects the inductor current-zero crossing point.
12	VCC	DC/DC converter bias voltage.
13	T2P	Active-low output that indicates a PSE has performed the IEEE 802.3at Type 2 hardware classification, or APD is active.
15	RTN	RTN is the negative rail input to the DC/DC converter, and the output of the PoE hotswap MOSFET.
17	VSS	Connect to the negative power rail derived from the PoE source.
—	Exposed Pad	This is the thermal flag for the IC and should be soldered to the plane, which is connected to V_{SS}.
Others	NC	Leave floating or connect to GND.

Block Diagram



Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
Input Voltage Range [DEN, VDD, RTN (Note 2)] to VSS	-0.3	95	V
Input Voltage Range [VDD, T2P] to RTN	-0.3	95	
Input Voltage Range VCC to RTN	-0.3	25	
Input Voltage Range CLS(Note 3) to VSS	-0.3	5.5	
Input Voltage Range [ZCS, CS, APD] to RTN	-0.3	5.5	
Input Voltage Range GATE to RTN	-0.3	15	
Junction Temperature Range	45	150	°C
Lead Temperature (Soldering,10s)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 4)	Min	Max	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance		45	°C/W
θ_{JC} Junction-to-Case Thermal Resistance		22.5	

Recommended Operating Conditions

Parameter	Min	Max	Unit
IN	0	72	V
Output Voltage	0	72	
Output Current	0	18	
Junction Temperature	-40	125	°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Note 2: I_{RTN} = 0 for V_{RTN} > 80V.
Note 3: Do not apply voltage to this pin.
Note 4: JESD 51-2，-5，-7，-8，-14 standard.

Electrical Characteristics

(C_{VCC} = 0.1μF, R_{DEN} = 24.9kΩ, R_{CLS} open, V_{VDD} - V_{VSS} = 48V, 9V ≤ V_{CC} ≤ 18V. Typical specifications are at T_J = 25°C, unless otherwise noted.)

DC-DC Controller (V_{SS} = RTN, all voltages referred to RT.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VCC						
V_{CC} Turn-on Threshold	$V_{VCC,ON}$		8.5	9	9.5	V
V_{CC} UVLO Hysteresis	$V_{VCC,HYS}$			2.6		V
V_{CC} OVP Voltage	$V_{VCC,OVP}$			22		V
Quiescent Current	I_Q		200	260	320	μA
Startup Current Source	I_{VCC}	V_{VDD} = 48V, V_{VCC} = 0V	0.5	1	2	mA
ZCS						
Voltage Reference	$V_{ZCS,REF}$		1.180	1.200	1.220	V
ZCS OVP Threshold	$V_{ZCS,OVP}$		1.35	1.45	1.55	V
Blanking Time for OFF Time	$t_{OFF,MIN}$			0.7		μs
CS						
Maximum Threshold Voltage	V_{ILIM}		0.90	1.05	1.23	V
Switching						
Max ON Time	$T_{ON,MAX}$			12		μs
Max OFF Time	$T_{OFF,MAX}$			600		μs
Maximum Switching Frequency	F_{MAX}			200		kHz
APD						
APD Threshold Voltage	$V_{APD,EN}$	V_{APD} rising	1.4	1.5	1.6	V
	$V_{APD,H}$	Hysteresis		0.30		V
APD Leakage Current		V_{APD} = 5.5V			1	μA
Thermal Shutdown						
Thermal Shutdown Temperature		T_J rising		150		°C
Hysteresis				20		°C

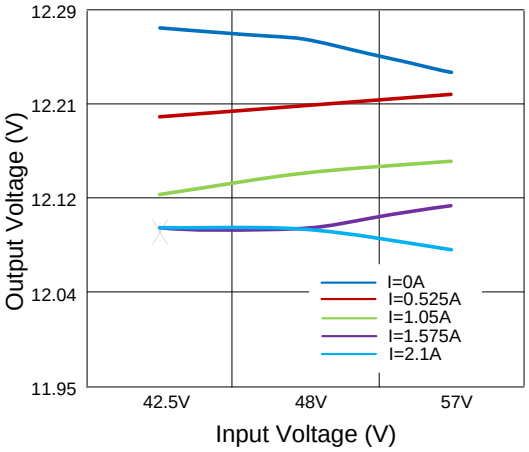
PD Interface (All voltages refer to V_{SS} unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Detection	DEN	V_{VDD} = RTN = V_{SUPPLY} positive				
Detection Current		V_{VDD} = 1.6V		60		μA
		V_{VDD} = 10V		400		μA
Detection Bias Current		V_{VDD} = 10V, float DEN, measure I_{SUPPLY}	35	46	58	μA
Hotswap Disable Threshold	$V_{PD,DIS}$		3	4	5	V
DEN Leakage Current		V_{DEN} = V_{VDD} = 57V, measure I_{DEN}		0.1	5	μA
Classification	CLS	V_{VDD} = RTN = V_{SUPPLY} positive				
Classification Current	I_{CLS}	R_{CLS} = 1270Ω		2		mA
		R_{CLS} = 243Ω		10		mA
		R_{CLS} = 137Ω		18		mA
		R_{CLS} = 90.9Ω		28		mA
		R_{CLS} = 63.4Ω		40		mA
Classification Regulator Lower Threshold	$V_{CL,ON}$	Regulator turns on, V_{DD} rising	9	11	13	V
	$V_{CL,H}$	Hysteresis	1	2	3	V
Classification Regulator Upper Threshold	$V_{CU,OFF}$	Regulator turns off, V_{DD} rising	21	22	23	V
	$V_{CU,H}$	Hysteresis	0.3	0.7	1.0	V
Leakage Current		V_{VDD} = 57V, V_{CLS} = 0V, DEN = V_{VSS}, measure I_{CLS}			1	μA
Hotswap MOSFET						
On Resistance				0.4	0.5	Ω
Current Limit				1.1		A
Inrush Limit				100		mA
Leakage Current		V_{VDD} = V_{RTN} = 95V, DEN = V_{VSS}			40	μA
V_{DD} UVLO						
V_{DD} UVLO Threshold	$V_{UVLO,R}$	V_{VDD} rising	34	35	36	V
	$V_{UVLO,H}$	Hysteresis		4.3		V
Thermal Shutdown						
Thermal Shutdown temperature		T_J rising		150		°C
Hysteresis				20		°C

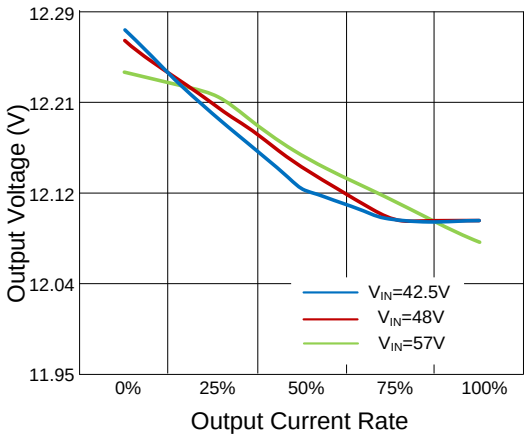
Typical Performance Characteristics

(Test condition: input voltage: 42.5VDC; output spec: 12VDC/2.1A; ambient temperature: 25±5 ℃; ambient humidity:65±25%, unless otherwise noted.)

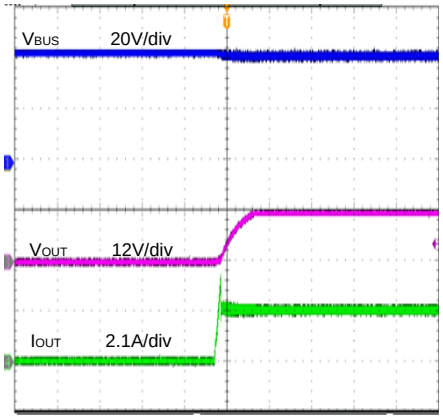
Line Regulation



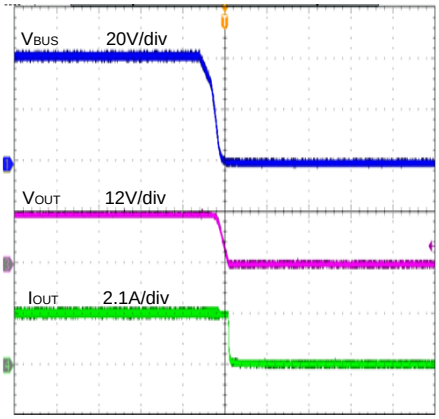
Load Regulation



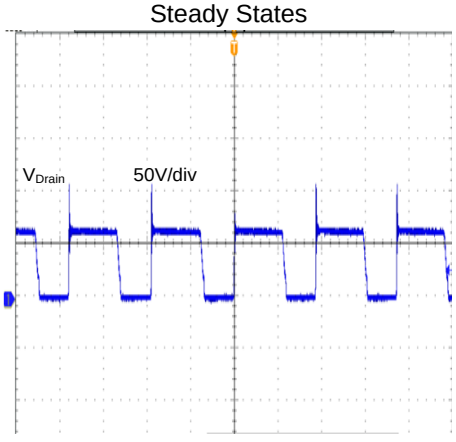
Startup



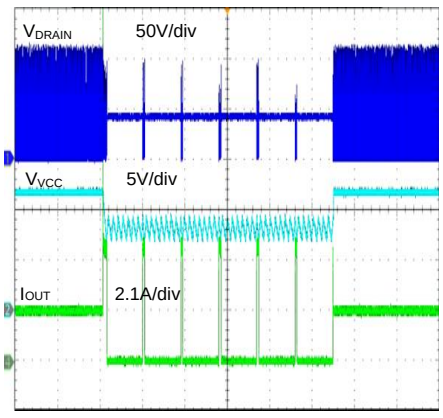
Shutdown



Steady States



Short Circuit Protection



Operation

Protocol

PoE Startup Sequence

The IEEE 802.3at standard requires two detection levels, two class and mark cycles, and start-up from the second mark event. Following the application of full voltage, V_{RTN} to V_{VSS} falls as the SY23215 charges C_{IN}. The converter then starts up and draws current, as shown in Figure 1.

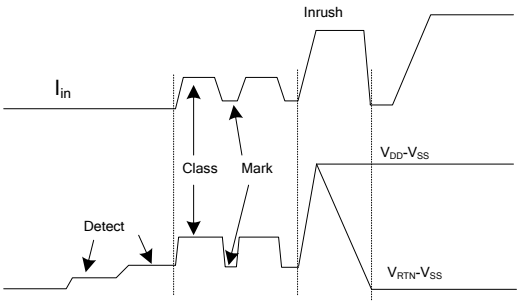


Figure 1. Start-up sequence

Detection

In order to identify a device as a valid PD, the power sourcing equipment (PSE) senses the ethernet connection by applying two voltages in a range of 2.8V to 10V on the ethernet cable, and then measuring the corresponding currents. An equivalent resistance is calculated using the formula ΔV/ΔI. During this phase, the PD must present a resistance between 23.75kΩ and 26.25kΩ. The value of the detection resistance must be selected, accounting for the typical drop in voltage of the diode bridge. The typical resistance value of 24.9kΩ can be used in most cases.

Classification

In classification mode, the PSE will classify the PD for one of five power levels or classes, shown in Table 1. This allows the PSE to efficiently manage power distribution. An external resistor (R_{CLS}) connected from CLS to V_{SS} sets the classification current. The PSE may disconnect a PD if it draws more than its stated class power. During hardware classification, the PSE presents a fixed voltage between 15.5V and 20.5V to the PD, which in turn draws a fixed current set by R_{CLS}. The PD current is measured by the PSE to determine which of the five available classes is advertised (see Table 1). To avoid excessive power dissipation, SY23215 disables classification while the input voltage is above 22V. The CLS reference voltage will be turned off if the PD thermal limit is triggered, or when APD or DEN is active.

Table 1. Class Resistor Selection

Class	Power at PD (W)	Class current (mA)	Resistor (Ω)
0	0.44–12.95	0–4	1270
1	0.44–3.84	9–12	243
2	3.84–6.49	17–20	137
3	6.49–12.95	26–30	90.9
4	13–25.5	36–44	63.4

Two-Event Classification and the T2P Pin

A Type-2 PSE may declare the availability of high power by performing two-event classification. A Type-2 PD presents Class 4 to indicate it is a high-power device. In two-event classification, a Type-2 PSE probes for power classification twice. As shown in Figure 1, the first classification event occurs when the PSE presents an input voltage between 15.5V and 20.5V, and the SY23215 presents a Class 4 load current. The PSE then drops the input voltage into the mark voltage range of 6.9V to 10V, signaling the first mark event.

The PSE repeats this sequence with the second classification and second mark event. This alerts the PD that a Type-2 PSE is present. The Type-2 PSE then applies power to the PD, and the SY23215 charges up the capacitor (C_{IN}) across the V_{DD} and RTN pins with a controlled inrush current. When C_{IN} is fully charged and SY23215 is switching on, the T2P pin presents an active-low signal. The T2P pin will also go low if APD is enabled. The T2P output becomes inactive when the SY23215 input voltage falls outside the normal operating range.

Inrush and Operational Current Limit

Once the classification is successfully completed, the PSE will raise its voltage. When the input voltage is above the UVLO turn-on threshold ($V_{UVLO,R}$) of 35V, the hotswap switch is turned on and the input capacitor is charged with a low current (inrush current) limit until the voltage across the hotswap switch is sufficiently low, which indicates that the switch supply capacitor is almost completely charged. Once the inrush current falls and the RTN drops below 1.7V, the PD current limit switches to the operational level.

Adapter Power Input

In some applications, it is desirable to power the PD from an auxiliary power source such as a wall adapter. The SY23215 supports forced operation from either power source. Figure 2 illustrates the recommended connection of adapter power to PD. The hotswap switch is disabled while the adapter is used to pull APD high (up to 1.5V), blocking the PoE source from powering the output.

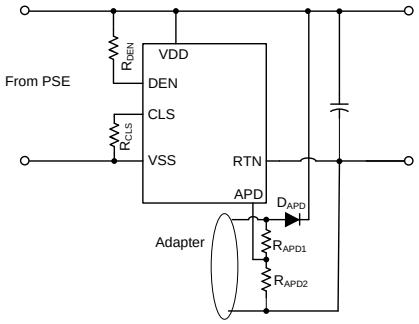


Figure 2. Adapter Power Input

Hotswap Features

The hotswap switch will be forced off under the following conditions:

- $V_{APD} > V_{APD,EN}$ (1.5V)
- $V_{DEN} \leq V_{PD,DIS}$ (4V, typical) when V_{VDD} - V_{VSS} is in the operational range
- PD overtemperature (OTP)
- V_{VDD} - V_{VSS} < PoE UVLO (30.5V, typical)

The internal hotswap MOSFET is protected against transient conditions with a current limit and deglitched foldback. Transient conditions include converter output short, shorts from V_{DD} to RTN, or transients on the input line. An overload on the hotswap MOSFET engages the current limit, which causes the RTN-to-V_{SS} voltage to rise. If V_{RTN} rises above 12V for longer than 400µs, the current limit reverts to the inrush limit, and turns the converter off.

DC-DC Controller Operation

Startup Operation

After the DC supply is powered on, the rectified BUS voltage ramps up. The capacitor (C_{VCC}) across the V_{CC} and RTN pins is charged by the BUS voltage through the internal startup circuit. Once V_{VCC} rises to $V_{VCC,ON}$, the internal blocks start operation. V_{VCC} will subsequently be pulled down by the power consumption of the circuitry until the auxiliary winding of the flyback transformer can supply sufficient energy to keep V_{VCC} greater than V_{VCC_OFF}.

The startup procedure is divided into two stages, as shown in Figure 3:

- C_{VCC} is charged during the t_{STC} stage.
- Output voltage is built up in the t_{STO} stage.

t_{STO} is typically much smaller than t_{STC}. Startup time t_{ST} includes both t_{STC} and t_{STO}.

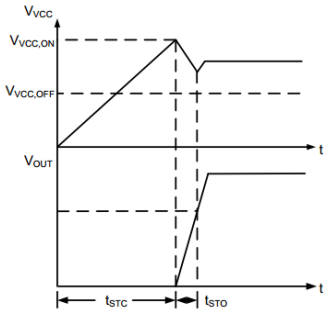


Figure 3. Startup

Quasi-Resonant (QR) Operation

QR operation provides low turn-on switching losses for the flyback converter.

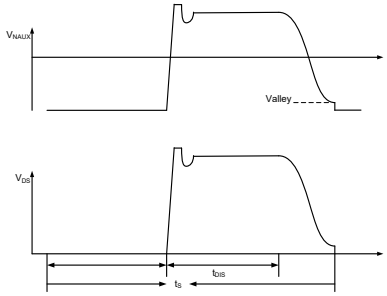


Figure 4. QR operation

The voltage across the drain and source of the primary MOSFET is reflected by the auxiliary winding of the flyback transformer. The ZCS pin uses a resistor-divider to detect the voltage across the auxiliary winding. The MOSFET will be switched on when the voltage across the drain and source of the primary MOSFET falls to the voltage valley.

Output Voltage Control

In order to achieve primary-side constant-voltage control, the output voltage is detected by the auxiliary winding voltage.

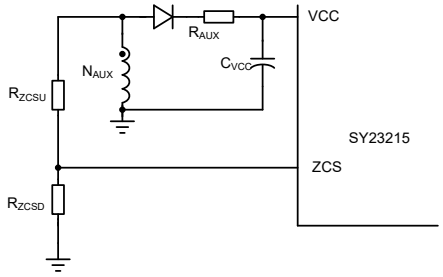


Figure 5. ZCS pin connection

As shown in Figure 5, the voltage across the auxiliary winding during OFF time is:

$$V_{AUX} = (V_{OUT} + V_{D\_F}) \times \frac{N_{AUX}}{N_S} \quad (1)$$

where N_{AUX} is the number of turns of auxiliary winding, N_S is the number of turns of secondary winding, and V_{D_F} is the forward voltage of the secondary power diode.

At the current zero-crossing point, V_{D_F} is nearly zero, so V_{OUT} is exactly proportional to V_{AUX}. The voltage of this point is sampled by the IC as the feedback of the output voltage. In theory, the resistor-divider is designed as follows:

$$\frac{V_{ZCS\_REF}}{V_{OUT}} = \frac{R_{ZCSD}}{R_{ZCSU} + R_{ZCSD}} \times \frac{N_{AUX}}{N_S} \quad (2)$$

where V_{ZCS_REF} is the internal voltage reference.

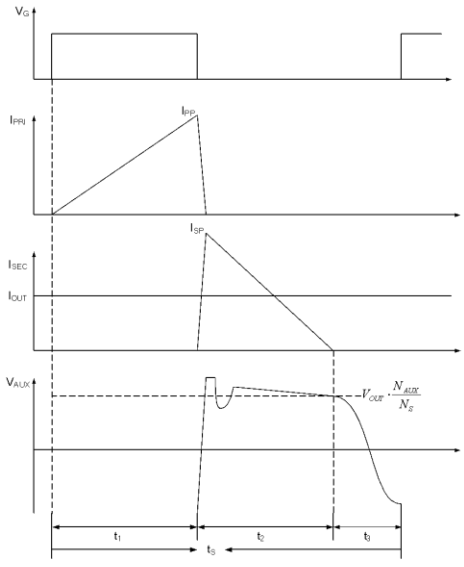


Figure 6. Auxiliary winding voltage waveforms

Fault Protection Modes

ZCS Pin Short Protection

The SY23215 protects against faults caused by a shorted ZCS pin. During startup, the voltage on the ZCS pin is monitored. In normal situations, the voltage on the ZCS pin reaches the sense-protection trigger level. When the ZCS voltage does not reach this level, the ZCS pin is shorted, and the protection is activated. The IC stops switching and discharges the V_{CC} voltage. Once V_{VCC} is below $V_{VCC,OFF}$, the IC will shut down and be charged again by V_{DD}.

CS Pin Short Protection

The SY23215 protects against faults caused by the CS pin shorting to RTN. During startup, the voltage on the CS pin is monitored. If the V_{CS} does not exceed 150mV after 2.5μs, the protection will be triggered, the device will stop switching, and the voltage at the V_{CC} pin will start falling. When the voltage drops below $V_{VCC,OFF}$, the IC will shut down and the V_{CC} will initiate a new startup sequence.

Output Overvoltage Protection

When the ZCS pin signal exceeds 1.45V, indicating an output overvoltage condition, the SY23215 will stop switching and discharge the V_{CC} voltage. Once V_{VCC} is below $V_{VCC,OFF}$, the IC will shut down and the V_{CC} will be charged again by V_{DD}.

V_{CC} Over Voltage Protection

When the V_{CC} voltage exceeds the threshold $V_{VCC,OVP}$, The SY23215 will stop switching, and the voltage at the V_{CC} pin will start falling. When the voltage drops below $V_{VCC,OFF}$, the IC will shut down and the V_{CC} will initiate a new startup sequence.

Output Short-Circuit Protection (SCP)

SCP will be triggered if V_{CC} falls below the threshold (7V, typical) $V_{CC,MIN}$ and the voltage of COMP is up to 2V. When the output is shorted to ground, the output voltage is clamped to zero, so V_{CC} will decrease as well. Once V_{VCC} is below $V_{VCC,MIN}$, the IC will shut down and the V_{CC} will be charged again by V_{DD}. To avoid overheating, a digital counter will record every time V_{CC} reaches $V_{VCC,ON}$. When the counter reaches 8, the SCP flag signal will be reset, as shown in Figure 7. Meanwhile, the device will continue attempting the startup sequence.

A filter resistor (R_{AUX}) is required to guarantee that SCP function is not affected by a voltage spike in the auxiliary winding.

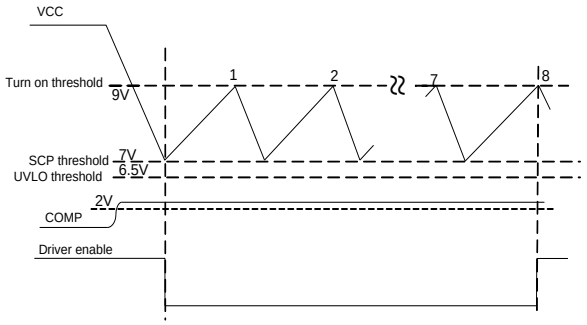


Figure 7. Output short-circuit protection

Power Device Design

MOSFET and Diode

The MOSFET and secondary-power diode maximum voltages are reached when the SY23215 is operating with the maximum input voltage and at full load:

$$V_{MOS\_DS\_MAX} = V_{DC\_MAX} + N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S \quad (3)$$

$$V_{D\_R\_MAX} = \frac{V_{DC\_MAX}}{N_{PS}} + V_{OUT} \quad (4)$$

where V_{DC_MAX} is maximum input DC voltage, N_{PS} is the turns ratio of the flyback transformer, V_{OUT} is the rated output voltage, V_{D_F} is the forward voltage of the secondary-power diode, and ΔV_S is the overshoot voltage clamped by the RCD snubber during OFF time.

The MOSFET and power-diode maximum currents are reached when the SY23215 is operating with minimum input voltage and at full load:

$$I_{MOS\_PK\_MAX} = I_{P\_PK\_MAX} \quad (5)$$

$$I_{MOS\_RMS\_MAX} = I_{P\_RMS\_MAX} \quad (6)$$

$$I_{D\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} \quad (7)$$

$$I_{D\_AVG} = I_{OUT} \quad (8)$$

where $I_{P\_PK\_MAX}$ and $I_{P\_RMS\_MAX}$ are maximum primary peak current and RMS current, which will be introduced later.

Transformer (N_{PS} and L_M)

N_{PS} is limited by the selected power MOSFET electrical characteristics:

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - V_{DC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \quad (9)$$

where $V_{MOS\_(BR)DS}$ is the breakdown voltage of the power MOSFET.

In quasi-resonant mode, each switching period cycle t_S consists of three parts: current-rising time t_1, current-falling time t_2, and quasi-resonant time t_3, as shown in Figure 8.

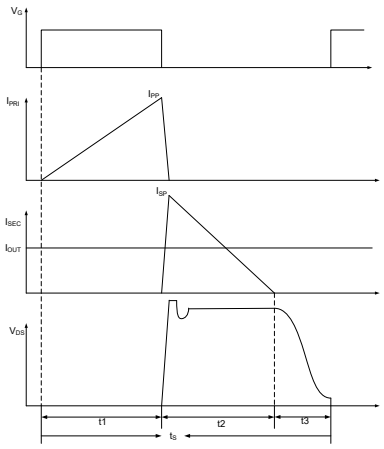


Figure 8. Switching waveforms

Maximum peak current through the MOSFET and the transformer occurs when the SY23215 is operating with minimum input DC RMS voltage, full load, and minimum switching frequency.

Once the minimum frequency $f_{S,MIN}$ is set, the inductance of the transformer can be calculated using the following steps:

1. Select NPS:

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - V_{DC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \quad (10)$$

2. Preset minimum frequency $f_{S,MIN}$
3. Compute inductor L_M and maximum primary peak current $I_{P\_PK\_MAX}$:

$$I_{P\_PK\_MAX} = \frac{2P_{OUT}}{\eta \times V_{DC\_MIN}} + \frac{2P_{OUT}}{\eta \times N_{PS} \times (V_{OUT} + V_{D\_F})} + \pi \sqrt{\frac{2P_{OUT}}{\eta} \times C_{Drain} \times f_{S\_MIN}}$$

(11)

$$L_M = \frac{2P_{OUT}}{\eta \times I_{P\_PK\_MAX}^2 \times f_{S\_MIN}} \quad (12)$$

where C_{DRAIN} is the parasitic capacitance at the MOSFET drain, η is the efficiency, and P_{OUT} is the rated full-load power.

4. Compute current-rising time t_1 and current-falling time t_2:

$$t_1 = \frac{L_M \times I_{P\_PK\_MAX}}{V_{BUS}} \quad (13)$$

$$t_2 = \frac{L_M \times I_{P\_PK\_MAX}}{N_{PS} \times (V_{OUT} + V_{D\_F})} \quad (14)$$

$$t_S = \frac{1}{f_{S\_MIN}} \quad (15)$$

5. Compute primary maximum RMS current $I_{P\_RMS\_MAX}$ for the transformer fabrication:

$$I_{P\_RMS\_MAX} = \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \times \sqrt{\frac{t_1}{t_S}} \quad (16)$$

6. Compute the secondary maximum peak current $I_{S\_PK\_MAX}$ and RMS current $I_{S\_RMS\_MAX}$ for the transformer fabrication:

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} \quad (17)$$

$$I_{S\_RMS\_MAX} = \frac{\sqrt{3}}{3} N_{PS} \cdot I_{P\_PK\_MAX} \cdot \sqrt{\frac{t_2}{t_S}} \quad (18)$$

Transformer Design (N_P, N_S, N_{AUX})

The design of the transformer follows the same steps as used for a generic flyback transformer, and includes the following parameters:

Necessary parameters	
Turns ratio	N_{PS}
Inductance	L_M
Primary maximum current	$I_{P\_PK\_MAX}$
Primary maximum RMS current	$I_{P\_RMS\_MAX}$
Secondary maximum RMS current	$I_{S\_RMS\_MAX}$

The steps are described below:

1. Select the magnetic core style and identify the effective area A_e.

2. Preset the maximum magnetic flux ΔB:

$$\Delta B = 0.22 \sim 0.26T$$

3. Compute primary turn N_P:

$$N_P = \frac{L_M \times I_{P\_PK\_MAX}}{\Delta B \times A_e} \quad (19)$$

4. Compute secondary turn N_S:

$$N_S = \frac{N_P}{N_{PS}} \quad (20)$$

5. Compute auxiliary turn N_{AUX}:

$$N_{AUX} = N_S \times \frac{V_{VCC}}{V_{OUT}} \quad (21)$$

where V_{VCC} is the nominal operating voltage of the V_{CC} pin (10V–12V is recommended).

6. Select an appropriate wire diameter. With $I_{P\_RMS\_MAX}$ and $I_{S\_RMS\_MAX}$, select an appropriate wire size, to make sure the current density ranges from 4A/mm² to 10A/mm².

7. If the winding area of the core and bobbin is too small, select a different core style with which can meet the requirements and re-run all the calculations until all requirements are met.

RCD Snubber for MOSFET

The power loss of the snubber P_{RCD} can be evaluated using the following equation:

$$P_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{\Delta V_S} \times \frac{L_K}{L_M} \times P_{OUT} \quad (22)$$

where N_{PS} is the turns ratio of the flyback transformer, V_{OUT} is the output voltage, V_{D_F} is the forward voltage of the power diode, ΔV_S is the overshoot voltage clamped by the RCD snubber, L_K is the inductor leakage, L_M is the inductance of the flyback transformer, and P_{OUT} is the output power.

The R_{RCD} is related to the power loss as follows:

$$R_{RCD} = \frac{(N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S)^2}{P_{RCD}} \quad (23)$$

The C_{RCD} is related to the voltage ripple of the snubber ΔV_{C_RCD} as follows:

$$C_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{R_{RCD} \times f_S \times \Delta V_{C\_RCD}} \quad (24)$$

CLS Resistor Selection

A resistor from CLS to V_{SS} programs the classification current per the 802.3at/af standard. The PD power ranges and corresponding resistor values are listed in Table 2. The power assigned should correspond to the maximum average power drawn by the PD during operation. The SY23215 supports class 0-4 power levels.

Table2. Class Resistor Selection

Class	Power at PD		Resistor
	Minimum (W)	Maximum (W)	
0	0.44	12.95	1270
1	0.44	3.84	243
2	3.84	6.49	137
3	6.49	12.95	90.9
4	13	25.5	63.4

APD Resistor Selection

Controlling the voltage at the APD pin forces power to come from an external adapter connected from V_{DD} to RTN by turning on the hot-swap switch. Select the APD divider resistors per Equation 25 where R_{APD_U}, R_{APD_D} are the upper and lower resistors in the APD resistor divider, V_{ADPTR_ON} is the desired adapter voltage that enables the APD function as adapter voltage rises, and V_{APD_EN} is the APD enable threshold voltage.

$$R_{APD\_U} = R_{APD\_D} \times (V_{APDTR\_ON} - V_{APD\_EN}) / V_{APD\_EN} \quad (25)$$

DEN Resistor Selection

The 802.3at/af standard specifies a detection signature resistance (R_{DEN}) between 23.7kΩ and 26.3kΩ. Connect a 24.9kΩ resistor from DEN to V_{DD} to provide the PoE detection signature.

V_{DD} to V_{SS} ESD Protection

Use of a transient-voltage suppressor (TVS) diode is recommended (see D1 in Figure 9). If an adapter is connected between the V_{DD} and RTN nodes, ringing caused by the input cable inductance along with the internal pin capacitance can occur. Adequate capacitive filtering or a TVS must keep this voltage below the absolute maximum ratings. Outdoor transient levels or special applications might require additional protection. In addition, For reliable operation when using a power adapter, please add a Schottky diode between RTN and V_{SS} (D2 in Figure 9).

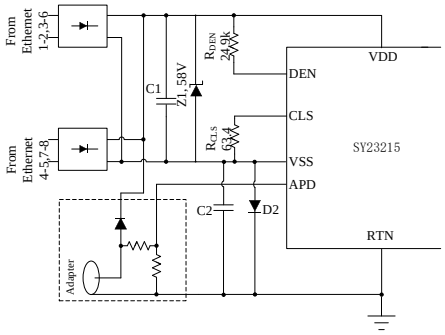


Figure 9. V_{DD} to V_{SS} ESD protection

Input Bypass Capacitor Selection

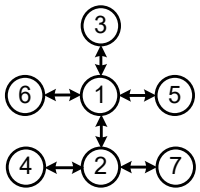
The 802.3at/af standard specifies an input bypass capacitor of 0.05μF to 0.12μF. A 0.1μF, 100V ceramic capacitor between V_{DD} and V_{SS} (C1 in Figure 9) is typically used when the input power source is PSE only (C2 not connected).

If an external adapter is also used to power the device, connect a capacitor (C1 in Figure 9) between V_{DD} and V_{SS}, and a capacitor (C2 in Figure 9) between RTN and V_{SS}. The recommended values for both C1 and C2 are 0.047μF/100V.

Layout Design

For optimal design, follow these PCB layout considerations:

- To achieve better EMI performance and reduce line frequency ripple, connect the output of the bridge rectifier to the BUS line capacitor first, then to the switching circuit.
- Minimize the area of the following switching circuit loops: primary power loop, secondary loop, and auxiliary power loop.
- Connect the bias supply trace to the bias supply capacitor first, instead of the GND pin. Place the bias supply capacitor next to the device.
- Keep the loop between the source pin, the current-sample resistor, and the GND pin as small as possible.
- Place the resistor-divider connected to the ZCS pin next to the IC.
- Connect the primary ground as follows:



Ground ①: Ground of BUS capacitor.

Ground ②: Ground of bias supply capacitor.

Ground ③: Ground node of auxiliary winding.

Ground ④: Ground node of divider resistor.

Ground ⑤: Primary ground node of Y capacitor.

Ground ⑥: Ground node of current-sample resistor.

Ground ⑦: Ground of IC GND.

Design Notes:

1. At no load, the secondary-side diode freewheeling time should be more than T_{OFF_MIN}.
2. V_{CC} voltage should be greater than 10V for all conditions.
3. At heavy load, the peak-to-peak voltage at the ZCS pin should be less than approximately 100mV after T_{OFF_MIN} time. This can be guaranteed by decreasing the leakage inductance and using the proper RCD snubber.
4. R_{ZCSU} is the upper resistor of the divider. Normally, its recommended value is between 30kΩ and 91kΩ.
5. Because the SY23215 has a built-in constant voltage (CV) loop, in order to ensure stability, choose an output capacitor value that makes C_{OUT} x (V_O/I_O) close to 5mS. For example, in the case of 12V/1A output, C_{OUT} = 5m/12 = 420μF. Select the output capacitor value in the range of 440μF to 470μF. The switching frequency ripple should also be considered. Reducing the ripple can be achieved by increasing the capacitance or using lower ESR capacitors. Using capacitors in parallel can help with reducing the overall ESR of the capacitor bank, enabling a ripple reduction.

Design Example

A step-by-step design example of a typical application is shown below.

1. Design specification.

Design Specification			
V_{DC}	42.5V–57V	V_{OUT}	12V
I_{OUT}	2.1A	η	82%

2. Transformer Design (N_{PS}, L_M).

Refer to the Power Device Design:

Conditions			
$V_{DC,MIN}$	42.5V	V_{DC_MAX}	57V
ΔV_S	50V	$V_{MOS\_(BR)DS}$	150V
$P_{OUT(max)}$	25W	V_{D_F}	1V
C_{DRAIN}	50pF	$f_{S,MIN}$	150kHz

a. Compute turns ratio N_{PS} first:

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - V_{DC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}}$$

$$= \frac{150V \times 0.9 - 57V - 50V}{12V + 1V}$$

$$= 2.15$$

N_{PS} is set to N_{PS} = 2

b. $f_{S,MIN}$ is preset: $f_{S,MIN}$ = 150kHz

c. Compute inductor L_M and maximum primary peak current $I_{P\_PK\_MAX}$:

$$I_{P\_PK\_MAX} = \frac{2P_{OUT}}{\eta \times V_{DC\_MIN}} + \frac{2P_{OUT}}{\eta \times N_{PS} \times (V_{OUT} + V_{D\_F})} + \pi \sqrt{\frac{2P_{OUT}}{\eta} \times C_{Drain} \times f_{S\_MIN}}$$

$$= \frac{2 \times 25W}{82\% \times 42.5V} + \frac{2 \times 25W}{82\% \times 2 \times (12V + 1V)} + 3.14 \times \sqrt{\frac{2 \times 25W}{82\%} \times 50pF \times 150kHz}$$

$$= 1.435A + 2.345A + 0.0671A$$

$$= 3.847A$$

$$L_M = \frac{2P_{OUT}}{\eta \times I_{P\_PK\_MAX}^2 \times f_{S\_MIN}}$$

$$= \frac{2 \times 25W}{0.82 \times (3.847A)^2 \times 150KHz}$$

$$= 27.5\mu H$$

Set: L_M = 28µH

d. Compute current-rising time t_1 and current-falling time t_2.

$$t_1 = \frac{L_M \times I_{P\_PK\_MAX}}{V_{DC\_MIN}} = \frac{28\mu H \times 3.847A}{42.5V} = 2.534\mu s$$

$$t_2 = \frac{L_M \times I_{P\_PK\_MAX}}{N_{PS} \times (V_{OUT} + V_{D\_F})} = \frac{28\mu H \times 3.847A}{2 \times (12V + 1V)} = 4.143\mu s$$

$$t_3 = \pi \times \sqrt{L_M \times C_{Drain}} = \pi \times \sqrt{28\mu H \times 50pF} = 0.117\mu s$$

$$t_S = t_1 + t_2 + t_3 = 2.534\mu s + 4.143\mu s + 0.117\mu s = 6.794\mu s$$

e. Compute primary maximum RMS current $I_{P\text{-}RMS\text{-}MAX}$ for the transformer fabrication:

$$I_{P\_RMS\_MAX} = \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \times \sqrt{\frac{t_1}{t_S}} = \frac{\sqrt{3}}{3} \times 3.847A \times \sqrt{\frac{2.534\mu s}{6.794\mu s}} = 1.356A$$

f. Compute secondary maximum peak current $I_{S\_PK\_MAX}$ and RMS current $I_{S\_RMS\_MAX}$ for the transformer fabrication:

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} = 2 \times 3.847A = 7.694A$$

$$I_{S\_RMS\_MAX} = N_{PS} \times \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \times \sqrt{\frac{t_2}{t_S}} = 2 \times \frac{\sqrt{3}}{3} \times 3.847A \times \sqrt{\frac{4.143\mu s}{6.794\mu s}} = 3.469A$$

3. Select the secondary power diode.

Refer to the Power Device Design:

Known conditions at this step			
V_{DC_MAX}	57V	N_{PS}	2
V_{OUT}	12V	V_{D_F}	1V

Compute the voltage and the current stress of secondary-power diode:

$$V_{D\_R\_MAX} = \frac{V_{DC\_MAX}}{N_{PS}} + V_{OUT}$$
$$= \frac{57V}{2} + 12V$$
$$= 40.5V$$

$$I_{D\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} = 2 \times 3.847A = 7.694A$$

$$I_{D\_AVG} = 2.1A$$

4. Select the current-sense resistor.

Known conditions at this step	
N_{PS}	2
V_{ILIM}	1V

a. The current-sense resistor is:

$$R_{SMAX} = \frac{V_{ILIM}}{I_{P\_PK\_MAX}}$$
$$= \frac{1V}{3.847A}$$
$$= 0.26\Omega$$

b. Set R_S (R_S = 0.25Ω).

5. Set the ZCS pin:

Refer to V_{OUT}.

a. Identify R_{ZCSU} needed for line regulation.

Parameters Designed	
R_{ZCSU}	56kΩ

b. Compute R_{ZCSD}

Conditions			
V_{OUT}	12V	V_{ZCS_REF}	1.2V
R_{ZCSU}	56kΩ	N_S	9
N_{AUX}	9		

$$R_{ZCSD} = \frac{R_{ZCSU}}{\frac{V_{OUT} \times N_{AUX}}{(V_{ZCS\_REF} + 0.1V) \times N_S} - 1} = \frac{56K}{\frac{12V \times 9}{(1.2V + 0.1) \times 9} - 1} = 6.8K$$

c. Set R_{ZCSD} (R_{ZCSD} = 6.8kΩ).

Note: In consideration of the internal circuit propagation delay, 0.1V is added to V_{ZCS_REF} for compensation.

6. Set the DEN pin. Connect a 24.9kΩ resistor from DEN to V_{DD}.

7. Set the CLS pin. Connect a 63.4Ω resistor from CLS to V_{SS}.

8. Set the APD pin. Set R_{APD2} = 0 to get POE function only.

Complete design:

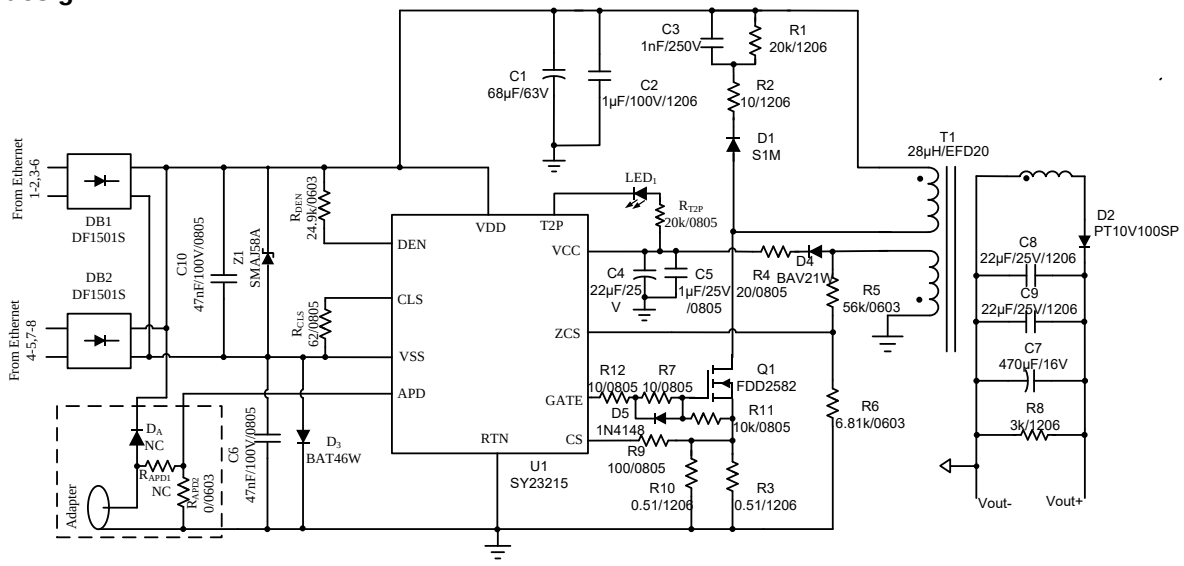
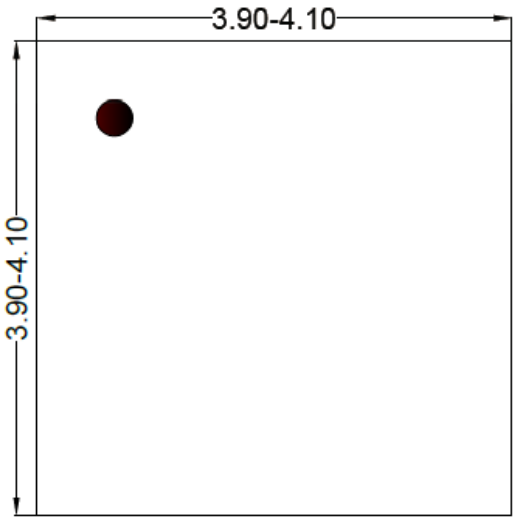
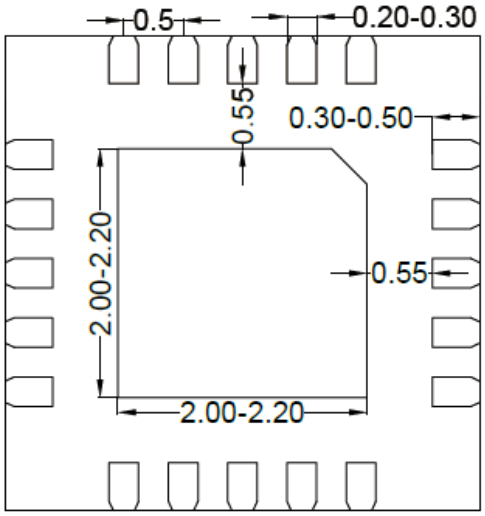


Figure 10. Design example, V_{IN} = 42.5V-57V (PoE input), V_{OUT} = 12V @ 2.1A

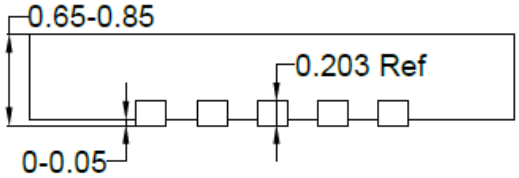
QFN4x4-20 Package Outline and PCB Layout



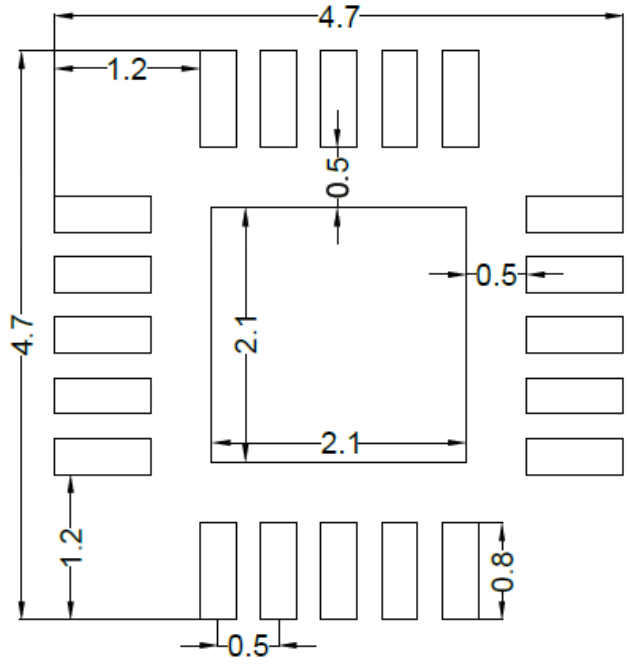
Top View



Bottom View



Front View

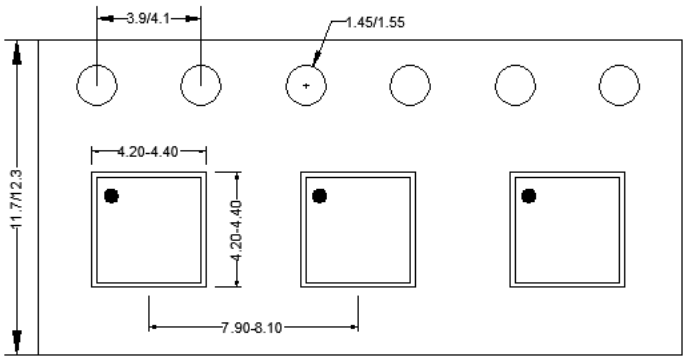


Recommended PCB layout
(Reference only)

***Note**: All dimensions are in millimeters and exclude mold flash and metal burr.*

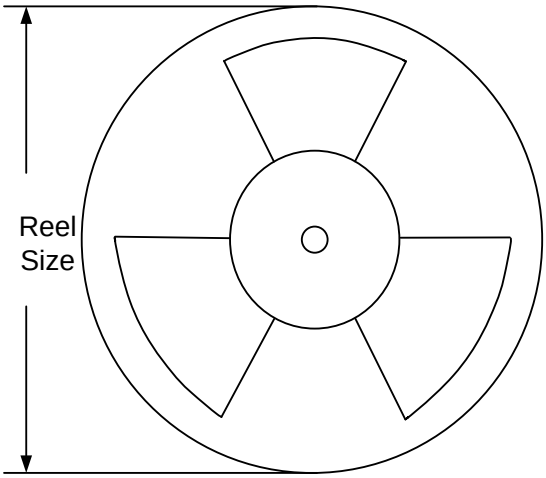
Taping and Reel Specification

QFN4×4 Taping Orientation



Feeding direction ↑

Carrier Tape and Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel (pcs)
QFN4x4	12	8	13"	400	400	5000

Others: NA