SY22818C

CCM+QR SSR Flyback Controller

General Description

The SY22818C is a peak current mode SSR Flyback controller targeting at fast charger application featuring a wide output range. It has a wide VCC operating range (10~90V) which can eliminate the external LDO circuit. It has the HV start-up circuit and low quiescent current which can achieve the low no-load loss. The SY22818C adopts the pseudo fixed frequency control to eliminate the slope compensation under CCM, which combines the CCM and QR mode together to achieve the optimized efficiency.

The SY22818C provides the comprehensive and reliable protections including BO, input OVP, output OVP/UVP, VCC OVP, OLP, external OTP, OTP, Secondary SR MOS SCP, etc.

The SY22818C is available with compact SO8 package.

Features

- Wide VCC Operating Range: 10~90V
- HV Start up
- Mixed CCM+QR Control Strategy
- Pseudo Fixed Frequency Control to Eliminate Slope Compensation under CCM
- 65kHz Fixed Switching Frequency under CCM
- 90kHz Switching Frequency Limit under QR Mode
- Frequency Fold Back for High Average Efficiency
- Minimum Switching Frequency Limited to 28kHz
- Burst Control for High Light Load Efficiency
- Comprehensive Protections Including BO, Input OVP, Output OVP/UVP, VCC OVP, OLP, External OTP, OTP, Secondary SR MOS SCP, etc.
- Gate Drive Capability: +70mA/-500mA
- Internal Soft-start Process
- Compact Package: SO8

Applications

- Fast Chargers
- AC/DC Adapters

Typical Applications

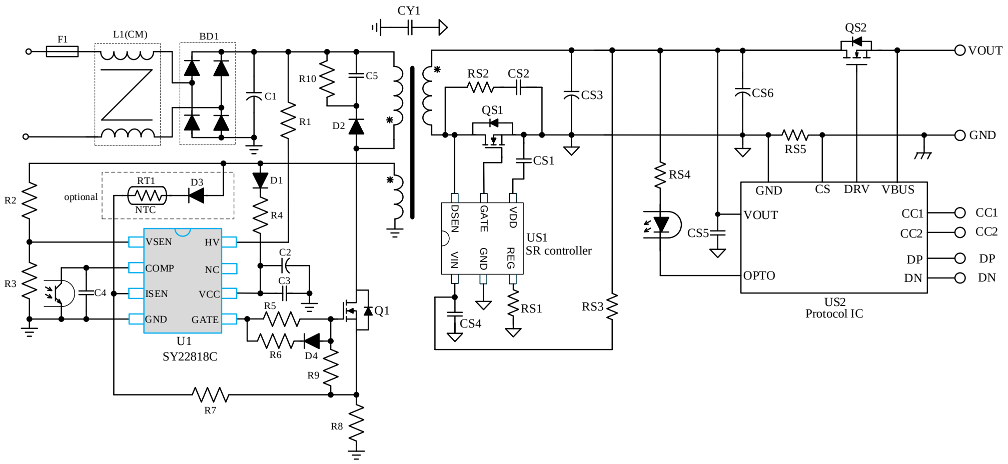
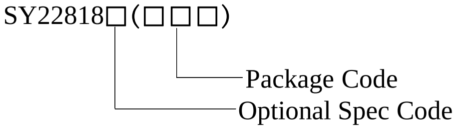
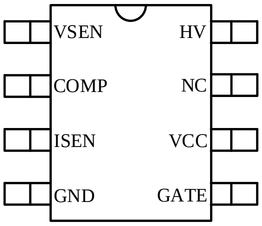


Fig.1 Typical Application Circuit

Ordering Information





Pinout (Top view)

Ordering Number	Package	Top Mark
SY22818CFAP	SO8	AADAxyz

x=year code, y=week code, z= lot number code

Pinout

Pin Number	Pin Name	Pin Description
1	VSEN	Multiple functions including valley detecting, input voltage sense and output voltage sense.
2	COMP	This pin is connected to an opto-coupler for output voltage feedback.
3	ISEN	Primary peak current sense and programmable external OTP.
4	GND	Ground.
5	GATE	Gate drive.
6	VCC	Power supply.
7	NC	
8	HV	High voltage starts up.

Block Diagram

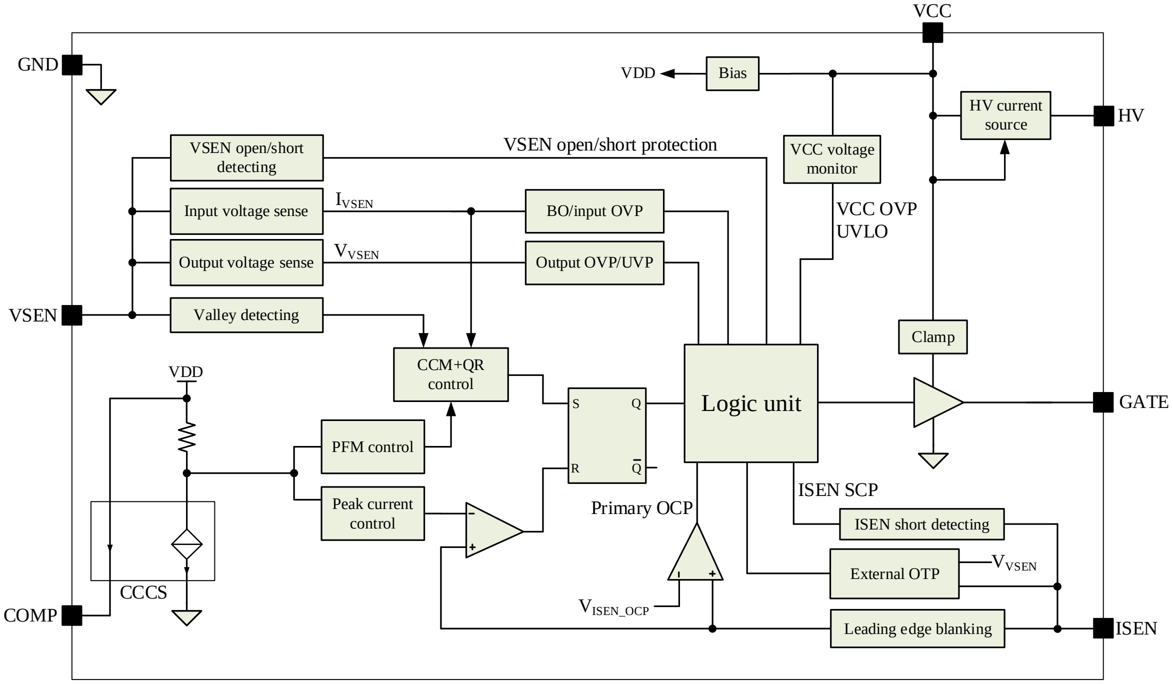


Fig.2 Block Diagram

Absolute Maximum Ratings (Note 1)

HV-- -0.3V~700V
VCC--- -0.3V~100V
GATE-- -0.3V~15V
VSEN, ISEN-- -0.3V~7V
COMP --- -0.3V~3.6V
Power Dissipation, at T_A = 25°C SO8 -------------------------1.1W
Package Thermal Resistance (Note 2)
SO8, θ_{JA}---125°C/W
SO8, θ_{JC}---60°C/W
Junction Temperature Range ---------------------------- -45°C to 150°C
Lead Temperature (Soldering, 10 sec.) ------------------- 260°C
Storage Temperature Range ----------------------------- -65°C to 150°C

Recommended Operating Conditions

V_{VCC}--- 10V~90V
Junction Temperature Range ---------------------------- -40°C to 125°C
Ambient Temperature Range ----------------------------- -40°C to 105°C

Electrical Characteristics

(V_{VCC} = 12V (Note 3), T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
HV Pin Section						
Break Down Voltage	V_{HV_BR}		700			V
Leakage Current	I_{HV_LK}	V_{HV}=700V_{DC}			2	μA
HV Current to Charge VCC	I_{HV}	V_{HV}=400V_{DC}		2.3		mA
VCC Pin Section						
Turn on Threshold	V_{VCC_ON}	V_{VCC} rising up	17	18	19	V
HV Current Source Enable Threshold	V_{VCC_MIN}	V_{VCC} falling down	8.35	9.0	9.65	V
Turn off Threshold	V_{VCC_OFF}	V_{VCC} falling down	7.45	8.0	8.55	V
OVP Threshold	V_{VCC_OVP}		90	94	100	V
Current Sink under Over Voltage Condition	I_{VCC_OVP}	V_{VCC}=V_{VCC_OVP}+0.1V	2	3	4	mA
Start-up Current	I_{VCC_ST}	V_{VCC}=V_{VCC_ON}-0.5V			100	μA
Quiescent Current	I_{VCC_Q}		200	280	360	μA
Operating Current	I_{VCC_OPT}	V_{VCC}=20V, C_L=1nF, F_{SW}=65kHz		2.2		mA
Current Sink under Fault Condition	I_{VCC_FAULT}		0.45	0.65	0.85	mA
ISEN Pin Section						
Max Peak Current Limit	V_{ISEN_MAX}		470	500	530	mV
Min Peak Current Limit	V_{ISEN_MIN}		115	138	160	mV
Primary OCP Threshold	V_{ISEN_OCP}		620	650	680	mV
Leading Edge Blanking	T_{ISEN_LEB}		260	430	600	ns
Blanking Time for ISEN Short Detecting	$T_{ISENSCP\_BLK}$	Low line condition	2.6	3.9	5.2	μs
Threshold Voltage for ISEN Short Detecting	V_{ISEN_SCP}		35	50	65	mV

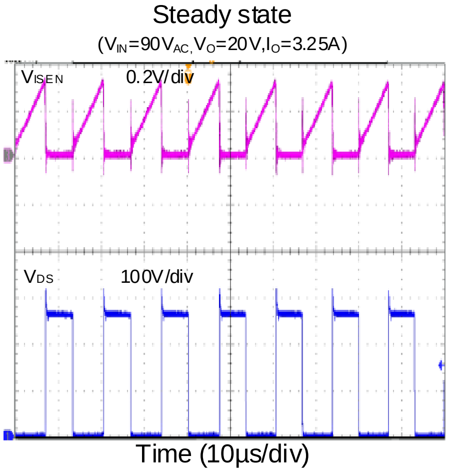
Ratio of External OTP Threshold to V_{VSEN}	$K_{EXOTP/VSEN}$			0.5		/
VSEN Pin Section						
Blanking Time for Output Voltage Sense after MOS is Turned Off	T_{VOSEN_BLK}	I_{COMP}=120uA	1	1.45	1.9	µs
Output OVP Threshold	V_{VSEN_OVP}		1.9	2.0	2.1	V
Output UVP Threshold	V_{VSEN_UVP}		125	150	175	mV
Output UVP Blanking Time during Start up	T_{STBLK_UVP}		10.8	17.8	24.5	ms
Brown Out Threshold Current	I_{BO}		90	100	110	µA
Brown In Hysteresis Current	I_{BI_HYS}			11		µA
Brown Out Debounce Time	T_{BO_DBC}		44	64	82	ms
High Line Condition (Force QR) Threshold Current	I_{LINE_H}		270	300	330	µA
Back to Low Line Condition Hysteresis Current	$I_{LINE\_L\_HYS}$			55		µA
Input OVP Threshold Current	I_{OVP}		484	540	596	µA
COMP Pin Section						
OLP Debounce Time	T_{OLP_DBC}		44	64	82	ms
Switching Frequency Section						
Frequency under CCM	F_{SW_CCM}		60	65	70	kHz
Frequency Limit under QR Mode	$F_{SW\_MAX\_QR}$		80	90	100	kHz
Minimum Switching Frequency	F_{SW_MIN}		20	28	36	kHz
Frequency Modulation Amplitude	$A_{FSW\_MOD\_AMP}$	Under CCM		±6%		
Frequency Modulation Period	T_{FSW_MOD}			500		µs
Maximum On Time	T_{ON_MAX}		12	16.5	21	µs
Maximum Off Time	T_{OFF_MAX}		180	245	310	µs
GATE Pin Section						
High Level Clamp	V_{GATE_CLAMP}	V_{VCC}=20V	12	13.5	15	V
Max Source Current	I_{SOURCE_MAX}	C_L=1nF		70		mA
Max Sink Current	I_{SINK_MAX}	C_L=1nF		500		mA
Internal OTP Section						
OTP Threshold	T_{OTP}			150		°C
Hysteresis to Recovery	T_{OTP_HYS}			24		°C
Soft Start Section						
Soft Start Time	T_{SS}		2.4	3.5	4.9	ms
Auto-recovery Control						
Re-start Timer	T_{RST}		1.4	2	2.6	s

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

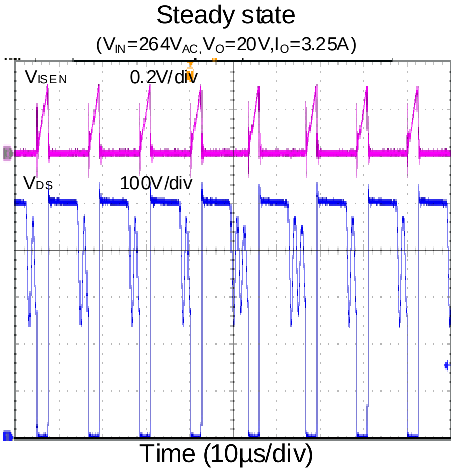
Note 2: θ_{JA} is tested on Silergy EVB, the EVB is two layer and 1oz copper is used.

Note 3: The increase VCC pin voltage gradually higher than V_{VCC_ON} voltage then turn down to 12V.

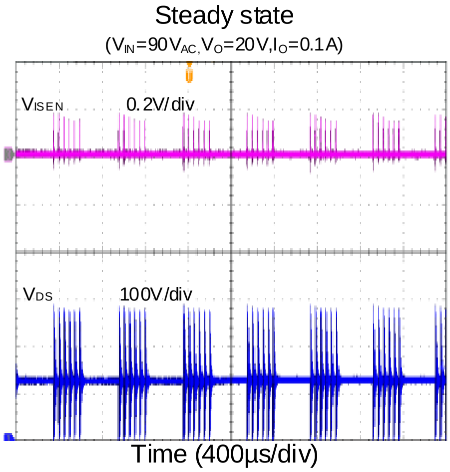
Typical Performance Characteristics


Steady state

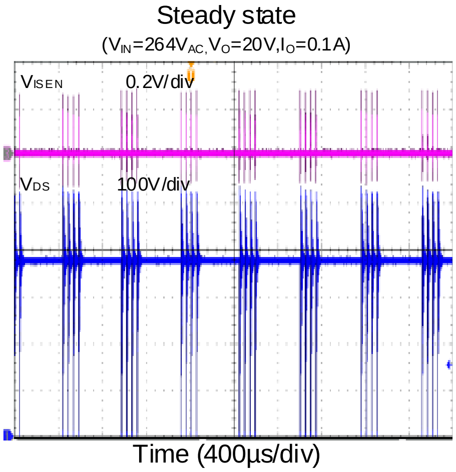
(V_{IN}=90V_{AC},V_O=20V,I_O=3.25A)


Steady state

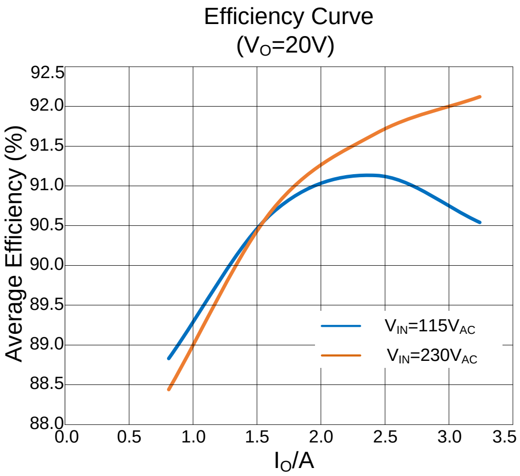
(V_{IN}=264V_{AC},V_O=20V,I_O=3.25A)


Steady state

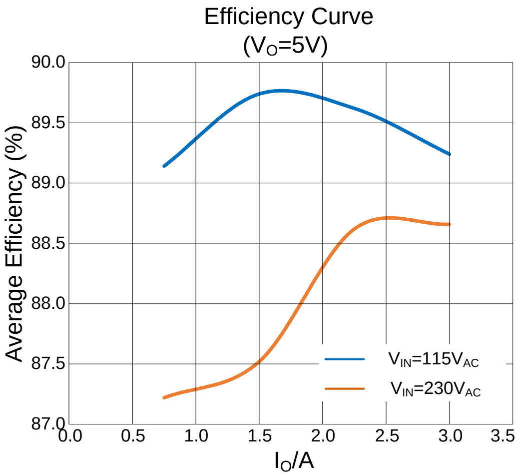
(V_{IN}=90V_{AC},V_O=20V,I_O=0.1A)


Steady state

(V_{IN}=264V_{AC},V_O=20V,I_O=0.1A)


Efficiency Curve

(V_O=20V)


Efficiency Curve

(V_O=5V)

Operation Principles

HV Start Up

The SY22818C has a high-voltage start up function to simplify the start-up circuit and achieve the low no load loss. The HV pin is recommended to connected to the BUS+ through a resistor R_{HV}. The R_{HV} is used to improve the reliability of the HV pin and the recommended resistance is 10kΩ~20kΩ.

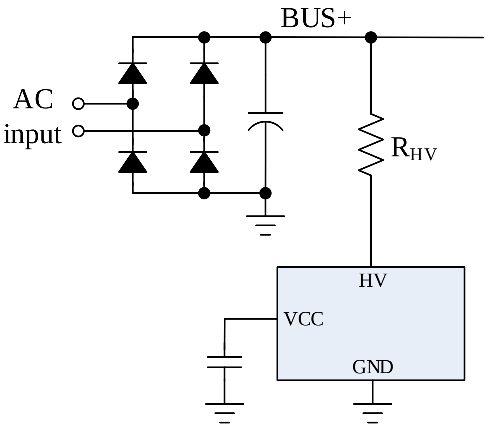


Fig.1 HV Start Up Circuit

Wide VCC Operating Range

The SY22818C has a wide VCC operating range from 10V to 90V, which is dedicated for the fast charger applications. The traditional external LDO circuit for the IC power supply can be eliminated to achieve the simple peripheral circuit. On the PCB layout， a ceramic capacitor C_1 is recommended to be mounted as close as possible to the VCC and GND pin of the IC.

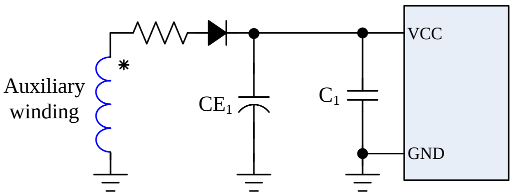


Fig.2 Simple IC Power Supply Circuit

CCM+QR Mixed Operating Principle

The SY22818C adopts the mixed control method that combines the CCM and QR mode together. The CCM frequency is fixed to 65kHz, while the QR mode frequency is limited to 90kHz. The transformer is designed that under the low line input and heavy load condition, the IC operates in CCM. While under the other conditions, the IC operates in QR mode (valley switching). Due to this mixed control method, the optimized efficiency and transformer size can be achieved.

Under the light load condition, the IC operates in Burst mode to further improve the light load efficiency. The Burst mode is controlled by COMP pin internal control voltage V_C. When the V_C is lower than the sleep mode threshold, the IC will stop switching and enter the sleep mode. Under the sleep mode, the current consumed by the IC is maintained to very low level (typical=280uA). When the V_C is higher than another exit sleep threshold, the IC will exit sleep mode and then resume normal operation. The lighter the load is, the longer the IC will stay in sleep mode.

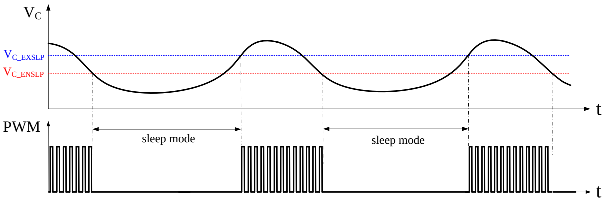


Fig.3 Timing Diagram of Burst Mode Control

Force QR at High Line Input Condition

If the secondary SR switcher is used，the CCM under the high-line input condition will not be generally allowed due to the lower converter efficiency and the higher voltage spike. The SY22818C adopts the forced QR mode control to guarantee the QR mode (valley turn on) under the high line input condition and steady state.

The SY22818C will sense the input voltage by the negative current I_{VSEN} of VSEN pin (flowing out of the VSEN pin), when the primary power MOS is turned on. When the primary power MOS is turned on, the VSEN pin will be internally clamped to 0V, since the negative voltage on auxiliary winding is proportional to the BUS voltage, the current flowing out of the VSEN pin will be proportional to BUS voltage. The SY22818C will compare the current flowing out of VSEN pin with the high-line threshold current I_{LINE_H} (typical=300uA). If the current flowing out of VSEN pin is larger than I_{LINE_H}, the input high-line condition will be recognized by the IC and the force QR mode will be enabled. When the VSEN pin negative current is lower than another threshold current I_{LINE_H}-$I_{LINE\_L\_HYS}$, the low-line input condition will be recognized by the IC and the force QR will be disabled, then the CCM operating will be allowed. The upper resistor of the VSEN pin resistor divider connected between the auxiliary windings will set input high-line condition threshold voltage. The input high-line condition threshold V_{IN_H} (RMS) is calculated as follows:

$$V_{IN\_H}=\frac{I_{LINE\_H}}{\sqrt{2}}\times\frac{N_P}{N_A}\times R_H$$

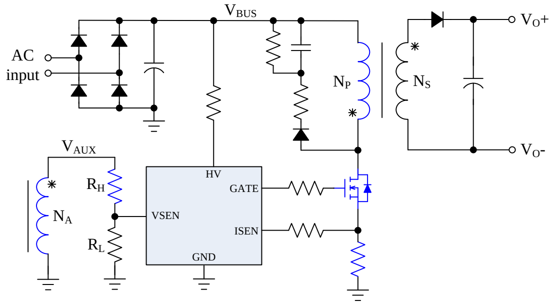


Fig.4 Illustration of Input Voltage Detecting

BO (Brown Out) Protection

During the Vin start-up, when the V_{VCC} rises to the V_{VCC_ON} threshold, the IC will check whether the input voltage is higher than the BI (brown in) threshold firstly. The 1st switching pulse is aimed to detect the input voltage condition. If the VSEN pin negative current I_{VSEN} is larger than the BI threshold, the IC will continue the normal switching. Otherwise, the IC will stop switching and enter auto-recovery mode.

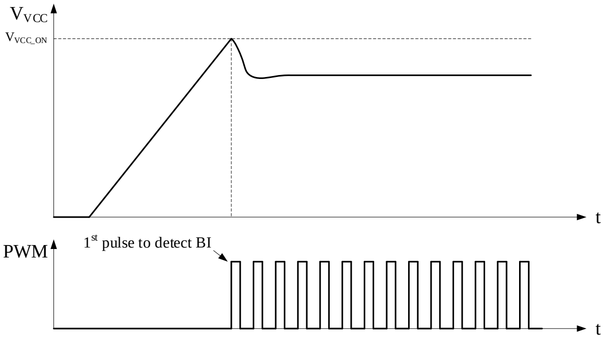


Fig.5 1st Detecting Pulse When Vin Start Up

Under the abnormal conditions, if the AC input voltage becomes lower and lower, the input current will become larger and larger, there is the high risk of AC components such as the NTC resistor, EMI choke and bridge rectifier which may be over heated and finally broken down. The SY22818C adopts the BO protection (input under voltage protection) to avoid over heating of the AC input components. It will detect the BUS voltage by the VSEN pin negative current I_{VSEN} when the primary power MOS is turned on. The IC will compare the I_{VSEN} with the internal BO threshold current I_{BO}, if the I_{VSEN} is lower than I_{BO}, and the sustained longer than BO debounce time T_{BO_DBC}, the IC will stop switching and enter the auto-recovery mode. The input BO threshold can be calculated as follows:

$$V_{IN\_BO}=\frac{I_{BO}}{\sqrt{2}}\times\frac{N_P}{N_A}\times R_H$$

Generally, the input BO threshold voltage is defined between 60Vac and 70Vac.

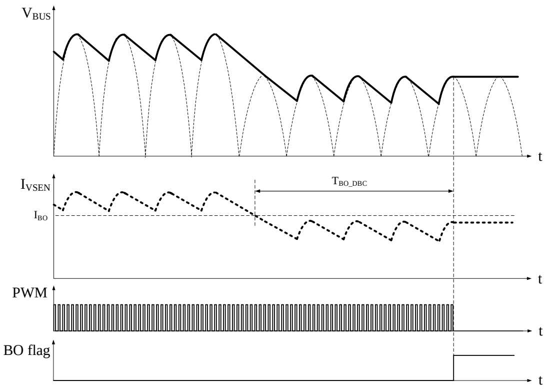


Fig.6 Timing Diagram of BO Protection

Input OVP

The VSEN pin negative current I_{VSEN} is also used to achieve the input OVP. If the I_{VSEN} is larger than the input OVP threshold current I_{OVP} and maintains for 4 consecutive switching cycles, the input OVP will be triggered, and the IC will stop switching and enter the auto-recovery mode. The input OVP threshold (RMS) can be calculated as follows:

$$V_{IN\_OVP}=\frac{I_{OVP}}{\sqrt{2}}\times\frac{N_P}{N_A}\times R_H$$

Programmable Output OVP/UVP

The SY22818C will sense output voltage by VSEN pin cycle by cycle, the programmable output OVP/UVP can be achieved. When the primary power MOS is turned off, the voltage on auxiliary winding V_{AUX} will be proportional to the output voltage V_O. The VSEN pin will sense the output voltage by a resistor divider (R_H and R_L) connected between the auxiliary windings.

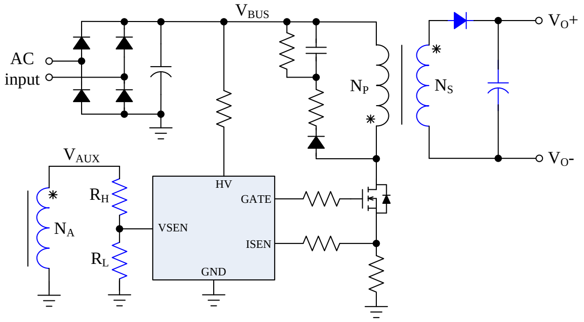


Fig.7 Circuit Diagram of Output Voltage Sense

The relationship between the VSEN pin voltage and the output voltage is shown as follows:

$$V_{VSEN}=V_O\cdot\frac{N_A}{N_S}\cdot\frac{R_L}{R_H+R_L}$$

Since the voltage spike will appear on the VSEN pin when the primary side power MOS is turned off as shown in below figure, to avoid false trigger of output OVP by the voltage spike, a blanking time T_{VOSEN_BLK} is adopted. The output voltage will only be sampled after the T_{VOSEN_BLK} elapse. The primary side RCD snubber should be carefully tuned to make sure that the voltage spike sustained time will not exceed T_{VOSEN_BLK}.

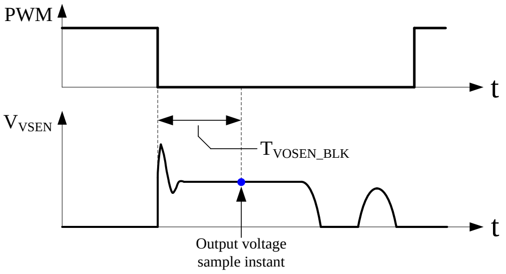


Fig.8 Illustration of Blanking Time for Output Voltage Sense

When the VSEN pin voltage rises above the OVP threshold V_{VSEN_OVP}, the IC will stop switching and enter the auto-recovery mode. The output OVP threshold is calculated as follows:

$$V_{O\_OVP}=V_{VSEN\_OVP}\cdot\frac{N_S}{N_A}\cdot\frac{R_H+R_L}{R_L}$$

For the fast charger applications, the output voltage varies according to the protocol controller, so the output OVP level should be determined by the maximum output voltage. For example, a fast charger claims the output voltage range from 3.3V to 20V, then the output OVP level will be equal to 20V multiplied by 120% (V_{O_OVP}=24V).

Note: The VSEN pin upper resistor R_H should be determined firstly according to the input BO threshold voltage (customer predefined), and then the lower resistor R_L of VSEN pin resistor divider is calculated according to the below equation.

$$R_L=R_H\cdot\frac{1}{\frac{N_A}{N_S}\cdot\frac{V_{O\_OVP}}{V_{VSEN\_OVP}}-1}$$

Programmable External OTP

The SY22818C features the programmable external OTP on ISEN pin. The circuit diagram is shown as fig.9. A fast-switching signal diode D_1, a NTC resistor RT_1 and a fine tune resistor R_{TUNE} are used to achieve the external OTP. When the primary power MOS is turned off, the volage on auxiliary winding will be proportional to the output voltage. The relationship between the ISEN pin voltage and the output voltage is shown as below equation:

$$V_{ISEN}=(\frac{N_A}{N_S}\cdot V_O-V_{D1})\cdot\frac{R_{OCP}+R_{ISEN}}{R_{RT1}+R_{TUNE}+R_{OCP}+R_{ISEN}}$$

For the fast charger applications, the output voltage varies within a specified range, e.g., 3.3~20V. To achieve the constant external OTP threshold which is not related with the output voltage, the adaptive ISEN pin external OTP threshold is adopted. The SY22818C makes the ISEN pin external OTP threshold to be proportional with the VSEN pin voltage ($V_{ISEN\_EXOTP}=K_{EXOTP/VSEN}\cdot V_{VSEN}$), so the external OTP threshold will be a constant value regardless of the output voltage. The calculation of the external OTP threshold is shown as follows (ignoring the forward voltage drop of D_1):

$$R_{NTC(OTP)}=(R_{OCP}+R_{ISEN})\cdot(\frac{1}{K_{EXOTP/VSEN}}\cdot\frac{R_H+R_L}{R_L}-1)-R_{TUNE}$$

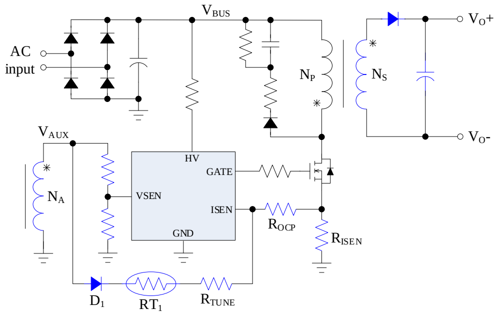


Fig.9 Circuit Diagram of External OTP

OLP (Over Load Protection)

When the output over load happens, the COMP pin internal voltage V_C will be pulled up to the high level, and the primary peak current will reach the maximum value. The SY22818C will compare the V_C with the internal OLP threshold, when the V_C is higher than the OLP threshold, a timer will begin to count. If the V_C is continuously higher than the OLP threshold resulted in OLP timer elapse, the SY22818C will stop switching and enter the auto-recovery mode.

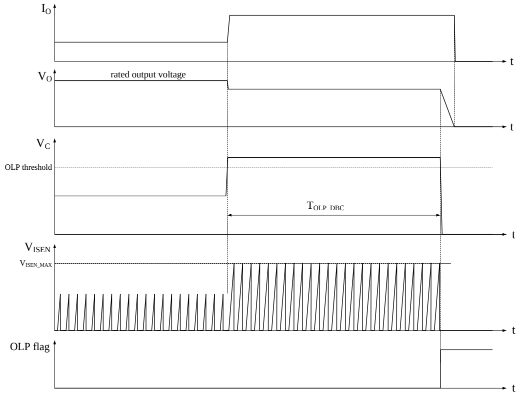


Fig.10 Timing diagram of OLP

Secondary SR MOS Short Circuit Protection

Under the secondary SR MOS short-circuit condition, when the primary power MOS is turned on, the primary current of the Flyback converter will increase with very high di/dt rate, during the ISEN pin leading edge blanking time, the primary peak current sense voltage V_{ISEN} will rise to a very high level without limit. The SY22818C adopts a primary OCP threshold V_{ISEN_OCP}, when the V_{ISEN} is larger than V_{ISEN_OCP} for 4 consecutive switching cycles, the secondary SR MOS short-circuit protection will be triggered, the IC will stop switching and enter auto-recovery mode.

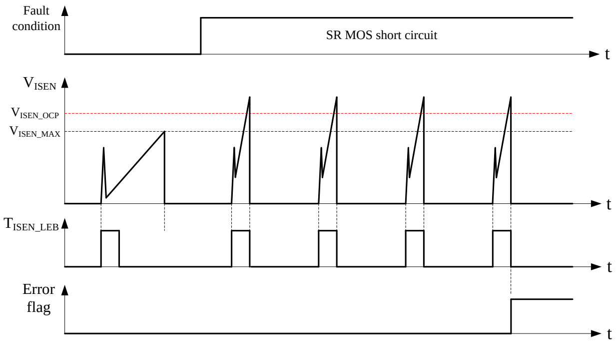


Fig.11 Timing Diagram of Primary OCP

ISEN Pin Short Circuit Protection

The SY22818C will check if the ISEN pin is shorted to GND during each switching cycle. When the primary side power MOS is turned on, a blanking time $T_{ISENSCP\_BLK}$ will be adopted, after this blanking time elapse, the IC will compare the ISEN pin voltage with the internal threshold voltage V_{ISEN_SCP} (typical=50mV). If the ISEN pin voltage is lower than this threshold voltage and lasts for 2 switching cycles, the ISEN pin shorted to GND fault is detected, the IC will stop switching and then enter the auto-recovery mode.

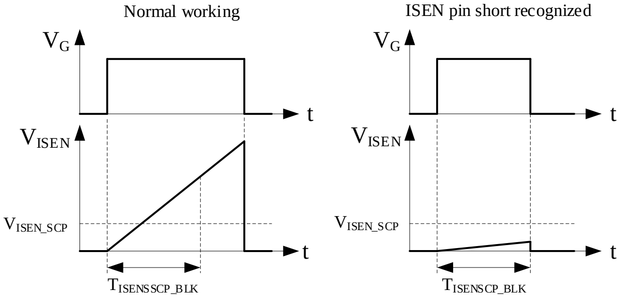


Fig.12 Illustration of ISEN Short Circuit Detecting

Internal OTP

The SY22818C monitors the die temperature in normal operating mode. Once the die temperature rises above the internal OTP threshold, the IC will stop switching and enter the auto-recovery mode. Once the die temperature drops below the recovery threshold (T_{OTP} -T_{OTP_HYS}), the IC will resume normal operating.

Power Supply Design Guide

BUS Capacitor Calculation

Generally, the bulk capacitor C_{BUS} is selected according to below rules:

1~2uF per watt of input power

$$C_{BUS\_MIN} = (1.0 \cdot P_{IN})\,uF$$

$$C_{BUS\_MAX} = (2.0 \cdot P_{IN})\,uF$$

To be more accurate, the BUS capacitor can be selected according to the predefined voltage ripple $\triangle V_{BUS}$ on BUS capacitor under the minimum AC input voltage and the full load condition as shown in the below figure.

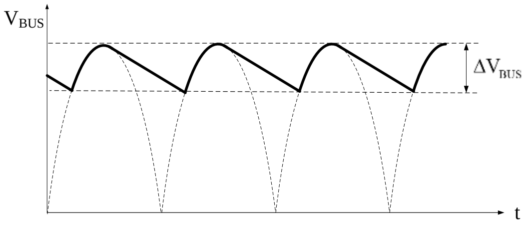


Fig.13 Illustration of Voltage Ripple on BUS Capacitor

When the voltage ripple $\triangle V_{BUS}$ is selected, the BUS capacitor can be calculated according to the following equation:

$$C_{BUS} = \frac{P_O}{\eta \cdot \pi \cdot f_{AC} \cdot \Delta V_{BUS}} \cdot \frac{\arcsin(1 - \frac{\Delta V_{BUS}}{\sqrt{2} \cdot V_{IN\_MIN}}) + \frac{\pi}{2}}{2\sqrt{2} \cdot V_{IN\_MIN} - \Delta V_{BUS}}$$

Where P_O is rated the output power, $\triangle V_{BUS}$ is predefined the voltage ripple on BUS capacitor, η is the converter efficiency, f_{AC} is the frequency of AC input voltage and V_{IN_MIN} is the minimum AC input voltage.

Transformer Parameter Calculation

1) Primary/Secondary Turns Ratio: N_{PS}

The maximum allowed N_{PS} is limited by the voltage stress of the primary power MOSFET:

$$N_{PS} \le \frac{V_{MOS\_BR} \cdot K_{DR} - \sqrt{2} \cdot V_{IN\_MAX} - \Delta V_{SN}}{V_{O\_MAX}}$$

Where V_{MOS_BR} is the breakdown voltage of the primary MOSFET, K_{DR} is V_{DS} de-rating factor of MOSFET, ΔV_{SN} is the voltage spike generated when the primary MOS is turned off, and V_{O_MAX} is the maximum output voltage.

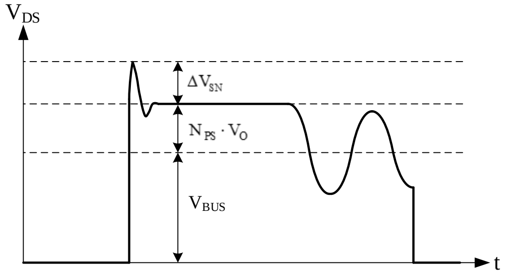


Fig.14 Illustration of Voltage Spike on Primary MOS

2) Primary Inductance: L_M

The primary inductance of transformer is related with the primary current ripple. Generally, the primary side current ripple is defined shown in the below figure. The current ripple factor is defined shown as follows:

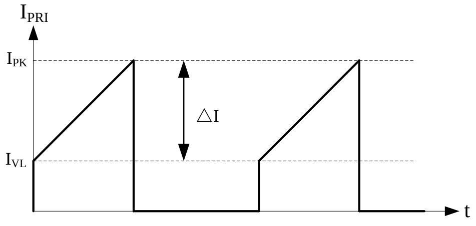


Fig.15 Illustration of Primary Current Ripple

$$K_{RP} = \frac{0.5 \cdot \Delta I}{I_{PK} - 0.5 \cdot \Delta I}$$

$K_{RP}<1$: CCM

$K_{RP}=1$: DCM (QR mode)

Generally, in order to get the optimized transformer size and the efficiency for universal input application, the CCM operating is selected under the low input and full load condition, the QR mode is selected under the high input and full load condition.

Based on the design experience, under the lowest input voltage and full load condition, it is recommended to choose K_{RP} between 0.3~0.5 for optimized performance. And for an initial start, K_{RP}=0.4 is selected. Once K_{RP} is selected, the primary inductance of transformer will be calculated according to the following equation:

$$L_M = \frac{V_{BUS\_MIN}{}^2 \cdot D_{MAX}{}^2 \cdot \eta}{2 \cdot P_O \cdot f_{SW} \cdot K_{RP}}$$

Where f_{SW} is the rated CCM switching frequency, P_O is the rated output power, η is the converter efficiency. D_{MAX} is the maximum duty cycle at V_{BUS_MIN} and the rated output power, and D_{MAX} is calculated according to the following equation:

$$D_{MAX} = \frac{N_{PS} \cdot V_O}{V_{BUS\_MIN} + N_{PS} \cdot V_O}$$

3) Turns of Primary Winding: N_P

(a) Select the magnetic core type, identify the effective cross-sectional area A_E

(b) Preset the maximum magnetic flux density B_{MAX} at the minimum BUS voltage and full load condition:

$$B_{MAX} = 0.2T \sim 0.3T$$

(c) Calculate maximum primary peak current I_{PK} at the rated output power:

$$I_{PK}=\frac{V_O\cdot I_O\cdot(1+K_{RP})}{V_{BUS\_MIN}\cdot D_{MAX}\cdot\eta}$$

(d) Calculate primary turns: N_P

$$N_P=\frac{L_M\cdot I_{PK}}{B_{MAX}\cdot A_E}$$

Where A_E is effective cross-sectional area of core

4) Turns of Secondary Winding: N_S

$$N_S=\frac{N_P}{N_{PS}}$$

5) Turns of Auxiliary Winding: N_A

Turns of the auxiliary winding is decided by the minimum VCC pin voltage under the normal operating. The minimum VCC pin voltage occurs under the minimum output voltage. Generally, the minimum VCC pin voltage should be guaranteed to be above 10V. Turns of the auxiliary winding can be initially calculated as follows:

$$N_A=\frac{10\cdot N_S}{V_{O\_MIN}}$$

The VCC pin voltage should be checked under the minimum output voltage and null-load condition, and the turns of auxiliary winding should be fine-tuned according to the actual test results.

Peak Current Sense Resistor Calculation

Under the minimum AC input voltage condition, when the BUS voltage is the maximum value and the primary peak current reaches the ISEN pin maximum setpoint, the maximum output current will be reached (OCP point). Under the OCP point, the primary peak current is calculated as follows:

$$D_{OCP}=\frac{N_{PS}\cdot V_O}{\sqrt{2}\cdot V_{IN\_MIN}+N_{PS}\cdot V_O}$$

$$I_{PK\_MAX}=\frac{P_O\cdot K_{OCP}}{\sqrt{2}\cdot V_{IN\_MIN}\cdot D_{OCP}\cdot\eta}+\frac{\sqrt{2}\cdot V_{IN\_MIN}\cdot D_{OCP}}{2\cdot L_M\cdot f_{SW}}$$

Where K_{OCP} is the OCP proportion, K_{OCP} is generally set to 120%~130%.

$$K_{OCP}=\frac{I_{O\_OCP}}{I_O}$$

After the maximum primary peak current calculated, the peak current sense resistor R_{ISEN} can be easily derived by the following equation:

$$R_{ISEN}=\frac{V_{ISEN\_MAX}}{I_{PK\_MAX}}$$

Where V_{ISEN_MAX} is ISEN pin current sense limit voltage (typical=0.5V).

The customer needs to fine tune the current sense resistor according to the converter actual OCP point. If the OCP point is larger than the target level, the R_{ISEN} should be tuned a little larger, If the OCP point is smaller than the target level, the R_{ISEN} should be tuned a little smaller.

Secondary SR MOS Selection

Under the conditions of the maximum BUS voltage and the maximum output voltage, the reverse voltage of the secondary rectification diode will reach the maximum level. The maximum value of SR MOS reverse voltage is calculated as follows:

$$V_{DS(SR)\_MAX}=\frac{\sqrt{2}\cdot V_{IN\_MAX}}{N_{PS}}+V_{O\_MAX}+V_{SPIKE}$$

Where V_{IN_MAX} is the maximum AC input voltage, N_{PS} is the primary/secondary turns ratio of transformer, V_{O_MAX} is maximum output voltage and V_{SPIKE} is the voltage spike generated when primary MOS is turned on.

Maximum peak current of SR MOS is calculated as equation below:

$$I_{D(SR)\_MAX}=I_{PK\_MAX}\cdot N_{PS}$$

Where I_{PK_MAX} is the maximum primary peak current at V_{BUS_MIN} and OCP point.

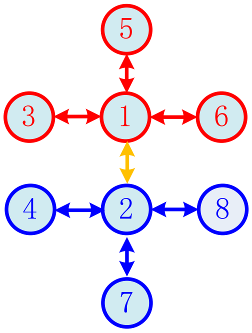
Layout Considerations

A proper PCB design must follow below guidelines:

(a) To achieve the good EMI performance and to reduce the line frequency voltage ripples, the output of the bridge rectifier should be connected to the BUS capacitor first, then to the switching circuit.

(b) The loop of all switching circuit should be kept as small as possible: primary power loop, secondary power loop and auxiliary power loop.

(c) The connection of primary ground is recommended as:



Ground ①: Ground of BUS capacitor

Ground ②: Ground of primary IC (SY22818C)

Ground ③: Ground node of auxiliary winding

Ground ④: Ground node of VSEN pin resistor divider

Ground ⑤: Ground of primary side Y capacitor

Ground ⑥: Ground of current sense resistor

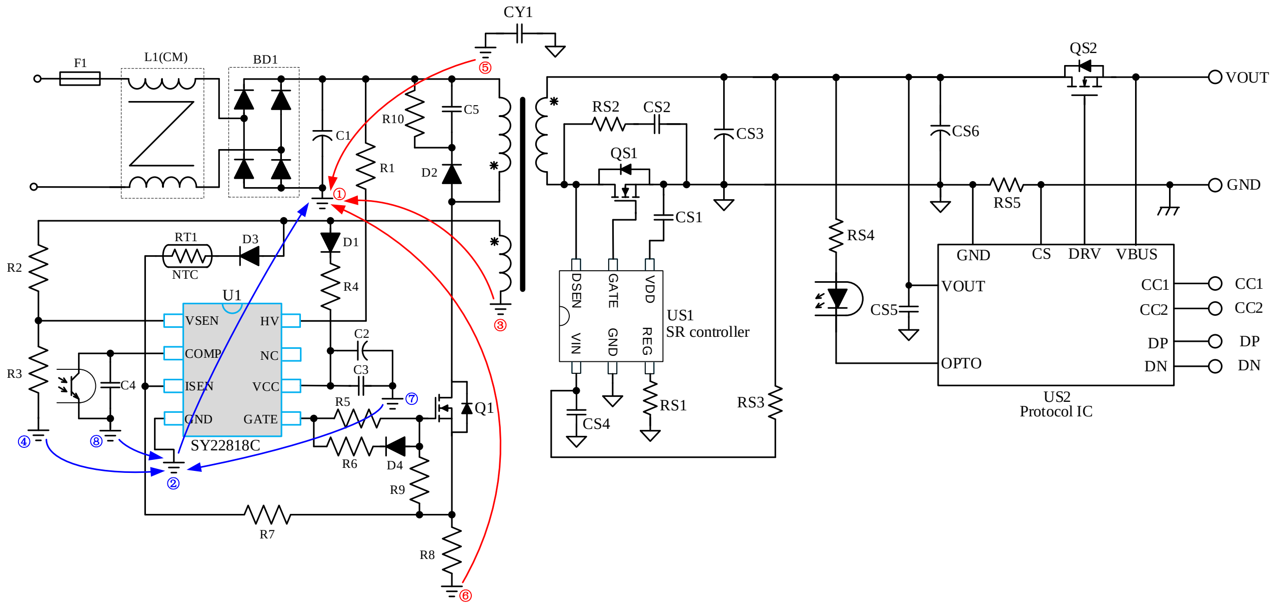
Ground ⑦: Ground of VCC pin capacitor

Ground ⑧: Ground of receiver of opto-coupler.

(d) Bias supply trace should be connected to the bias supply capacitor first and then to the GND pin. The bias supply capacitor should be put right beside the IC.

(e) The ceramic capacitor C3 should be mounted as close as possible to IC's VCC and GND pin.

(f) The resistor divider connected to VSEN pin is recommended to be put close to the IC.



Design Example of 65W Quick Charger

A design example of typical application is shown below step by step.

Input/Output Specification

Parameter	Symbol	Value
Input voltage range	V_{IN}	90~264Vac
AC input frequency	f_{AC}	50Hz
Rated output power	P_O	65W
PDO output	V_O	5V/3A, 9V/3A, 15V/3A, 20V/3.25A
Output OVP threshold	V_{O_OVP}	24V
OCP proportion	K_{OCP}	130%

Preset Parameter

Parameter	Symbol	Value
Break down voltage of power MOS	V_{MOS_BR}	650V
V_{DS} de-rating factor of power MOS	K_{DR}	90%
Spike on V_{DS} during power MOS turn off	ΔV_{SN}	80V
Converter efficiency	η	88%
Primary current ripple factor	K_{RP}	0.4
Voltage ripple on BUS capacitor	ΔV_{BUS}	63V
Input high line condition threshold	V_{IN_H}	180Vac
Transformer effective cross-sectional area	A_E	96.6 mm^2 (RM10)
Voltage spike on SR MOS	V_{SPIKE}	7V

1) BUS Capacitor Selection

Voltage ripple on BUS capacitor is set to: ΔV_{BUS}=63V

$$C_{BUS} = \frac{P_O}{\eta \cdot \pi \cdot f_{AC} \cdot \Delta V_{BUS}} \cdot \frac{\arcsin\left(1-\frac{\Delta V_{BUS}}{\sqrt{2}\cdot V_{IN\_MIN}}\right)+\frac{\pi}{2}}{2\sqrt{2}\cdot V_{IN\_MIN}-\Delta V_{BUS}} = \frac{65}{88\%\times 3.14\times 50\times 63}\cdot\frac{\arcsin\left(1-\frac{63}{\sqrt{2}\times 90}\right)+\frac{\pi}{2}}{2\sqrt{2}\times 90-63} = 81.8\mathrm{uF}$$

Select BUS capacitor: $C_{BUS} = 82\mathrm{uF}$

Minimum BUS voltage:

$$V_{BUS\_MIN} = \sqrt{2}\cdot V_{IN\_MIN} - \Delta V_{BUS} = \sqrt{2}\times 90 - 63 = 64\mathrm{V}$$

2) Transformer Design

(a)Calculate primary/secondary turns ratio: N_{PS}

Maximum output voltage: $V_{O\_MAX} = 20\mathrm{V}$

$$N_{PS} \le \frac{V_{MOS\_BR}\cdot K_{DR} - \sqrt{2}V_{IN\_MAX} - \Delta V_{SN}}{V_{O\_MAX}} = \frac{650\times 0.9 - \sqrt{2}\cdot 264 - 80}{20} = 6.58$$

N_{PS} is selected to: $N_{PS} = 6$

(b) Calculate maximum duty cycle D_{MAX} at minimum BUS voltage and rated output power condition

$$D_{MAX}=\frac{N_{PS}\cdot V_{O\_MAX}}{V_{BUS\_MIN}+N_{PS}\cdot V_{O\_MAX}}=\frac{6\times 20}{64+6\times 20}=65.2\%$$

(c) Calculate primary inductance: L_M

$$L_M=\frac{{V_{BUS\_MIN}}^2\cdot {D_{MAX}}^2\cdot \eta}{2\cdot P_O\cdot f_{SW}\cdot K_{RP}}=\frac{64^2\times 65.2\%^2\times 88\%}{2\times 65\times 65k\times 0.4}=453.3uH$$

Select $L_M=450uH$

(d)Calculate primary peak current at minimum BUS voltage and rated output power condition:

$$I_{PK}=\frac{P_O}{V_{BUS\_MIN}\cdot D_{MAX}\cdot \eta}+\frac{V_{BUS\_MIN}\cdot D_{MAX}}{2\cdot L_M\cdot f_{SW}}=\frac{65}{64\times 65.2\%\times 88\%}+\frac{64\times 0.652}{2\times 450u\times 65k}=2.48A$$

(e)Calculate primary winding turns: N_P

Transformer core effective cross-sectional area: $A_E=96.6\cdot 10^{-6}m^2$

Maximum allowed flux density at rated output power: $B_{MAX}=0.27T$

$$N_P=\frac{L_M\cdot I_{PK}}{B_{MAX}\cdot A_E}=\frac{450u\times 2.48}{0.27\times 96.6\times 10^{-6}}=42.8$$

Select primary winding turns: N_P=42

(f) Calculate secondary winding turns: N_S

$$N_S=\frac{N_P}{N_{PS}}=\frac{42}{6}=7$$

Select secondary turns: N_S=7

(g) Calculate auxiliary winding turns: N_A

Minimum VCC pin voltage is set to: $V_{VCC(AUX)}$=10V

$$N_A=\frac{V_{VCC(AUX)}\cdot N_S}{V_{O\_MIN}}=\frac{10\times 7}{3.3}=21.2$$

Select auxiliary winding turns: N_A=21

Note: Auxiliary winding turns should be fine-tuned according to actual VCC pin voltage under minimum output voltage and no-load condition

(h) If other transformer core type is selected, then re-calculate (e)~(g).

3) Current Sense Resistor Calculation:

(a)Calculate duty cycle under minimum input voltage (maximum BUS voltage): D_{OCP}

$$D_{OCP}=\frac{N_{PS}\cdot V_{O\_MAX}}{\sqrt{2}\cdot V_{IN\_MIN}+N_{PS}\cdot V_{O\_MAX}}=\frac{6\times 20}{\sqrt{2}\times 90+6\times 20}=48.5\%$$

(b)Calculate primary side peak current at OCP point: I_{PK_MAX}

$$I_{PK\_MAX}=\frac{P_O\cdot K_{OCP}}{\sqrt{2}\cdot V_{IN\_MIN}\cdot D_{OCP}\cdot\eta}+\frac{\sqrt{2}\cdot V_{IN\_MIN}\cdot D_{OCP}}{2\cdot L_M\cdot f_{SW}}=\frac{65\times130\%}{\sqrt{2}\times90\times48.5\%\times88\%}+\frac{\sqrt{2}\times90\times48.5\%}{2\times450u\times65k}=2.61A$$

(c)Calculate current sense resistor: R_{ISEN}

$$R_{ISEN}=\frac{V_{ISEN\_MAX}}{I_{PK\_MAX}}=\frac{0.5}{2.61}=0.192\Omega$$

Note: ISEN pin current sense resistor R_{ISEN} should be fine-tuned according to the actual OCP point.

4) Secondary SR MOS Selection

(a)Maximum reverse voltage calculation:

$$V_{DS(SR)\_MAX}=\frac{\sqrt{2}\cdot V_{IN\_MAX}}{N_{PS}}+V_{O\_MAX}+V_{SPIKE}=\frac{\sqrt{2}\times264}{6}+20+7=89.2V$$

Considering voltage derating, SR MOS with 100V rating is recommended.

(b)Maximum instantaneous SR MOS current:

$$I_{D(SR)\_MAX}=N_{PS}\cdot I_{PK\_MAX}=6\times2.61=15.7A$$

5) Calculate VSEN Pin Resistor Divider

(a)Firstly, calculate VSEN pin upper resistor: R_H

Predefined input voltage high line condition threshold: V_{IN_H}=180Vac

$$R_H=\frac{\sqrt{2}\cdot V_{IN\_H}}{I_{LINE\_H}}\cdot\frac{N_A}{N_P}=\frac{\sqrt{2}\cdot180}{300u}\cdot\frac{21}{42}=424.3k\Omega$$

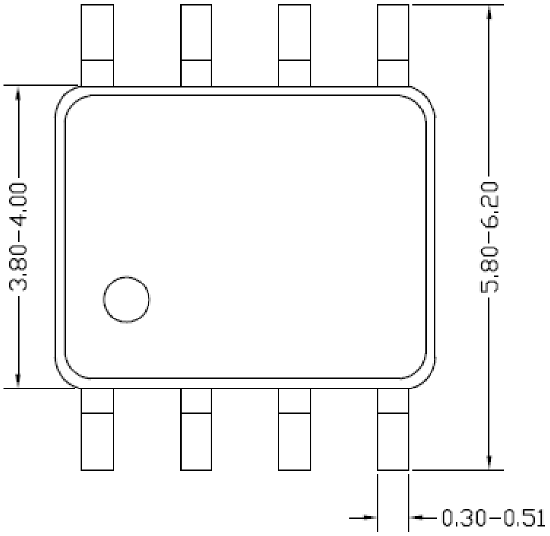
Select R_H=420k

(b) After R_H is determined, then calculate lower resistor R_L:

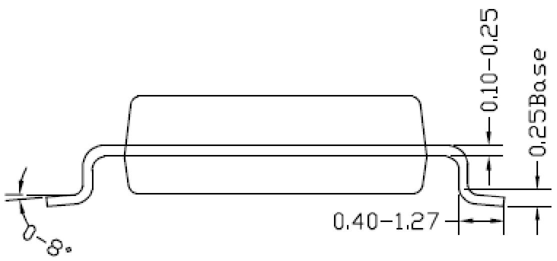
$$R_L=\frac{1}{\frac{V_{O\_OVP}}{V_{VSEN\_OVP}}\cdot\frac{N_A}{N_S}-1}\cdot R_H=\frac{1}{\frac{24}{2}\cdot\frac{21}{7}-1}\cdot420k=19.4k\Omega$$

Select R_L=19 k

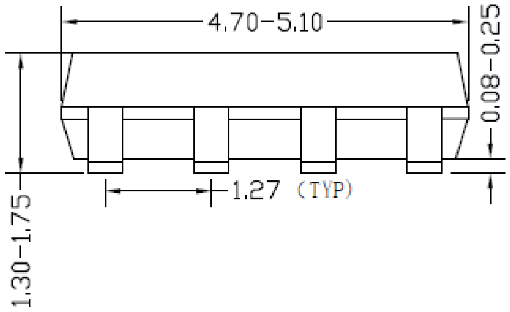
SO8 Package outline & PCB layout design



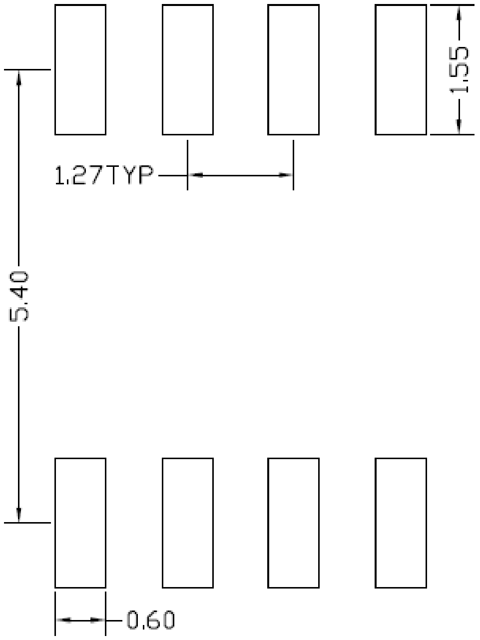
Top view



Side view



Front view

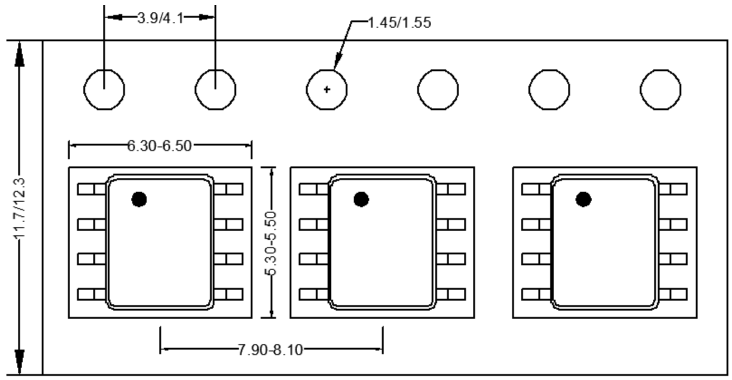


Recommended Pad Layout
(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

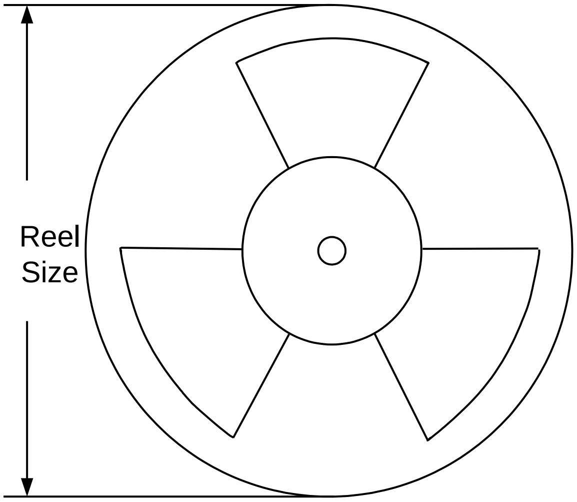
Taping & Reel Specification

1. Taping orientation for packages（SO8）



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SO8	12	8	13"	400	400	2500

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	**Revision**	**Change**
December 1, 2023	Revision 1.0	Initial Release

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