SY23407

Flyback Regulator
With Primary Side CC/CV Control

General Description

SY23407 is a single stage Flyback regulator targeting at Constant Current/Constant Voltage (CC/CV) applications. It integrates a 700V MOSFET in a compact SO7 to minimize the size. Both the output current and voltage are sensed on the primary side, eliminating the opto-coupler and the secondary side feedback circuitry, and minimizing the overall system cost.

SY23407 adopts the quasi-resonant operation mode and adaptive PWM/PFM control to achieve the highest average efficiency and best EMI performance. The no load switching frequency can be as low as 250Hz, minimizing the no-load power loss.

SY23407 has programmable cable compensation to provide a better load regulation for the output voltage at the cable terminals. When SY23407 is used with secondary side synchronous rectifier which has watch dog inside, fast dynamic load response can be achieved.

SY23407 has brown-in and brown-out functions. In addition, SY23407 provides reliable protections including VIN Over Voltage Protection (VIN OVP), output Over Voltage Protection (OVP), output Under Voltage Protection (UVP), Short Circuit Protection (SCP), Over Temperature Protection (OTP), etc.

Features

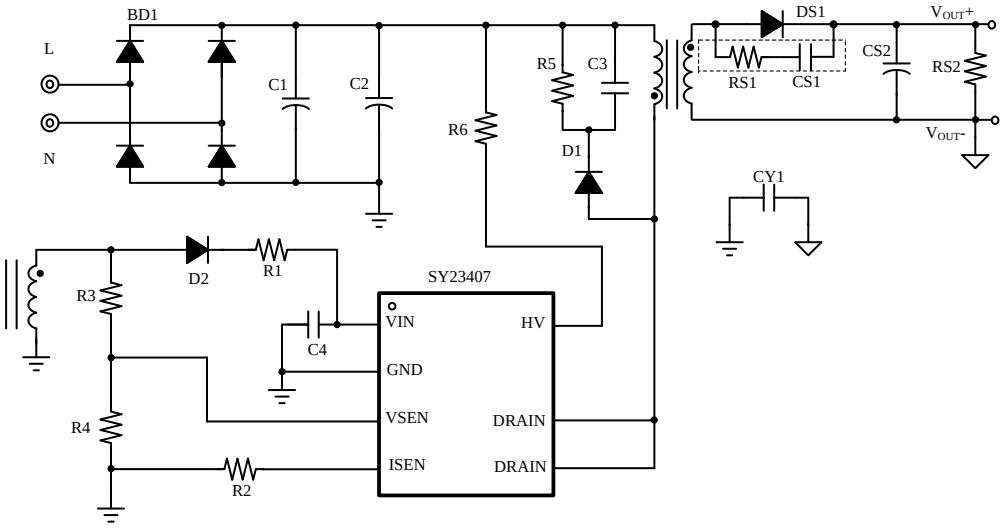
- Tight PSR CC/CV Regulation Over Entire Operating Range
- QR-mode Operation for High Efficiency
- PWM/PFM Control for High Average Efficiency
- Fast Dynamic Load Transient Response
- Cable Compensation for Better Load Regulation
- No-load Power is Less than 20mW
- Integrated HV Start up Circuit
- Brown-in and Brown-out Function
- Reliable Protections for OVP, UVP, SCP, OTP
- Reliable Protections for Safety Requirement
- Minimum Switching Frequency Limitation 250Hz
- Maximum Switching Frequency Limitation 90kHz
- Integrated 700V MOSFET
- RoHS Compliant and Halogen Free
- Compact Package: SO7

Applications

- AC/DC Adapters
- Battery Chargers
- Home Appliances

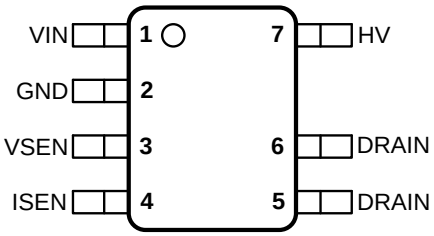
Recommended operating output power	
Products	85~265Vac
SY23407	12W

Typical Applications



Ordering Information

SY23407□(□□)□
- Temperature Code
- Package Code
- Optional Spec Code



Pinout (top view)

Ordering Number	Package	Top Mark
SY23407FQC	SO7	CLKxyz

x=year code, y=week code, z= lot number code

Pinout

Pin Number	Pin Name	Pin Description
1	VIN	Power supply pin. Bypass this pin to the GND pin with a ceramic capacitor.
2	GND	Ground pin.
3	VSEN	Output voltage sense pin. This pin receives the auxiliary winding voltage by a resistor divider. The value of the resistor divider also programs the cable impedance, brown-in and brown-out values. This pin also senses the winding voltage to provide the QR operation and detect the awakening signals.
4	ISEN	Current sense pin. The current sense resistor is placed between this pin and the GND pin.
5	DRAIN	Drain of the internal power MOSFET.
6	DRAIN	Drain of the internal power MOSFET.
7	HV	Internal high voltage start-up pin.

Absolute Maximum Ratings (Note 1)

VIN---------- -0.3V~26V
VSEN ---------- -0.3V~3.6V
ISEN---------- -0.3V~3.6V
Supply Current I_{VIN} ---------- 20mA
DRAIN---------- 700V
HV---------- 700V
Power Dissipation, @ T_A = 25°C SO7 ---------- 1.1W
Package Thermal Resistance (Note 2)
SO7, θ_{JA} ---------- 125°C/W
SO7, θ_{JC} ---------- 60°C/W
Junction Temperature Range ---------- -45°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions

VIN---------- 9V~21V
ISEN---------- 0V~1V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 105°C

Electrical Characteristics

(V_{VIN} = 12V (Note 3), T_A = 25°C unless otherwise specified)

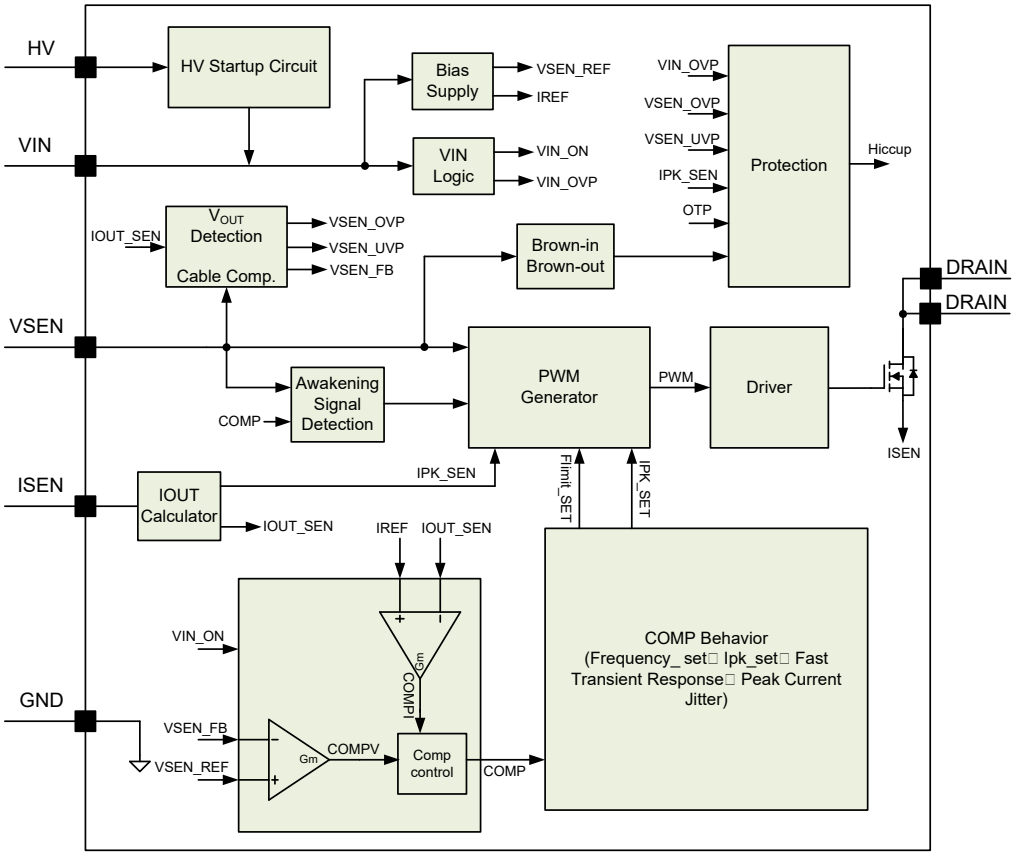
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
VIN Turn-on Threshold	V_{VIN_ON}		18.5	20.5	22.5	V
VIN Turn-off Threshold	V_{VIN_OFF}		6	7	8	V
VIN OVP Voltage	V_{VIN_OVP}			24		V
VIN Start Up Current	I_{VIN_ST}	V_{VIN}<V_{VIN_ON}	55	85	115	μA
Operating Current	I_{VIN}	f=80kHz		1.7		mA
Quiescent Current	I_Q	f=250Hz		160		μA
Discharge Current in OVP Mode	I_{VIN_OVP}	V_{VIN}=12V		3		mA
Current Feedback Modulator Section						
Internal Reference Voltage	V_{IREF}		0.410	0.42	0.430	V
ISEN Pin Section						
Current Limit Voltage	V_{ISEN_LIM}		0.95	1.05	1.15	V
VSEN Pin Section						
OVP Voltage Threshold	V_{VSEN_OVP}		1.44	1.5	1.56	V
UVP Voltage Threshold	V_{VSEN_UVP}			0.75		V
Internal Reference Voltage	V_{VSEN_REF}		1.232	1.25	1.268	V
Cable Compensation Coefficient	K_3			75		μA/V
VSEN Brown-in Detecting Current	I_{VSEN_BRIN}			100		μA
VSEN Brown-out Detecting Current	I_{VSEN_BROUT}			350		μA
HV Pin Section						
Breakdown Voltage of HV FET	V_{BV_HV}	V_{VIN}>V_{VIN_ON}, I_{DS}=250μA	700			V
HV Start Up Current	I_{HV_ST}	V_{VIN}<V_{VIN_ON}		350		μA
Integrated MOSFET Section						
Break Down Voltage	V_{BV}	V_{GS}=0V, I_{DS}=250uA	700			V
Static Drain-Source On-Resistance	R_{DSON}	V_{GS}=10V, I_{DS}=1A		4		Ω
Switching Section						
Max ON Time	T_{ON_MAX}			24		μs
Min ON Time	T_{ON_MIN}			450		ns
Max OFF Time	T_{OFF_MAX}			4		ms
Min OFF Time	T_{OFF_MIN}		1.7	2.2	2.6	μs
Minimum Switching Period	T_{PERIOD_MIN}		9.5	11	12.5	μs
Thermal Section						
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Temperature Hysteresis	T_{SD_HYS}			15		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause perm anent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on "2 x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal via to bottom layer ground plane.

Note 3: Increase VIN pin voltage gradually higher than V_{VIN_ON} voltage then turn down to 12V.

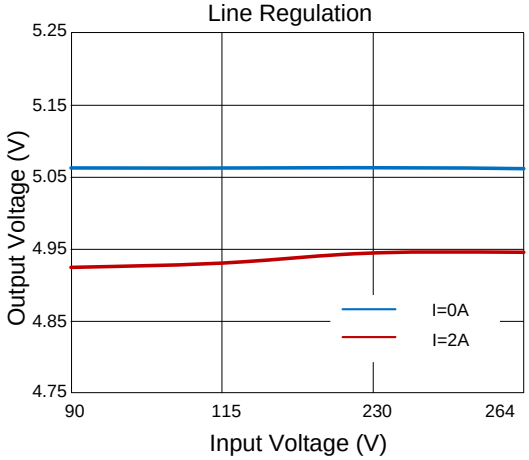
Block Diagram



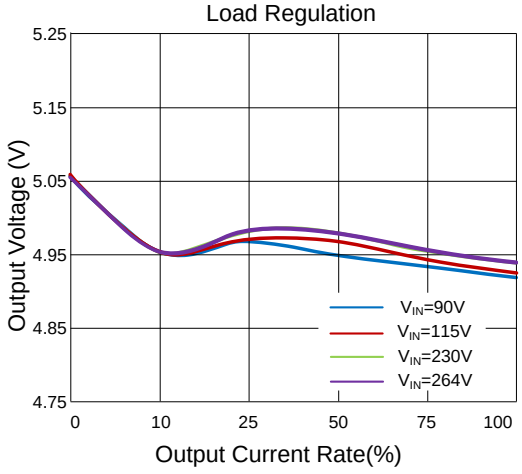
Typical Performance Characteristics

(Test condition: input voltage: 90~264Vac; output spec: 5Vdc_2A; output cable: 22AWG_1.2m; secondary side device: SY52267; Ambient temperature: 25±5 ℃; Ambient humidity: 65±25 %.)

Line Regulation

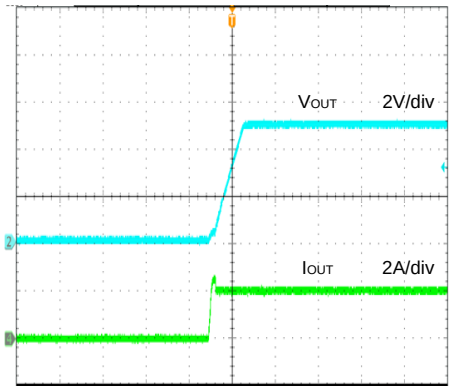


Load Regulation



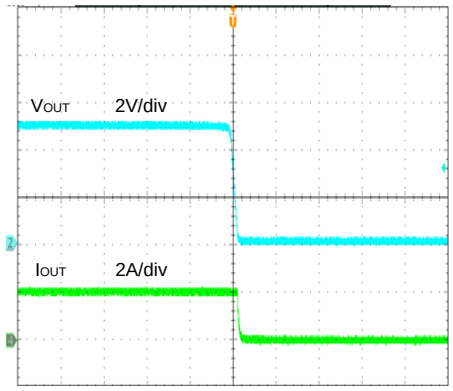
Startup

(V_{IN}=230$V_{(AC)}$)



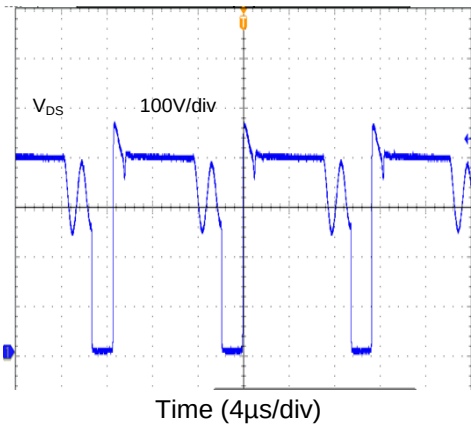
Shutdown

(V_{IN}=230$V_{(AC)}$)



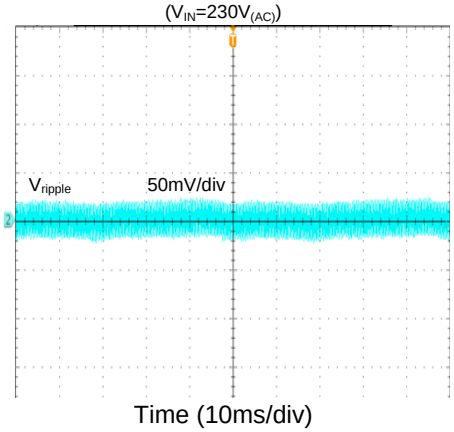
Steady States

(V_{IN}=230$V_{(AC)}$)



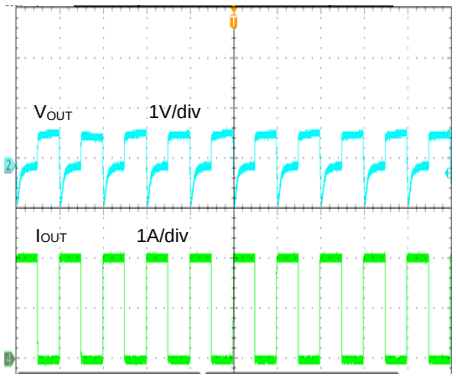
Output Voltage Ripple

(V_{IN}=230$V_{(AC)}$)



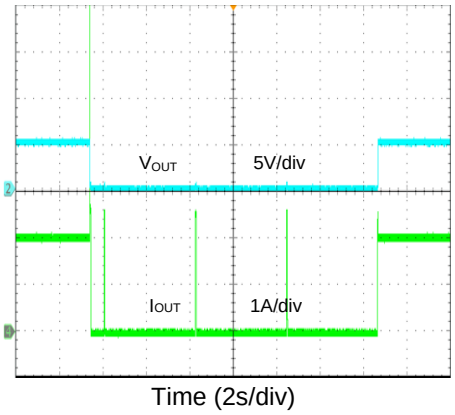
Load Transient

(V_{IN}=230$V_{(AC)}$)

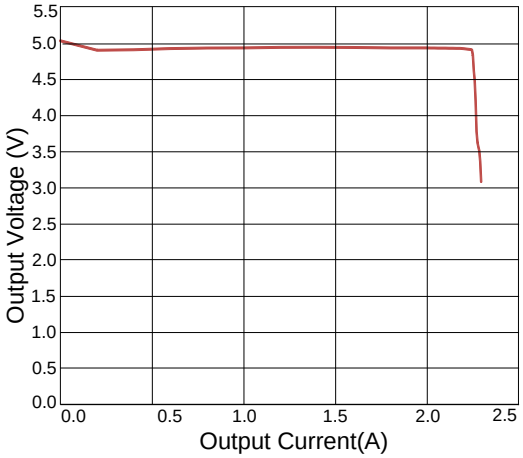


Short Circuit Protection

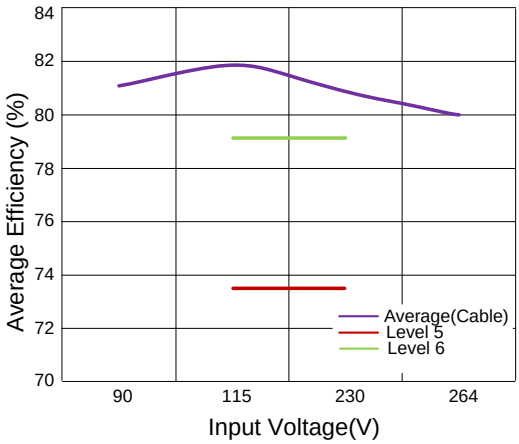
(V_{IN}=230$V_{(AC)}$)



Output Voltage vs. Output Current



Average Efficiency vs. Input Voltage



Operation Principles

Start up operation

To achieve better light load performance, HV start up design is added. After AC supply or DC BUS is powered on, the capacitor C_{VIN} across VIN and GND pin is charged up by BUS voltage through internal HV start up circuit. Once V_{VIN} rises up to V_{VIN_ON}, the internal blocks start to work. V_{VIN} will be pulled down by internal consumption of IC until the auxiliary winding of Flyback transformer could supply enough energy to maintain V_{VIN} above V_{VIN_OFF}.

The whole start up procedure is divided into two sections shown in Fig.1. t_{STC} is the C_{VIN} charged up section, and t_{STO} is the output voltage built-up section. The start up time t_{ST} composes of t_{STC} and t_{STO}, and usually t_{STO} is much smaller than t_{STC}.

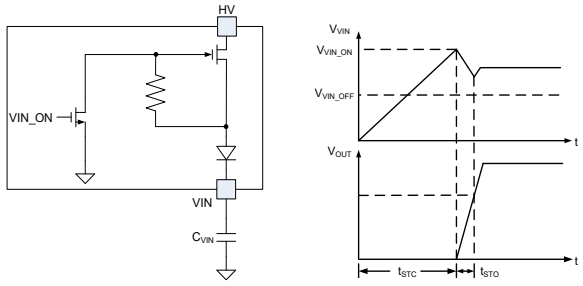


Fig.1 Start up

The C_{VIN} are designed by rules below:

(a) Select C_{VIN} to obtain an ideal start up time t_{ST}, and ensure the output voltage is built up at one time.

$$C_{VIN} = \frac{\left(I_{HV\_ST} - I_{VIN\_ST}\right) \times t_{ST}}{V_{VIN\_ON}} \quad (1)$$

Where, I_{HV_ST} is start up current on HV pin, I_{VIN_ST} is start up current of VIN internal circuit.

(b) If the C_{VIN} is not big enough to build up the output voltage at one time, increase C_{VIN} until the ideal start up procedure is obtained.

Shut down operation

After AC supply or DC BUS is powered off, the energy stored in the BUS capacitor will be discharged. When the auxiliary winding of Flyback transformer can not supply enough energy to VIN pin, V_{VIN} will drop down. Once V_{VIN} is lower than V_{VIN_OFF}, the driver circuit of SY23407 will be turned off and C_{VIN} will be re-charged through HV start up circuit until V_{VIN} reaches V_{VIN_ON}, then V_{VIN} will drop to V_{VIN_OFF} again by an internal discharging current and repeat this start up process 2 times. After finishing this process, the IC will stop working.

If the AC supply or DC BUS is powered on during the 2 times repeated processes, SY23407 will be real started up after the repeated processes are finished.

The shut down and re-start up procedure is shown in Fig.2. At t_1, AC supply is powered off, then SY23407 shuts down. At t_2, AC supply is powered on, but SY23407 doesn't start up. At t_3, SY23407 starts up.

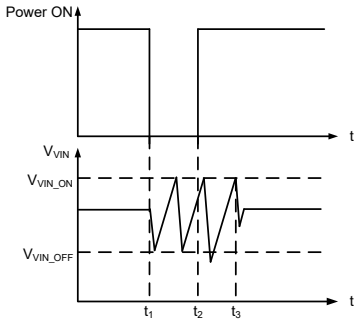


Fig.2 Shut down and re-start up

Quasi-resonant operation (valley detection)

The Quasi-Resonant switching mode is applied, which means to turn on the integrated MOSFET at voltage valley. QR mode operation provides low turn-on switching losses for Flyback converter.

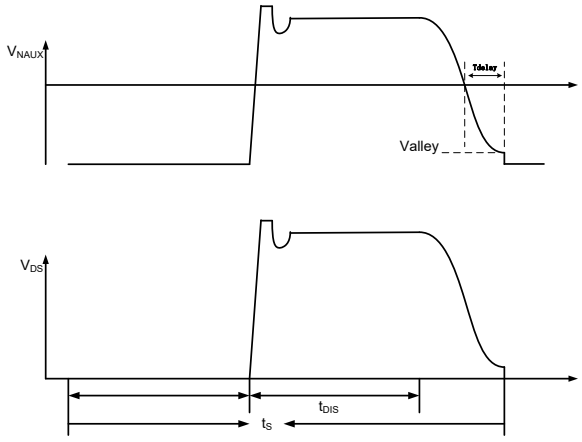


Fig.3 QR mode operation

The voltage across drain and source of the primary integrated MOSFET is reflected to the auxiliary winding

of the Flyback transformer. VSEN pin detects the voltage across the auxiliary winding by a resistor divider. As shown in Fig.3, when the voltage on VSEN pin across zero, the MOSFET would be turned on after 400ns delay.

Output voltage control (CV control)

In order to achieve primary side constant voltage control, the output voltage is sensed by the auxiliary winding. The auxiliary winding and VSEN pin connection is shown in Fig.4.

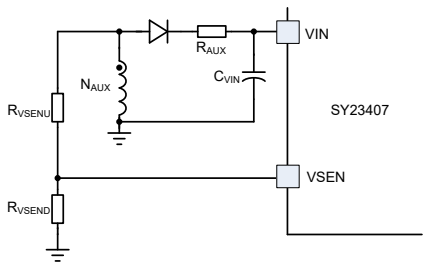


Fig.4 VSEN pin connection

As shown in Fig.5, during OFF time, the voltage across the auxiliary winding is

$$V_{AUX} = (V_{OUT} + V_{D\_F}) \times \frac{N_{AUX}}{N_S} \quad (3)$$

Where, N_{AUX} is the turns of auxiliary winding; N_S is the turns of secondary winding; V_{D_F} is the forward voltage of the power diode.

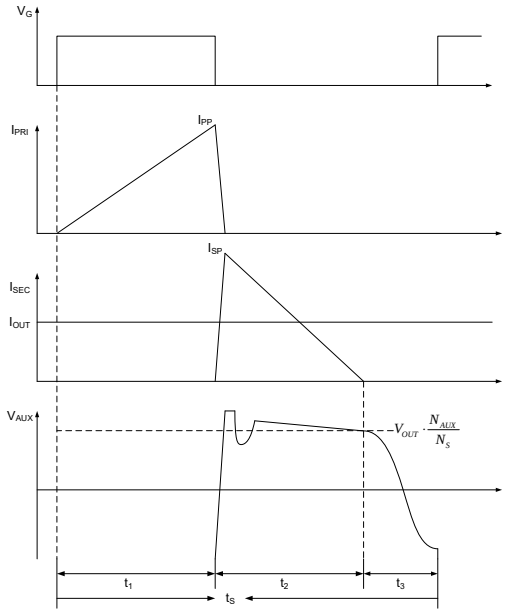


Fig.5 Auxiliary winding voltage waveforms

At the current zero-crossing point, V_{D_F} is zero, so V_{OUT} is proportional to V_{AUX}. The voltage of this point is sampled by the IC as the feedback of output voltage. The resistor divider is designed by

$$\frac{V_{VSEN\_REF}}{V_{OUT}} = \frac{R_{VSEND}}{R_{VSENU} + R_{VSEND}} \times \frac{N_{AUX}}{N_S} \quad (4)$$

Where, R_{VSEND} and R_{VSENU} are the lower divider and upper divider resistors on the VSEN pin, respectively, and V_{VSEN_REF} is the internal voltage reference at 1.25V.

Output current control (CC control)

The output current is regulated by SY23407 with primary side detection technology, the maximum output current I_{OUT_LIM} can be set by

$$I_{OUT\_LIM} = \frac{k_1 \times V_{IREF} \times N_{PS}}{R_S} \quad (5)$$

Where, k_1 is the output current weight coefficient, which is 0.5; V_{IREF} is the internal reference voltage; R_S is the current sense resistor.

k_1 and V_{IREF} are internal constant parameters, I_{OUT_LIM} can be programmed by N_{PS} and R_S.

$$R_S = \frac{k_1 \times V_{IREF} \times N_{PS}}{I_{OUT\_LIM}} \quad (6)$$

When the over current operation or short circuit operation happens, the output current will be limited at I_{OUT_LIM}. The V-I curve is shown as Fig.6.

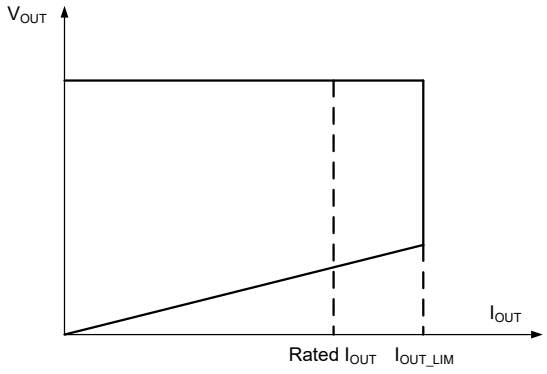


Fig.6 V-I curve

The IC provides line regulation modification function to improve line regulation performance of the output current limit. The current compensation is mainly related

with R_{VSENU}, larger compensation is achieved with smaller R_{VSENU}.

Cable impedance compensation

SY23407 has cable impedance compensation to regulate the output voltage for better load regulation at cable terminal. When the converter output load increases from no load to full load, the voltage decreasing on the output cable is compensated by VSEN upper resistor R_{VSENU}.

$$R_{VSENU} = \frac{R_{Cable}}{2k_3 \cdot R_S} \cdot \frac{N_P}{N_S} \cdot \frac{N_{AUX}}{N_S} \quad (7)$$

Where, R_{cable} is the resistance on the cable, k_3 is cable compensation coefficient, R_S is the current sense resistor.

The cable compensation effect can be adjusted by changing the resistance of R_{VSENU} to achieve good load regulation of different output cables. The larger R_{VSENU}, the stronger cable compensation effect will be.

If the output current is lower than 10% of the maximum output current I_{OUT_LIM}, the cable compensation is disabled.

Fast transient response

SY23407 has a dynamic load awakening detection function to achieve fast transient response. When it is used with secondary side synchronous rectifier which has watch dog inside, fast dynamic load response can be achieved.

When output voltage V_{OUT} drops at dynamic load, secondary side watch dog detects the drop and produces an awakening signal. The awakening signal can be transferred to primary side by transformer winding coupling, and can be detected by SY23407 through VSEN pin. If the awakening signal on VSEN pin is higher than 0.15V continues longer than 500ns after a blanking time, SY23407 will be awakened by this signal to generate PWM pulses immediately to prevent V_{OUT} drops. Then the transient performance can be improved.

Brown-in and brown-out

SY23407 has brown-in and brown-out detection function. During the integrated MOSFET ON time, the current flowing through VSEN pin is proportional to BUS voltage V_{BUS} and inversely proportional to R_{VSENU}. The brown-in/out function is implemented inside by detecting the I_{VSEN_BR} current.

The brown-in BUS voltage V_{BUS_BI} is

$$V_{BUS\_BI} = I_{VSEN\_BRIN} \times R_{VSENU} \times \frac{N_P}{N_{AUX}} \quad (8)$$

The brown-out BUS voltage V_{BUS_BO} is

$$V_{BUS\_BO} = I_{VSEN\_BROUT} \times R_{VSENU} \times \frac{N_P}{N_{AUX}} \quad (9)$$

Where, I_{VSEN_BRIN} is VSEN brown-in detecting current, I_{VSEN_BROUT} is VSEN brown-out detecting current.

Higher brown-in/out BUS voltage can be achieved by larger R_{VSENU}. For conventional applications, N_P/N_{AUX} ≈5~7, so R_{VSENU} is recommended between 43kΩ~56kΩ.

Over temperature protection (OTP)

SY23407 includes over-temperature protection (OTP) circuitry to prevent the overheating due to the excessive power dissipation. It will shut down the switching operation when the junction temperature is higher than the OTP threshold, about 150℃. In OTP mode, if the junction temperature decreases by approximately 15℃, the IC will resume the normal operation. For a continuous normal operation, provide an adequate cooling so that the junction temperature does not exceed the OTP threshold.

VIN voltage OVP protection

When the VIN voltage is higher than V_{VIN_OVP} threshold, SY23407 will stop switching and discharge the VIN voltage. Once V_{VIN} is lower than V_{VIN_OFF}, SY23407 will shut down and then enter into hiccup mode.

Output voltage OVP protection

When the VSEN pin sampled signal is higher than 1.5V, reflecting output over voltage condition, SY23407 will stop switching and discharge the VIN voltage. Once V_{VIN} is lower than V_{VIN_OFF}, SY23407 will shut down and then enter into hiccup mode.

Output voltage UVP protection

When the VSEN pin sampled signal is lower than 0.75V, reflecting output under voltage condition, SY23407 will stop switching and discharge the VIN voltage. Once V_{VIN} is lower than V_{VIN_OFF}, SY23407 will shut down and then enter into hiccup mode.

Short circuit protection (SCP)

When the output is shorted to ground, the output voltage is clamped to zero. The valley signal of the auxiliary winding voltage might not be detected by the VSEN pin. In this case, VIN voltage decreases and the integrated MOSFET cannot be turned on until maximum off time is

reached. Once V_{VIN} is lower than V_{VIN_OFF}, SY23407 will shut down and then enter into hiccup mode.

The hiccup mode procedure in SCP condition is shown in Fig.7. At t_1, SY23407 enters into SCP mode, then V_{VIN} decreases to V_{VIN_OFF} and C_{VIN} will be re-charged through HV start up circuit until V_{VIN} reaches V_{VIN_ON}, then V_{VIN} will drop to V_{VIN_OFF} again by an internal discharging current and repeat this start up process 2 times. At t_2, SY23407 starts up again. At t_3, SY23407 detects that it works in under voltage condition before V_{VIN} decreases to V_{VIN_OFF} during start up stage, then it removes the internal discharging current to increase the start up time to reduce the power loss in SCP condition.

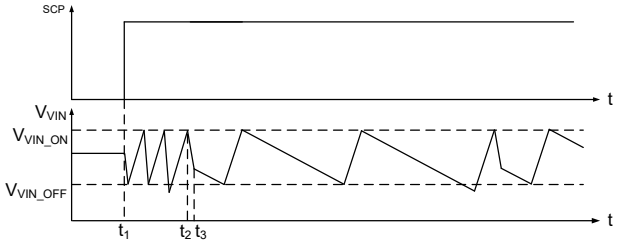


Fig.7 Hiccup mode in SCP condition

If the output voltage is not low enough to disable the valley detection in short condition, SY23407 will operate in CC mode until V_{VIN} decreases lower than V_{VIN_OFF}.
As shown in Fig.8, a filter resistor R_{AUX} is needed to prevent the SCP function from being affected by the voltage spikes of the auxiliary winding.

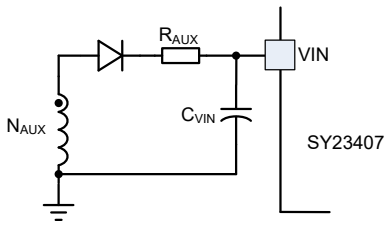


Fig.8 Filter resistor R_{AUX}

VSEN pin short protection
SY23407 has a protection against the faults caused by a short circuit between the VSEN pin and GND. If the VSEN voltage does not reach the sense protection trigger voltage, the VSEN pin is considered to be shorted to GND and the protection is activated: SY23407 will stop switching and discharges the VIN voltage. Once V_{VIN} drops below V_{VIN_OFF}, SY23407 will shut down and enter into hiccup mode. To ensure reliable detection, the lower divider resistor on the VSEN pin should be larger than 2kΩ.

ISEN pin short protection
SY23407 has a protection against the faults caused by a short circuit between the ISEN pin and GND. If the ISEN voltage does not reach the sense protection trigger voltage, the ISEN pin is considered to be shorted to GND and the protection is activated: SY23407 will stop switching and discharge the VIN voltage. Once V_{VIN} drops below V_{VIN_OFF}, SY23407 will shut down and then enter into hiccup mode.

VSEN pin upper divider resistor open circuit protection
SY23407 has a protection against the faults caused by a VSEN pin upper divider resistor open circuit condition. If the upper divider resistor is disconnected, SY23407 will stop switching and discharge the VIN voltage. Once V_{VIN} drops below V_{VIN_OFF}, SY23407 will shut down and enter into hiccup mode.

Power Supply Design Considerations

Power rating
The temperature rise of 10W typical application is shown as below.

Products	Input range	Output		Temperature rise
SY23407	85Vac~264Vac	10W	5V/2A	60℃

The test is conducted in a natural cooling condition at 25℃ ambient temperature.

Transformer design considerations (N_{PS} and L_M)

In Quasi-Resonant mode, each switching period cycle, t_S, consists of three parts: current rising time t_1, current falling time t_2 and quasi-resonant time t_3 shown in Fig.9.

Under the conditions of the minimum input AC RMS voltage and full load, the switching frequency is minimum value, while the peak current through integrated MOSFET is maximum value.

Once the minimum frequency f_{S_MIN} is set, the inductance of the transformer could be designed. The design flow is shown as below:

(a) Select N_{PS}

N_{PS} is limited by the electrical stress of the internal power MOSFET:

$$N_{PS} \le \frac{V_{BV} \times 90\% - \sqrt{2} V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \quad (10)$$

Where, V_{BV} is the breakdown voltage of the integrated MOSFET, V_{D_F} is the forward voltage of secondary power diode, ΔV_S is the overshoot voltage clamped by RCD snubber during OFF time.

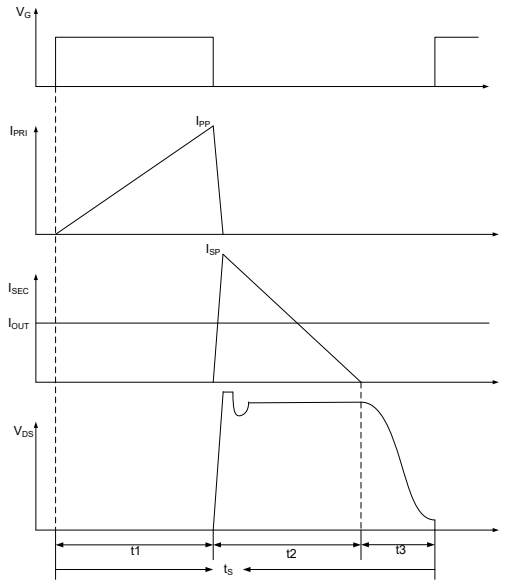


Fig.9 switching waveforms

(b) Preset minimum frequency f_{S_MIN}

(c) Calculate inductor L_M and maximum primary peak current $I_{P\_PK\_MAX}$

$$I_{P\_PK\_MAX} = \frac{2P_{OUT}}{\eta \times V_{DC\_MIN}} + \frac{2P_{OUT}}{\eta \times N_{PS} \times (V_{OUT} + V_{D\_F})} + \pi \sqrt{\frac{2P_{OUT}}{\eta} \times C_{DS} \times f_{S\_MIN}} \quad (11)$$

$$L_M = \frac{2P_{OUT}}{\eta \times I_{P\_PK\_MAX}^2 \times f_{S\_MIN}} \quad (12)$$

Where, C_{DS} is the parasitic capacitance at drain of the integrated MOSFET, η is the efficiency, and P_{OUT} is the rated full load power.

(d) Calculate current rising time t_1 and current falling time t_2

$$t_1 = \frac{L_M \times I_{P\_PK\_MAX}}{V_{BUS}} \quad (13)$$

$$t_2 = \frac{L_M \times I_{P\_PK\_MAX}}{N_{PS} \times (V_{OUT} + V_{D\_F})} \quad (14)$$

$$t_3 = \pi \times \sqrt{L_M \times C_{DS}} \quad (15)$$

$$t_S = t_1 + t_2 + t_3 \quad (16)$$

(e) Calculate primary maximum RMS current $I_{P\_RMS\_MAX}$ for the transformer fabrication.

$$I_{P\_RMS\_MAX} = \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \times \sqrt{\frac{t_1}{t_S}} \quad (17)$$

(f) Calculate secondary maximum peak current $I_{S\_PK\_MAX}$ and RMS current $I_{S\_RMS\_MAX}$ for the transformer fabrication.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} \quad (18)$$

$$I_{S\_RMS\_MAX} = \frac{\sqrt{3}}{3} N_{PS} \times I_{P\_PK\_MAX} \times \sqrt{\frac{t_2}{t_S}} \quad (19)$$

Transformer design considerations

The key transformer parameters are shown below:

Necessary parameters	
Primary to secondary turns ratio	N_{PS}
Inductance	L_M
Primary maximum current	$I_{P\_PK\_MAX}$
Primary maximum RMS current	$I_{P\_RMS\_MAX}$
Secondary maximum RMS current	$I_{S\_RMS\_MAX}$

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area A_e.

(b) Preset the maximum magnetic flux ΔB

ΔB=0.22~0.3T

(c) Calculate primary turns N_P

$$N_P = \frac{L_M \times I_{P\_PK\_MAX}}{\Delta B \times A_e} \quad (20)$$

(d) Calculate secondary turns N_S

$$N_S = \frac{N_P}{N_{PS}} \quad (21)$$

(e) Calculate auxiliary turns N_{AUX}

$$N_{AUX} = N_S \times \frac{V_{VIN}}{V_{OUT}} \quad (22)$$

Where, V_{VIN} is the working voltage of VIN pin, 12V~15V is recommended in calculation.

(f) Select an appropriate wire diameter

With $I_{P\_RMS\_MAX}$ and $I_{S\_RMS\_MAX}$, select appropriate wire to achieve the current density between 4A/mm^2 and 10A/mm^2.

(g) If the window area of the core and bobbin is not big enough, reselect the core style, go to step **(a)** and redesign the transformer until the ideal transformer is achieved.

Diode selection

Under the conditions of the maximum input voltage and full load, the voltage stress of secondary power diode is maximum.

$$V_{D\_R\_MAX} = \frac{\sqrt{2}V_{AC\_MAX}}{N_{PS}} + V_{OUT} \quad (23)$$

Where, V_{AC_MAX} is the maximum input AC RMS voltage, N_{PS} is the primary to secondary turns ratio of the Flyback transformer and V_{OUT} is the rated output voltage.

Under the conditions of the minimum input voltage and full load, the current stress of power diode is maximum.

$$I_{D\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} \quad (24)$$

$$I_{D\_AVG} = I_{OUT} \quad (25)$$

Where, $I_{P\_PK\_MAX}$ is the maximum primary peak current.

In order to achieve fast dynamic load response, synchronous rectifier SY52267 is usually used to instead of diode in secondary side.

Input capacitor C_{BUS} selection

Generally, the input capacitor C_{BUS} is selected by

$$C_{BUS} = 2 \sim 3\mu F / W ,$$

or more accurately by

$$C_{BUS} = \frac{\arcsin(1 - \frac{\Delta V_{BUS}}{\sqrt{2}V_{AC\_MIN}}) + \frac{\pi}{2}}{\pi} \times \frac{P_{OUT}}{\eta} \times \frac{1}{2f_{IN}V_{AC\_MIN}^2[1-(1-\frac{\Delta V_{BUS}}{\sqrt{2}V_{AC\_MIN}})^2]} \quad (26)$$

Where, ΔV_{BUS} is the voltage ripple of BUS line.

RCD snubber for MOSFET selection

The power loss of the snubber P_{RCD} is evaluated as:

$$P_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{\Delta V_S} \times \frac{L_K}{L_M} \times P_{OUT} \quad (27)$$

Where, N_{PS} is primary to secondary turns ratio, V_{OUT} is the output voltage, V_{D_F} is the forward voltage of the power diode, ΔV_S is the overshoot voltage clamped by RCD snubber, L_K is the leakage inductor, L_M is the inductance of the Flyback transformer and P_{OUT} is the output power.

The R_{RCD} is calculated as:

$$R_{RCD} = \frac{(N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S)^2}{P_{RCD}} \quad (28)$$

The C_{RCD} is calculated as:

$$C_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{R_{RCD} \times f_S \times \Delta V_{C\_RCD}} \quad (29)$$

Where, f_S is switching frequency, ΔV_{C_RCD} is the voltage on C_{RCD}.

The D_{RCD} is recommended to use a slow reverse recovery diode, such as S1M or 1N4007.

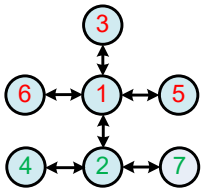
In order to reduce the leakage inductance resonance, a resistor is usually connected in series with the diode D_{RCD}. Normally, the resistor is recommended between 43Ω and 200Ω.

Layout Considerations

A proper PCB design must follow the below guidelines:
(a) To achieve a good EMI performance and to reduce the line frequency voltage ripples, the output of the bridge rectifier should be connected to the BUS line capacitor first, then to the switching circuit.

(b) The circuit loop of all switching circuit should be kept as small as possible: primary power loop, secondary loop and auxiliary power loop.

(c) The connection of primary ground is recommended as:

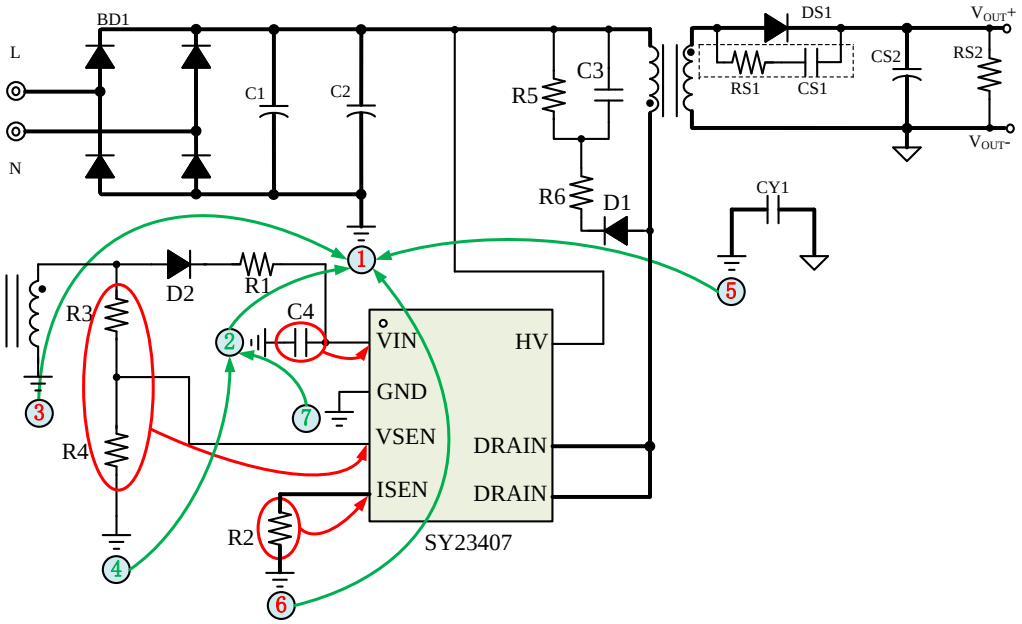


Ground ①: ground of BUS line capacitor
Ground ②: ground of bias supply capacitor
Ground ③: ground node of auxiliary winding
Ground ④: ground node of divider resistor
Ground ⑤: primary ground node of Y capacitor
Ground ⑥: ground node of current sense resistor
Ground ⑦: ground of IC GND

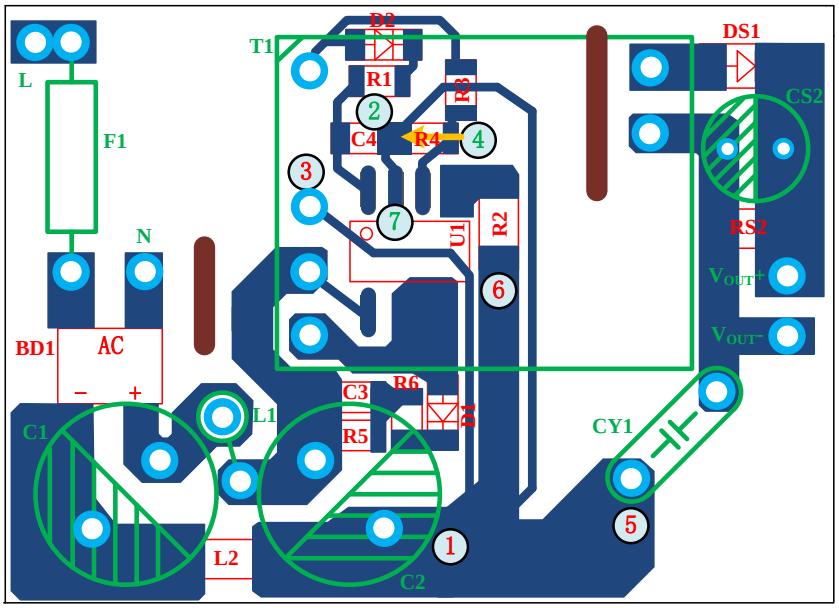
(d) Bias supply trace should be connected to the bias supply capacitor first and then to the VIN pin and GND pin. A ceramic capacitor should be put close to the IC VIN pin and GND pin.

(e) The loop consisting of ‘ISEN pin – current sense resistor – GND pin’ should be kept as small as possible.

(f) The resistor divider connected to VSEN pin is recommended to be put close to the IC.



Note： Ground node of current sample resistor must be connected to the ground of bus line capacitor.



Example layout

Design Notes

1. At no load, the secondary side diode freewheeling time should be more than 2.2us.
2. VIN voltage should be designed between 9V~21V during all conditions.
3. RCD snubber's influence:
   At no load or light load, the off-time of main switch is very long and the snubber capacitor's voltage may be discharged to a small value. When the primary switch turns on and then turns off, the primary winding current needs a longer than normal time to charge up the snubber capacitor. This might affect the feedback voltage sensing. Normally, the snubber capacitor should be selected between 330pF~1nF.
   At heavy load, the peak to peak voltage at the VSEN pin should be less than approximately 100mV after off-min time (2.2us). This can be guaranteed by decreasing the leakage inductance and using proper RCD snubber.
4. R_{VSENU} is the upper resistor of the divider. Normally, its value is recommended between 43kΩ~56kΩ.

Design Example

A design example of typical application is shown below step by step.
Note: All selected parameter (set value) need to adjust according to the practical condition.

#1. Identify design specification

Design Specification			
V_{AC}(RMS)	90V~264V	V_{OUT}	5V
I_{OUT}	2A	Efficiency	82% (board end)

#2. Transformer design (N_{PS}, L_M, N_P, N_S, N_{AUX})

(**1**)Refer to **Transformer selection (N_{PS} and L_M)**

Conditions			
V_{AC_MIN}	90V	V_{AC_MAX}	264V
ΔV_S	75V	V_{BV}	700V
P_{OUT}（Max）	10W	V_{D_F}	1V
C_{DS}	100pF	f_{S_MIN}	60kHz
ΔV_{BUS}	30% V_{BUS_MIN}		

(a) Calculate turns ratio N_{PS} first

$$N_{PS} \le \frac{V_{BV}\times 90\%-\sqrt{2}V_{AC\_MAX}-\Delta V_S}{V_{OUT}+V_{D\_F}} = \frac{700V\times 0.9-\sqrt{2}\times 264V-75V}{5V+1V} = 30.275$$

N_{PS} is set to

N_{PS}=15

(b)f_{S_MIN} is preset

f_{S_MIN}=60kHz

(c) Calculate inductor L_M and maximum primary peak current $I_{P\_PK\_MAX}$

$$I_{P\_PK\_MAX} = \frac{2P_{OUT}}{\eta\times\left(\sqrt{2}V_{AC\_MIN}-\Delta V_{BUS}\right)} + \frac{2P_{OUT}}{\eta\times N_{PS}\times(V_{OUT}+V_{D\_F})} + \pi\sqrt{\frac{2P_{OUT}}{\eta}\times C_{DS}\times f_{S\_MIN}}$$

$$= \frac{2\times 10W}{0.82\times(\sqrt{2}\times 90V-0.3\times\sqrt{2}\times 90V)} + \frac{2\times 10W}{0.82\times 15\times(5V+1V)} + \pi\times\sqrt{\frac{2\times 10W}{0.82}\times 100pF\times 60kHz}$$

$$= 0.583A$$

$$L_M = \frac{2P_{OUT}}{\eta\times I_{P\_PK\_MAX}^2\times f_{S\_MIN}} = \frac{2\times 10W}{0.82\times(0.583A)^2\times 60kHz} = 1.197mH$$

Set: L_M=1.1mH. (Note: The actual value generally should be less than the calculated value)

(d) Calculate current rising time t_1 and current falling time t_2

$$t_1 = \frac{L_M \times I_{P\_PK\_MAX}}{\sqrt{2}V_{AC\_MIN} - \Delta V_{BUS}} = \frac{1.1mH \times 0.583A}{\sqrt{2} \times 90V - 0.3 \times \sqrt{2} \times 90V} = 7.195\mu s$$

$$t_2 = \frac{L_M \times I_{P\_PK\_MAX}}{N_{PS} \times (V_{OUT} + V_{D\_F})} = \frac{1.1mH \times 0.583A}{15 \times (5V + 1V)} = 7.123\mu s$$

$$t_3 = \pi \times \sqrt{L_M \times C_{DS}} = \pi \times \sqrt{1.1mH \times 100pF} = 1.042\mu s$$

$$t_S = t_1 + t_2 + t_3 = 7.195\mu s + 7.123\mu s + 1.042\mu s = 15.36\mu s$$

(e) Calculate primary maximum RMS current $I_{P\_RMS\_MAX}$ for the transformer fabrication.

$$I_{P\_RMS\_MAX} = \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \times \sqrt{\frac{t_1}{t_S}} = \frac{\sqrt{3}}{3} \times 0.583A \times \sqrt{\frac{7.195\mu s}{15.36\mu s}} = 0.23A$$

(f) Calculate secondary maximum peak current $I_{S\_PK\_MAX}$ and RMS current $I_{S\_RMS\_MAX}$ for the transformer fabrication.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} = 15 \times 0.583A = 8.741A$$

$$I_{S\_RMS\_MAX} = N_{PS} \times \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \times \sqrt{\frac{t_2}{t_S}} = 15 \times \frac{\sqrt{3}}{3} \times 0.583A \times \sqrt{\frac{7.123\mu s}{15.36\mu s}} = 3.437A$$

(2) Refer to **Transformer number of turns selection (N_P, N_S, N_{AUX})**

(a) Select the magnetic core style, identify the effective area A_e. Take EF15-10 for calculation example. Its A_e is 37mm^2. The EF15-10 can be replaced by other reasonable magnetic core style.

(b) Preset the maximum magnetic flux ΔB. Usually, ΔB=0.22~0.3T .

Set: ΔB=0.29T .

(c) Calculate primary turn N_P

$$N_P = \frac{L_M \times I_{P\_PK\_MAX}}{\Delta B \times A_e} = \frac{1.1mH \times 0.583A}{0.29T \times 37 \times 10^{-6} m^2} = 59.743$$

Set: N_P=60

(d) Calculate secondary turn N_S

$$N_S = \frac{N_P}{N_{PS}} = \frac{60}{15} = 4$$

Set: N_S=4

(e) Calculate auxiliary turn N_{AUX}

$$N_{AUX}=\frac{N_S\times V_{VIN}}{V_{OUT}}=\frac{4\times 13V}{5V}=10.4$$

Set: N_{AUX}=10

Where, V_{VIN} is the working voltage of VIN pin, 12V~15V is recommended in calculation.

(f) Select an appropriate wire diameter

With $I_{P\_RMS\_MAX}$ and $I_{S\_RMS\_MAX}$, select appropriate wire to make sure the current density ranges from 6A/mm^2 to 12A/mm^2.

Primary wire diameter selection: current density j_P is set to 10A/mm^2.

Calculate primary wire cross-sectional area $S_1=\frac{I_{P\_RMS\_MAX}}{j_P}=\frac{0.23A}{10A/mm^2}=0.023mm^2$

Calculate primary wire diameter $D_1=2\times\sqrt{\frac{S_1}{\pi}}=2\times\sqrt{\frac{0.023mm^2}{\pi}}=0.171mm$

Set: D_1=0.18mm

Secondary wire diameter selection: current density j_S is set to 10A/mm^2.

The calculate secondary wire cross-sectional area $S_2=\frac{I_{S\_RMS\_MAX}}{j_S}=\frac{3.437A}{10A/mm^2}=0.344mm^2$

The calculate secondary wire diameter $D_2=2\times\sqrt{\frac{S_2}{\pi}}=2\times\sqrt{\frac{0.344mm^2}{\pi}}=0.662mm$

Set: D_2=0.65mm

For different transformer types, the actual primary and secondary wire diameters can be adjusted to achieve the best winding structure.

(g) If the winding area of the core and bobbin is not enough, reselect the core style, go to **(a)** and redesign the transformer until the ideal transformer is achieved.

#3. Select secondary power diode

Refer to **Diode selection**.

Calculate the voltage and the current stress of secondary power diode

$$V_{D\_R\_MAX}=\frac{\sqrt{2}V_{AC\_MAX}}{N_{PS}}+V_{OUT}=\frac{\sqrt{2}\times 264V}{15}+5V=29.89V$$

$$I_{D\_PK\_MAX}=N_{PS}\times I_{P\_PK\_MAX}=15\times 0.583A=8.745A$$

$$I_{D\_AVG}=2A$$

Usually, SY52267 is used to cooperate with SY23407 instead of diode in secondary side for fast dynamic load response.

#4. Select the input capacitor C_{BUS}

Refer to **Input capacitor C_{BUS}**.

Known conditions at this step			
V_{AC_MIN}	90V	ΔV_{BUS}	30% V_{BUS_MIN}

$$C_{BUS}=\frac{\arcsin(1-\frac{\Delta V_{BUS}}{\sqrt{2}V_{AC\_MIN}})+\frac{\pi}{2}}{\pi}\times\frac{P_{OUT}}{\eta}\times\frac{1}{2f_{IN}V_{AC\_MIN}^2[1-(1-\frac{\Delta V_{BUS}}{\sqrt{2}V_{AC\_MIN}})^2]}$$

$$=\frac{\arcsin(1-\frac{0.3\times\sqrt{2}\times 90V}{\sqrt{2}\times 90V})+\frac{\pi}{2}}{\pi}\times\frac{10W}{0.82}\times\frac{1}{2\times 50\times(90V)^2\times[1-(1-\frac{0.3\times\sqrt{2}\times 90V}{\sqrt{2}\times 90V})^2]}$$

$= 22.05\mu F$

Set: C_{BUS}=20 μF

Where, ΔV_{BUS} is the voltage ripple of BUS line.

#5. Select VIN pin capacitor C_{VIN}

Refer to **Start up**.

Conditions			
I_{HV_ST}	350μA (typical)	V_{VIN_ON}	20.5V (typical)
I_{VIN_ST}	85μA (typical)	t_{ST}	0.5s (designed by user)

Design C_{VIN}

$$C_{VIN}=\frac{(I_{HV\_ST}\text{-}I_{HV\_LK})\times t_{ST}}{V_{VIN\_ON}}=\frac{(350\mu A\text{-}85\mu A)\times 0.5s}{20.5V}=6.46\mu F$$

Set: C_{VIN}=4.7μF

#6. Select ISEN pin resistor R_S

Refer to **Output current control (CC control)**.

Known conditions at this step			
k_1	0.5	N_P	60
N_S	4	V_{IREF}	0.42V
I_{OUT_LIM}	2.4A		

The current sense resistor is

$$R_S = \frac{k_1 \times V_{IREF}}{I_{OUT\_LIM}} \times \frac{N_P}{N_S} = \frac{0.5 \times 0.42V}{2.4A} \times \frac{60}{4} = 1.313\Omega$$

Set: R_S=1.8Ω//2.4Ω

The actual current sense resistor needs to be adjusted slightly to meet the requirement of I_{OUT_LIM}.

#7. Select VSEN pin resistors R_{VSENU} and R_{VSEND}

Refer to **Output voltage control (CV control)**.

First calculate R_{VSENU}

Conditions			
V_{OUT}	5V	V_{VSEN_REF}	1.25V
R_{Cable}	0.2Ω (Cable: 22AWG_1.2m)	N_P	60
N_S	4	N_{AUX}	10
K_3	75μA/V		

$$R_{VSENU} = \frac{R_{Cable}}{2K_3 \times R_S} \times \frac{N_P}{N_S} \times \frac{N_{AUX}}{N_S} = \frac{0.2\Omega}{2 \times 75\mu A/V \times 1.03\Omega} \times \frac{60}{4} \times \frac{10}{4} = 48.34k\Omega$$

Set: R_{VSENU} =51kΩ

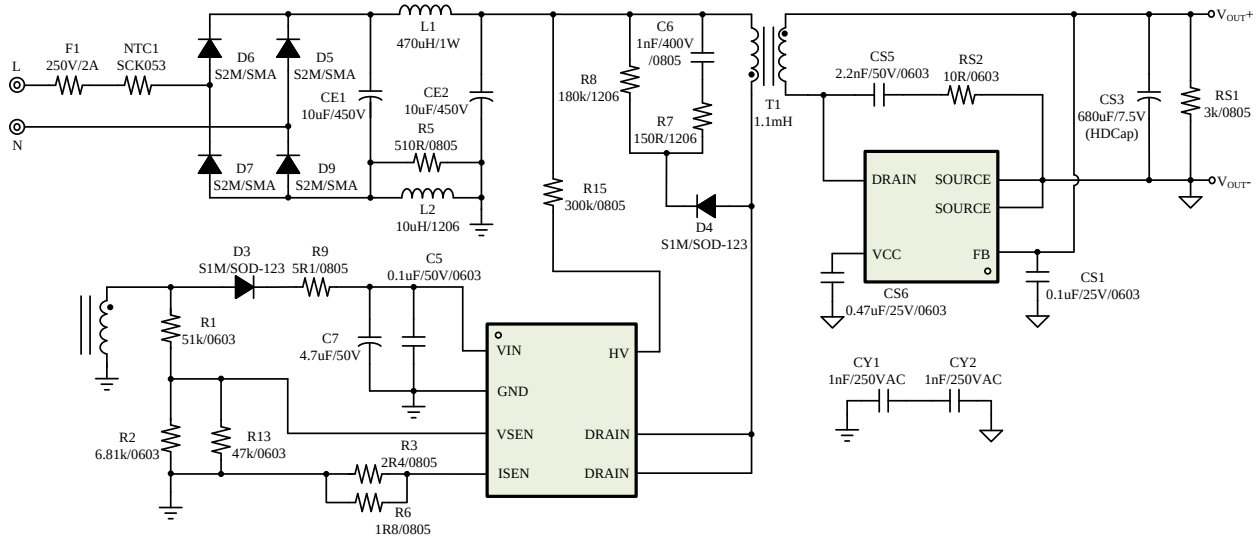
Then calculate R_{VSEND}

$$R_{VSEND} = \frac{R_{VSENU}}{\frac{V_{OUT} \times N_{AUX}}{V_{VSEN\_REF} \times N_S} - 1} = \frac{51k\Omega}{\frac{5V \times 10}{1.25V \times 4} - 1} = 5.667k\Omega$$

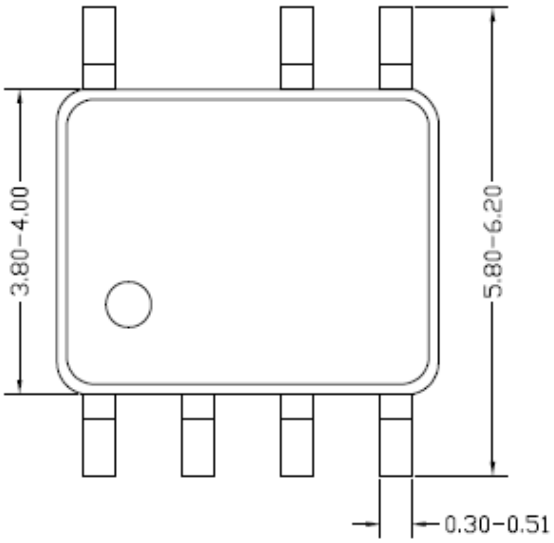
Set: R_{VSEND} =6.81kΩ//47kΩ

The actual VSEN resistors need to be adjusted slightly to meet the requirement of output voltage.

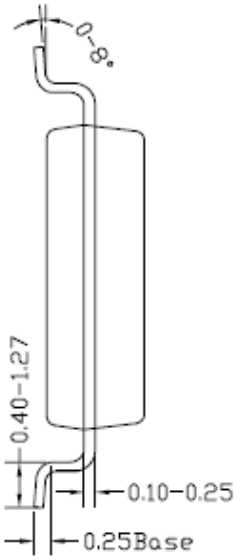
#8. Final result



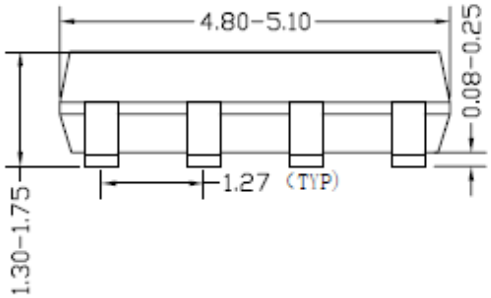
SO7 Package Outline & PCB Layout Design



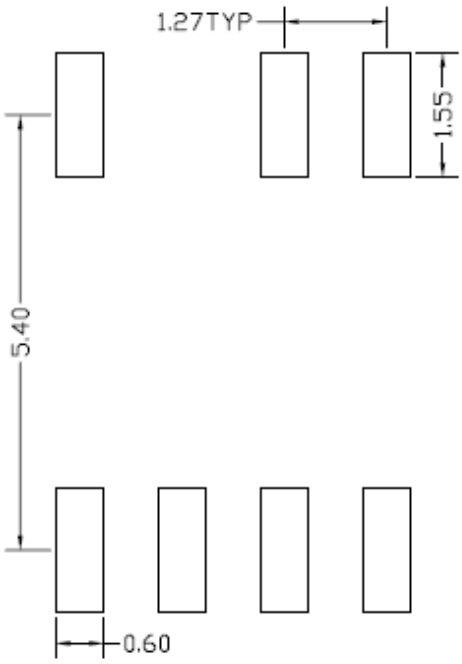
Top View



Side View A



Side View B



Recommended PCB Layout
(Reference only)

Notes: 1, All dimension in millimeter and exclude mold flash & metal burr

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
September 30,2019	Revision 0.9	Initial Release

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