

## Features

- Integrated 900V MOSFET
- Very Tight Primary Side CV/CC Regulation
- Quasi-resonant Mode and PWM/PFM Control for Higher Average Efficiency
- Internal CC/CV Loop Compensation
- Low Start Up Current: 5 $\mu$ A Max
- HV Start Up Circuit to Reduce No-load Loss
- Maximum Switching Frequency Limitation 125kHz
- VREG OVP Function for Strong Magnetic Field Test
- Reliable Protections for OCP,SCP,VCCOVP,VSEN SCP, OTP
- Compact Package: SSOP10

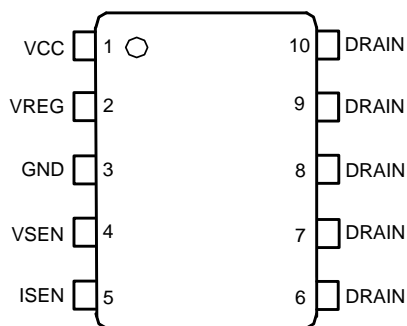
## Applications

- Power Supply for STB Home Appliances, Smart Power Meter and Other Appliances with High AC Input Voltage

Recommended operating output power	
Products	85~450Vac
SY23433B	7W

Fig.1 Schematic Diagram

## Pinout (top view)



(SSOP10)

**Top Mark:** CLLxyz (device code: CLL, x=year code, y=week code, z= lot number code)

Pin	Name	Description
1	VCC	Power supply pin.
2	VREG	Aux-winding voltage detection pin. Connect this pin to a voltage sensing circuit (shown in fig.1) to prevent the output voltage from raising too high with light load during strong magnetic field test.
3	GND	Ground pin.
4	VSEN	Inductor current zero-crossing detection pin. This pin receives the auxiliary winding voltage by a resistor divider and detects the inductor current zero crossing point.
5	ISEN	Current sense pin. Connect this pin to the source of the primary switch.
6~10	DRAIN	Drain of the internal power MOSFET.

## Absolute Maximum Ratings (Note 1)

VCC	-----	-0.3V~25V
VREG	-----	-0.3V~3.3V
ISEN	-----	-0.3V~3.6V
VSEN	-----	-0.3V~V <sub>VCC</sub> +0.3V
DRAIN	-----	900V
Power Dissipation, @ TA = 25°C SSOP10	-----	1.1W
Package Thermal Resistance (Note 2)		
SSOP10, $\theta_{JA}$	-----	125°C/W
SSOP10, $\theta_{JA}$	-----	60°C/W
Junction Temperature Range	-----	-45°C to 150°C
Lead Temperature (Soldering, 10 sec.)	-----	260°C
Storage Temperature Range	-----	-65°C to 150°C

## Recommended Operating Conditions (Note 3)

VCC	-----	10V~17V
ISEN	-----	0V~1V
Junction Temperature Range	-----	-40°C to 125°C
Ambient Temperature Range	-----	-40°C to 105°C

## Block Diagram

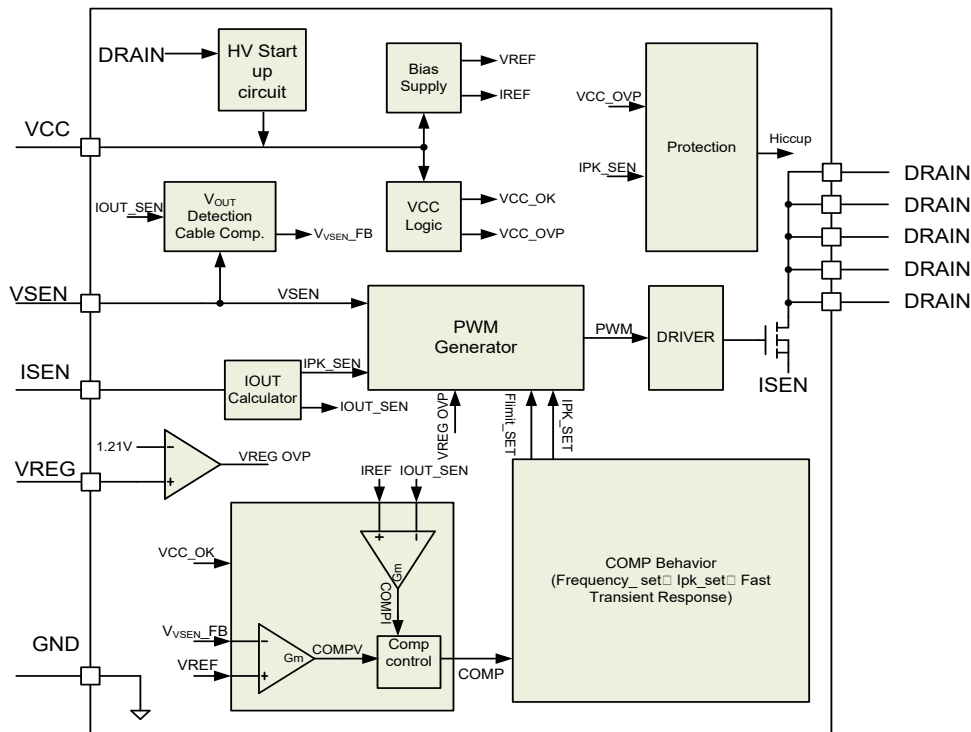


Fig.2 Block Diagram

## Electrical Characteristics

(V<sub>CC</sub> = 12V (Note 3), T<sub>A</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Power Supply Section</b>						
VCC Operating Range	V <sub>VCC_RANGE</sub>		8.5		21	V
VCC Turn-on Threshold	V <sub>VCC_ON</sub>		19.4	21	22.6	V
VCC Turn-off Threshold	V <sub>VCC_OFF</sub>		6.6	7.6	8.6	V
VCC OVP Voltage	V <sub>VCC_OVP</sub>			24		V
Start Up Current	I <sub>ST</sub>	V <sub>VCC</sub> < V <sub>VCC_OFF</sub>		2.3	5	μA
Operating Current	I <sub>VCC</sub>	f=100kHz		1.5		mA
Quiescent Current	I <sub>Q</sub>	f=2kHz	200	350	500	μA
Discharge Current in OVP Mode	I <sub>VCC_OVP</sub>	V <sub>VCC</sub> =12V		5		mA
Internal HV Start Up VCC Charge Current	I <sub>HV_STARTUP</sub>			0.35		mA
<b>Current Feedback Modulator Section</b>						
Internal Reference Voltage for Output Current	V <sub>REF</sub>		0.411	0.42	0.429	V
<b>VREG Pin Section</b>						
VREG Pin OVP Voltage Threshold	V <sub>VREG_OVP</sub>		1.1	1.21	1.3	V
<b>ISEN Pin Section</b>						
Current Limit Voltage	V <sub>ISEN_LIM</sub>		0.9	1	1.1	V
<b>VSEN Pin Section</b>						
Internal Reference Voltage	V <sub>REFV</sub>		1.238	1.25	1.262	V
<b>Integrated MOSFET Section</b>						
Breakdown Voltage	V <sub>BV</sub>	V <sub>GS</sub> =0V, I <sub>DS</sub> =250μA	900			V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =12V, I <sub>DS</sub> =0.1A, T <sub>A</sub> =25°C		13.4		Ω
Drain Current Continuous	I <sub>DS</sub>	T <sub>A</sub> =25°C			0.35	A
<b>Switching Section</b>						
Max ON Time	T <sub>ON_MAX</sub>			18		μs
Min ON Time	T <sub>ON_MIN</sub>			350		ns
Max OFF Time	T <sub>OFF_MAX</sub>		450	550	700	μs
Min OFF Time	T <sub>OFF_MIN</sub>		1.2	1.7	2.2	μs
Maximum Switching Frequency	F <sub>MAX</sub>		95	120	145	kHz
<b>Thermal Section</b>						
Thermal Shutdown Temperature	T <sub>SD</sub>			150		°C
Thermal Shutdown Recovery Hysteresis				30		°C

**Note 1:** Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:** θ<sub>JA</sub> is measured in the natural convection at T<sub>A</sub> = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on “2 x 2” FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

**Note 3:** Increase VCC pin voltage gradually higher than V<sub>VCC\_ON</sub> voltage then regulated to 12V.

## Operation

SY23433B is a flyback regulator with several features to enhance performance of the converters.

It integrates a 900V MOSFET to handle high AC input voltage and enhance reliability of the converters.

To achieve higher efficiency and better EMI performance, SY23433B drives Flyback converters in the Quasi-Resonant mode; the maximum switching frequency is limited to 125kHz.

The output current is monitored by primary side detection technology, and the maximum output current can be programmed in Over Current Protection and Short Circuit Protection.

SY23433B can be applied in power supply for STB home appliances, smart power meter and other appliances with high AC input voltage.

A special OVP function of VREG pin has been integrated in SY23433B to prevent the output voltage from raising too high with light load during strong magnetic field test, which is special request for power meter. The OVP function should cooperate with a voltage sensing circuit shown in Fig.1.

SY23433B is available with SSOP10 package.

## Applications Information

### Start up

After AC supply or DC BUS is powered on, the capacitor  $C_{VCC}$  across VCC and GND pin is charged up by BUS voltage through an internal HV start up circuit. Once  $V_{VCC}$  rises up to  $V_{VCC-ON}$ , the internal blocks start to work.  $V_{VCC}$  will be pulled down by internal consumption of IC until the auxiliary winding of Flyback transformer could supply enough energy to maintain  $V_{VCC}$  above  $V_{VCC-OFF}$ .

The whole start up procedure is divided into two sections shown in Fig.3.  $t_{STC}$  is the  $C_{VCC}$  charged up section, and  $t_{STO}$  is the output voltage built-up section. The start up time  $t_{ST}$  composes of  $t_{STC}$  and  $t_{STO}$ , and usually  $t_{STO}$  is much smaller than  $t_{STC}$ .

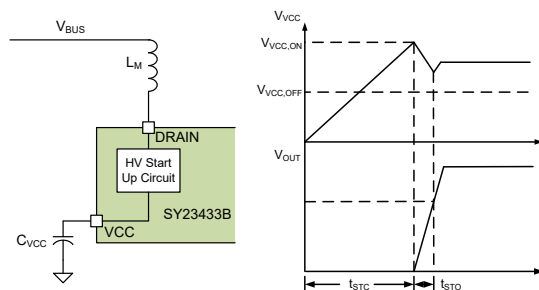


Fig.3 Start up

The  $C_{VCC}$  are designed by rules below:

Select  $C_{VCC}$  to obtain an ideal start up time  $t_{ST}$ , and ensure the output voltage is built up at one time.

$$C_{VCC} = \frac{(I_{HV,Startup} - I_{ST}) \times t_{ST}}{V_{VCC-ON}} \quad (1)$$

If the  $C_{VCC}$  is not big enough to build up the output voltage at one time, increase  $C_{VCC}$  until the ideal start up procedure is obtained.

### Shut down

After AC supply or DC BUS is powered off, the energy stored in the BUS capacitor will be discharged. When the auxiliary winding of Flyback transformer can not supply enough energy to VCC pin,  $V_{VCC}$  will drop down. Once  $V_{VCC}$  is below  $V_{VCC-OFF}$ , the IC will stop working and  $V_{COMP}$  will be discharged to zero.

### Quasi-Resonant Operation

QR mode operation provides low turn-on switching losses for Flyback converter.

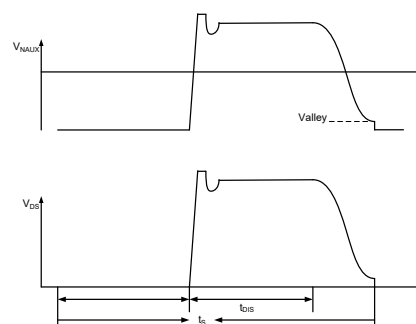


Fig.4 QR mode operation

The voltage across drain and source of the primary MOSFET is reflected by the auxiliary winding of the Flyback transformer. VSEN pin detects the voltage across the auxiliary winding by a resistor divider. When the voltage across drain and source of the primary MOSFET is at voltage valley, the MOSFET would be turned on.

## Output Voltage Control (CV control)

In order to achieve primary side constant voltage control, the output voltage is detected by the auxiliary winding voltage.

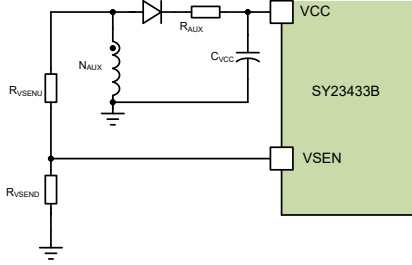


Fig.5 VSEN pin connection

As shown in Fig.5, during OFF time, the voltage across the auxiliary winding is

$$V_{AUX} = (V_{OUT} + V_{D-F}) \times \frac{N_{AUX}}{N_S} \quad (2)$$

$N_{AUX}$  is the turns of auxiliary winding;  $N_S$  is the turns of secondary winding;  $V_{D-F}$  is the forward voltage of the power diode.

At the current zero-crossing point,  $V_{D-F}$  is nearly zero, so  $V_{OUT}$  is proportional with  $V_{AUX}$  exactly. The voltage of this point is sampled by the IC as the feedback of output voltage. The resistor divider is designed by

$$\frac{V_{VSEN-REF}}{V_{OUT}} = \frac{R_{VSEND}}{R_{VSENU} + R_{VSEND}} \times \frac{N_{AUX}}{N_S} \quad (3)$$

Where  $V_{VSEN-REF}$  is the internal voltage reference.

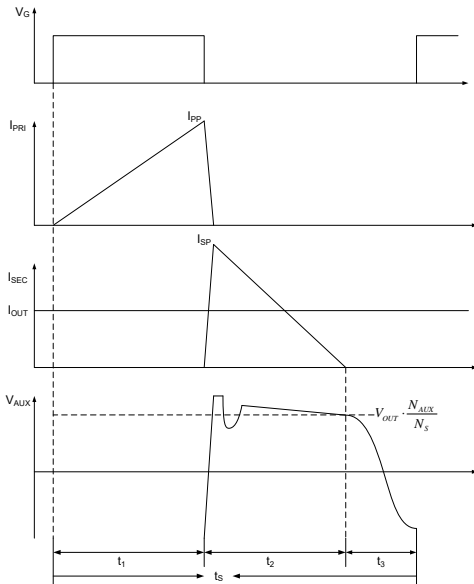


Fig.6 Auxiliary winding voltage waveforms

## Output Current Control (CC control)

The output current is regulated by SY23433B with primary side detection technology, the maximum output current  $I_{OUT-LIM}$  can be set by

$$I_{OUT-LIM} = \frac{k_1 \times V_{REF} \times N_{PS}}{R_S} \quad (4)$$

Where  $k_1$  is the output current weight coefficient;  $V_{REF}$  is the internal reference voltage;  $R_S$  is the current sense resistor.

$k_1$  and  $V_{REF}$  are all internal constant parameters,  $I_{OUT-LIM}$  can be programmed by  $N_{PS}$  and  $R_S$ .

$$R_S = \frac{k_1 \times V_{REF} \times N_{PS}}{I_{OUT}} \quad (5)$$

$k_1$  is set to 0.5

When over current operation or short circuit operation happens, the output current will be limited at  $I_{OUT-LIM}$ . The V-I curve is shown as Fig.7.

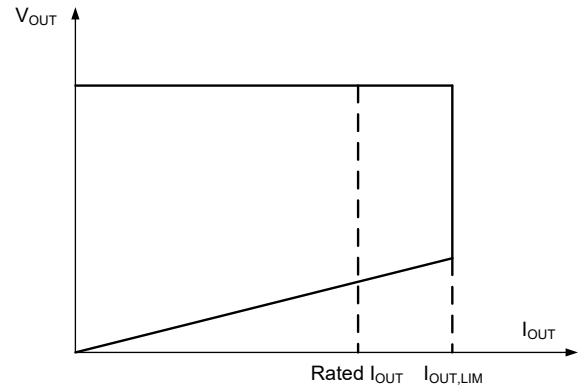


Fig.7 V-I curve

The IC provides line regulation modification function to improve line regulation performance of the output current.

Due to the sample delay of ISEN pin and other internal delay, the output current increases with increasing input BUS line voltage. A small compensation voltage  $\Delta V_{ISEN-C}$  is added to ISEN pin during ON time to improve such performance. This  $\Delta V_{ISEN-C}$  is adjusted by the upper resistor of the divider connected to VSEN pin.

$$\Delta V_{ISEN-C} = V_{BUS} \times \frac{N_{AUX}}{N_P} \times \frac{1}{R_{VSENU}} \times k_2 \quad (6)$$

Where  $R_{VSENU}$  is the upper resistor of the divider;  $k_2$  is an internal constant as the modification coefficient.

The compensation is mainly related with  $R_{VSENU}$ , larger compensation is achieved with smaller  $R_{VSENU}$ . Normally,  $R_{VSENU}$  ranges from 50kΩ~150kΩ.

## Short Circuit Protection (SCP)

There are two kinds of situations, one is the valley signal cannot be detected by VSEN, the other is the valley signal can be detected by VSEN.

When the output is shorted to ground, the output voltage is clamped to zero. The voltage of the auxiliary winding is proportional to the output winding, so valley signal cannot be detected by VSEN. There are two cases, the one is without valley detection, MOSFET cannot be turned on until maximum off time is reached. If MOSFET is turned on with maximum off-time for 64 times continuously which can not detected valley, IC will be shut down and enter into hiccup mode. The other is that IC will be shut down and enter into hiccup mode when  $V_{VCC}$  below  $V_{VCC-OFF}$  within 64 times.

When the output voltage is not low enough to disable valley detection in short condition, SY23433B will operate in CC mode until VCC is below  $V_{VCC-OFF}$ .

In order to guarantee SCP function not effected by voltage spike of auxiliary winding, a filter resistor  $R_{AUX}$  is needed.

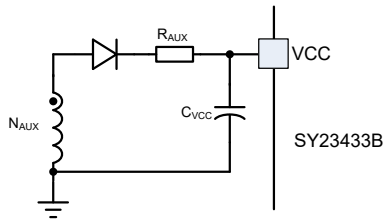


Fig. 8 Filter resistor  $R_{AUX}$

## OVP Function of VREG Pin

The aux-winding voltage is sensed by the circuit shown in Fig.9. R1 and R2 compose a voltage divider. The divided voltage is positive input of VREG OVP comparator. The OVP threshold is 1.21V. If VREG voltage exceeds 1.21V, the SY23433B will stop PWM pulse immediately. When the VREG voltage falls below 1.21V, the PWM will recover. The value of R1, R2 and C2 will determine the average output voltage when OVP occurs. C3 is a filter capacitor and usually on the order of pF.

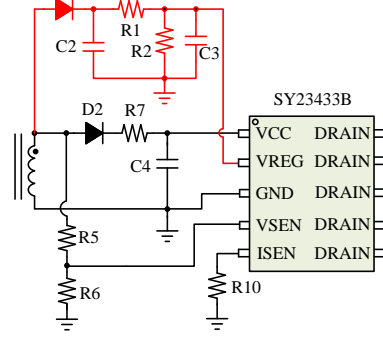


Fig. 9 circuit of VREG OVP

## VSEN Pin Short Protection

The SY23433B has a protection against faults caused by a shorted VSEN pin or a shorted pull-down resistor. During start-up, the voltage on the VSEN pin is monitored. In normal situations, the voltage on the VSEN pin reaches the sense protection trigger level. When the VSEN voltage does not reach this level, the VSEN pin is shorted and the protection is activated. The IC stops switching and discharge the VCC voltage. Once  $V_{VCC}$  is below  $V_{VCC-OFF}$ , the IC will shut down and be charged again by HV start up. In order to ensure reliable detection, the pull-down resistor should larger than 2kΩ.

## Power Device Design

### MOSFET and Diode

When the operation condition is with maximum input voltage and full load, the voltage stress of MOSFET and secondary power diode is maximized.

$$V_{MOS\_DS\_MAX} = \sqrt{2}V_{AC\_MAX} + N_{PS} \times (V_{OUT} + V_{D,F}) + \Delta V_S \quad (7)$$

$$V_{D\_R\_MAX} = \frac{\sqrt{2}V_{AC\_MAX}}{N_{PS}} + V_{OUT} \quad (8)$$

Where  $V_{AC\_MAX}$  is maximum input AC RMS voltage;  $N_{PS}$  is the turns ratio of the Flyback transformer;  $V_{OUT}$  is the rated output voltage;  $V_{D,F}$  is the forward voltage of secondary power diode;  $\Delta V_S$  is the overshoot voltage clamped by RCD snubber during OFF time.

When the operation condition is with minimum input voltage and full load, the current stress of MOSFET and power diode is maximized.

$$I_{MOS\_PK\_MAX} = I_{P\_PK\_MAX} \quad (9)$$

$$I_{MOS\_RMS\_MAX} = I_{P\_RMS\_MAX} \quad (10)$$

$$I_{D\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} \quad (11)$$

$$I_{D\_AVG} = I_{OUT} \quad (12)$$

Where  $I_{P\_PK\_MAX}$  and  $I_{P\_RMS\_MAX}$  are maximum primary peak current and RMS current, which will be introduced later.

### Transformer ( $N_{PS}$ and $L_M$ )

$N_{PS}$  is limited by the electrical stress of the power MOSFET:

$$N_{PS} \leq \frac{V_{MOS\_BR/DS} \times 90\% - \sqrt{2} V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \quad (13)$$

Where  $V_{MOS\_BR/DS}$  is the breakdown voltage of the power MOSFET;  $V_{AC\_MAX}$  is maximum input AC RMS voltage.

In Quasi-Resonant mode, each switching period cycle  $t_s$  consists of three parts: current rising time  $t_1$ , current falling time  $t_2$  and quasi-resonant time  $t_3$  shown in Fig.10.

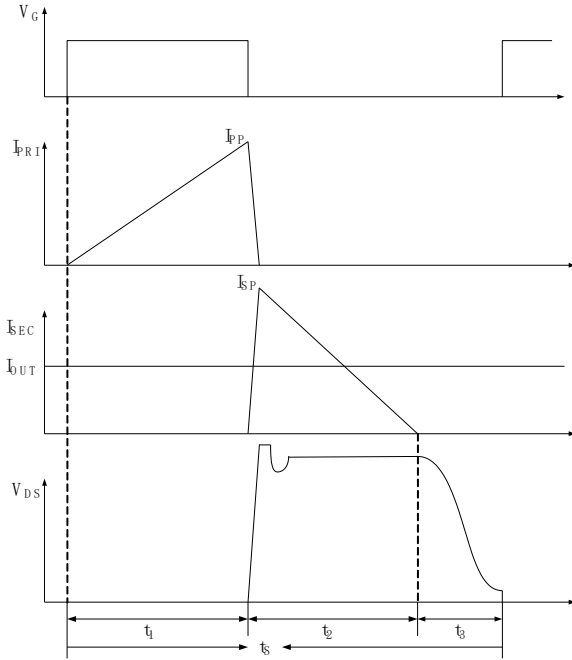


Fig.10 switching waveforms

When the operation condition is with minimum input AC RMS voltage and full load, the switching frequency is minimum frequency, the maximum peak current through MOSFET and the transformer happens.

Once the minimum frequency  $f_{S\_MIN}$  is set, the inductance of the transformer could be induced. The design flow is shown as below:

(a) Select  $N_{PS}$ ;

$$N_{PS} \leq \frac{V_{MOS\_BR/DS} \times 90\% - \sqrt{2} V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \quad (14)$$

(b) Preset minimum frequency  $f_{S\_MIN}$ ;

(c) Compute inductor  $L_M$  and maximum primary peak current  $I_{P\_PK\_MAX}$ ;

$$I_{P\_PK\_MAX} = \frac{2P_{OUT}}{\eta \times V_{DC\_MIN}} + \frac{2P_{OUT}}{\eta \times N_{PS} \times (V_{OUT} + V_{D\_F})} + \pi \sqrt{\frac{2P_{OUT}}{\eta} \times C_{Drain} \times f_{S\_MIN}} \quad (15)$$

$$L_M = \frac{2P_{OUT}}{\eta \times I_{P\_PK\_MAX}^2 \times f_{S\_MIN}} \quad (16)$$

Where  $C_{Drain}$  is the parasitic capacitance at drain of MOSFET;  $\eta$  is the efficiency;  $P_{OUT}$  is rated full load power;  $V_{DC\_MIN}$  is minimum input DC RMS voltage.

(d) Compute current rising time  $t_1$  and current falling time  $t_2$ ;

$$t_1 = \frac{L_M \times I_{P\_PK\_MAX}}{V_{DC\_MIN}} \quad (17)$$

$$t_2 = \frac{L_M \times I_{P\_PK}}{N_{PS} \times (V_{OUT} + V_{D\_F})} \quad (18)$$

$$t_s = \frac{1}{f_{S\_MIN}} \quad (19)$$

(e) Compute primary maximum RMS current  $I_{P\_RMS\_MAX}$  for the transformer fabrication;

$$I_{P\_RMS\_MAX} = \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \sqrt{\frac{t_1}{t_s}} \quad (20)$$

(f) Compute secondary maximum peak current  $I_{S\_PK\_MAX}$  and RMS current  $I_{S\_RMS\_MAX}$  for the transformer fabrication.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} \quad (21)$$

$$I_{S\_RMS\_MAX} = \frac{\sqrt{3}}{3} N_{PS} \times I_{P\_PK\_MAX} \times \sqrt{\frac{t_2}{t_s}} \quad (22)$$

### Transformer Design ( $N_P$ , $N_S$ , $N_{AUX}$ )

The design of the transformer is similar with ordinary Flyback transformer. The parameters below are necessary:

Necessary parameters	
Turns ratio	$N_{PS}$
Inductance	$L_M$
Primary maximum current	$I_{P-PK-MAX}$
Primary maximum RMS current	$I_{P-RMS-MAX}$
Secondary maximum RMS current	$I_{S-RMS-MAX}$

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area  $A_e$ ;

(b) Preset the maximum magnetic flux  $\Delta B$ ;

$$\Delta B = 0.22 \sim 0.26 T$$

(c) Compute primary turn  $N_P$ ;

$$N_P = \frac{L_M \times I_{P-PK-MAX}}{\Delta B \times A_e} \quad (23)$$

(d) Compute secondary turn  $N_S$ ;

$$N_S = \frac{N_P}{N_{PS}} \quad (24)$$

(e) Compute auxiliary turn  $N_{AUX}$ ;

$$N_{AUX} = N_S \times \frac{V_{VCC}}{V_{OUT}} \quad (25)$$

Where  $V_{VCC}$  is the working voltage of VCC pin (11V~13V is recommended);

(f) Select an appropriate wire diameter;

With  $I_{P-RMS-MAX}$  and  $I_{S-RMS-MAX}$ , select appropriate wire to make sure the current density ranges from 4A/mm<sup>2</sup> to 10A/mm<sup>2</sup>.

(g) If the winding area of the core and bobbin is not enough, reselect the core style, go to (a) and redesign the transformer until the ideal transformer is achieved.

### Input capacitor $C_{BUS}$

Generally, the input capacitor  $C_{BUS}$  is selected by

$$C_{BUS} = 2 \sim 3 \mu F / W$$

Or more accurately by

$$C_{BUS} = \frac{\arcsin(1 - \frac{V_{DC,MIN}}{\sqrt{2}V_{AC,MIN}}) + \frac{\pi}{2}}{\pi} \frac{P_{OUT}}{\eta} \frac{1}{2f_{IN} V_{AC,MIN}^2 (1 - \frac{V_{DC,MIN}}{\sqrt{2}V_{AC,MIN}})^2} \quad (26)$$

Where  $V_{DC,MIN}$  is the minimum voltage of BUS line;  $f_{IN}$  is AC line frequency;

### RCD Snubber for MOSFET

The power loss of the snubber  $P_{RCD}$  is evaluated first.

$$P_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D,F}) + \Delta V_S}{\Delta V_S} \times \frac{L_K}{L_M} \times P_{OUT} \quad (27)$$

Where  $N_{PS}$  is the turns ratio of the Flyback transformer;  $V_{OUT}$  is the output voltage;  $V_{D,F}$  is the forward voltage of the power diode;  $\Delta V_S$  is the overshoot voltage clamped by RCD snubber;  $L_K$  is the leakage inductor;  $L_M$  is the inductance of the Flyback transformer;  $P_{OUT}$  is the output power.

The  $R_{RCD}$  is related with the power loss:

$$R_{RCD} = \frac{[N_{PS} \times (V_{OUT} + V_{D,F}) + \Delta V_S]^2}{P_{RCD}} \quad (28)$$

The  $C_{RCD}$  is related with the voltage ripple of the snubber  $\Delta V_{C-RCD}$ :

$$C_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D,F}) + \Delta V_S}{R_{RCD} \times f_s \times \Delta V_{C-RCD}} \quad (29)$$

## Layout

(a) To achieve better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to the BUS line capacitor first, then to the switching circuit;

(b) The ground of the BUS line capacitor, the ground of the current sample resistor and the signal ground of the IC should be connected in a star connection;

(c) The circuit loop of all switching circuit should be kept small: primary power loop, secondary loop and auxiliary power loop.

## Design Example

A design example of multiple output power supply of smart power meter y is shown below step by step.

### #1. Identify Design Specification

Design Specification			
V <sub>AC,MIN</sub>	85V	V <sub>AC,MAX</sub>	300V
V <sub>OUT1</sub>	16V	I <sub>OUT1</sub>	0.2A
V <sub>OUT2</sub>	16V	I <sub>OUT2</sub>	0.2A
P <sub>OUT,Total</sub>	6.4W	η	75%
f <sub>IN,MIN</sub>	60KHz		

### #2. Transformer Design (N<sub>PS</sub> and L<sub>M</sub>)

Refer to Power Device Design

Conditions			
V <sub>AC,MIN</sub>	85V	V <sub>AC,MAX</sub>	300V
P <sub>OUT</sub>	6.4W	f <sub>S,MIN</sub>	60kHz
Parameters designed			
V <sub>MOS-(BR)DS</sub>	900V	ΔV <sub>S</sub>	80V
C <sub>Drain</sub>	100pF	V <sub>D,F</sub>	0.7V

(a) Compute turns ratio N<sub>PS</sub> first;

$$\begin{aligned}
 N_{PS} &\leq \frac{V_{MOS-(BR)DS} \times 90\% - \sqrt{2} V_{AC,MAX} - \Delta V_S}{V_{OUT} + V_{D,F}} \\
 &= \frac{900V \times 0.9 - \sqrt{2} \times 300V - 80V}{16V + 0.7V} \\
 &= 18.3
 \end{aligned}$$

N<sub>PS</sub> is set to

$$N_{PS} = 7$$

(b) f<sub>S,MIN</sub> is preset ;

$$f_{S,MIN} = 60kHz$$

(c) Compute inductor L<sub>M</sub> and maximum primary peak current I<sub>P,PK,MAX</sub>;

$$\begin{aligned}
 I_{P,PK,MAX} &= \frac{2P_{OUT}}{\eta \times (\sqrt{2} V_{AC,MIN} - \Delta V_{BUS})} + \frac{2P_{OUT}}{\eta \times N_{PS} \times (V_{OUT} + V_{D,F})} + \pi \sqrt{\frac{2P_{OUT}}{\eta} \times C_{Drain} \times f_{S,MIN}} \\
 &= \frac{2 \times 6.4W}{0.75 \times (\sqrt{2} \times 85V - 0.3 \times \sqrt{2} \times 85V)} + \frac{2 \times 6.4W}{0.75 \times 7 \times (16V + 0.7V)} + \pi \times \sqrt{\frac{2 \times 6.4W}{0.75} \times 100pF \times 60KHz} \\
 &= 0.381A
 \end{aligned}$$

$$L_m = \frac{2P_{OUT}}{\eta \times I_{P,PK,MAX}^2 \times f_{S,MIN}}$$

$$= \frac{2 \times 6.4W}{0.75 \times (0.381A)^2 \times 60KHz}$$

$$= 1.96mH$$

Set

$$L_M = 1.96mH$$

(d) Compute current rising time  $t_1$  and current falling time  $t_2$ ;

$$t_1 = \frac{L_M \times I_{P,PK,MAX}}{V_{BUS}} = \frac{1.96mH \times 0.381A}{\sqrt{2} \times 85V} = 6.21\mu s$$

$$t_2 = \frac{L_m \times I_{P,PK,MAX}}{N_{PS} \times (V_{OUT} + V_{D,F})} = \frac{1.96mH \times 0.381A}{7 \times (16V + 0.7V)} = 6.39\mu s$$

$$t_3 = \pi \times \sqrt{L_M \times C_{Drain}} = \pi \times \sqrt{1.96mH \times 100pF} = 1.39\mu s$$

$$t_s = t_1 + t_2 + t_3 = 6.21\mu s + 6.39\mu s + 1.39\mu s = 13.99\mu s$$

(e) Compute primary maximum RMS current  $I_{P,RMS,MAX}$  for the transformer fabrication;

$$I_{P,RMS,MAX} = \frac{\sqrt{3}}{3} I_{P,PK,MAX} \times \sqrt{\frac{t_1}{t_s}} = \frac{\sqrt{3}}{3} \times 0.381A \times \sqrt{\frac{6.21\mu s}{13.99\mu s}} = 0.147A$$

(f) Compute secondary maximum peak current  $I_{S,PK,MAX}$  and RMS current  $I_{S,RMS,MAX}$  for the transformer fabrication.

$$I_{S,PK,MAX} = N_{PS} \times I_{P,PK,MAX} = 7 \times 0.381A = 2.667A$$

$$I_{S,RMS,MAX} = N_{PS} \times \frac{\sqrt{3}}{3} I_{P,PK,MAX} \times \sqrt{\frac{t_2}{t_s}} = 7 \times \frac{\sqrt{3}}{3} \times 0.381A \times \sqrt{\frac{6.39\mu s}{13.99\mu s}} = 1.041A$$

### #3. MOSFET and Diode Design

Conditions			
$V_{AC,MAX}$	300V	$N_{PS}$	7
$V_{OUT1}$	16V	$V_{D,F}$	0.7V
$V_{OUT2}$	16V	$N_{PS2}$	7
$\Delta V_S$	80V	$\eta$	75%

(a) Compute the voltage and the current stress of MOSFET:

$$V_{MOS,DS,MAX} = \sqrt{2} V_{AC,MAX} + N_{PS} \times (V_{OUT} + V_{D,F}) + \Delta V_S$$

$$= \sqrt{2} \times 300V + 7 \times (16V + 0.7V) + 80V$$

$$= 621V$$

$$I_{MOS,PK,MAX} = I_{P,PK,MAX} = 0.381A$$

$$I_{MOS\_RMS\_MAX} = I_{P\_RMS\_MAX} = 0.147A$$

(b) Compute the voltage and the current stress of secondary power diode

$$V_{D1\_R\_MAX} = V_{D2\_R\_MAX} = \frac{\sqrt{2}V_{AC\_MAX}}{N_{PS}} + V_{OUT} = \frac{\sqrt{2} \times 300V}{7} + 16V = 76.6V$$

$$I_{D1\_AVG} = I_{OUT1} = I_{OUT2} = 0.2A$$

#4. Select the input capacitor  $C_{IN}$

Refer to input capacitor  $C_{IN}$  Design

Known conditions at this step			
$V_{AC\_MIN}$	85V	$\Delta V_{BUS}$	30% $V_{AC\_MIN}$

$$C_{BUS} = \frac{\arcsin(1 - \frac{\Delta V_{BUS}}{\sqrt{2}V_{AC\_MIN}}) + \frac{\pi}{2}}{\pi} \times \frac{P_{OUT}}{\eta} \times \frac{1}{2f_{IN} V_{AC\_MIN}^2 [1 - (1 - \frac{\Delta V_{BUS}}{\sqrt{2}V_{AC\_MIN}})^2]}$$

$$= \frac{\arcsin(1 - \frac{0.3 \times \sqrt{2} \times 85V}{\sqrt{2} \times 85V}) + \frac{\pi}{2}}{\pi} \times \frac{6.4W}{0.75} \times \frac{1}{2 \times 50Hz \times 85V^2 \times [1 - (1 - \frac{0.3 \times \sqrt{2} \times 85V}{\sqrt{2} \times 85V})^2]}$$

$$= 12.4\mu F$$

$$\text{Set } C_{BUS} = 12\mu F$$

The rated voltage of BUS E-cap is 450V or 500V

Where  $\Delta V_{BUS}$  is the voltage ripple of BUS line.

#5. Set current sense resistor to achieve ideal output current

Refer to **Primary-side constant-current control**

Known conditions at this step			
$k_1$	0.5	$N_{PS}$	7
$V_{REF}$	0.42V	$I_{OUT\_LIM}$	0.5A

The current sense resistor is

$$R_s = \frac{k_1 \times V_{REF} \times N_{PS}}{I_{OUT}}$$

$$= \frac{0.5 \times 0.42V \times 7}{0.5A}$$

$$= 2.94\Omega$$

$$\text{Set } R_s = 3\Omega$$

## #6. Set VSEN pin

Refer to V<sub>OUT</sub>

First identify R<sub>VSENU</sub> need for line regulation.

Parameters Designed			
R <sub>VSENU</sub>	43kΩ		

Then compute R<sub>VSEND</sub>

Conditions			
V <sub>OUT</sub>	16V	V <sub>VSEN_REF</sub>	1.25V
R <sub>VSENU</sub>	43kΩ		

Set N<sub>AUX</sub>=N<sub>S</sub>

$$R_{VSEND} = \frac{R_{VSENU}}{\frac{V_{OUT} N_{AUX}}{V_{VSEN\_REF} N_S} - 1} = \frac{43K}{\left(\frac{16V}{1.25V} - 1\right)} = 3.64K$$

R<sub>VSEND</sub>=3.6kΩ

## #7. Design output voltage OVP point during strong magnetic field test

First identify the maximum output voltage is 20V.

Set R<sub>VREG1</sub>=22kΩ

$$R_{VREG2} = \frac{R_{VREG1}}{\frac{V_{O,OVP}}{V_{REG,OVP}} - 1} = \frac{22}{\frac{20}{1.2} - 1} = 1.4k$$

Set R<sub>VREG2</sub>=1.5kΩ

## #8. Design RCD snubber

Refer to Power Device Design

Conditions			
V <sub>OUT</sub>	16V	ΔV <sub>S</sub>	80V
N <sub>PS</sub>	7	L <sub>K</sub> /L <sub>M</sub>	3%
P <sub>OUT</sub>	6.4W		

The power loss of the snubber is

$$P_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D_F}) + \Delta V_S}{\Delta V_S} \times \frac{L_K}{L_M} \times P_{OUT}$$

$$= \frac{7 \times (16V + 0.7V) + 80V}{80V} \times 0.03 \times 6.4W$$

$$= 0.47W$$

The resistor of the snubber is

$$R_{RCD} = \frac{[N_{PS} \times (V_{OUT} + V_{D_F}) + \Delta V_S]^2}{P_{RCD}}$$

$$= \frac{[7 \times (16V + 0.7V) + 80V]^2}{0.47W}$$

$$= 82k\Omega$$

The capacitor of the snubber is

$$C_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D_F}) + \Delta V_S}{R_{RCD} f_{S,MIN} \Delta V_{C\_RCD}}$$

$$= \frac{7 \times (16V + 0.7V) + 80V}{82k\Omega \times 60kHz \times 70V}$$

$$= 571pF$$

## #9. Final Result

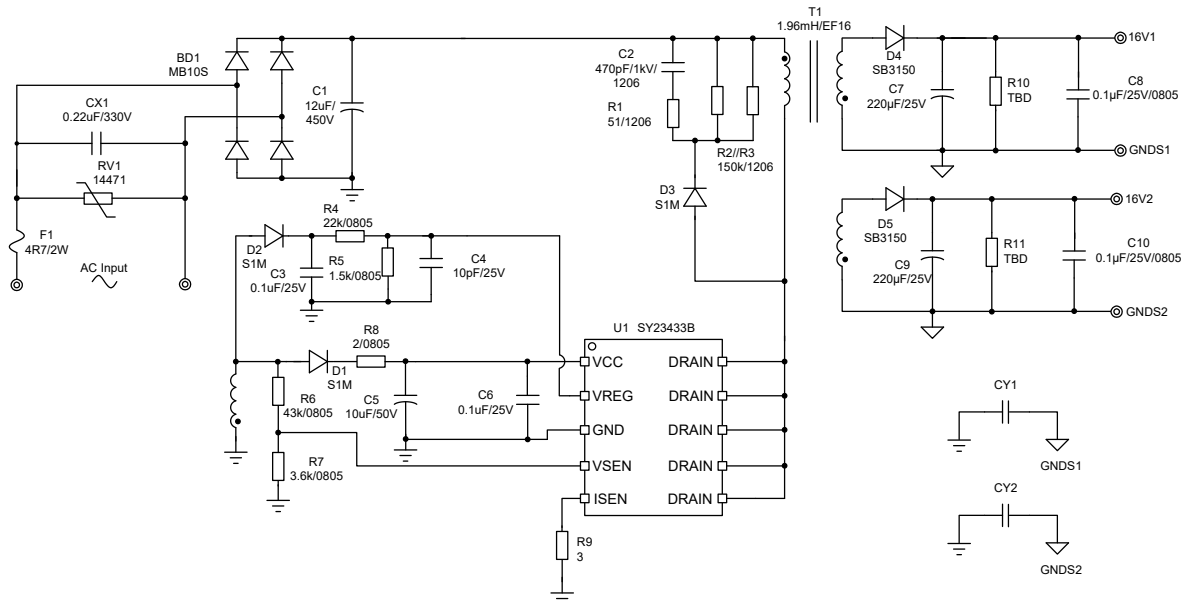
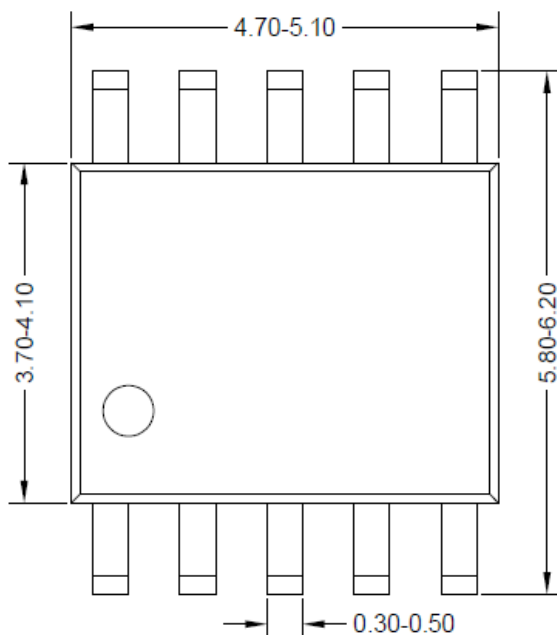
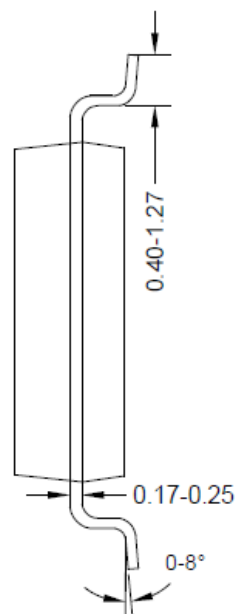


Fig.11 Final Result

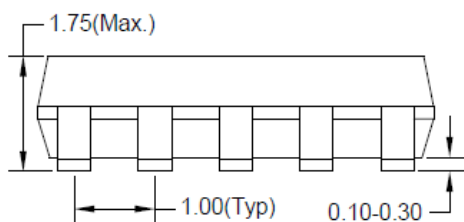
## SSOP10 Package Outline Drawing



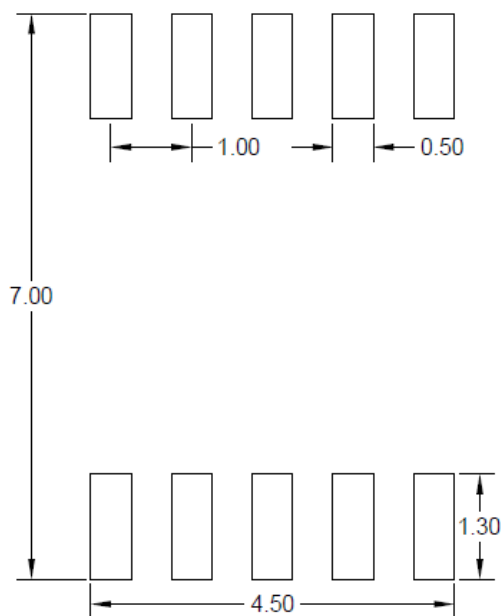
Top view



Side view



Front view



Recommended PCB layout

(Reference only)

**Notes:** All dimension in millimeter and exclude mold flash & metal burr.

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## Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
March 6, 2019	Revision 0.9	Initial Release

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