SY20867A

Single-channel, Adjustable Voltage Monitor in Ultra-small Package

General Description

The SY20867A is a voltage monitor which operates from 1.7V to 6.5V and has a low quiescent current with an active-high push-pull output.

The SY20867A monitors voltage above 500mV with 1% threshold accuracy over temperature and provides a programmable delay time using external capacitors. The SY20867A offers an active-high enable input to power on and off the output. The SY20867A is ideal for power-supply sequencing, reset sequencing, and power-switching applications. Multiple devices can be cascaded for complex sequencing applications.

The SY20867A is fully specified over the T_J = -40℃ to 125℃ operating temperature range. The SY20867A is available in an ultra-small DFN1.45mm×1mm-6 pin package.

Features

- Adjustable Threshold Down to 500mV
- Operating voltage: 1.7V to 6.5V
- Threshold Accuracy: 1% Over Temperature
- Capacitor-Adjustable Delay Time
- Active-High Enable Input
- Low Quiescent Current: 9μA (Typical)
- External Enable Input
- Temperature Range: -40°C to 125°C
- Compact Package: DFN1.45x1.0-6

Applications

- DSPs, Microcontrollers and Microprocessors
- Notebook and Desktop Computers
- PDAs and Handheld Products
- Portable and Battery-Powered Products
- FPGAs and ASICs

Typical Application

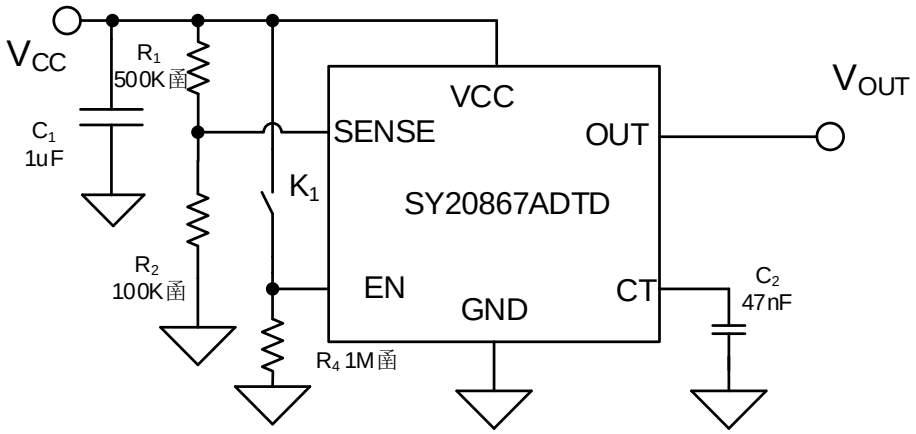


Figure 1. Schematic Diagram

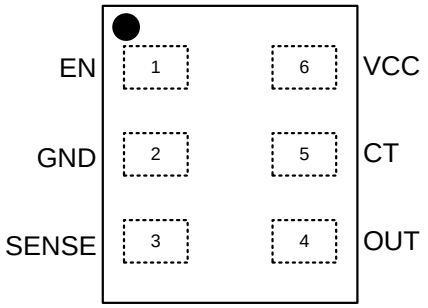
Ordering Information

Ordering Part Number	Package Type	Top Mark
SY20867ADTD	DFN1.45×1-6 RoHS Compliant and Halogen Free	**R*xyz***

Device code: R

x=year code, y=week code, z= lot number code

Pinout (top view)



Pin Name	Pin NO.	I/O	Pin Description
CT	5	I	Capacitor-adjustable delay. The CT pin offers a user-adjustable delay time. Connecting this pin to a ground-referenced capacitor sets the delay time for SENSE rising above 0.5V to OUT asserting or EN asserting to OUT asserting. $t_{pd(r)}(s) = [C_{CT}(\mu F) \times 4] + 40\mu s$
EN	1	I	Active high input. Driving EN low makes OUT go low immediately, independent of V_{SENSE}. With V_{SENSE} already above V_{IT+}, drive EN high to make OUT go high after the capacitor-adjust delay time.
GND	2	-	Ground.
SENSE	3	I	This pin is connected to the monitored voltage using a external resistor divider. The output asserts after the capacitor-adjustable delay time when VSENSE rises above 0.5V, and EN is asserted. The output de-asserts after a minimal propagation delay (16µs) when VSENSE falls below $V_{IT+} - V_{HYS}$.
OUT	4	O	OUT is a push-pull output that is immediately driven low after V_{SENSE} falls below ($V_{IT+} - V_{HYS}$) or the EN input is low. OUT goes high after the capacitor-adjustable delay time when V_{SENSE} is greater than V_{IT+} and the EN pin is high.
VCC	6	I	Supply voltage input. Connect a 1.7V to 6.5V supply to VCC to power the device. Place a 0.1µF ceramic capacitor close to this pin.

Block Diagram

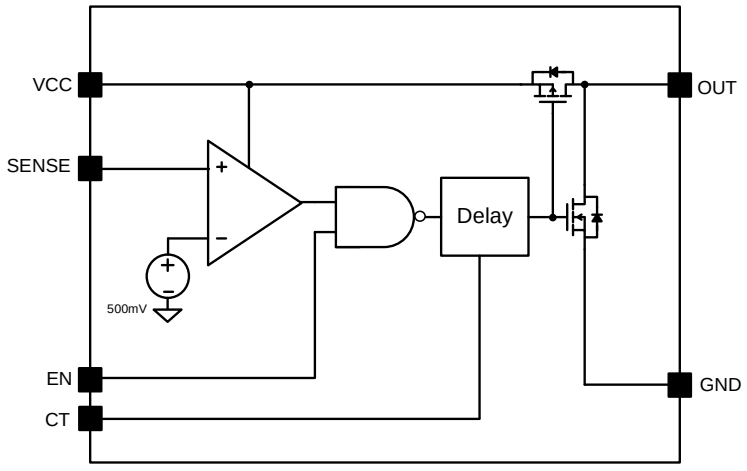


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VCC, EN, SENSE	-0.3	7	V
CT, OUT	-0.3	VCC+0.3	V
OUT Current	-10	+10	mA
Lead Temperature (Soldering, 10s)		260	°C
Junction Temperature, Operating	-40	125	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	293.8	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	165.1	
P_D Power Dissipation TA = 25°C	0.34	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VCC	1.7	6.5	V
OUT, CT, EN, SENSE	0	6.5	
OUT Current	0.0003	1	mA

Electrical Characteristics

Over the operating temperature range of T_J = -40°C to 125°C, and 1.7V < V_{CC} < 6.5V, unless otherwise noted. Typical values are at T_J = 25°C and V_{CC} = 3.3V.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{CC}		1.7		6.5	V
Power on Reset Voltage	V_{POR}	V_{OL} (max) =0.2V, I_{OUT} =15uA (Note 4)		0.72		V
Supply Current (into the VCC pin)	I_{CC}	V_{CC}=3.3V, T_A=25°C, No load		9	12	μA
		V_{CC}=3.3V, T_A=125°C, No load		12	14	μA
		V_{CC}=6.5V, T_A=25°C, No load		11	13.5	μA
		V_{CC}=6.5V, T_A=125°C, No load		14	16	μA
Positive-going Input Threshold Voltage	V_{IT+}	V_{SENSE} rising, -40°C <T_J < 125°C	0.495	0.5	0.505	V
Hysteresis Voltage	V_{HYS}	V_{SENSE} falling		5		mV
SENSE Input Current	I_{SENSE}	V_{SENSE} = 0V to V_{CC} (Note 5)	-15		15	nA
CT Pin Charge Current	I_{CT}		260	310	360	nA
CT Pin Comparator Threshold Voltage	V_{CT}		1.18	1.238	1.299	V
CT Pin Down Resistance	R_{CT}			200		Ω
Low-level Input Voltage (EN/#EN pin)	V_{IL}				0.4	V
High-level Input Voltage (EN/#EN)	V_{IH}		1.4			V
Under Voltage Lockout	V_{UVLO}	V_{CC} falling, (Note 6)	1.3		1.7	V
EN/#EN Leakage		EN/#EN = V_{CC} or GND	-100		100	nA

Low-level Output Voltage	V_{OL}	V_{CC} ≥ 1.2V, I_{SINK} = 90μA			0.3	V
		V_{CC} ≥ 2.25V, I_{SINK} = 0.5mA			0.3	V
		V_{CC} ≥ 4.5V, I_{SINK} = 1mA			0.4	V
High-level Output Voltage （push-pull）	V_{OH}	V_{CC} ≥ 2.25V, I_{SOURCE} = 0.5mA	0.8VCC			V
		V_{CC} ≥ 4.5V, I_{SOURCE} = 1mA	0.8VCC			V

Timing Requirements

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SENSE (rising) to OUT Propagation Delay	$t_{PD(r)}$	V_{SENSE} rising, C_{CT} = open		40		μs
		V_{SESNE} rising, C_{CT} = 0.047μF		190		ms
Sense (falling) to OUT Propagation Delay	$t_{PD(f)}$	V_{SENSE} falling	3	6	16	μs
Start-up Delay		(Note 7)		50		μs
EN Pin Minimum Pulse Duration	t_W		1			μs
EN Glitch Rejection	t_{EN_GLH}			100		ns
EN to OUT Delay Time (Output Disable)	t_{d_off}	EN de-asserted to output de-asserted		200		ns
EN to VOUT Delay Time	t_{d_ct}	EN asserted to output asserted delay, C_{CT}=open		20		μs
		EN asserted to output asserted delay, C_{CT}= 0.047uF		190		ms

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: ΘJA is measured in the natural convection at TA = 25°C on a low effective single-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions

Note 4: The lowest supply voltage (VCC) at which output is active (OUT is low); t_{r_VCC} > 15 μs/V. Below V_{POR}, the output cannot be determined.

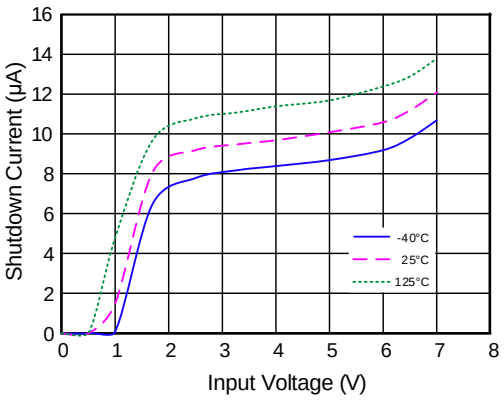
Note 5: Specified by design.

Note 6: When VCC falls below the UVLO threshold, the output de-asserts (OUT goes low). Below V(POR), the output cannot be determined.

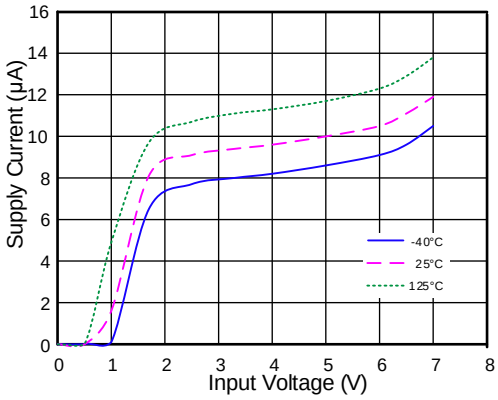
Note 7: During power on, V_{CC} must exceed 1.7V for at least 50μs (plus propagation delay time, $t_{PD(r)}$) before the output is in the correct state.

Typical Operating Characteristics

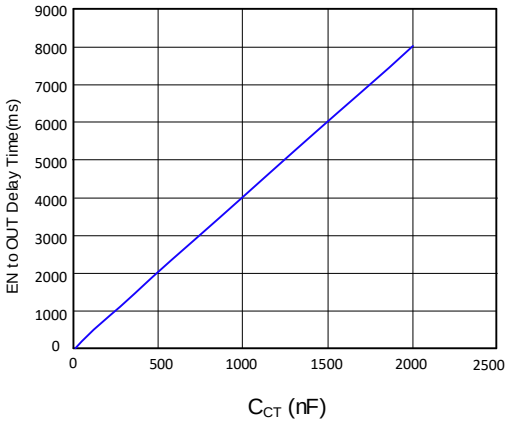
Shutdown Current vs. Input Voltage
(EN=0V, SENSE=0V, C_{IN}=1μF, CT=Null)



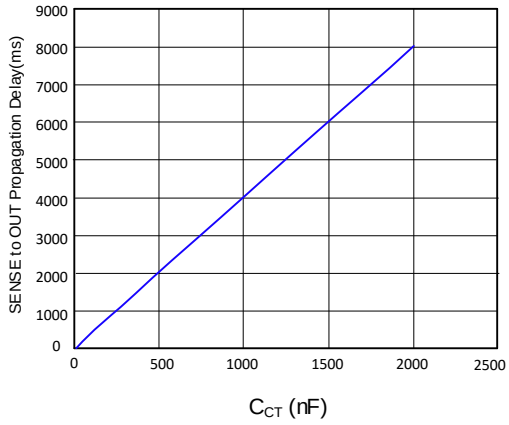
Supply Current vs. Input Voltage
(EN=V_{CC}, SENSE=0.6V, C_{IN}=1μF, CT=Null)



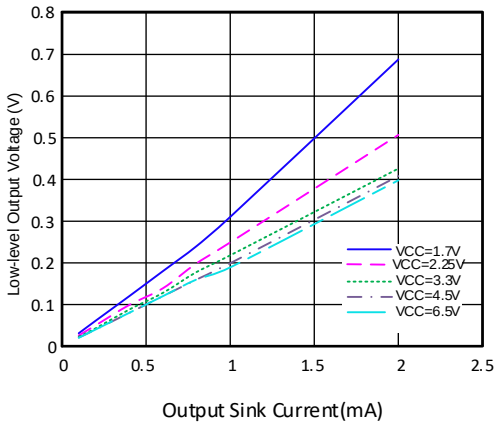
EN（Rising) to OUT Delay Time vs. C_{CT}
(V_{CC}=3.3V, EN=3V, SENSE=0.6V, C_{IN}=1μF, Null Load)



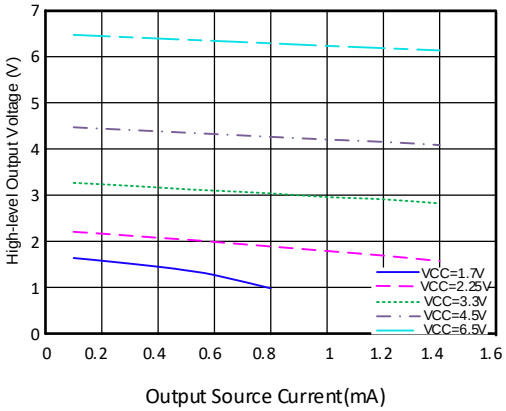
SENSE（Rising) to OUT Propagation Delay vs. C_{CT}
(V_{CC}=3.3V, EN=3V, SENSE=0.6V, C_{IN}=1μF, Null Load)



Output Voltage Low vs. Output Sink Current
(EN=0V SENSE=0V C_{IN}=1uF CT=Null)

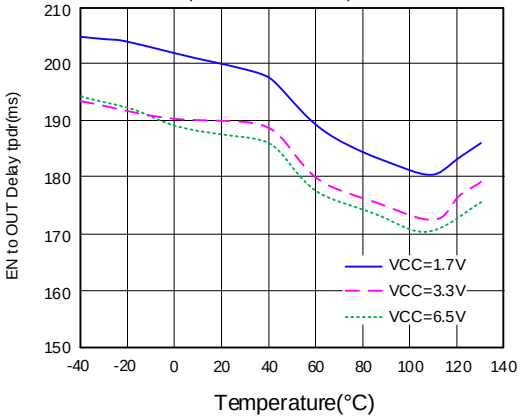


High-level output voltage vs. Output Source Current
(EN=3V SENSE=3V C_{IN}=1uF CT=Null)



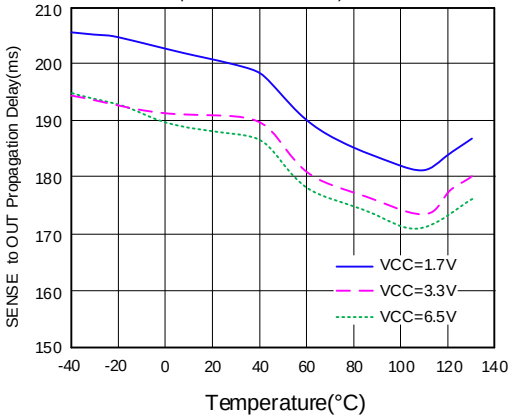
EN to OUT Delay vs. Temperature

(EN=3V, SENSE=0V to 0.6V, C_{IN}=1μF, CT=47nF, Output Sink Current=1mA)



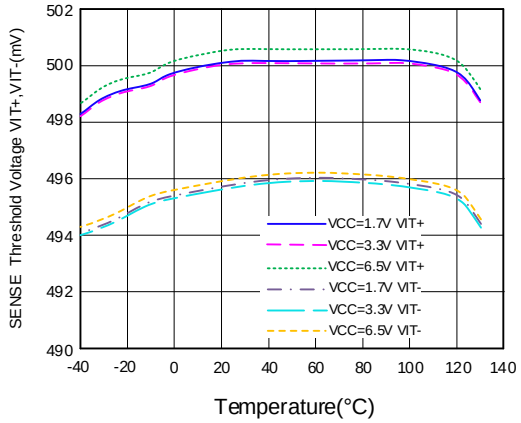
SENSE to OUT Propagation Delay vs. Temperature

(EN=3V, SENSE=0V to 0.6V, C_{IN}=1μF, CT=47nF, Output Sink Current=1mA)



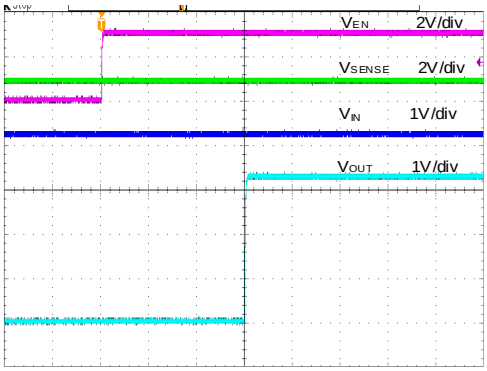
SENSE Threshold Voltage vs. Temperature

(EN=3V C_{IN}=1uF CT=Null)



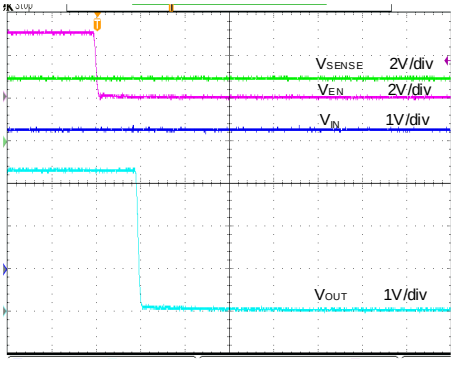
Startup from Enable

(V_{CC}=3.3V, EN=0V to 3V, C_{IN}=1μF, SENSE=3V, CT=Null)



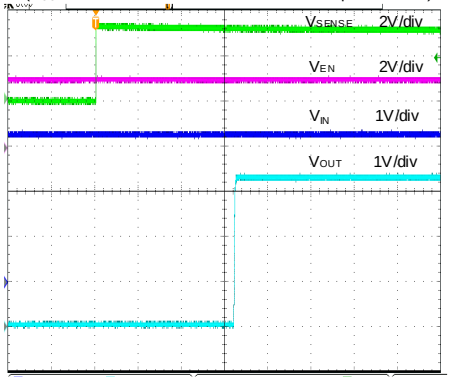
Shutdown from Enable

(V_{CC}=3.3V, EN=3V to 0V, C_{IN}=1μF, SENSE=3V, CT=Null)



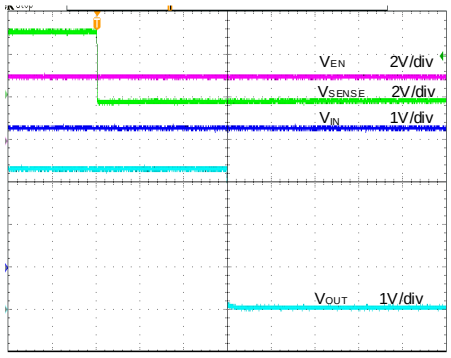
Startup from SENSE

(V_{CC}=3.3V, EN=3V, SENSE=0V to 3V, C_{IN}=1μF, CT=Null)



Shutdown from SENSE

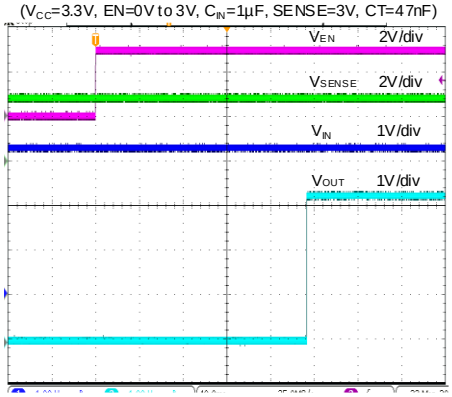
(V_{CC}=3.3V, EN=3V, SENSE=3V to 0V, C_{IN}=1μF, CT=Null)



Time (2μs/div)

Startup from Enable

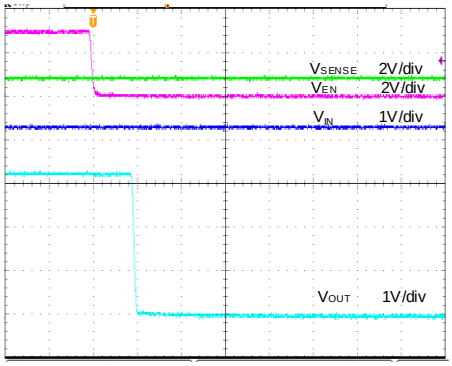
(V_{CC}=3.3V, EN=0V to 3V, C_{IN}=1μF, SENSE=3V, CT=47nF)



Time (40ms/div)

Shutdown from Enable

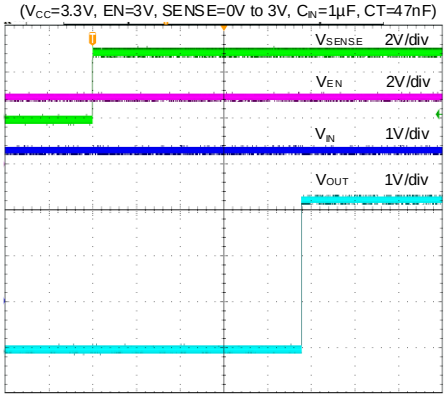
(V_{CC}=3.3V, EN=3V to 0V, C_{IN}=1μF, SENSE=3V, CT=47nF)



Time (200ns/div)

Startup from SENSE

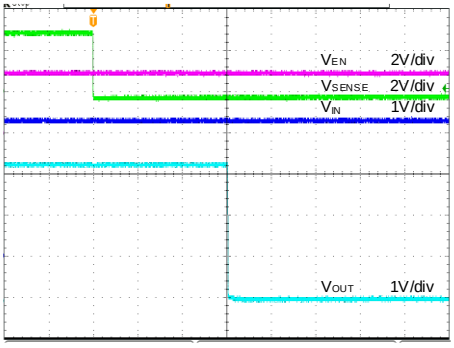
(V_{CC}=3.3V, EN=3V, SENSE=0V to 3V, C_{IN}=1μF, CT=47nF)



Time (40ms/div)

Shutdown from SENSE

(V_{CC}=3.3V, EN=3V, SENSE=3V to 0V, C_{IN}=1μF, CT=47nF)



Time (2μs/div)

Overview

The SY20867A operates from 1.7V to 6.5V and features low quiescent current with an active-high push-pull output.

The SY20867A monitors voltage above 500mV with 1% threshold accuracy over temperature, and provides a programmable delay time using an external capacitor. The SY20867A offers an active-high enable input to power on and off the output. The SY20867A is ideal for power-supply sequencing, reset sequencing, and power-switching applications. Multiple devices can be cascaded for complex sequencing applications.

The SY20867A is available in an ultra-small DFN1.45×1-6 package and is fully specified over the T_J = -40℃ to 125℃ operating temperature range.

Table 1. SY20867ADTD Truth Table

CONDITIONS		OUTPUT	STATUS
ENABLE = high	SENSE < VIT+	OUT = low	Output not asserted
ENABLE = low	SENSE < VIT+	OUT = low	Output not asserted
ENABLE = low	SENSE > VIT+	OUT = low	Output not asserted
ENABLE = high	SENSE > VIT+	OUT = high	Output asserted after delay

Timing Diagram

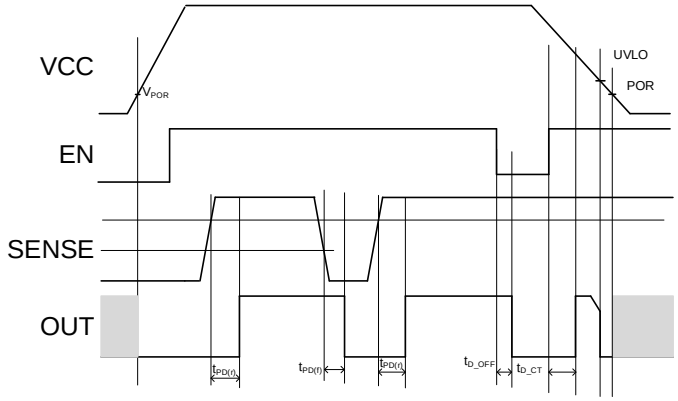
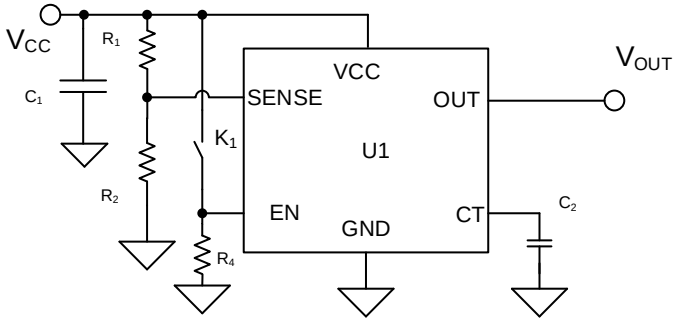


Figure 3. SY20867A Timing Diagram

Application Information

Schematic



BOM List

Reference Designator	Description	Part Number	Manufacturer
U1		SY20867ADTD	
C1	1μF/50V, 0603, X5R	GRM188R61H105K	Murata
C2	47nF/25V, 0603, X5R	GRM188R71H473K	Murata
R1	500kΩ, 0603		
R2	100kΩ, 0603		
R4	1MΩ, 0603		

Input Pin (SENSE)

The SENSE input pin can monitor a system voltage greater than 0.5V. If the voltage on the SENSE pin reaches V_{IT+}, and ENABLE is high, the output is asserted after the capacitor-adjustable delay time elapses. The output is de-asserted when the voltage on the SENSE pin falls below (VIT+ - Vhys). The comparator has a built-in hysteresis to ensure noise free output assertions and de-assertions. Although not required in most cases, using a 1nF to 10nF bypass capacitor at the SENSE input for noisy applications to reduce sensitivity to transients and parasitic layout is recommended. Equation 1 can be used to determine the target threshold voltage:

$$V_{TARGET} = (1+R1/R2) \times 0.5\ (V) \qquad (1)$$

Output Delay Time Pin (CT)

The OUT delay time can be adjusted by adding an external capacitor between the CT pin and ground. If the CT pin is floating, the device uses a delay of 40μs. The adjustable delay time can be determined using Equation 2:

$$t_{pd(r)}\ (s) = [C_{CT}\ (\mu F) \times 4] + 40\ \mu s \qquad (2)$$

The reset delay time is determined by the time it takes for an on-chip, precision 310nA current source to charge the external capacitor to 1.24V. When SENSE > V_{IT+} and ENABLE is high, the internal current source is enabled and starts charging the external capacitors. The corresponding OUT will be asserted when the CT voltage across a capacitor reaches 1.24V. Note that a ceramic capacitor is recommended and that stray capacitance around this pin may cause errors in the reset delay time.

Output pin (OUT)

For typical applications, the output is connected to the processor's reset/enable input (DSP, CPU, FPGA, ASIC, etc.) or to a voltage regulator's input.

The SY20867A integrates push-pull output. This configuration doesn't require pull-up resistors, saving space on the board. However, all the interface logic levels must be examined for compatibility.

Enable Function

An external logic signal from processors can assert enable input to turn the output on or off.

The SY20867A offers an active-high enable input (ENABLE). Driving ENABLE high forces OUT high. The 0.4V (maximum) low and 1.4V (minimum) high allows the ENABLE input to be driven from a 1.5V or higher system supply.

Driving ENABLE high for the SY20867A device with VSENSE > VIT+ makes OUT go high after the capacitor-adjustable delay time.

PCB Layout Guide

For the best performance of the SY20867ADTD, the following guidelines must be followed:

- Keep all power traces as short and wide as possible and use at least 1-ounce copper for all power traces.
- Place a ground plane under all circuitry to lower resistance and inductance and improve DC and transient performance.
- Place the VCC decoupling capacitor close to the device.
- Avoid using long traces for the VCC supply node. The VCC capacitor (CVCC) and parasitic inductance from the supply to the capacitor can form an LC tank and create ringing with peak voltages above the maximum VCC voltage.
- Place the input and output capacitors close to the device and connect them to the ground plane to reduce noise coupling.

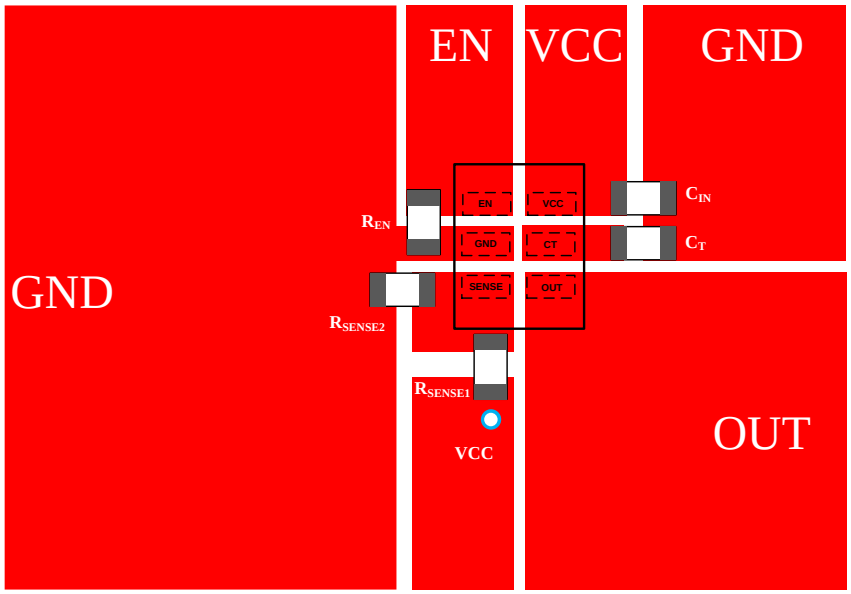
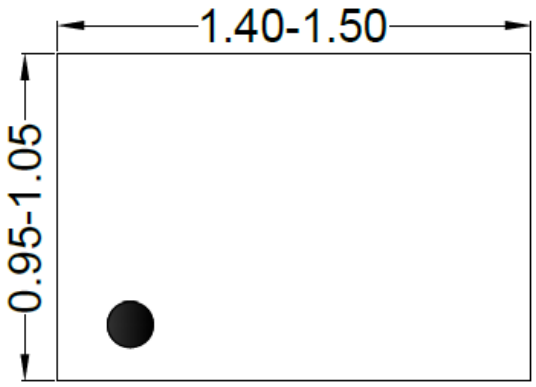
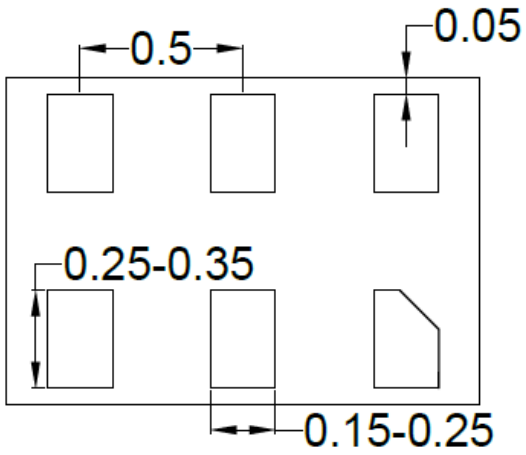


Figure 4. PCB Layout Suggestion

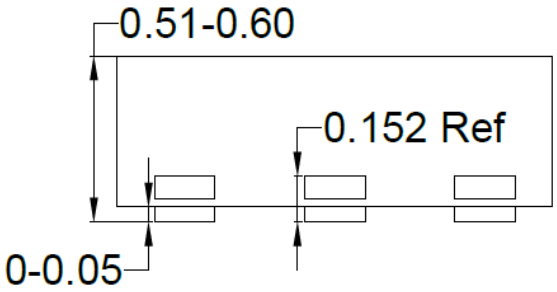
DFN1.45×1-6 Package Outline Drawing



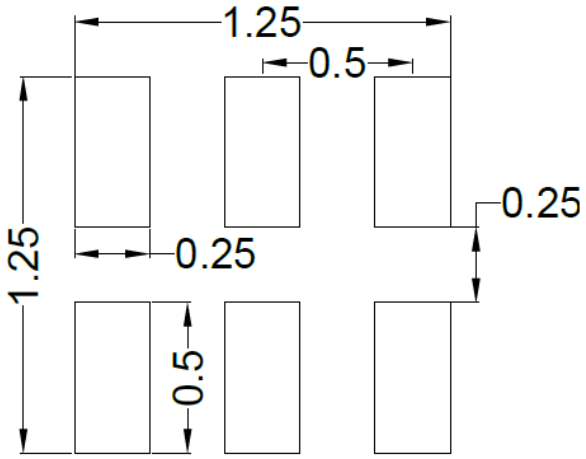
Top View



Bottom View



Side View

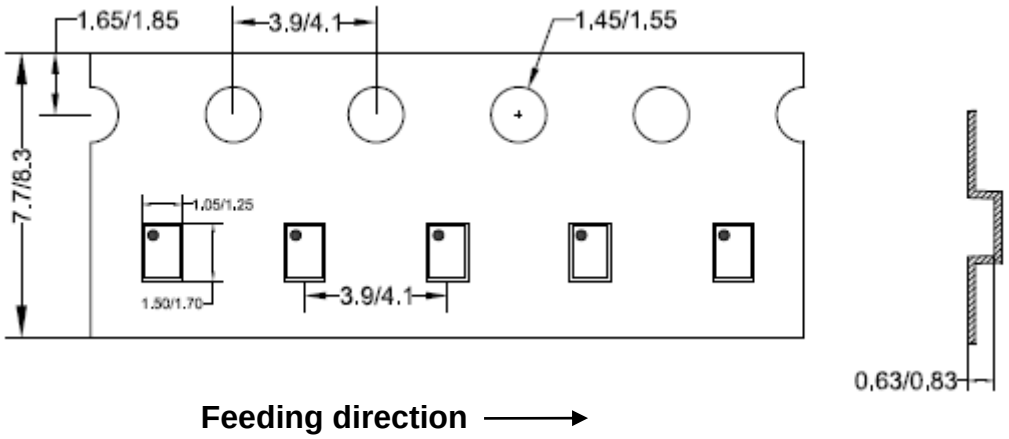


Recommended PCB Layout
(Reference only)

Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

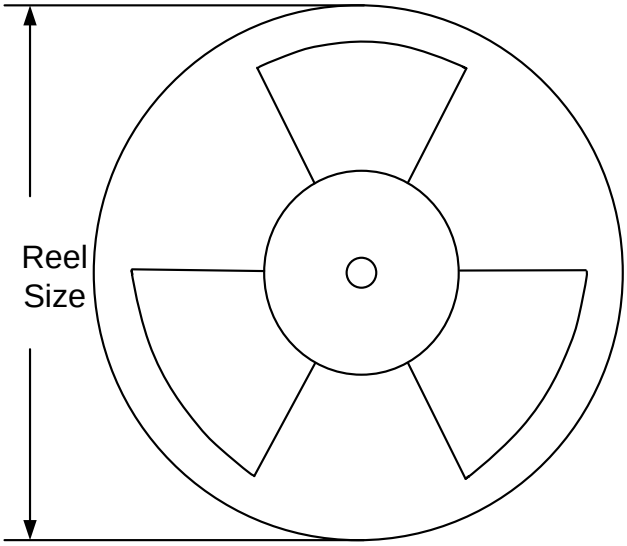
Taping & Reel Specification

Taping Orientation



Feeding direction ⟶

Carrier Tape & Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN1.45×1	8	4	7"	400	160	3000

Revision History

Date	Revision	Change
July 03, 2025	Revision 1.0A	The logic gate in the Block Diagram changed from AND gate to NAND gate (Page 2)
Aug. 25, 2023	Revision 1.0	Language improvements for clarity.
Dec. 03, 2021	Revision 0.9	Initial Release

Revision history is for reference only and may not be comprehensive or complete.

IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.

2. Applications. Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.

3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.

4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of a Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

5. **Terms and conditions of commercial sale**. Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at http://www.silergy.com/stdterms, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.

6. **No offer to sell or license**. Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com