SY8202

High Efficiency, 1.7A, 28V Input Synchronous Step Down Regulator

General Description

The SY8202 develops high efficiency 500kHz synchronous step-down DC/DC converter capable of delivering 1.7A current. The device operates over a wide input voltage range from 4.5V to 28V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The SY8202 adopts the instant PWM architecture to achieve fast transient responses for high step down applications and high efficiency at light loads. In addition, it operates at pseudo-constant frequency of 500 kHz under heavy load conditions to minimize the size of inductor and capacitor.

Features

- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 350mΩ/150mΩ
- 4.5V-28V Input Voltage Range
- 1.7A Output Current Capability
- 500kHz Switching Frequency Minimizes the External Components
- Instant PWM Architecture to Achieve Fast Transient Responses
- Internal Soft-start Limits the Inrush Current
- Cycle-by-cycle Valley Current Limitation
- ±2.0% 0.6V Reference
- RoHS Compliant and Halogen Free
- Compact Package: TSOT23-6

Ordering Information

SY8202 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY8202ADC	TSOT23-6	--

Applications

- Set Top Box
- Portable TV
- Access Point Router
- DSL Modem
- LCD TV

Typical Applications

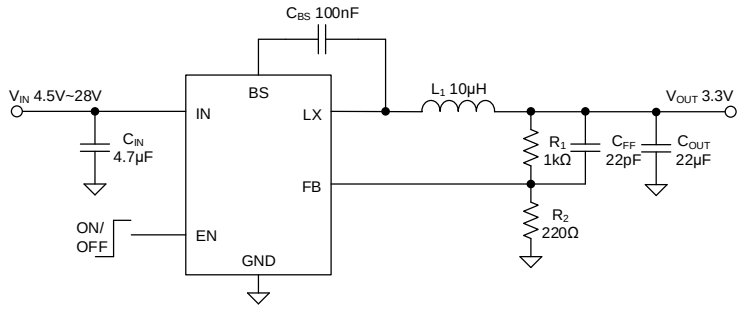


Figure 1. Schematic Diagram

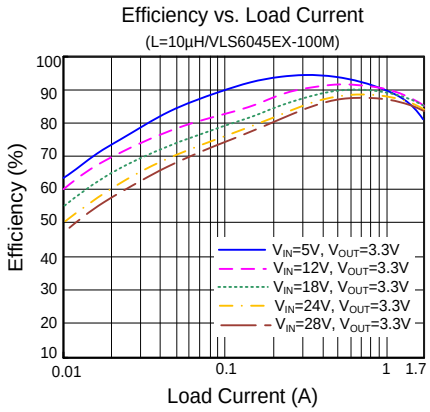
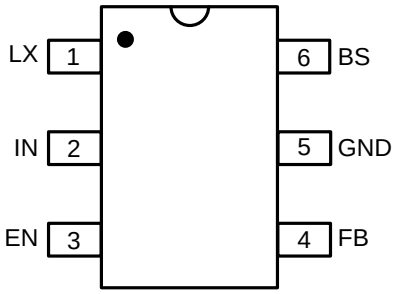


Figure 2. Efficiency vs. Load Current

Pinout (Top View)

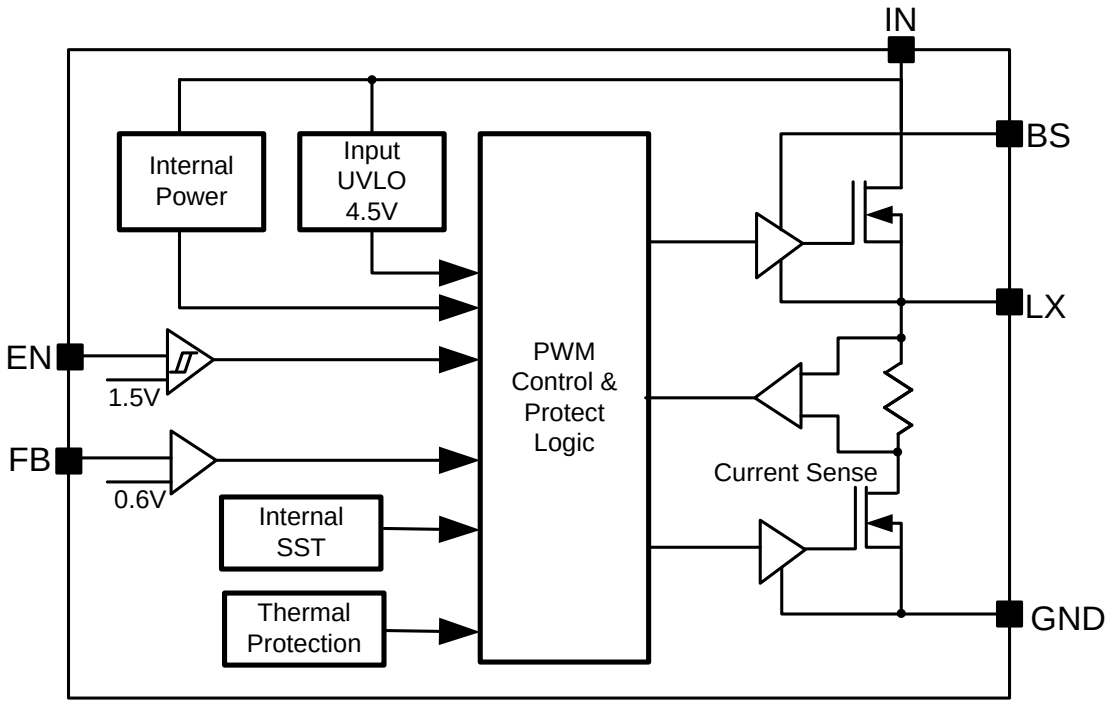


(TSOT23-6)

Top Mark: 2Q*xyz* (device code: 2Q, ***x=year code, y=week code, z= lot number code)***

Pin Name	Pin Number	Pin Description
LX	1	Inductor pin. Connect this pin to the switching node of inductor.
IN	2	Input pin. Decouple this pin to the GND pin with at least a 4.7μF ceramic capacitor.
EN	3	Enable control. Pull high to turn on. Do not leave this pin floating.
FB	4	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.6V\times(1+R_1/R_2)$
GND	5	Ground pin.
BS	6	Boot-strap pin. Supply high side gate driver. Connect a 0.1μF ceramic capacitor between the BS and the LX pin.

Block Diagram



Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- -0.3V to 30V
LX, EN Voltage---------- -0.3V to V_{IN} + 0.3V
FB, BS-LX Voltage---------- -0.3V to 4V
Power Dissipation, P_D @ T_A = 25°C TSOT23-6 ---------- 1.5W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 66°C/W
θ_{JC} ---------- 15°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
Dynamic LX Voltage in 10ns Duration (Note 3) ---------- IN+3V to GND-5V

Recommended Operating Conditions (Note 4)

Supply Input Voltage ---------- 4.5V to 28V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, V_{OUT} = 1.2V, L = 4.7µH, C_{OUT} = 22µF, T_A = 25°C, I_{OUT} = 1A, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.5		28	V
Input UVLO Threshold	V_{UVLO}				4.5	V
Quiescent Current	I_Q	I_{OUT}=0, V_{FB}=V_{REF}×105%		400		µA
Shutdown Current	I_{SHDN}	EN=0		5	10	µA
Feedback Reference Voltage	V_{REF}		588	600	612	mV
FB Input Current	I_{FB}	V_{FB}=3.3V	-50		50	nA
Top FET RON	$R_{DS(ON)1}$			350		mΩ
Bottom FET RON	$R_{DS(ON)2}$			150		mΩ
EN Rising Threshold	$V_{EN,R}$		1.5			V
EN Falling Threshold	$V_{EN,F}$				0.4	V
EN Input Current	I_{EN}	V_{EN}=3.3V			1	µA
Min ON Time	$t_{ON,MIN}$			50		ns
Min OFF Time	$t_{OFF,MIN}$			100		ns
Switching Frequency	f_{SW}	V_{OUT}=5V, CCM		500		kHz
Bottom FET Valley Current Limit	$I_{LIM,BOT}$		1.7			A
Thermal Shutdown Temperature	T_{SD}			150		˚C
Thermal Shutdown Hysteresis	T_{HYS}			15		˚C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a 2OZ two-layer Silergy evaluation board. Paddle of TSOT23-6 package is the case position for SY8202 θ_{JC} measurement.

Note 3: This dynamic LX voltage spec is tested under 20MHz oscilloscope bandwidth.

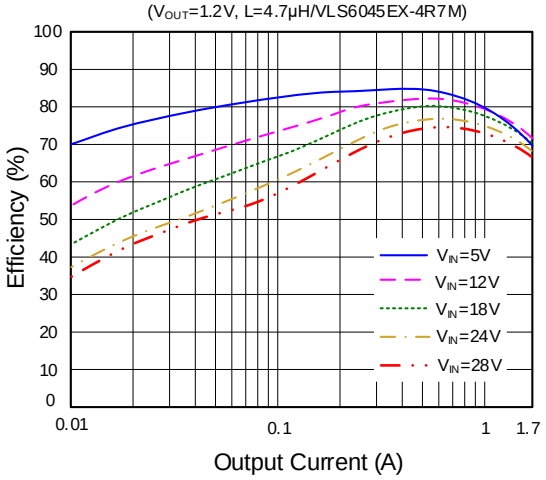
Note 4: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

(T_A = 25°C, V_{IN} = 24V, V_{OUT} =3.3V, L = 10µH, C_{OUT} = 22µF, I_{OUT} = 1.7A, unless otherwise specified)

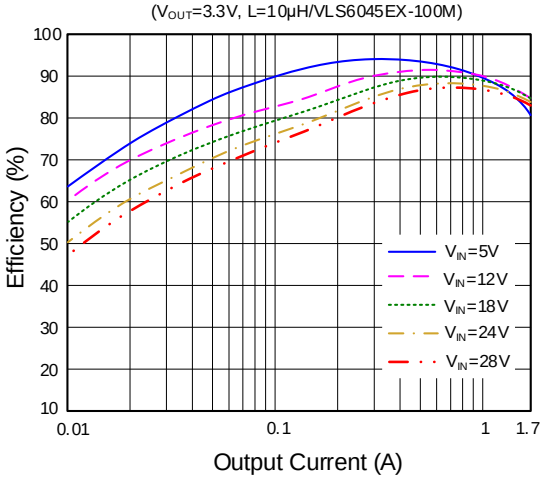
Efficiency vs. Output Current

(V_{OUT}=1.2V, L=4.7µH/VLS6045EX-4R7M)



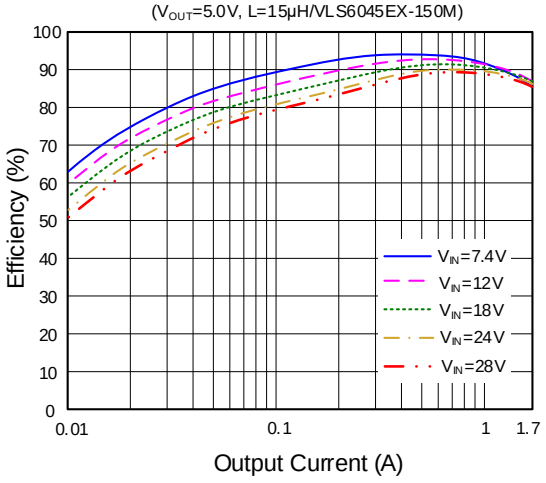
Efficiency vs. Output Current

(V_{OUT}=3.3V, L=10µH/VLS6045EX-100M)



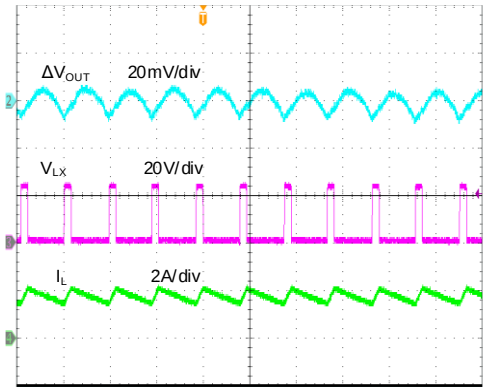
Efficiency vs. Output Current

(V_{OUT}=5.0V, L=15µH/VLS6045EX-150M)



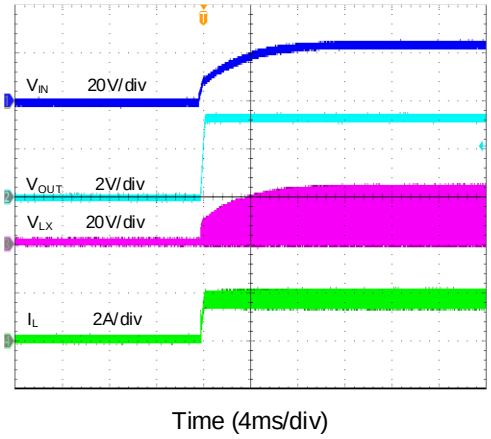
Output Ripple

(V_{IN}=24V, V_{OUT}=3.3V, I_{OUT}=1.7A)



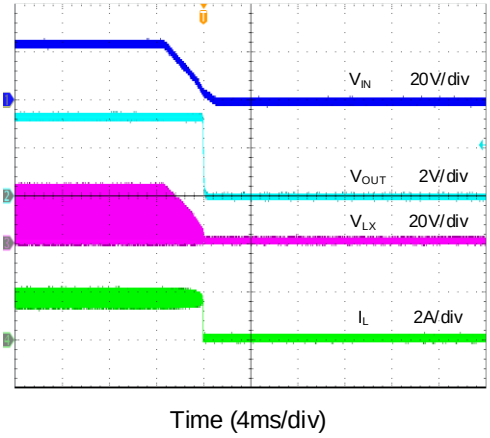
Startup from V_{IN}

(V_{IN}=24V, V_{OUT}=3.3V, I_{OUT}=1.7A)



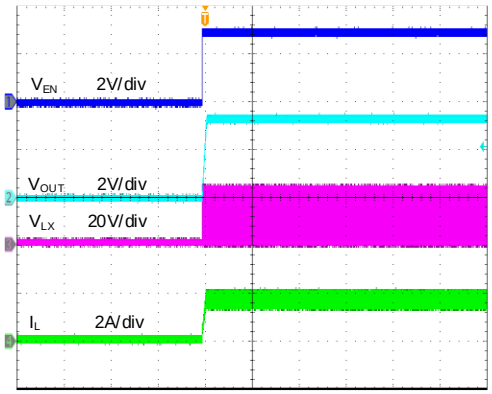
Shutdown from V_{IN}

(V_{IN}=24V, V_{OUT}=3.3V, I_{OUT}=1.7A)



Startup from EN

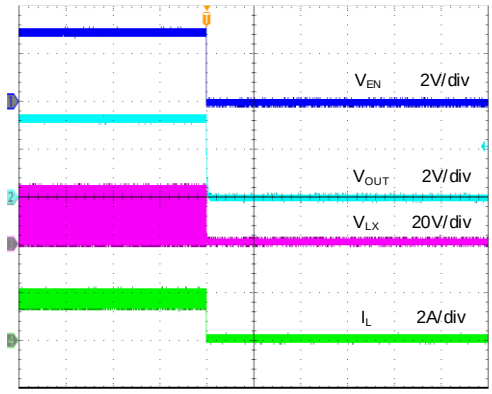
(V_{IN}=24V, V_{OUT}=3.3V, I_{OUT}=1.7A)



Time (4ms/div)

Shutdown from EN

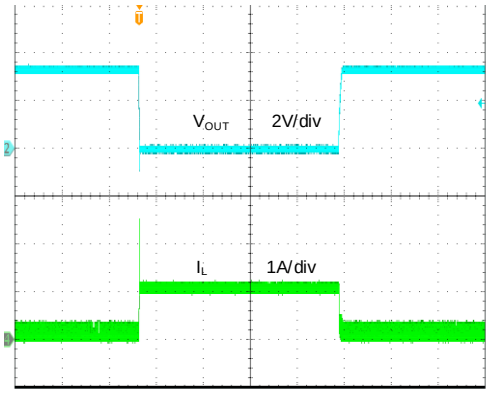
(V_{IN}=24V, V_{OUT}=3.3V, I_{OUT}=1.7A)



Time (4ms/div)

Short Circuit Protection

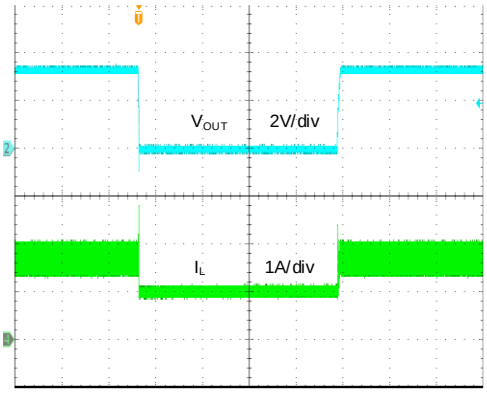
(V_{IN}=24V, V_{OUT}=3.3V, I_{OUT}=0A~short)



Time (4ms/div)

Short Circuit Protection

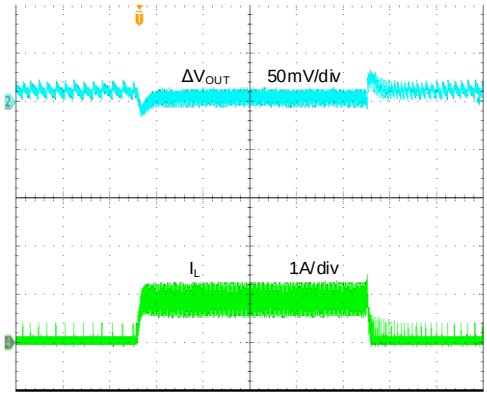
(V_{IN}=24V, V_{OUT}=3.3V, I_{OUT}=1.7A~short)



Time (4ms/div)

Load Transient

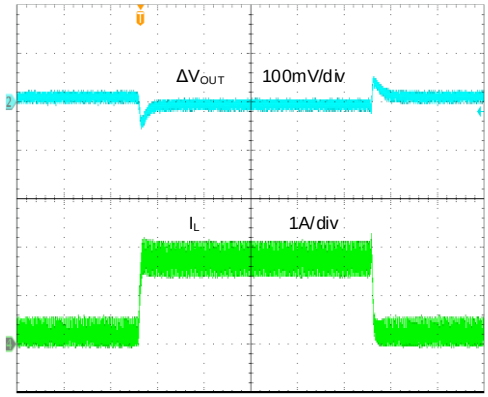
(V_{IN}=24V, V_{OUT}=3.3V, I_O=0A~0.85A)



Time (100μs/div)

Load Transient

(V_{IN}=24V, V_{OUT}=3.3V, I_O=0.17A~1.7A)



Time (100μs/div)

Operation

The SY8202 is a high efficiency 500kHz synchronous step-down DC/DC regulator capable of delivering up to 1.7A load current. It can operate over a wide input voltage range from 4.5V to 28V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss. The SY8202 adopts the instant PWM architecture to achieve fast transient responses for high step-down applications and high efficiency at light loads.

The SY8202 provides protection functions such as cycle by cycle current limiting and thermal shutdown protection. The SY8202 will sense the output voltage conditions for the fault protection.

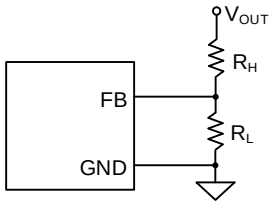
Applications Information

Because of the high integration in the SY8202, the application circuit based on this regulator is rather simple. Only the input capacitor C_{IN}, the output capacitor C_{OUT}, the output inductor L and the feedback resistors (R_H and R_L) need to be selected for the targeted applications specifications.

Feedback Resistor Dividers R_H and R_L:

Choose R_H and R_L to program the proper output voltage. For example, if V_{OUT} is 3.3V, R_H=1kΩ is chosen, then using following equation, R_L can be calculated to be 222Ω:

$$R_L = \frac{0.6V}{V_{OUT} - 0.6V} R_H$$



Input Capacitor C_{IN}:

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D(1-D)}$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins. In this case, a 4.7μF low ESR ceramic capacitor is recommended.

Output Capacitor C_{OUT}:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use an X5R or better grade ceramic capacitor greater than 22μF capacitance.

Output Inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{f_{SW} \times I_{OUT,MAX} \times 40\%}$$

where fsw is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY8202 is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1\text{-}V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mΩ to achieve a good overall efficiency.

Minimum Duty Cycle and Maximum Duty Cycle

In the COT architecture, there is no limitation for small duty cycles, since even at very low duty cycles, the switching frequency can be reduced as needed once the on-time is close to the minimum on time, to always ensure a proper operation.

The device can support at least 70% maximum duty cycle operation under -40℃ ~ 85℃ condition.

In PFM light load operation, when the duty cycle is up to maximum duty cycle limitation, the device will enter CCM operation even though the load current is null.

Soft-start

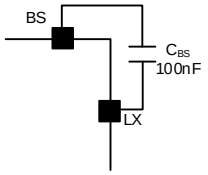
The SY8202 has a built-in soft-start to control the rise rate of the output voltage and limit the input current surge during IC start-up. The typical soft-start time is 300μs.

Enable Operation

Pulling the EN pin low (<0.4V) will shut down the device. During shutdown mode, the SY8202 shutdown current drops to lower than 5μA. Driving the EN pin high (>1.5V) will turn on the IC again.

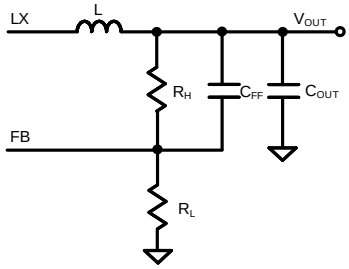
External Bootstrap Capacitor

This capacitor provides the gate driver voltage for internal high side MOSEFET. A 100nF low ESR ceramic capacitor connected between the BS pin and the LX pin is recommended.



Load Transient Considerations:

The SY8202 integrates the compensation components to achieve good stability and fast transient responses. Adding a small value ceramic cap in parallel with R_H may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements.



Layout Design:

The layout design of SY8202 regulator is relatively simple. For the best efficiency and minimum noise problem, we should place the following components close to the IC: C_{IN}, L, R_H, R_L and C_{FF}.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) C_{IN} must be close to Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

4) The components R_H and R_L, and the trace connecting to the FB pin must not be adjacent to the LX net on the PCB layout to avoid the noise problem.

5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1MΩ resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

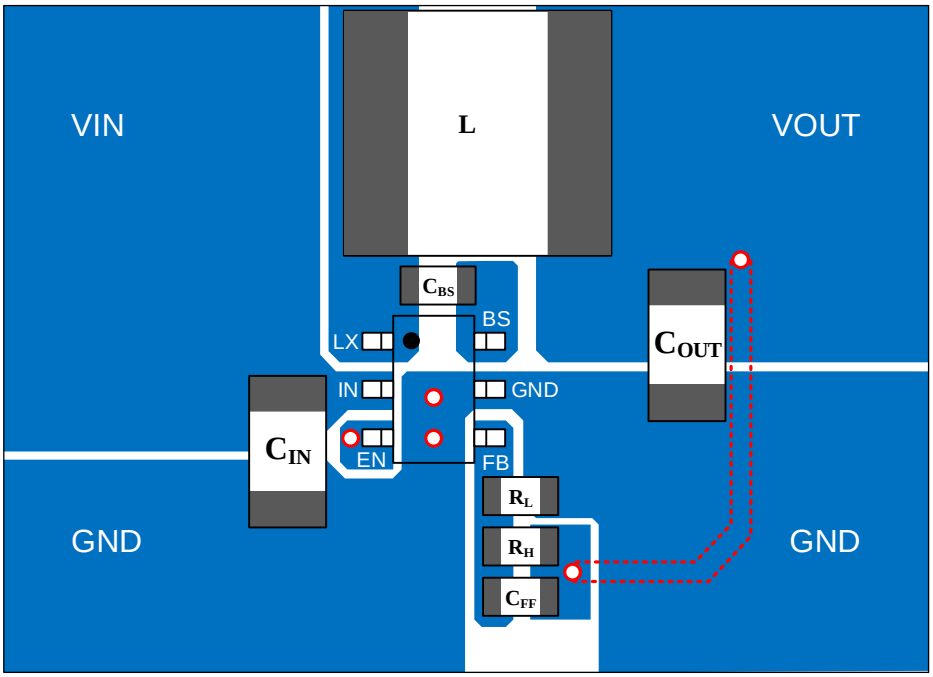
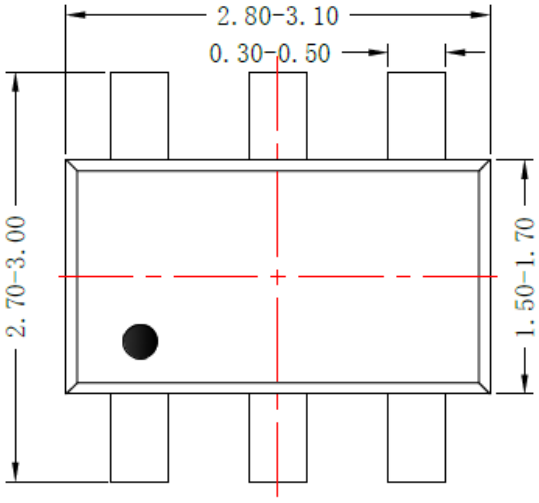
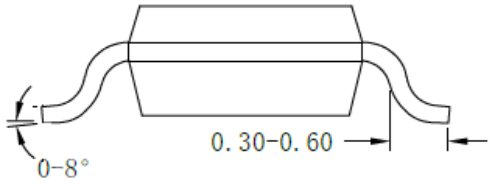


Figure3. PCB Layout Suggestion

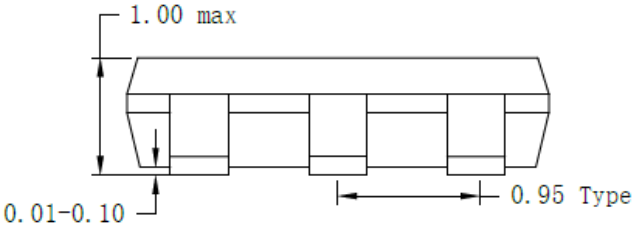
TSOT23-6 Package Outline & PCB Layout



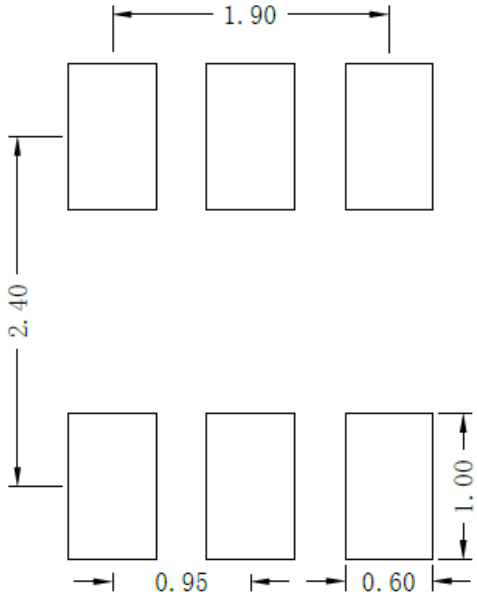
Top view



Side view



Front view



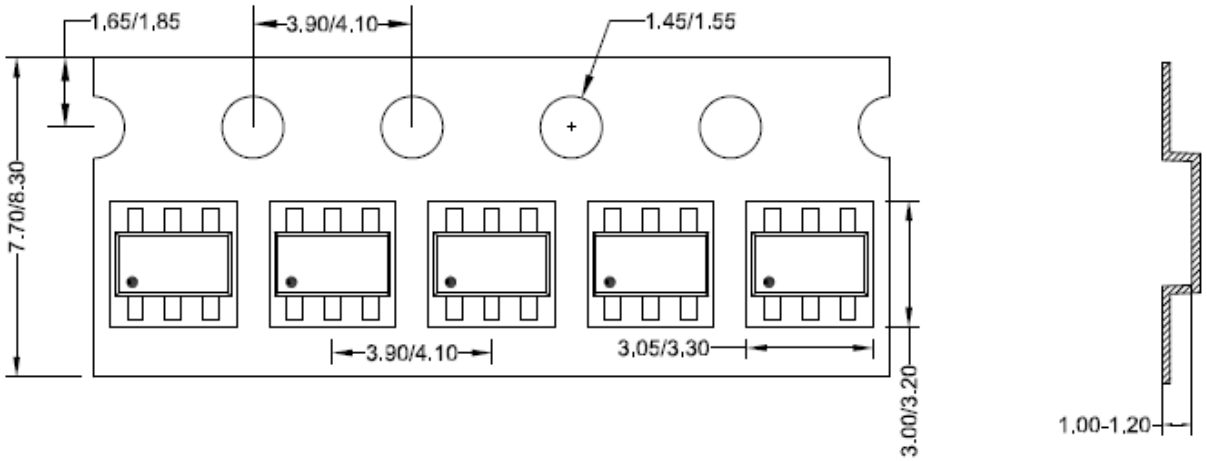
Recommended Pad Layout

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

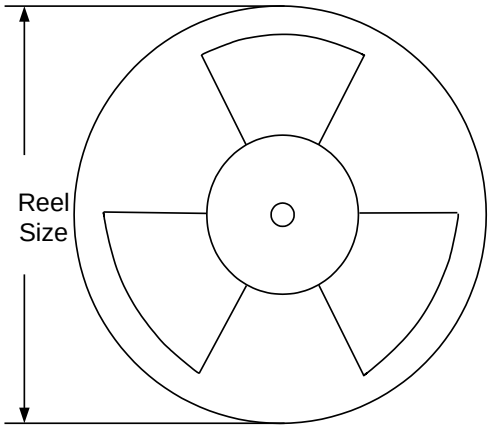
1. Taping orientation

TSOT23-6



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
TSOT23-6	8	4	7"	400	160	3000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Nov.11, 2022	Revision 0.9A	Updated the lead width of package (Page 9)
June.22, 2021	Revision 0.9	Initial Release

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