SY26004

High-Efficiency, 6V, 4A
2.4MHz Synchronous Step-Down Regulator

General Description

The SY26004 high efficiency 2.4MHz synchronous Buck converter operates over a wide input voltage range from 2.5V to 6V and is capable of delivering up to 4A output current. It integrates a top FET and a bottom FET with very low $R_{DS(ON)}$ to minimize conduction loss.

The SY26004 adopts a constant on-time and ripple-based control strategy to achieve fast transient responses. The input and output capacitors, the inductor, and the resistor-divider components must be selected for the targeted application specifications.

The SY26004 is available in a space-saving, low-profile DFN2×2-7 package.

Features

- Low $R_{DS(ON)}$ for Internal Switches: 25mΩ Top, 17mΩ Bottom
- 2.5~6V Input Voltage Range
- Up to 4A Output Current
- Constant On-time and Ripple-based Control
- Low 23μA Quiescent Current
- High 2.4MHz Switching Frequency Minimizes Required External Components
- Internal Soft-Start Limits Inrush Current
- 100% Dropout Operation
- Power-Good Indicator
- Hiccup Mode for Short-Circuit Protection
- Output Auto-Discharge Function
- RoHS-Compliant and Halogen-Free
- Compact DFN2×2-7 Package

Applications

- Set-Top Box
- USB Dongle
- Media Player
- Smartphone

Typical Application

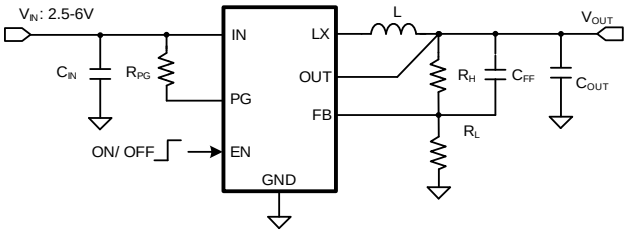


Figure 1. Schematic Diagram

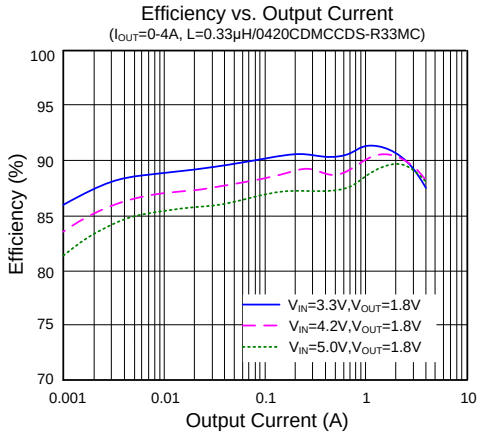


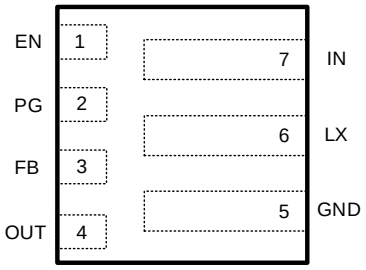
Figure 2. Efficiency vs. Output Current

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY26004SYD	DFN2×2-7 RoHS-Compliant, Halogen-Free	**4Nxyz**

x=year code, y=week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	EN	Enable control. Pull high to turn on the device and pull low to turn off the device. Do not leave this pin floating.
2	PG	Power-good indicator. Open-drain output when the output voltage is above 90% of the regulation point.
3	FB	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.6\times(1+R_H/R_L)$.
4	OUT	Output pin for stable operation. Connect to the output of the Buck regulator.
5	GND	Power Ground pin.
6	LX	Inductor pin. Connect this pin to the switching node of the inductor.
7	IN	Input pin. Decouple this pin to the GND pin with at least a 22µF ceramic capacitor.

Block Diagram

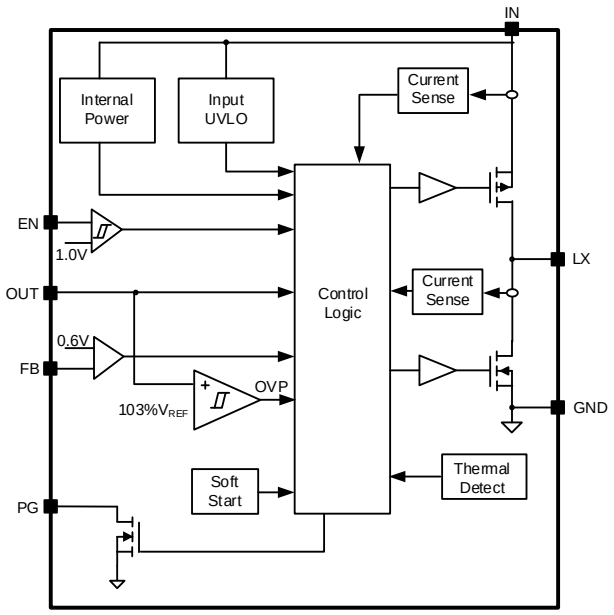


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN	-0.3	7	V
EN, FB, PG	-0.3	IN + 0.3	
LX	-0.3	6.5	
LX, 40ns duration	-3	7.5	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering,10s)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	35	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	10	
P_D Power Dissipation T_A = 25°C	2.86	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	2.5	6	V
Output Voltage	0.6	6	
Output Current		4	A
Junction Temperature	-40	125	°C

Electrical Characteristics

(V_{IN} = 5V, V_{OUT} = 1.8V, L =0.33μH, C_{OUT} = 22μF, T_J = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Voltage	V_{IN}		2.5		6.0	V
	UVLO Rising Threshold	$V_{IN,UVLO}$		2.05	2.2	2.3	V
	UVLO Hysteresis	$V_{IN,HYS}$			200		mV
	Quiescent Current	I_Q	V_{FB} = 105% × V_{REF}		23	35	μA
	Shutdown Current	I_{SHDN}	V_{EN} = 0V		0.1	1	μA
Output	Reference Voltage	V_{REF}	I_{OUT} = 1A, CCM	0.591	0.6	0.609	V
	Soft-Start Time	t_{SS}	From EN high to 95% V_{OUT}		0.8		ms
	Discharge on Resistance	R_{DIS}			10		Ω
MOSFET	Top FET $R_{DS(ON)}$	$R_{DS(ON)1}$			25		mΩ
	Bottom FET $R_{DS(ON)}$	$R_{DS(ON)2}$			17		mΩ
	Top FET Current Limit	$I_{LMT,TOP}$		5.0	6.0	7.0	A
	Bottom FET Current Limit	$I_{LIM,BOT}$		3.6			A
Enable (EN)	Input Voltage High	$V_{EN,H}$		1.0			V
	Input Voltage Low	$V_{EN,L}$				0.4	V
	Pull Down Resistance	R_{EN}			400		kΩ
Power-Good	Thresholds	$V_{PG,F}$	V_{FB} falling, PG from high to low	86	88	91	%
		$V_{PG,R}$	V_{FB} rising, PG from low to high	93	95	98	%
COT	Switching Frequency	f_{SW}	I_{OUT} = 1A, CCM		2.4		MHz
	Minimum On Time	$t_{ON,MIN}$			50		ns
	Maximum Duty Cycle	D_{MAX}		100			%
OTP	Temperature	T_{OTP}			150		°C
	Temperature Hysteresis	T_{HYS}			20		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} of SY26004SYD is measured in the natural convection at T_A = 25°C on a 2oz two-layer Silergy evaluation board. Pin 5 is the case position for SY26004SYD θ_{JC} measurement.

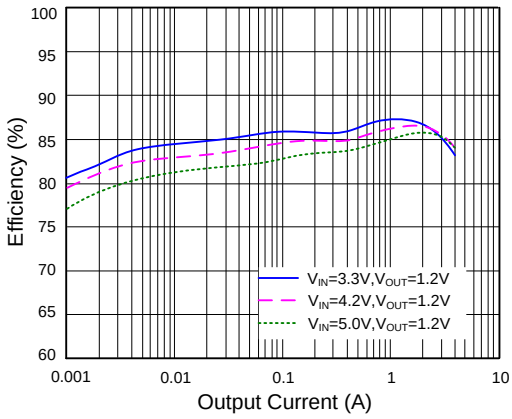
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

(SY26004SYD, T_A = 25°C, V_{IN} = 5V, V_{OUT} = 1.8V, L = 0.33μH, C_{OUT} = 22μF×2, unless otherwise noted)

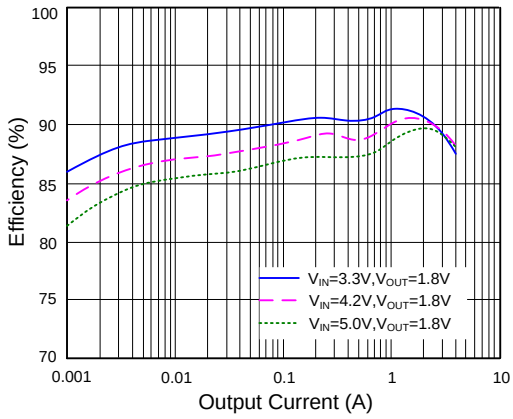
Efficiency vs. Output Current

(I_{OUT}=0-4A, L=0.22μH/0420CDMCCDS-R22MC)



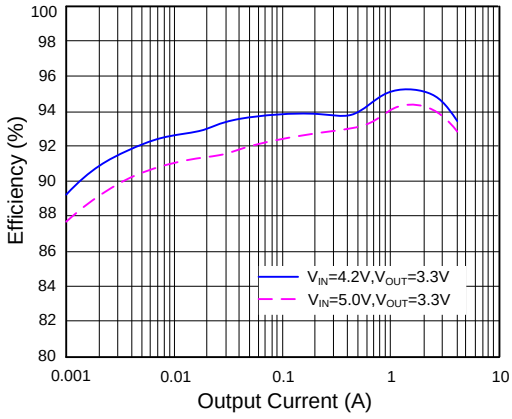
Efficiency vs. Output Current

(I_{OUT}=0-4A, L=0.33μH/0420CDMCCDS-R33MC)



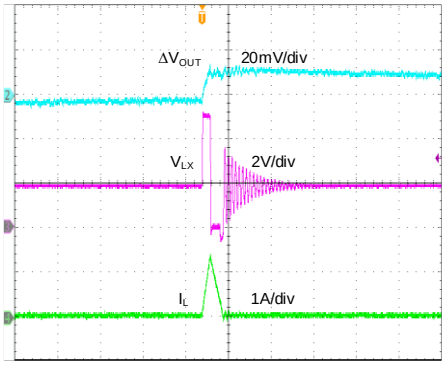
Efficiency vs. Output Current

(I_{OUT}=0-4A, L=0.47μH/0420CDMCCDS-R47MC)



Output Ripple

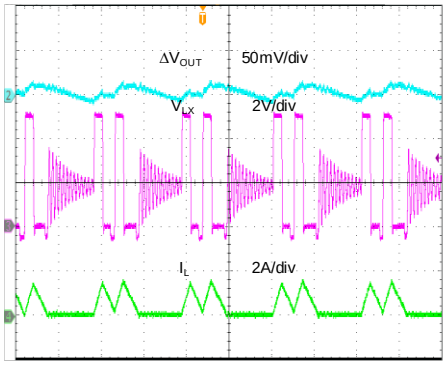
(V_{IN}=5.0V, V_{OUT}=1.8V, I_{OUT}=0A)



Time (1μs/div)

Output Ripple

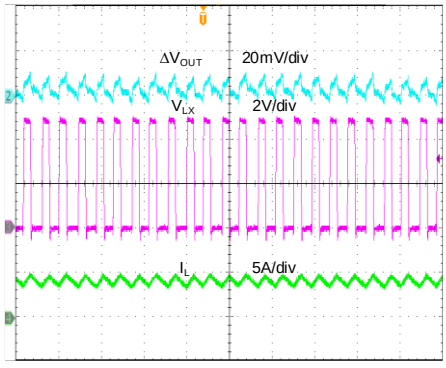
(V_{IN}=5.0V, V_{OUT}=1.8V, I_{OUT}=0.4A)



Time (1μs/div)

Output Ripple

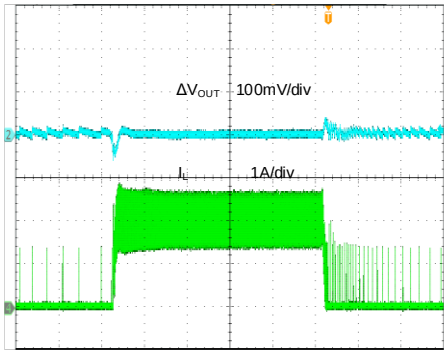
(V_{IN}=5.0V, V_{OUT}=1.8V, I_{OUT}=4A)



Time (1μs/div)

Load Transient

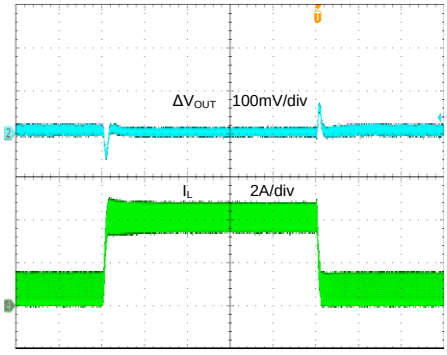
(V_{IN}=5.0V, V_{OUT}=1.8V, I_{LOAD}=0A~2A)



Time (100μs/div)

Load Transient

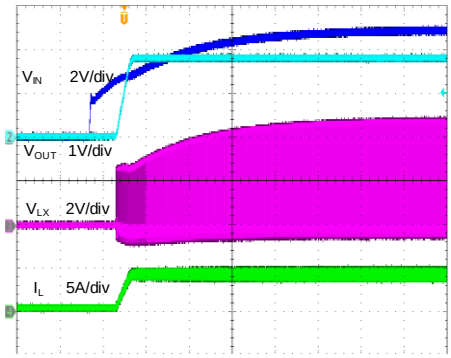
(V_{IN}=5.0V, V_{OUT}=1.8V, I_{LOAD}=0.4A~4A)



Time (100μs/div)

Startup from V_{IN}

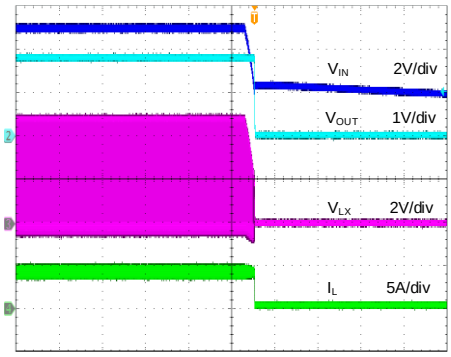
(V_{IN}=5.0V, V_{OUT}=1.8V, R_{LOAD}=0.45Ω)



Time (2ms/div)

Shutdown from V_{IN}

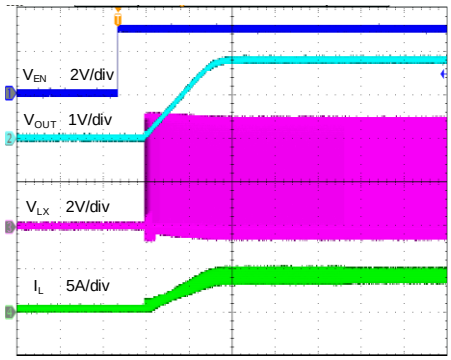
(V_{IN}=5.0V, V_{OUT}=1.8V, R_{LOAD}=0.45Ω)



Time (2ms/div)

Startup from Enable

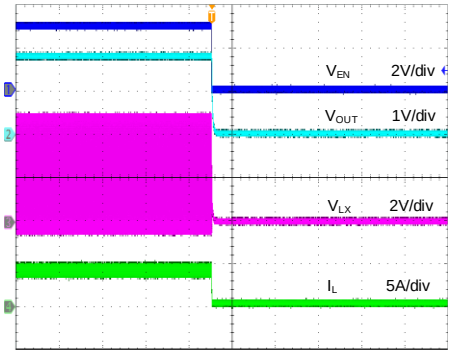
(V_{IN}=5.0V, V_{OUT}=1.8V, R_{LOAD}=0.45Ω)



Time (400μs/div)

Shutdown from Enable

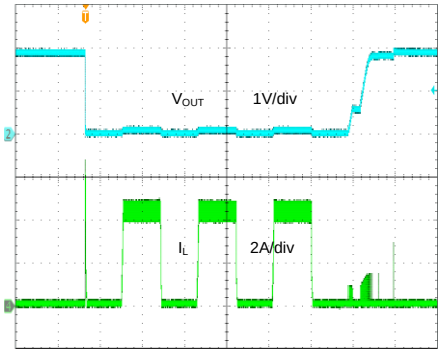
(V_{IN}=5.0V, V_{OUT}=1.8V, R_{LOAD}=0.45Ω)



Time (400μs/div)

Short Circuit Protection

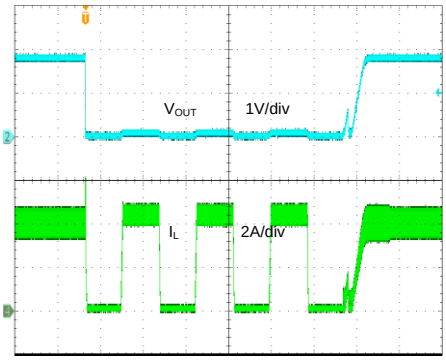
(V_{IN}=5.0V, V_{OUT}=1.8V, I_{LOAD}=0A~Short)



Time (2ms/div)

Short Circuit Protection

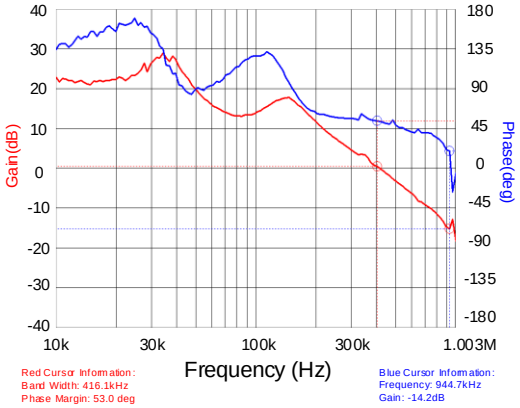
(V_{IN}=5.0V, V_{OUT}=1.8V, I_{LOAD}=4.0A~Short)



Time (2ms/div)

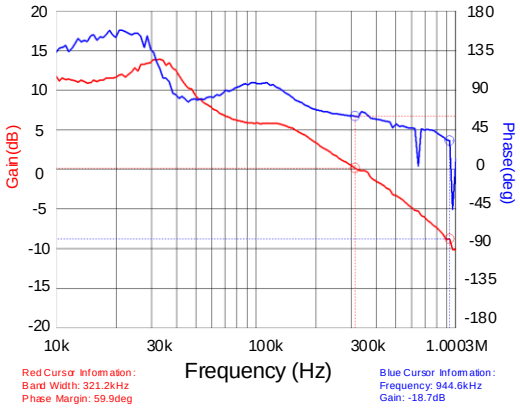
Bode Plot

(V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=4A)



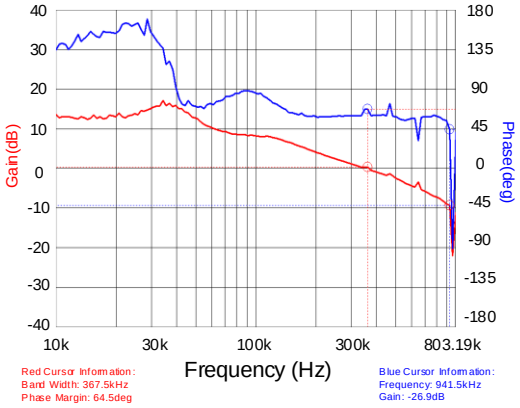
Bode Plot

(V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=4A)



Bode Plot

(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=4A)



Detailed Description

The SY26004 is a high-efficiency 2.4MHz synchronous Buck converter capable of delivering up to 4A output current. It can operate over a wide input voltage range from 2.5V to 6V, and integrates a top FET and bottom FET with very low $R_{DS(ON)}$ to minimize conduction loss.

Constant-On-Time and Ripple-Based Control

The SY26004 adopts constant on-time and ripple-based control strategy. The output voltage is fed back directly, and the inductor current ripple information obtained is constructed as a voltage ramp, when this ramp reaches internal V_{COMP}, the bottom FET will turn off and the top FET will turn on for a fixed period of time (constant t_{ON}). The t_{ON} is internally calculated according to the input voltage, output voltage and desired switching frequency (f_{SW}).

$$t_{ON} = \frac{V_{OUT}}{f_{SW} \times V_{IN}}$$

The top FET turns off after a period of t_{ON}. This instant-PWM architecture achieves fast transient response for high step-down applications and high efficiency at light loads.

Enable Control

The EN input is a high-voltage-capable input with logic-compatible threshold. When the EN is driven higher than 1V, normal device operation will be enabled. When driven to lower than 0.4V, the device will shut down, reducing input current to less than 1μA.

Output Power-Good Indicator

The power-good indicator is an open drain output controlled by a window comparator connected to the feedback signal. If V_{FB} is higher than $V_{PG, F}$, PG will be high-impedance. Otherwise, it will be pulled low. PG should be connected to V_{IN} or another voltage source through a resistor (e.g. 10kΩ~100kΩ).

Fault Protection Modes

Output Current Limit

With load current increasing, as soon as the top FET current exceeds the peak current-limit threshold, the top FET will turn off. If the load current continues to increase, the output voltage will drop.

Output Under Voltage Protection (UVP)

If V_{OUT} is less than approximately 50% of the target output voltage for at least a UVP delay time (when the output short-circuits or the load current is much higher than the maximum current capacity), the output undervoltage protection (UVP) will be triggered, and the device will enter the hiccup protection mode.

When the output fault conditions are removed during hiccup on-time, the internal soft-start circuit voltage V_{SS} will be pulled low temporarily to avoid output overshoot if V_{FB} exceeds the UVP threshold, and then the V_{SS} will rise smoothly to ramp the output to the desired voltage during a new soft-start cycle.

Output Over Voltage Protection (OVP)

If the output voltage rises above the feedback regulation level, the top FET will naturally remain off, and the bottom FET will remain on until the inductor current reaches zero and the switching actions are suppressed. The switching actions will be resumed once the ramp signals are lower than the reference voltage.

Over Temperature Protection (OTP)

The SY26004 includes overtemperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds 150°C. Once the junction temperature cools by approximately 15°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature will not exceed the OTP threshold.

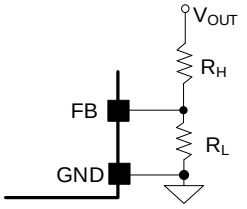
Application Information

The following paragraphs describe the selection process for the input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L, and feedback resistors R_H and R_L.

Feedback Resistor-Divider R_H and R_L

Choose R_H and R_L to program the proper output voltage. A value between 1kΩ and 1MΩ is recommended for both resistors. If R_L is chosen as 120kΩ, then R_H can be calculated as follows:

$$R_L = \frac{0.6\text{V}}{V_{OUT} - 0.6\text{V}} R_H$$



Input Capacitor C_{IN}

For the best performance, select a typical X5R or a better grade ceramic capacitor with a 6.3V rating, and greater than 10μF capacitance. The capacitor should be placed as close as possible to the device, while also minimizing the loop area formed by C_{IN} and the IN/GND pins. When selecting an input capacitor, ensure that its voltage rating is at least 20% greater than the maximum voltage of the

input supply. X5R or X7R dielectric types are the most often selected due to their small size, low cost, surge

current capability, and high RMS current rating over a wide temperature and voltage range.

In situations where the input rail is supplied through long wires, it is recommended to add some bulk capacitance like electrolytic, tantalum or polymer type capacitors to reduce the overshoot and ringing caused by the added parasitic inductance.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, use an input capacitor with an RMS current rating greater than 50% of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.
Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1-D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. A single 10µF X5R capacitor is sufficient in most applications.

Output Inductor L
Consider the following when choosing this inductor:

1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{f_{sw} \times I_{OUT,MAX} \times 0.4}$$

where f_{SW} is the switching frequency and I_{OUT},MAX is the maximum load current.

The SY26004 has high tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

2) The inductor's saturation current rating must be greater than the peak inductor current under full load:

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Use an inductor with DCR less than 50mΩ to achieve good overall efficiency.

Output Capacitor C_{OUT}
Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting the component. For the best performance, use an X5R or a better grade ceramic capacitor with a 6.3V rating, and capacitance greater than 10µF.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed:

The output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple).
When calculating total ripple, consider both.

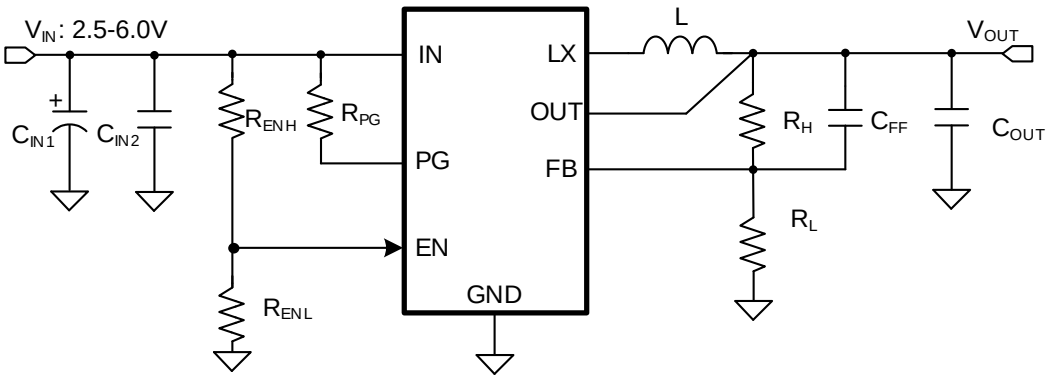
$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

The capacitive ripple might be higher because the effective capacitance for ceramic capacitors decreases with the voltage across the terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

Load-Transient Considerations
The SY26004 integrates compensation components to achieve good stability and fast transient responses. In some applications, adding a ceramic capacitor (feedforward capacitor C_{FF}) in parallel with R_H may further speed up the load-transient responses. It is recommended for applications with large load transient step requirements.

Application Schematic (V_{OUT} = 1.8V)



BOM List

Reference Designator	Description	Part Number	Manufacturer
L	0.33µH	0420CDMCCDS-R33MC	Sumida
C_{IN1}	100µF/25V(electrolytic capacitor)		
C_{IN2}	22µF/6.3V, 0603, X5R	C2012X5R0J226M	TDK
C_{OUT}	22µF/6.3V, 0603, X5R	C2012X5R0J226M	TDK
C_{FF}	NC		
R_H	100kΩ, 1%, 0603		
R_L	49.9kΩ, 1%, 0603		
R_{PG}	100kΩ, 1%, 0603		
R_{ENH}	10kΩ, 1%, 0603		
R_{ENL}	1MΩ, 1%, 0603		

Recommended Component Values for Typical Applications

V_{OUT}(V)	R_H(kΩ)	R_L(kΩ)	C_{FF}(pF)	L/Part Number	C_{OUT}
1.2	100	100	22	0.22µH/0420CDMCCDS-R22MC	22µF/6.3V, 0603, X5R
1.8	100	49.9	22	0.33µH/0420CDMCCDS-R33MC	22µF/6.3V, 0603, X5R
3.3	100	22.1	22	0.47µH/0420CDMCCDS-R47MC	22µF/6.3V, 0603, X5R

Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation:

Input Capacitors: Place the input capacitors as close as possible to the IN and GND pins, minimizing the loop formed by these connections. The input capacitor should be connected to the IN and GND by wide copper plane.

Output Capacitors: Connect the C_{OUT} negative terminal to the GND pin using wide copper traces instead of vias, in order to achieve better accuracy and stability of output voltage.

Feedback Network: Place the feedback components (R_H, R_L, and C_{FF}) as close to the FB pin as possible. Avoid routing the feedback line near LX, or other high-frequency signals as it is noise-sensitive. Use a Kelvin connection to connect with C_{OUT} rather than the inductor output terminal.

LX Connection: Keep the LX area small to prevent excessive EMI, while providing a wide copper trace to minimize parasitic resistance and inductance.

Control Signals: It is not recommended to connect control signals directly to V_{IN}. A resistor in a range of 1kΩ to 1MΩ should be used if the lines are pulled high to V_{IN}.

GND Vias: Place an adequate number of vias on the GND layer around the device for better thermal performance.

PCB Board: To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. A ground plane is highly recommended if board space allows. Connect the ground pad to a large copper area to enhance thermal performance.

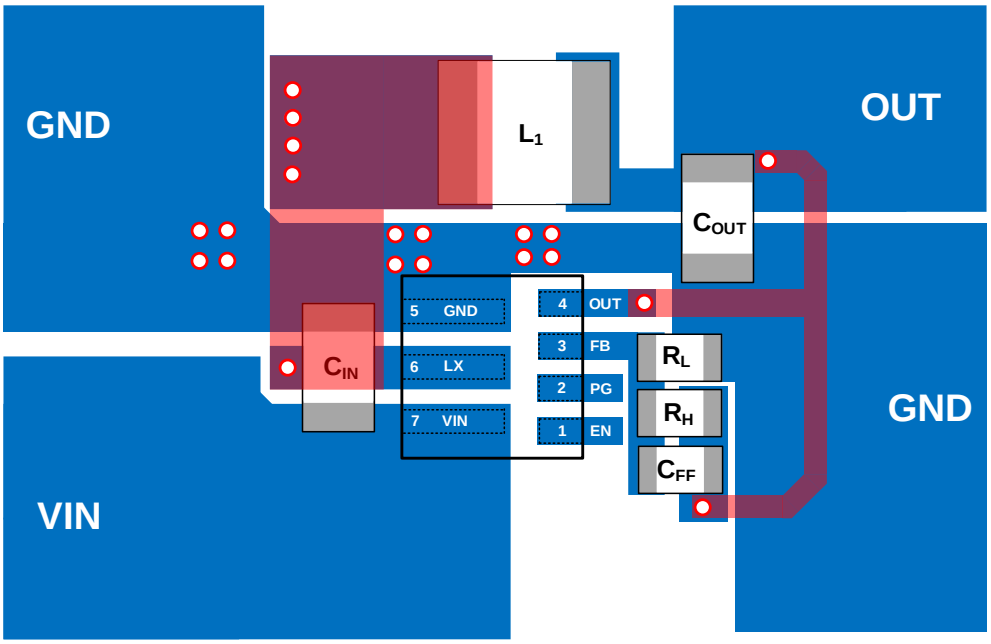
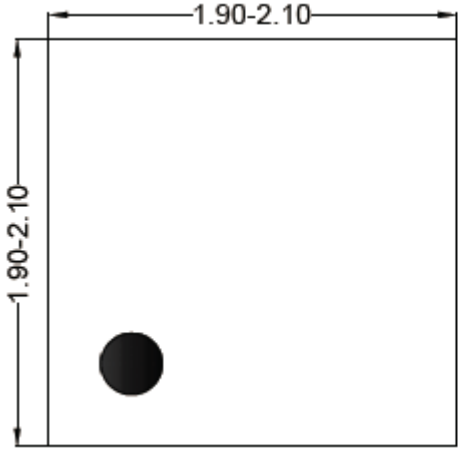
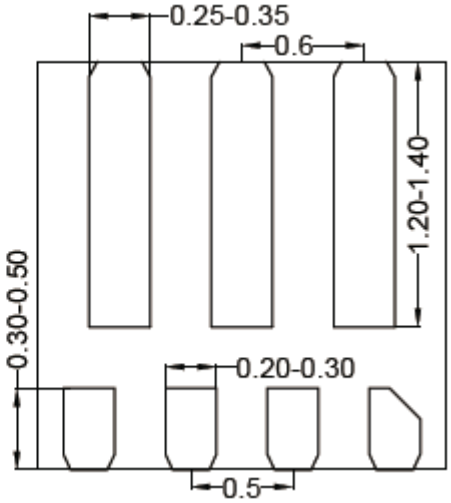


Figure 4. Suggested PCB Layout

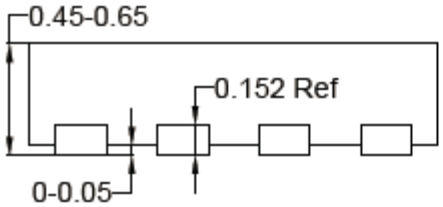
DFN2×2-7 Package Outline Drawing



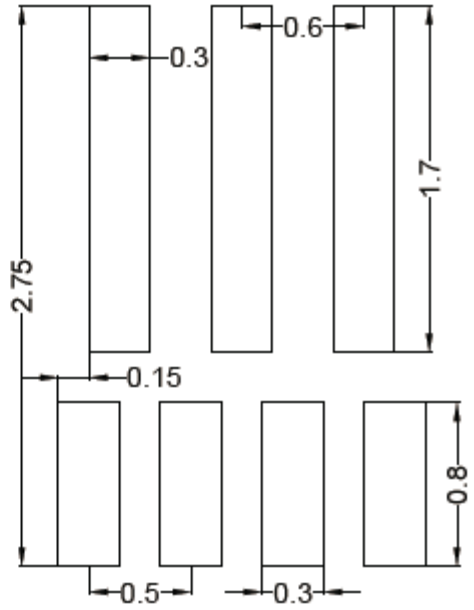
Top View



Bottom View



Side View



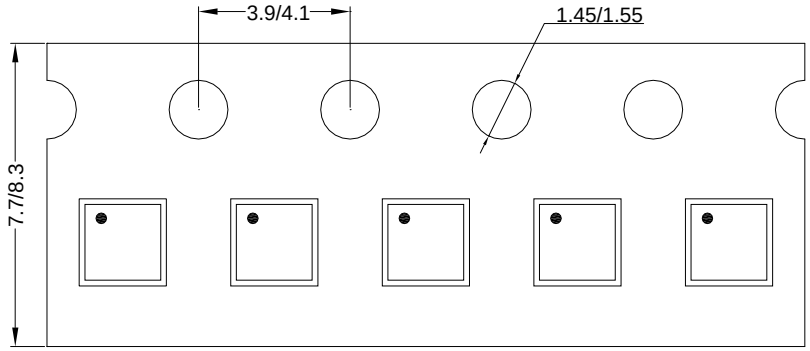
Recommended PCB layout
(Reference only)

Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

Taping and Reel Specification

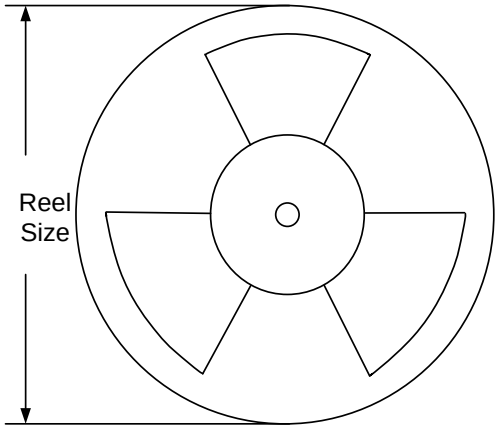
Taping Orientation

DFN2×2



Feeding Direction ⟶

Carrier Tape and Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel (pcs)
DFN2×2	8	4	7"	400	160	3000

Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, it is not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
Jan. 17, 2019	Revision 0.9	Initial Release
Sept.28, 2022	Revision 1.0	Production Release

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