SY20774D

5A, Single Cell Li-Ion DC/DC Switching Charger with I²C Control, USB Detection and OTG JEITA Compliant, Power Path Management

General Description

The SY20774D is a fully-integrated switching battery charger with system power path management devices for single cell Li-Ion and Li-polymer battery in a wide range of tablet and other portable devices. Its low impedance power path optimizes switching conversion efficiency, reduces battery charging time and extends battery life during the discharging mode. The I²C serial interface with charging and system settings makes the device a truly flexible solution.

The device supports a wide range of input sources, including standard USB host port, USB charging port and non-standard DC adapter. The SY20774D takes the result from the internal USB port identification circuit thru DP/DM compliant with BC1.2. The SY20774D can be compliant with USB 2.0 and USB 3.0 power spec with input current and voltage regulation. Meanwhile, the SY20774D meets USB On-the-go operation power rating specification by supplying 5V (programmable) on BUS with current limit up to 2.4A (programmable).

The power path management regulates the system voltage slightly above battery voltage but does not drop below 3.5V minimum system voltage (programmable). With this feature, the switching converter will keep working to support the system load even when the battery is completely depleted or removed. When the input current limit or voltage limit is reached, the power path management will reduce the charging current to zero firstly. If the system load continues to increase, the power path will discharge the battery to provide the power required by system. This supplement mode operation prevents overloading the input source.

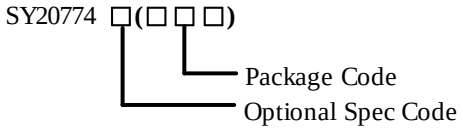
The device initiates and completes a charging cycle without software control. It automatically detects the battery voltage and charges the battery in three phases: preconditioning, constant current and constant voltage. At the end of the charging cycle, the charger will automatically be terminated when the charge current is below a preset limit in the constant voltage phase. When the full battery falls below the recharge threshold, the charger will automatically start another charging cycle. The SY20774D can be compliant with JEITA spec for the Li-Ion battery.

The device provides various safety features for battery charging and system operation, including negative thermistor monitoring, charging safety timer and over-voltage/over-current protections. The thermal regulation reduces charge current when the junction temperature exceeds 120°C(programmable).

The STAT output reports the charging status and any fault conditions. The INT immediately notifies the host when a fault occurs.

The SY20774D is available in QFN4×4-24 package.

Ordering Information



Ordering Number	Package type	Note
SY20774DQCQ	QFN4×4-24	

Features

- High Efficiency 5A 1.5MHz Buck Mode Charger
  - Support 3.9V-14V Input Voltage Range
  - Programmable IDPM/VDPM to Support the USB and Adapter
  - Support USB SDP/DCP/CDP and Non-Standard Adapter Detection
  - 3.84-4.608V Adjustable Charge Voltage
  - Support Narrow VDC Power Path Management
  - JEITA Compliance
  - ±0.5% Charge Voltage Regulation
  - Accelerate Charge Time by Battery Path Impedance Compensation
  - Charge Status Outputs for LED or Host Processor
- Maximum 2.4A 500KHz/1.5MHz Boost OTG Current
  - 4.55-5.51V Adjustable OTG Output Voltage
  - Selectable OTG Output Current Limit
  - Up to 2.4A OTG Current Limit on BUS
  - ±1.5% Output Regulation in Boost Mode
- Battery Monitor for Voltage, Temperature and Charge Current Measurements
- Full BATFET Control to Support Shipping Mode, Wake Up, and System Reset
- Up to 9A Battery Discharge Current
- Safety
  - Battery Temperature Sensing for Charge and Boost Mode
  - Battery Charging Safety Timer
  - Thermal Regulation and Thermal Shutdown
  - Input/System Over-voltage Protection
  - MOSFET Over-current Protection
- Low Battery Leakage Current and Support Shipping Mode
- 4mm × 4mm QFN-24 Package

Applications

- Smart Phone
- Tablet PC
- Power Bank
- Portable Internet Devices

Typical Applications

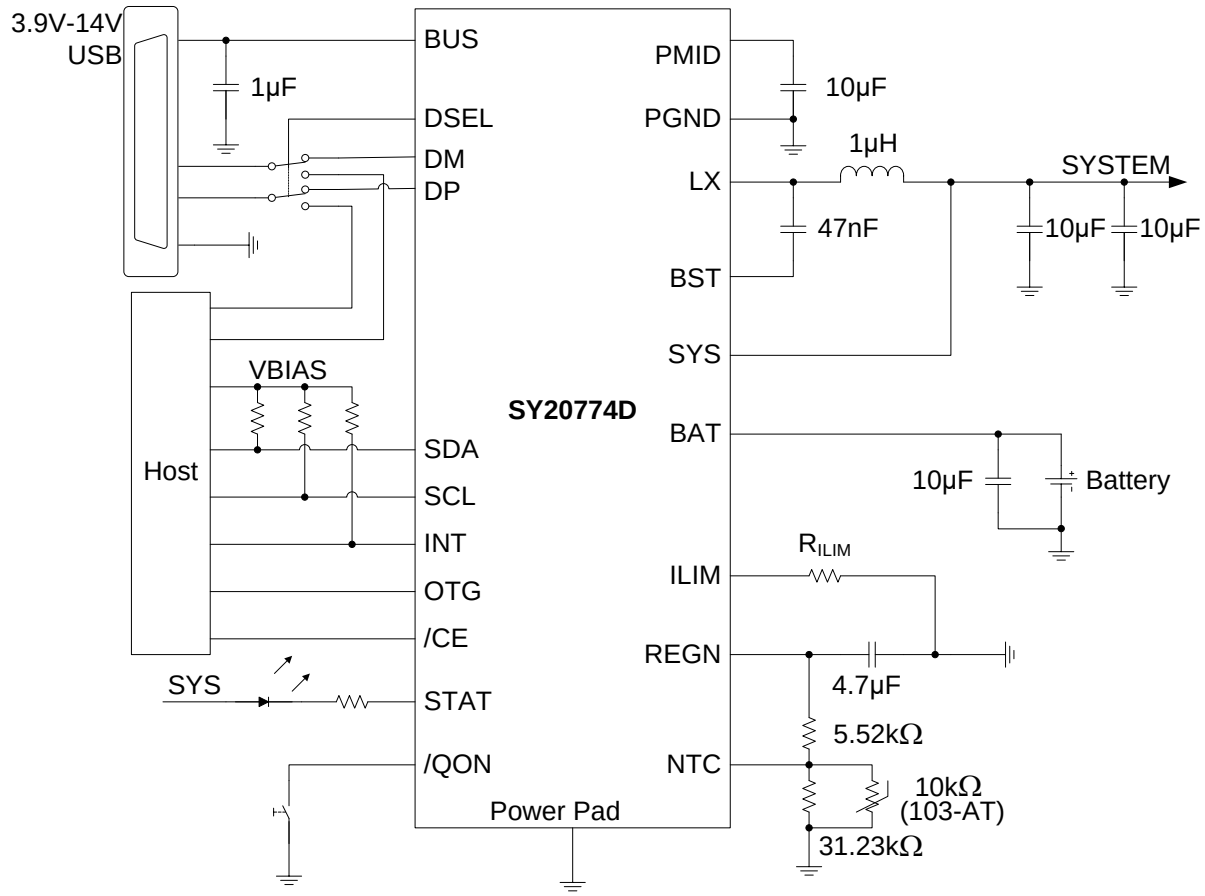
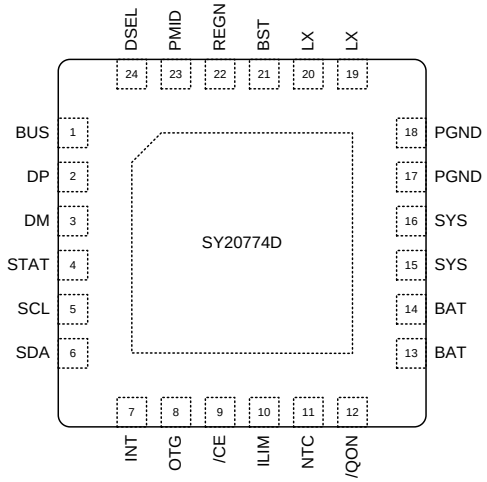


Figure 1. Schematic Diagram

Pinout (top view)



Top Mark: EWH*xyz*(device code: **EWH**, ***x=year code, y=week code, z= lot number code)***

Pin Description

Pin Name	Pin Number	Pin Description
BUS	1	Charger power input pin. Connect a 1μF ceramic capacitor from BUS to PGND as close as possible to the IC.
DP	2	USB identification port. USB detection strategy is compliant with BC1.2. SDP, CDP, DCP and adapter port can be identified according to the detection results thru DP/DM pins.
DM	3	
STAT	4	Open drain charge status indication pin. Pull up to a logic rail via 10kΩ resistor. STAT pin low indicates charge in progress; high indicates charge done or charge disabled. When any charge fault occurs, STAT pin will blink at 1Hz. The STAT pin function can be disabled by setting STAT_DIS bit.
SCL	5	I^2C Interface clock pin. Pull up to a logic rail via 10kΩ resistor.
SDA	6	I^2C Interface data pin. Pull up to a logic rail via 10kΩ resistor.
INT	7	Open-drain interrupt output. Pull up to a logic rail via 10kΩ resistor. The INT pin generates active low, 256μs pulse to notify the host about charge status and charge fault.
OTG	8	Boost mode active high enable pin. Boost mode will be enabled when REG03[5]=1 and OTG pin is high.
/CE	9	Charge mode active low enable pin. Battery charging will be enabled when REG03[4]=1 and /CE pin =Low. /CE pin must be pulled high or low.
ILIM	10	ILIM pin sets the maximum input current limit. A resistor is connected from ILIM pin to ground to set the maximum limit as I_{INMAX}= K_{ILIM} /R_{ILIM}. The actual input current limit is the lower one set by ILIM and by I^2C REG00[5:0]. The ILIM pin function can be disabled by setting EN_ILIM bit to 0.

NTC	11	Connect a resistor divider from REGN to NTC to GND to achieve battery thermal protection. Charge or discharge will suspend when NTC pin is out of range. Recommend 103AT-2 thermistor.
/QON	12	BATFET enables control in shipping mode and BATFET reset function. When BATFET is in shipping mode, logic high to low transition on this pin with minimum of T_{QON_LOW} low level turns on BATFET to exit shipping mode. This pin is internally pulled up to maintain default high logic. When BUS is not plugged-in and BATFET_DIS=0, a logic low of T_{QON_RST} resets system power by turning BATFET off for T_{BATFET_RST} and then re-enable BATFET.
BAT	13,14	Battery connection point to the positive terminal of the battery pack. The internal BATFET is connected between BAT and SYS. Connect a at least 10uF ceramic capacitor to the BAT pin.
SYS	15,16	System connection point. The internal BATFET is connected between BAT and SYS. When the battery falls below the minimum system voltage, switch-mode converter will keep SYS above the minimum system voltage.
PGND	17,18	Power ground connection. Internally, PGND is connected to the source of the n-channel LSFET. On PCB layout, connect this pin directly to ground connection of input and output capacitors.
LX	19,20	Switching node pin. Connect this pin to external inductor.
BST	21	HSFET driver positive supply. Connect a 47nF bootstrap capacitor between LX and BST.
REGN	22	LSFET driver positive supply. Connect a 4.7μF ceramic capacitor between REGN and analog GND. The capacitor should be placed closely to the IC. REGN also serves as bias rail of NTC pin.
PMID	23	Connect this pin to the drain of the reverse blocking MOSFET and the drain of HSFET. Connect a 10μF capacitor between PMID and PGND. The capacitor should be placed closely to the IC.
DSEL	24	Open-drain DP/DM multiplexer selection control. Pull up to a logic rail via 10kΩ resistor. During input source type detection, the pin outputs low to indicate DP/DM detection is in progress. When detection is done, the pin keeps low if HVDCP is detected. The pin returns to float and pulls high by resistor when other input source type is detected.
Exposed pad	-	Exposed pad beneath the IC for heat dissipation. Always solder exposed pad to the board, and have vias on the power pad plane star-connecting to PGND and ground plane for high-current power converter.

Block Diagram

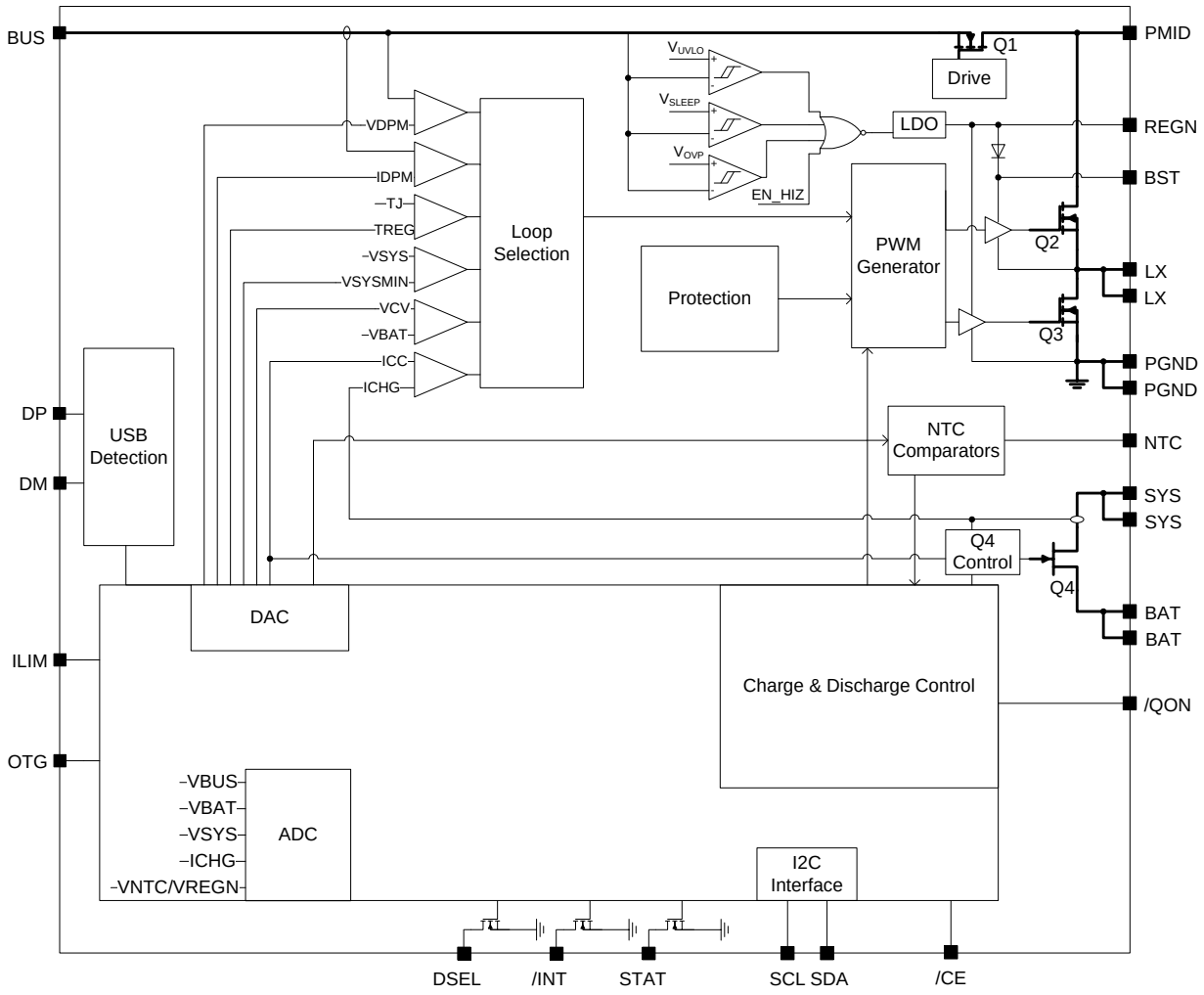


Figure 2. Block Diagram

Absolute Maximum Ratings (Note 1)

BUS, PMID, LX, DP, DM, DSEL, /CE, OTG, SCL, SDA, ILIM, STAT, INT, /QON ---------- -0.3V to +18V
NTC, BAT, SYS, BST-LX, REGN ---------- -0.3V to +6V
Package Thermal Resistance (Note 2)
QFN4×4-24 θ_{JA} ---------- 33.3 °C/W
QFN4×4-24 θ_{JC} ---------- 29.7 °C/W
Junction Temperature Range ---------- -40°C to +150°C
Operating Temperature Range ---------- -40°C to +100°C
Storage Temperature ---------- -65°C to +150°C

ESD Susceptibility
HBM (Human Body Mode) ----------2kV
CDM (Charge Device Mode) ----------750V

Recommended Operating Conditions (Note 3)

BUS, PMID, LX ---------- 0V to +16V
Others ---------- 0V to +5.5V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{BUS_UVLOZ}<V_{BUS}<V_{ACOV} and V_{BUS}>V_{BAT}+V_{SLEEPZ}, T_A=25℃ for typical values unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
QUIESCENT CURRENTS						
Battery Discharge Current (BAT)	I_{BAT}	V_{BUS}<V_{BUS_UVLOZ}, V_{BAT}=4.2 V, leakage between BAT and BUS			5	μA
		High-Z Mode, no BUS, battery monitor disabled, BATFET disabled		12	22	μA
		High-Z Mode, no BUS, battery monitor disabled, BATFET enabled		32	55	μA
Input Supply Current in High-Z Mode	I_{BUS_HIZ}	V_{BUS}=5V, battery monitor disabled, no battery, High-Z mode enabled		15	35	μA
		V_{BUS}=12V, battery monitor disabled, no battery, High-Z mode enabled		25	50	μA
Input Supply Current (BUS)	I_{BUS}	V_{BUS}>V_{BUS_UVLOZ}, V_{BUS}>V_{BAT}, converter not switching		1.5	3	mA
		V_{BUS}> V_{BUS_UVLOZ}, V_{BUS}>V_{BAT}, converter switching, charge disabled, V_{BAT}=3.2V, I_{SYS}=0A		3		mA
		V_{BUS}> V_{BUS_UVLOZ}, V_{BUS}>V_{BAT}, converter switching, charge disabled, V_{BAT}=3.8V, I_{SYS}=0A		3		mA
Battery Discharge Current in Boost Mode	$I_{OTGBOOST}$	V_{BAT}=4.2V, Boost mode, I_{BUS}=0A, converter switching		3.5		mA
BUS/BAT POWER UP						
BUS Operating Range	V_{BUS_OP}		3.9		14	V
BUS for Active IC and I^2C, No Battery	V_{BUS_UVLOZ}	Rising value to active I^2C	3	3.3	3.6	V
Sleep Mode Falling Threshold	V_{SLEEP}	V_{BUS} falling, V_{BUS}-V_{BAT}	25	65	120	mV
Sleep Mode Rising Threshold	V_{SLEEPZ}	V_{BUS} rising, V_{BUS}-V_{BAT}	220	270	320	mV
BUS Over-voltage Rising Threshold	V_{ACOV}	V_{BUS} rising	13.9	14.3	14.6	V
BUS Over-voltage Recovery Threshold	V_{ACOV_RC}	V_{BUS} falling		300		mV
Battery for Active I^2C,no BUS	V_{BAT_UVLOZ}	Rising value to active I^2C	1.9	2.1	2.3	V
Battery Depletion Threshold	V_{BAT_DPL}	V_{BAT} falling	2.15	2.3	2.5	V
Battery Depletion Recovery Threshold	V_{BAT_DPLZ}	V_{BAT} rising	2.3	2.5	2.7	V

POWER PATH MANAGEMENT						
System Regulation Voltage	V_{SYS_MAX}	I_{SYS} = 0A, V_{BAT}>V_{SYSMIN}, Q4 off, V_{BAT} up to 4.35V, V_{SYS}=V_{BAT}+50mV	4.39	4.4	4.45	V
	V_{SYS_MIN}	I_{SYS}=0A, V_{BAT}<V_{SYSMIN}=3.5V, Q4 off, V_{SYS}=V_{BAT}+150mV	3.55	3.65	3.75	V
Internal High-side Reverse Blocking MOSFET On-resistance	$R_{ON(RBFET)}$			25		mΩ
Internal High-side Switching MOSFET On-resistance Between PMID and LX	$R_{ON(HSFET)}$			25		mΩ
Internal Low-side Switching MOSFET On-resistance Between LX and PGND	$R_{ON(LSFET)}$			15		mΩ
BATTERY CHARGER						
Charge Voltage Regulation Accuracy	$V_{BAT\_REG\_ACC}$	V_{BAT_REG} = 4.208V and 4.352V	-0.5%		0.5%	
Fast Charge Current Regulation Accuracy	$I_{ICHG\_REG\_ACC}$	V_{BAT} = 3.8V, I_{CHG} = 1792mA	-4%		4%	
Battery LOWV Falling Threshold	$V_{BATLOWV}$	Fast charge to precharge, REG06[1]=0, V_{BAT} falling	2.6	2.8	2.9	V
Battery LOWV Rising Threshold	$V_{BATLOWV\_HYST}$	Precharge to fast charge, REG06[1]=0, V_{BAT} rising	2.8	3.0	3.1	V
Termination Current Accuracy	I_{TERM_ACC}	I_{TERM} = 256mA, I_{CHG} = 960mA	-20%		20%	
Battery Short Voltage	V_{SHORT}	V_{BAT} falling	1.9	2.0	2.1	V
Battery Short Voltage Hysteresis	V_{SHORT_HYST}	V_{BAT} rising		200		mV
Battery Short Current	I_{SHORT}	V_{BAT}<2.2V		100		mA
Recharge Threshold Below V_{BAT_REG}	V_{RECHG}	V_{BAT} falling, REG06[0]=0	70	110	150	mV
Recharge Deglitch Time	t_{RECHG}	V_{BAT} falling, REG06[0]=0		20		ms
SYS-BAT MOSFET On-Resistance	$R_{ON(BATFET)}$			10		mΩ

INPUT VOLTAGE/CURRENT REGULATION						
Absolute Input Voltage Regulation Accuracy	$V_{INDPM\_REG\_ACC}$	Set absolute VINDPM=4.4V	-2%		2%	
Input Current Limit Range	I_{INDPM_RANGE}		100		3250	mA
USB Input Current Regulation Limit, V_{BUS}=5V, Current Drawn from LX	I_{USB_DPM}	USB 100mA	85	90	100	mA
		USB 150mA	125	130	150	mA
		USB 500mA	425	450	500	mA
		USB 900mA	765	800	900	mA
Input Current Regulation Accuracy	I_{ADPT_DPM}	I^2C Set input current limit above 900mA	-15%		0%	
I_{INMAX} = K_{ILIM}/R_{ILIM}	K_{ILIM}	Input current regulation by ILIM pin=1.5A	350	375	400	AΩ
DP/DM DETECTION						
DP/DM Voltage source	V_{DP_SRC}, V_{DM_SRC}		0.5	0.6	0.7	V
Data Detect Voltage	V_{DAT_REF}		250		400	mV
BAT OVER-VOLTAGE PROTECTION						
Battery Over-voltage Threshold	V_{BATOVP}	V_{BAT} rising, as percentage of V_{BAT_REG}	102.5%	104%	105.5%	
Battery Over-voltage Hysteresis	V_{BATOVP_HYST}	V_{BAT} falling, as percentage of V_{BAT_REG}		2%		
BAT DISCHARGE OVER-CURRENT PROTECTION						
BATFET Discharge Over-current Threshold	I_{BATFET_OCP}		9	11	13	A
THERMAL REGULATION AND THERMAL SHUTDOWN						
Junction Temperature Regulation Accuracy	$T_{Junction\_REG}$	REG08[1:0]=11		120		℃
Thermal Shutdown Rising Temperature	T_{TSD}	Temperature rising		160		℃
Thermal Shutdown Hysteresis	T_{TSD_HYS}	Temperature falling		30		℃
JEITA THERMISTER Comparator						
T1(0℃) Threshold, Charge Suspended below this Temp	V_{T1}	V_{NTC} rising, as percentage to V_{REGN}, REG07[0]=0	72.55	73.25	73.95	%
Charge Back to I_{CHG}/2 and V_{REG} above this Temp	V_{T1_HYS}	Hysteresis, V_{NTC} falling, REG07[0]=0		1.25		%
T2(10℃) Threshold, Charge Back to I_{CHG}/2 and V_{REG} below this Temp	V_{T2}	V_{NTC} rising, as percentage to V_{REGN}, REG07[0]=0	67.55	68.25	68.95	%
Charge Back to I_{CHG} and V_{REG} above this Temp	V_{T2_HYS}	Hysteresis, V_{NTC} falling, REG07[0]=0		1.25		%

T3(45℃) Threshold, Charge Back to I_{CHG} and V_{REG}-150mV above This Temp	V_{T3}	V_{NTC} falling, as percentage to V_{REGN}, REG09[4]=0	44.05	44.75	45.45	%
Charge Back to I_{CHG} and V_{REG} below this Temp	V_{T3_HYS}	Hysteresis, V_{NTC} rising, REG09[4]=0		1.2		%
T4(60℃) Threshold, Charge Suspended above this Temp	V_{T4}	V_{NTC} falling, as percentage to V_{REGN}, REG09[4]=0	33.65	34.35	35.05	%
Charge Back to I_{CHG} and V_{REG}-150mV below this Temp	V_{T4_HYS}	Hysteresis, V_{NTC} rising, REG09[4]=0		1.2		%
BOOST MODE THERMISTER COMPARATOR						
Cold Temperature Threshold 0, NTC Pin Voltage Rising Threshold	V_{BCOLD0}	As Percentage to V_{REGN} (Approx.-10℃ w/103AT)	76.3	77	77.7	%
Falling Hysteresis	V_{BCOLD0_HYS}	(Approx.1℃ w/103AT)		1.25		%
Cold Temperature Threshold 1, NTC Pin Voltage Rising Threshold	V_{BCOLD1}	As Percentage to V_{REGN} (Approx.-20℃ w/103AT)	79.3	80	80.7	%
Falling Hysteresis	V_{BCOLD1_HYS}	(Approx.1℃ w/103AT)		1.25		%
Hot Temperature Threshold 0, NTC Pin Voltage Falling Threshold	V_{BHOT0}	As Percentage to V_{REGN} (Approx.55℃ w/103AT)	37.05	37.75	38.45	%
Rising Hysteresis	V_{BHOT0_HYS}	(Approx.3℃ w/103AT)		1.2		%
Hot Temperature Threshold 1, NTC Pin Voltage Falling Threshold	V_{BHOT1}	As Percentage to V_{REGN} (Approx.60℃ w/103AT)	33.65	34.35	35.05	%
Rising Hysteresis	V_{BHOT1_HYS}	(Approx.3℃ w/103AT)		1.2		%
Hot Temperature Threshold 2, NTC Pin Voltage Falling Threshold	V_{BHOT2}	As Percentage to V_{REGN} (Approx.65℃ w/103AT)	30.55	31.25	31.95	%
Rising Hysteresis	V_{BHOT2_HYS}	(Approx.3℃ w/103AT)		1.2		%
BUCK MODE OPERATIONS						
HSFET Cycle-by-cycle Current Limit	I_{HSFET_OCP}			8		A
PWM Switching Frequency	F_{SW}		1300	1500	1700	kHz
BOOST MODE OPERATIONS						
PWM Switching Frequency	F_{SW_BOOST1}	V_{BAT}=3.2V, V_{BUS}=5V, I_{BUS}=1A, REG02[5]=0	1300	1500	1700	kHz
PWM Switching Frequency	F_{SW_BOOST2}	V_{BAT}=3.2V, V_{BUS}=5V, I_{BUS}=1A, REG02[5]=1	465	550	635	kHz
OTG Output Voltage	V_{OTG_REG}	I_{BUS}=0	4.5		5.5	V
OTG Output Voltage Accuracy	$V_{OTG\_REG\_ACC}$	I_{BUS}=0	-1.5%		1.5%	
Battery Voltage Exiting Boost Mode	V_{OTG_BAT}	V_{BAT} falling	2.7	2.8	2.9	V

OTG Mode Output Current Limit	I_{OTG_OCP}	BOOST_LIM≥1.2A	100%	120%	140%	
OTG Over-voltage Threshold	V_{OTG_OVP}		5.8	6	6.2	V
OTG Over-voltage Threshold Hysteresis	$V_{OTG\_OVP\_HYS}$			300		mV
LSFET Cycle-by-cycle Current Limit	I_{OTG_ILIM}		5.5	7	8.5	A
REGN LDO						
REGN LDO Output Voltage	V_{REGN}	V_{BUS} = 5V, I_{REGN} = 20mA		4.8		V
REGN LDO Current Limit	I_{REGN}	V_{BUS} = 5V, V_{REGN} = 3.8V	50			mA
BATTERY MONITOR						
Resolution	RES			7		bits
/QON TIMING						
/QON Low Time to Turn on BATFET and Exit Ship Mode	T_{QON_LOW}		1.25		2.25	s
/QON Low Time to Reset BATFET	T_{QON_RST}		12		18	s
Reset Duration(BATFET Off time)	T_{BATFET_RST}		0.35		0.55	s
t_{SM_DLY}	Enter ship mode delay	BATFET_DIS=1,BATFET_DLY=1	10		15	s
LOGIC I/O PIN CHARACTERISTICS (OTG, /CE, STAT, /QON, DSEL)						
Input Low Threshold	V_{ILOW}				0.4	V
Input High Threshold	V_{IHGH}		1.3			V
Output Low Saturation Voltage	V_{OUT_LOW}				0.4	V
I²C INTERFACE (SDA, SCL, INT)						
Input High Threshold Level	V_{IH}		1.3			V
Input Low Threshold Level	V_{IL}				0.4	V
Output Low Threshold Level	V_{OL}				0.4	V
SCL Clock Frequency	f_{SCL}				400	kHz
DIGITAL CLOCK AND WATCHDOG TIMER						
Watchdog Timeout	t_{WDT}	REGN LDO disabled, REG07[5:4]=11	112	160	208	s
		REGN LDO enabled, REG07[5:4]=11	136	160	184	

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

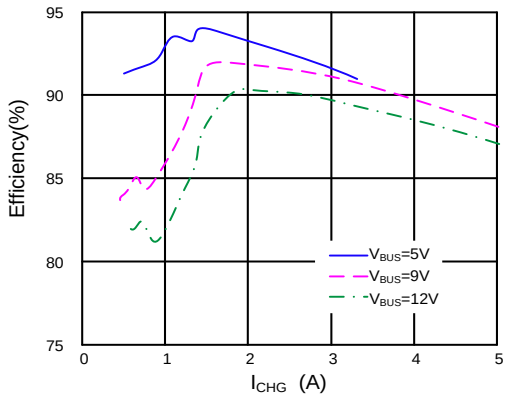
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective four layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

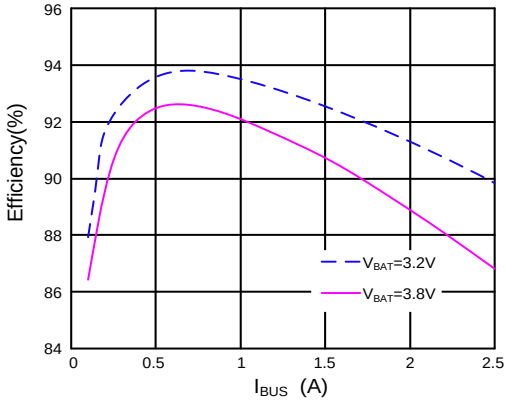
Typical Performance Characteristics

T_A=25°C, V_{BUS}=5V, 1cell battery, unless otherwise specified.

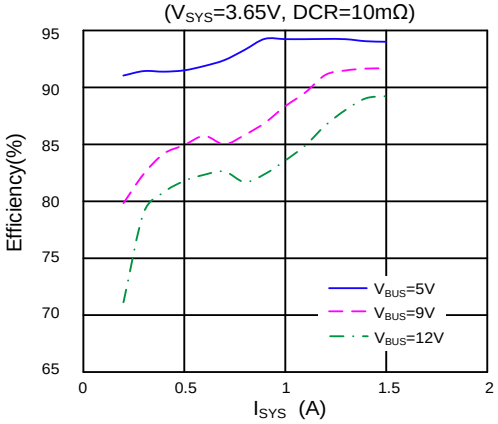
Efficiency vs. Charge Current (CC Mode)
(V_{BAT}=3.8V, DCR=10mΩ)



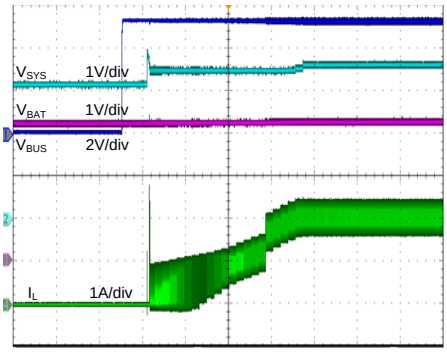
Efficiency vs. I_{BUS} (Boost Mode)
(V_{BUS}=5V, DCR=10mΩ)



Efficiency vs. I_{SYS} (Charge Disable)
(V_{SYS}=3.65V, DCR=10mΩ)

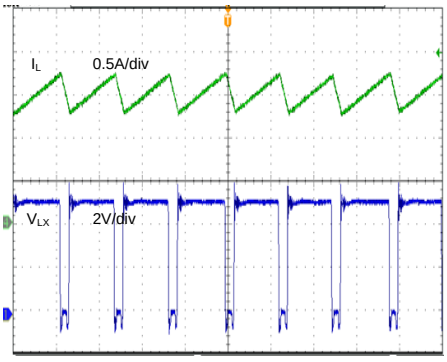


Adapter Plug-in in Default Mode
(V_{BAT}=3.1V)



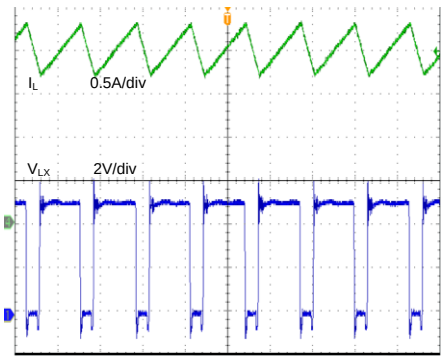
Time (400ms/div)

CV Mode Steady State
(V_{BAT}=4.2V)



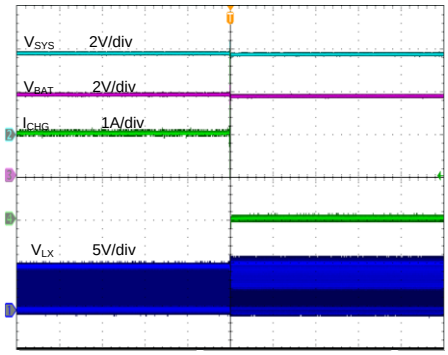
Time (400ns/div)

CC Mode Steady State
(V_{BAT}=3.7V)



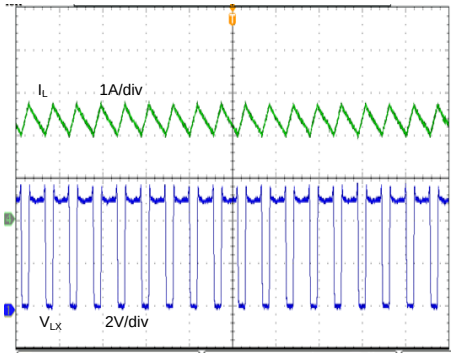
Time (400ns/div)

Charge Enable to Disable



Time (2ms/div)

Boost Mode Steady State
(I_{SYS}=1.5A)



Time (1µs/div)

I²C Registers

Address: 6AH

REG00

BIT	Name	POR	DESCRIPTION
7	EN_HIZ	0	**Enable HIZ Mode:** 0–Disable, 1–Enable
6	EN_ILIM	1	**Enable ILIM Pin:** 0–Disable, 1–Enable
5:0	IINLIM[5:0]	001000	**Input current limit:** (Actual input current limit is the lower of I²C or ILIM pin) IINLIM=100mA+50mA*[IINLIM] Range:100mA(000000)-3.25A(111111) 000000=100mA 000001=150mA … 001000=500mA(Default) … 111111=3.25A IINLIM will be changed according to the adapter type after input DP/DM detection is done. USB Host SDP=500mA USB CDP=1.5A USB DCP=3.25A

REG01

BIT	Name	POR	DESCRIPTION
7:6	BHOT[1:0]	00	**BOOST mode Hot Temperature Monitor Threshold:** 00-VBHOT0 Threshold (Typ. 37.75%) 01-VBHOT1 Threshold (Typ. 34.35%) 10/11-VBHOT2 Threshold (Typ. 31.25%)
5	BCOLD	0	**BOOST mode Cold Temperature Monitor Threshold**: 0-VBCOLD0 Threshold (Typ. 77%) 1-VBCOLD1 Threshold (Typ. 80%)

4:0	VINDPM_OS[4:0]	00110	**Input Voltage Limit Offset:** VINDPM_OS=100mV*[VINDPM_OS] Range:0mV-3100mV 00000=0mV 00001=100mV … 00110=600mV(Default) … 11111=3100mV Final minimum VINDPM threshold is clamped at 3.9V When V_{BUS}@no load is ≤6V, the VINDPM_OS is used for calculating VINDPM value. When V_{BUS}@no load is ＞6V, the VINDPM_OS*2 is used for calculating VINDPM value.

REG02

BIT	Name	POR	DESCRIPTION
7	CONV_START	0	**ADC Conversion Start Control:** 0-ADC not active 1-Start ADC Conversion This bit is read-only when CONV_RATE=1. The bit stays high during ADC conversion or pending ADC conversion during input source detection.
6	CONV_RATE	0	**ADC Conversion Rate Selection:** 0-One Short ADC Conversion 1-Start 1s continuous Conversion When CONV_RATE=0, CONV_START requires to be set to start conversion. When CONV_RATE=1, ADC conversion starts automatically and CONV_START is set during conversion.
5	BOOST_FREQ	0	**Boost Mode Frequency Selection:** 0-1.5MHz 1-500kHz Writing to this bit is ignored when OTG_CONFIG is enabled.
4	AICL_EN	1	**Adaptive Input Current Limit Enable:** 0-Disable 1-Enable
3	HVDCP_EN	1	**HVDCP Enable:** 0-Disable HVDCP handshake 1-Enable HVDCP handshake
2	HV_TYPE	0	**Higher Voltage Types can be Requested:** 0-9V 1-12V

1	FORCE_DPDM	0	**Force DP/DM detection:** 0-Not in DP/DM detection 1-Force DP/DM detection
0	AUTO_DPDM_EN	1	**Automatic DP/DM detection Enable:** 0-Disable DP/DM detection when BUS is plugged-in. 1-Enable DP/DM detection when BUS is plugged-in.

REG03

BIT	Name	POR	DESCRIPTION
7	BAT_LOAD_EN	0	**Battery Load (10mA) Enable**: 0-Disable 1-Enable
6	WD_RST	0	**I²C Watchdog Timer Reset:** 0-Normal 1-Reset Back to 0 after timer reset.
5	OTG_CONFIG	0	**Boost (OTG)Mode Configuration:** 0-OTG Disable 1-OTG Enable
4	CHG_CONFIG	1	**Charge Enable Configuration:** 0-Charge Disable 1-Charge Enable
3:1	SYS_MIN[2:0]	101	**Minimum System Voltage Limit:** SYS_MIN=3.0V+[SYS_MIN]*0.1V Range:3.0V-3.7V 000=3.0V 001=3.1V … 101=3.5V(Default) … 111=3.7V
0	Reserved	0	Reserved

REG04

BIT	Name	POR	DESCRIPTION
7	EN_PUMPX	0	Current Pulse Control Enable 0-Disable Current pulse control(default) 1-Enable Current pulse control(PUMPX_UP and PUMPX_DN)
6:0	ICHG[6:0]	0100000	**Fast Charge Current Limit:** ICHG=[ICHG]*64mA Range:0mA(0000000)-5056mA(1001111) 0000000=0mA(Disable Charge) 0000001=64mA … 0100000=2048mA(Default) … 1001111~1111111=5056mA

REG05

BIT	Name	POR	DESCRIPTION
7:4	IPRECHG[3:0]	0001	**Precharge Current Limit:** IPRECHG=64mA+[IPRECHG]*64mA Range:64mA-1024mA 0000=64mA 0001=128mA(Default) … 1111=1024mA
3:0	ITERM[3:0]	0011	**Termination Current Limit:** ITERM=64mA+[ITERM]*64mA Range:64mA-1024mA 0000=64mA 0001=128mA … 0011=256mA(Default) … 1111=1024mA

REG06

BIT	Name	POR	DESCRIPTION
7:2	VREG[5:0]	010111	**Charge Voltage Limit:** VREG=3.840V+[VREG]*16mV Range:3.840V-4.608V(110000) 000000=3.840V 000001=3.856V … 010111=4.208V(Default) … 110000~111111=4.608V
1	BATLOWV	1	**Battery Precharge to Fast Charge Threshold:** 0-2.8V 1-3.0V
0	VRECHG	0	**Battery Recharge Threshold Offset:** 0-100mV 1-200mV

REG07

BIT	Name	POR	DESCRIPTION
7	EN_TERM	1	**Charging Termination Enable:** 0-Disable 1-Enable
6	STAT_DIS	0	**STAT pin Disable:** 0-Enable 1-Disable
5:4	WATCHDOG[1:0]	01	**I^2C Watchdog Timer Setting:** 00-Disable timer 01-40s 10-80s 11-160s
3	EN_TIMER	1	**Charging Safety Timer Enable:** 0-Disable 1-Enable
2:1	CHG_TIMER[1:0]	10	**Fast Charge Timer Setting:** 00-5 hrs 01-8 hrs 10-12 hrs 11-20 hrs
0	JEITA_ISET (0℃-10℃)	1	**JEITA Low Temperature Current Setting:** Percentage with respect to ICHG register REG04[6:0] 0-50% 1-20%

REG08

BIT	Name	POR	DESCRIPTION
7:5	BAT_COMP[2:0]	000	**IR Compensation Resistor Setting:** BAT_COMP=[BAT_COMP]*20mΩ Range:0-140mΩ 000=0mΩ(Default) 001=20mΩ … 111=140mΩ
4:2	VCLAMP[2:0]	000	**IR Compensation Voltage Clamp:** VCLAMP= [VCLAMP]*32mV. The regulation voltage is clamped at VREG+VCLAMP. Range:0-224mV 000=0mV (Default) 001=32mV … 111=224mV
1:0	TREG[1:0]	11	**Thermal Regulation Threshold:** 00-60°C 01-80°C 10-100°C 11-120°C (Default)

REG09

BIT	Name	POR	DESCRIPTION
7	FORCE_AICL	0	**Force Start Adaptive Input Current Limit:** 0-Do not force 1-Force
6	TMR2X_EN	1	**Safety Timer Setting during Input DPM and Thermal Regulation:** 0-Safety timer not slowed by 2X during input DPM or thermal regulation. 1-Safety timer slowed by 2X during input DPM or thermal regulation.
5	BATFET_DIS	0	**Force BATFET Off:** 0-Allow Q4 turn on 1-Turn off Q4
4	JEITA_VSET (45℃-60℃)	0	**JEITA High Temperature Voltage Setting:** 0-VREG-150mV 1-VREG
3	BATFET_DLY	0	**BATFET turn off delay control:** 0-Turn off BATFET immediately when BATFET_DIS is set. 1-Turn off BATFET with the delay t_{SM_DLY} when

			BATFET_DIS is set.
2	BATFET_RST_EN	1	**BATFET Reset Enable:** 0-Disable BATFET reset function 1-Enable BATFET reset function
1	PUMPX_UP	0	**Current pulse control to request higher voltage:** 0-Disable 1-Enable
1	PUMPX_DN	0	**Current pulse control to request lower voltage:** 0-Disable 1-Enable

REG0A

BIT	Name	POR	DESCRIPTION
7:4	BOOSTV[3:0]	0111	**Boost Mode Voltage Regulation:** VBOOST=4.55V+[BOOSTV]*64mV Range:4.55V-5.51V 0000=4.55V 0001=4.614V … 0111=4.998V(Default) … 1001=5.126V … 1111=5.51V
3	Reserved	0	Reserved
2:0	BOOST_LIM[2:0]	011	**Boost Mode Current Limit:** 000=0.5A 001=0.75A 010=1.2A 011=1.4A 100=1.65A 101=1.875A 110=2.15A 111=2.45A

REG0B(Read only)

BIT	Name	POR	DESCRIPTION
7:5	BUS_STAT[2:0]	NA	**BUS Status register:** 000:No input 001:USB Host SDP 010:USB CDP 011:USB DCP 100:HVDCP 101:Unknown Adapter 110:Non-Standard Adapter 111:OTG
4:3	CHRG_STAT[1:0]	NA	**Charging status:** 00-Not Charging 01-Pre-charge (V_{BAT} <$V_{BATLOWV}$) 10-Fast Charging 11-Charge Termination Done
2	PG_STAT	NA	**Power Good Status:** 0-Not Power Good 1-Power Good
1	SDP_STAT	NA	**USB Input Status:** 0-USB100 input is detected 1-USB500 input is detected This bit always read 1 when BUS_STAT is not “001”.
0	VSYS_STAT	NA	**VSYS Regulation Status:** 0-Not in SYSMIN regulation (V_{BAT}>V_{SYSMIN}) 1-In SYSMIN regulation (V_{BAT}<V_{SYSMIN})

REG0C (Read only)

BIT	Name	POR	DESCRIPTION
7	WATCHDOG_FAULT	NA	**Watchdog Fault status:** 0-Normal 1-Watchdog timer expiration
6	BOOST_FAULT	NA	**Boost Mode Fault Status:** 0-Normal 1-BUS overloaded in OTG, or BUS OVP, or battery is too low
5:4	CHRG_FAULT[1:0]	NA	**Charge Mode Fault Status:** 00-Normal 01-Input fault (BUS OVP or V_{BAT}<V_{BUS}<3.8V) 10-Thermal shutdown 11-Charge Safety Timer Expiration
3	BAT_FAULT	NA	**Battery Fault Status:** 0-Normal 1-BATOVP

2:0	NTC_FAULT[2:0]	NA	**NTC Fault Status:** Buck Mode: 000-Normal 010-NTC Warm 011-NTC Cool 101-NTC Cold 110-NTC Hot Boost Mode: 000-NTC Normal 101-NTC Cold 110-NTC Hot

REG0D

BIT	Name	POR	DESCRIPTION
7	VINDPM_MODE	0	**VINDPM Threshold Setting Method:** 0-Run Relative VINDPM Threshold 1-Run Absolute VINDPM Threshold
6:0	VINDPM[6:0]	0010010	**Absolute VINDPM Threshold:** VINDPM=2.6V+[VINDPM]*100mV Range:3.9V(0001101)-15.3V(1111111) 0000000~0001101=3.9V 0001110=4.0V … 0010010=4.4V(Default) … 1111111=15.3V

REG0E (Read only)

BIT	Name	POR	DESCRIPTION
7	THERM_STAT	NA	**Thermal Regulation Status:** 0-Normal 1-In Thermal Regulation
6:0	BATV[6:0]	NA	**ADC Conversion of Battery Voltage(BATV):** BATV=2.304V+[BATV]*20mV Range: 2.304V(0000000)-4.844V(1111111) 0000000=2.304V(Default) 0000001=2.324V … 1111111=4.844V

REG0F (Read only)

BIT	Name	POR	DESCRIPTION
7	Reserved	0	0
6:0	SYSV[6:0]	NA	**ADC Conversion of System Voltage(SYSV):** SYSV=2.304V+[SYSV]*20mV Range: 2.304V(0000000)-4.844V(1111111) 0000000=2.304V(Default) 0000001=2.324V … 1111111=4.844V

REG10 (Read only)

BIT	Name	POR	DESCRIPTION
7	Reserved	0	Reserved
6:0	NTCPCT[6:0]	NA	**ADC Conversion of NTC Voltage (NTC) as percentage of REGN:** NTC/REGN=21%+[NTCPCT]*0.465% Range:21%(0000000)-80.055%(1111111) 0000000=21%(Default) 0000001=21.465% … 1111111=80.055%

REG11 (Read only)

BIT	Name	POR	DESCRIPTION
7	BUS_GD	NA	**BUS GOOD Status:** 0-No BUS attached 1-BUS attached
6:0	BUSV [6:0]	NA	**ADC Conversion of BUS Voltage(VBUS):** BUSV =2.6V+[BUSV]*100mV Range:2.6V(0000000)-15.3V(1111111) 0000000=2.6V(Default) 0000001=2.7V … 1111111=15.3V

REG12(Read only)

BIT	Name	POR	DESCRIPTION
7	Reserved	0	
6:0	ICHGR[6:0]	NA	**ADC Conversion of Charge current (ICHG) for $V_{BAT}>V_{SHORT}$:** ICHGR=[ICHGR]*50mA Range:0mA(0000000)-6350mA(1111111) 0000000=0mA(Default)

			0000001=50mA … 1111111=6350mA Note: For V_{BAT}<V_{SHORT}, this register returns 0000000.

REG13(Read only)

BIT	Name	POR	DESCRIPTION
7	VDPM_STAT	NA	**VINDPM Status:** 0-Not in VINDPM 1-In VINDPM
6	IDPM_STAT	NA	**IINDPM Status:** 0-Not in IINDPM 1-In IINDPM
5:0	IDPM_LIM[5:0]	NA	**Current Input Current Limit setting:** IDPM_LIM=100mA+[IDPM_LIM]*50mA Range:100mA(000000)-3.25A(111111) 000000=100mA(Default) 000001=150mA … 111111=3250mA

REG14

BIT	Name	POR	DESCRIPTION
7	REG_RST	0	**Register Reset:** 0-Keep current register setting(Default) 1-Reset to default register value and reset safety timer Reset to 0 after register reset is completed
6	AICL_OPTIMIZED	NA	**Adaptive Input Current Limit Status:** 0-Detection in process 1-Maximum input current detected
5:3	PN[2:0]	NA	**Device Configuration:** 001
2	NTC_PROFILE	NA	**Temperature profile:** 0-Cold/Hot window 1-JEITA
1:0	DEV_REV[1:0]	NA	**Device Revision:** Start from 00

Operation Principle

The SY20774D is a fully-integrated switching battery charger with system power path management devices for single cell Li-ion and Li-polymer battery in a wide range of tablet and other portable devices. It integrates the input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and BATFET (Q4) between system and battery. The extremely low R_{DSON} achieves very high conversion efficiency up to 5.056A charging current. The device also integrates the bootstrap diode for the high-side gate drive.

Power-On-Reset (POR)

The internal bias circuits are powered from the higher voltage between BUS and BAT. When BUS rises above V_{BUS_UVLOZ} or BAT rises above V_{BAT_UVLOZ}, the sleep comparator, battery depletion comparator and BATFET driver will be active. I^2C interface is ready for communication. The host can access all the registers after POR.

Power Up from Battery without DC Source

If only battery is present and the voltage is above depletion threshold (V_{BAT_DPLZ}), the BATFET will turn on and provide power to system. The device in HIZ mode and the REGN LDO stays off to minimize the quiescent current. The low R_{DSON} in BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time. The device always monitors the discharge current through BATFET. When the system is overloaded or shorted, the device will immediately turn off BATFET and latch off until the input source plugs in again or one of the methods describe in section “BATFET Enable Mode” to re-enable BATFET.

Power Up from DC Source

When the DC source plugs in, the SY20774D will check the input source voltage to turn on REGN LDO and all the bias circuits. It will also check and set the input current limit before starting the Buck converter when AUTO_DPDM_EN bit is set.

REGN LDO

The REGN LDO supplies internal bias circuits as well as the HSFET and LSFET gate drive. The LDO also provides bias rail to NTC external resistors. The pull-up rail of STAT can be connected to REGN as well.

When the device is in high impedance mode (HIZ) with REGN LDO off, the device will draw less than I_{BUS_HIZ} from BUS during HIZ state. The battery will power up the system when the device is in HIZ mode.

Blocking FET (Q1)

After REGN LDO powers up, the SY20774D turns on the blocking FET to reduce the power loss.

Input Source Qualification

After REGN LDO powers up, SY20774D will check the current capability of the input source. The input source capability is qualified by the internal active detection circuit.

Once a good input source is present, the status register BUS_GD bit will go high. An INT is asserted to the host.

Input Source Type Detection

After the REGN LDO is powered, the charger device will run input source type detection when AUTO_DPDM_EN bit is set and a DC source plugs in.

The SY20774D can set input current limit through DP/DM pins. The SY20774D follows the USB battery charging specification 1.2 (BC1.2) and to detect input source (SDP/CDP/DCP) and non-standard (Apple/Samsung) adapter through USB DP/DM lines.

The host can over-write IINLIM register to change the input current limit if necessary. The charger input current will always be limited by the IINLIM register and ILIM pin at all time regardless of adaptive input current limit (AICL) is enabled or disabled.

When AUTO_DPDM_EN is disabled, the input source type detection will be bypassed.

Force Input Current Limit Detection

The host can force the charger device to run input current limit detection by setting FORCE_DPDM bit. After the detection is complete, FORCE_DPDM will return to 0 by itself and input source type detection result will be updated.

Input voltage limit setting

The device supports wide range of input voltage limit (3.9V-14V) source and provides two methods to set input voltage limit (VINDPM) threshold to facilitate autonomous detection.

1. Absolute VINDPM (VINDPM_MODE=1).

By setting VINDPM_MODE bit to 1, the relative VINDPM threshold setting algorithm is disabled. Register VINDPM is writable and allows host to set the absolute threshold of VINDPM function.

2. Relative VINDPM based on VINDPM_OS register (VINDPM_MODE=0)

When VINDPM_MODE bit is 0 (default), the relative VINDPM threshold setting algorithm is enabled, the VINDPM register is read only and the charger controls the register by using VINDPM threshold setting algorithm. The algorithm allows a wide range of adapter (V_{BUS_OP}) to be used with flexible VINDPM threshold.

Converter Power-Up

After the input current and voltage are set, the converter will be enabled and the HSFET and LSFET starts switching. If battery charging is disabled, BATFET will turn off. Otherwise, BATFET will stay on to charge the battery.

The SY20774D will provide soft-start when ramps up the system rail. When the system rail is below 2.2V, the input current limit will be 100mA.

As a battery charger, the SY20774D deploys a 1.5MHz Buck regulator. Internal compensation network allows minimizing the peripheral circuit design.

In order to improve light-load efficiency, the device switches to PFM control at light load.

Adaptive Input Current Limit (AICL)

The SY20774D uses adaptive input current limit (AICL) to identify maximum power point of input source. The algorithm automatically identifies maximum input current limit of power source to avoid source overload.

Boost Mode Operation from Battery

The SY20774D can supply power from the battery to other portable devices on BUS input port. The SY20774D employs a 500kHz or 1.5MHz (selectable using BOOST_FREQ bit) Boost regulator.

Any fault during Boost operation, including BUS over voltage, or over current, or battery too low (V_{BAT}<V_{OTG_BAT}), sets the BOOST_FAULT register to 1 and an INT is asserted.

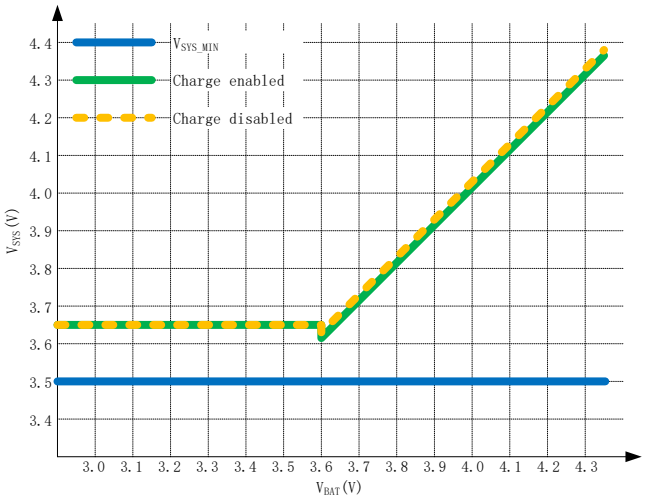
During Boost mode, the status register BUS_STAT is set to 111, the BUS output is 5V by default and the output current limit can reach up to 2.4A, selected via I^2C (BOOST_LIM bits).

Power Path Management

The SY20774D accommodates a wide range of input sources from USB, wall adapter, or car battery. The device provides automatic power path selection to supply the system (SYS) from input source (BUS), battery (BAT), or both.

Narrow VDC Architecture

The device deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by SYS_MIN bits. Even with a fully depleted battery the system is regulated above the minimum system voltage (default 3.5V), The status register VSYS_STAT bit will go high when the system is in minimum system voltage regulation.



Dynamic Power Management

The SY20774D can manage the input power limit very well. It has input VINDPM and IINDPM function to protect the input source from over-loading.

When input source is over-loaded, either the current will exceed the input current limit (IINLIM) or the voltage will fall below the input voltage limit (VINDPM). The device will reduce the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero but the input source is still over-loading, the system voltage will start to drop. Once the system voltage falls below the battery voltage, the device will automatically enter the supplement mode where the BATFET turns on and battery starts discharging so that the system is supported from both the input source and battery.

During DPM mode, the status register VDPM_STAT or IDPM_STAT will go high.

Battery Charging Management

The SY20774D charges 1-cell Li-Ion battery with up to 5.0A charge current for high capacity tablet battery. The 10mΩ BATFET improves charging efficiency and minimizes the voltage drop during discharging.

Autonomous Charging Cycle

With battery charging enabled at POR (CHG_CONFIG bit =1 and /CE pin is low), SY20774D can complete a charging cycle without host involvement. The device default charging parameters are listed below.

Default Charging Setting	
VREG, Charge Voltage	4.208 V
ICHG, Charge Current	2.048 A
IPRECHG, Pre-charge Current	128 mA
ITERM, Termination Current	256 mA
CHG_TIMER, Fast Charge Timer	12 hours

The charger device automatically terminates the charging cycle when the charging current is below termination threshold and in constant voltage charge phase. When a full battery voltage is discharged below recharge threshold (REG06[0]), the SY20774D will automatically start another charging cycle.

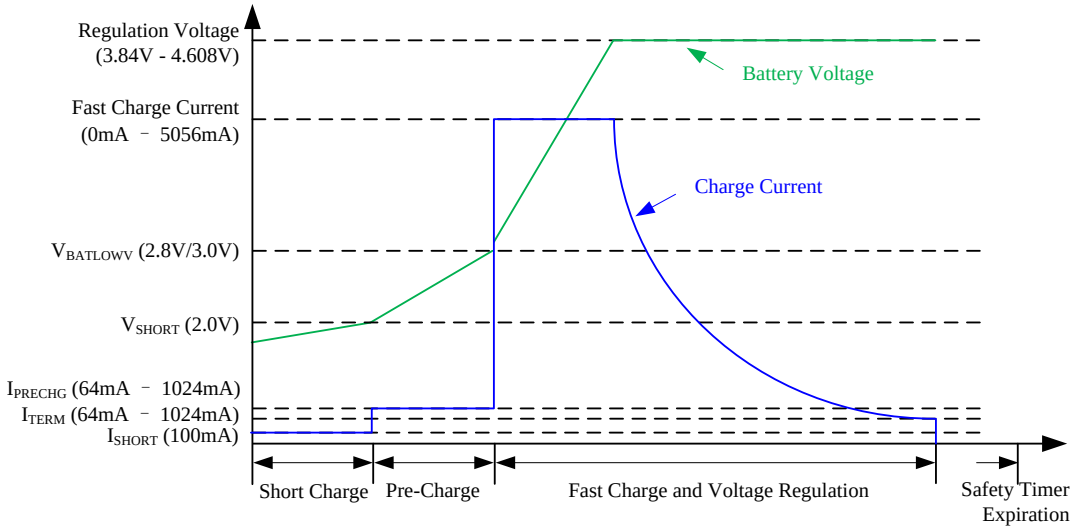
The STAT output indicates the charging status of charging (LOW), charging completion or charge disable (HIGH) or charging fault (Blinking). The STAT output can be disabled by setting STAT_DIS bit. The status register CHRG_STAT indicates different charging phases: 00-charging disable, 01-pre-charge, 10-fast charge (constant current) and constant voltage mode, 11-charging done. Once a charging cycle is complete, an INT will be asserted to notify the host.

The host can always control the charging operation and optimize the charging parameters by writing to the registers through I^2C.

Battery Charging Profile

The device charges the battery in three phases: pre-charge, constant current and constant voltage. At the beginning of a charging cycle, the device checks the battery voltage and applies current.

If the charger device is in DPM regulation or thermal regulation during charging, the actual charging current will be less than the programmed value. In this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate.



Charging Termination

The SY20774D will terminate a charge cycle when in constant voltage charge, and the current is below termination current. After the charging cycle is complete, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn back on to engage supplement mode.

When termination occurs, the CHRG_STAT is 11, and an INT is asserted to the host. Termination can be disabled by writing 0 to EN_TREM.

Charging Safety Timer

The SY20774D has safety timer to prevent extended charging cycle due to abnormal battery conditions.

The device keeps charging the battery until the fast charging safety timer expired. The duration of safety timer can be set by the CHG_TIMER bits (default = 12 hours). Once the safety timer is expired, the fault register CHRG_FAULT bits will be set to 11 and an INT will be asserted to the host. The safety timer feature can be disabled by setting EN_TIMER bit.

During input voltage/current regulation or thermal regulation, the safety timer counts at half clock rate. For example, if the charger is in input current regulation (IINDPM) throughout the whole charging cycle, and the safety time is set to 5 hours, the safety timer will expire in 10 hours. This feature can be disabled by writing 0 to REG09[6].

Host Mode and Default Mode

The SY20774D can operate with or without host. In default mode, the SY20774D can be used as an autonomous charger with no host or with host in sleep.

When the charger is in default mode, WATCHDOG_FAULT bit is high. When the charger is in host mode, WATCHDOG_FAULT is low.

After power-on-reset, the device starts in default mode. The registers are in the default settings.

Any host writing command to I^2C transitions the device from default mode to host mode. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WD_RST bit before the watchdog timer expires or disable watchdog timer by setting WATCHDOG bit to 0.

When the watchdog timer is expired, the device gets back to the default mode.

Battery Monitor

The device includes a battery monitor to provide fully measurements, including battery voltage, system voltage, thermistor voltage, BUS voltage, and charging current. The results are reported in Battery Monitor Register (REG0E-REG12). The battery monitor can be configured for two conversion modes, by setting CONV_RATE bit: one-shot conversion (default) and continuous conversion.

For one-shot conversion, the CONV_START bit can be set to start one conversion. During the conversion, the CONV_START is set until the conversion is done. The conversion is done after Tconv (max 1s). When one-shot conversion is initiated during input source type detection, the CONV_START bit is set to indicate conversion is postponed until detection done and conversions is done.

For continuous conversion, the CON_RATE bit can be set to start the conversion every 1 second automatically. During the conversion, the CONV_START is set to indicate conversion is in process. The battery monitor exits continuous conversion mode when CONV_RATE is cleared.

Status Outputs (/PG STAT and INT)

Power Good Indicator (/PG)

In the SY20774D, PG_STAT bit is set to indicate a good input source.

Charging Status Indicator (STAT)

The SY20774D indicates charging state on the open drain STAT pin. The STAT pin can drive LED as the application diagram shows.

STAT Pin State	
CHARGING STATE	STAT
Charging in progress (including recharge)	LOW
Charging complete	HIGH
Sleep mode, charge disable	HIGH
Charge suspend	blinking at 1Hz

Interrupt to Host (INT)

In some applications, the host does not always monitor the charger operation. The INT notifies the system on the device operation.

When a fault occurs, the charger device will send out INT and latches the fault state in REG0C until the host reads the fault register. Before the host reads REG0C and all the faults (not including watchdog timer fault) are cleared, the charger device would not send any INT upon new faults.

In order to read the current fault status, the host has to read REG0C two times consecutively. The 1st reads fault register status from the last INT and the 2nd reads the current fault register status. The only exception is NTC_FAULT which always reports the actual condition on the NTC pin.

BATFET (Q4) Control

BATFET Disable Mode (Shipping mode)

To extend battery life and minimize power when system is powered off during system idle, shipping, or storage, the device can turn off BATFET so that the system voltage is zero to minimize the battery leakage current.

When the host set BATFET_DIS bit, the charger can turn off BATFET immediately or delay by t_{SM_DLY} as configured by BATFET_DLY bit.

BATFET Enable Mode (Exit Shipping mode)

When the BATFET is disabled (in shipping mode) and indicated by setting BATFET_DIS, Plugging in adapter or a logic high to low transition on /QON pin with t_{QON_LOW} can enable BATFET to restore system power:

BATFET System Reset

The BATFET functions as a load switch between battery and system when input source is not plugged-in. By changing the state of BATFET from OFF to ON, system connects to SYS can be effectively have a power-on-reset.

The function can be disabled by setting BATFET_RST_EN bit to 0.

Protections

Input Current Limit on ILIM

For safe operation, the SY20774D has an additional hardware pin to limit maximum input current on ILIM pin. The input maximum current is set by a resistor from ILIM pin to ground as:

$$I_{INMAX} = \frac{K_{ILIM}}{R_{ILIM}}$$

The actual input current limit is the lower value between ILIM setting and register setting IINLIM. If ILIM pin is open, the input current is limited to zero. If ILIM pin is short to ground, the input current limit will be set by the register.

The ILIM pin function can be disabled by setting EN_ILIM bit to 0. When the pin is disabled, both input current limit function and monitoring will not be available.

Thermal Regulation and Thermal Shutdown

BUCK Mode

The SY20774D monitors the internal junction temperature T_J to avoid overheating the chip and limits the IC surface temperature. When the internal junction temperature exceeds the preset limit (TREG bits), the device will lower down the charge current. The wide thermal regulation range from 60°C to 120°C allows the user to optimize the system thermal performance.

During thermal regulation, the actual charging current is usually below the programmed battery charging current. Therefore, termination is disabled, the safety timer runs at half the clock rate, and the status register THERM_STAT goes high.

Additionally, the device has thermal shutdown to turn off the converter and BATFET. The fault register CHRG_FAULT is 10 and an INT is asserted to the host. The BATFET and converter are enabled to recover when the IC temperature is below T_{TSD} - T_{TSD_HYS}.

BOOST Mode

The device monitors the internal junction temperature to provide thermal shutdown during boost mode. When the IC junction temperature exceeds T_{TSD}, the boost mode will be disabled by setting OTG_CONFIG low.

Voltage and Current Monitoring in Buck Mode

The SY20774D closely monitors the input and system voltage, as well as HSFET and LSFET current for safe buck mode operation.

Input Over-Voltage (ACOV)

The maximum input voltage for buck mode operation is V_{BUS_OP}. If BUS voltage exceeds V_{ACOV}, the device will stop switching immediately. During input over voltage (ACOV), the fault register CHRG_FAULT will be set to 01. An INT is asserted to the host.

System Over-Voltage Protection (SYSOVP)

The charger device monitors the voltage at SYS. When system over-voltage is detected, the converter will be stopped to protect components connected to SYS from high voltage damage.

Voltage and Current Monitoring in Boost Mode

The SY20774D closely monitors the BUS voltage, as well as HSFET and LSFET current to ensure safe boost mode operation.

Over Current Protection

The charge device closely monitors the RBFET(Q1), HSFET(Q2) and LSFET(Q3) current to ensure safe Boost operation.

During over-current condition when Boost output current exceeds (BOOST_LIM), the device will always operate in hiccup mode for protection. Once the over current condition is removed, the Boost output will recover. The fault register bit BOOST_FAULT is set high to indicate fault in Boost operation. An INT is also sent to the host.

Over-Voltage Protection

Once the BUS voltage exceeds V_{OTG_OVP}, the SY20774D stops switching and clears OTG_CONFIG bit and exits Boost mode. The fault register BOOST_FAULT is set high to indicate fault in Boost operation. An INT is sent to the host.

Battery Protection

Battery Over-Voltage Protection (BATOVP)

The battery over-voltage limit is clamped at 4% above the battery regulation voltage. When battery over voltage occurs, the charger device will immediately disable charge. The fault register BAT_FAULT will go high and an INT will be asserted to the host.

Battery Over-discharge Protection

When battery voltage is discharged below V_{BAT_DPL}, the BATFET will be turned off to protect battery from over discharge. To recover from over-discharge, an input source is required at BUS. When an input source is plugged in, the BATFET will turn on again.

If the battery voltage falls below V_{SHORT}, the charge current will be reduced to short charge or pre-charge current for battery safety.

System Over-Current Protection

If the system is shorted or BATFET OCP occurs, the BATFET will be latched off. Section “BATFET Enable Mode” can reset the latch off condition and turn on BATFET.

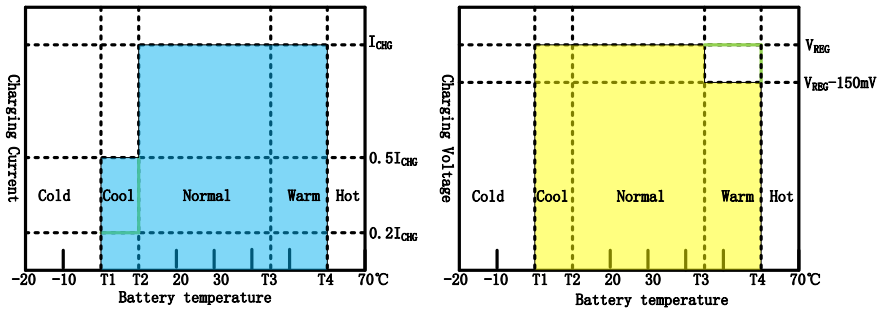
Thermistor Temperature Window

The SY20774D continuously monitors battery temperature by measuring the voltage between the NTC pin and ground, typically determined by a negative temperature coefficient thermistor and an external voltage divider.

Charging JEITA Guideline Compliance

JEITA recommends suspending the battery charging process when NTC pin voltage is out of the V_{T1} to V_{T4} range, and recovering charging process once the NTC voltage is within the range. JEITA also recommends that the charge current to be reduced to at least half of the charge current or lower at cool temperature (T1–T2), and the charge voltage to be reduced less than nominal charge voltage at warm temperature (T3–T4).

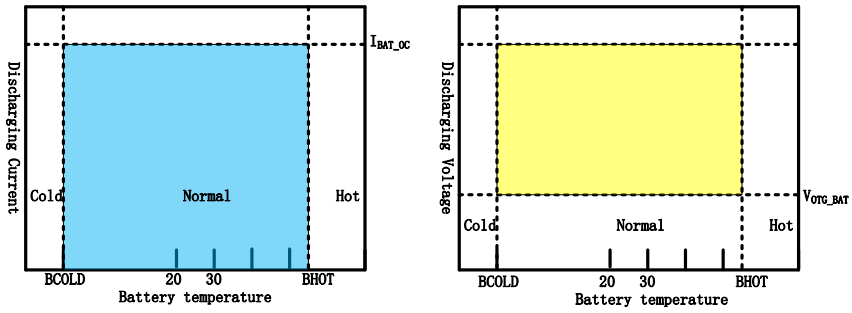
The SY20774D provides flexibility charge voltage/current settings beyond the JEITA requirement. REG09 bit[4] is used for setting the charge voltage to be same as or 150mV lower than the nominal charge voltage (REG06 bit[7:2]) at warm temperature (T3–T4). REG07 bit[0] is used for setting the current setting to be 20% or 50% of fast charge current (REG04 bit[6:0]) at cool temperature (T1–T2).



When the NTC fault occurs, the fault register NTC_FAULT will indicate the actual condition on NTC pin and an INT will be asserted to the host. The STAT pin will indicate the fault when charging is suspended.

Discharging Cold/Hot Temperature Window

The device will terminate the battery discharging process when NTC pin voltage is out of the V_{BCOLD} to V_{HOT} range. To allow the discharge, the battery temperature must be within this range. The threshold of V_{BCOLD} and V_{HOT} is selectable by setting REG01.



When the NTC fault occurs, the fault register NTC_FAULT will indicate the actual condition on NTC pin and an INT will be asserted to the host.

Serial Interface

The SY20774D uses I²C compatible interface for flexible charging parameter programming and instantaneous device status reporting. Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address 6AH, receiving control inputs from the master device like micro controller or a digital signal processor. The I²C interface supports both standard mode (up to 100kbits), and fast mode (up to 400kbits).

Both SDA and SCL are bi-directional lines, connecting to the positive supply voltage via a current source or pull- up resistor. When the bus is free, both lines will be HIGH. The SDA and SCL pins are open drain.

Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

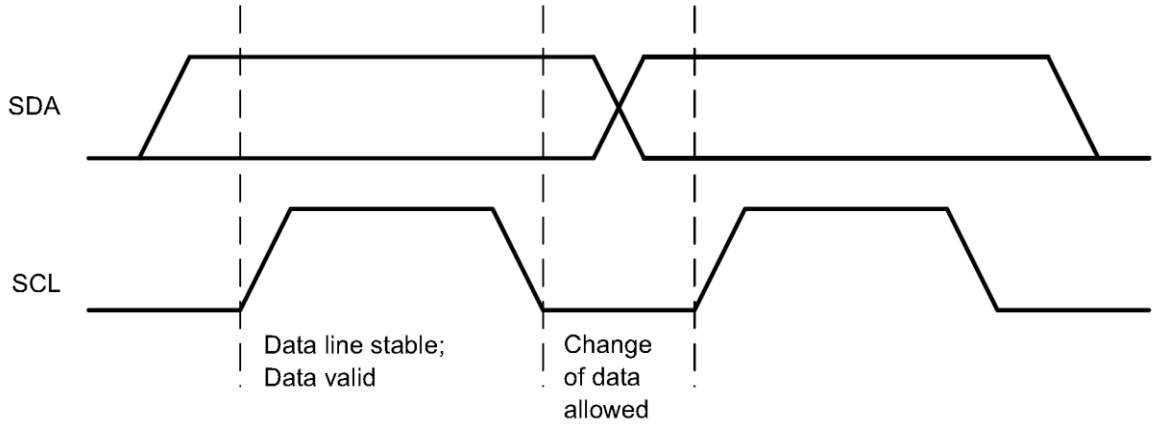


Figure 3. Bit Transfer on the I²C Bus

START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

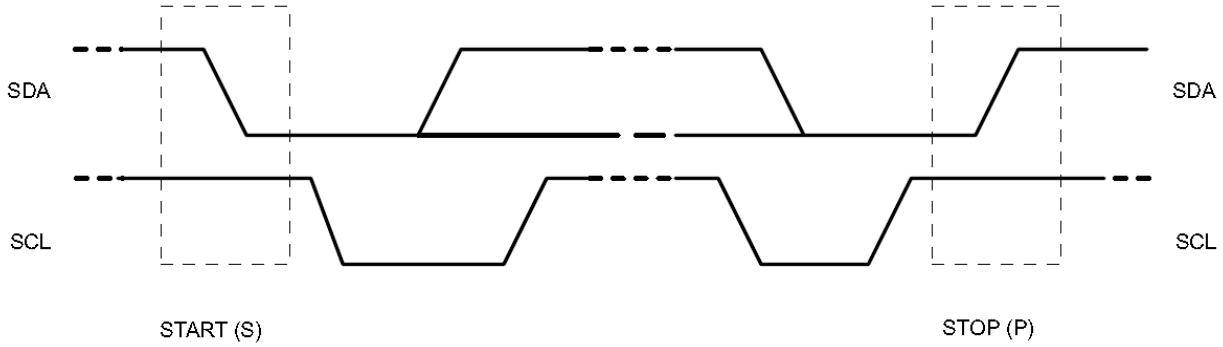


Figure 4. START and STOP conditions

Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

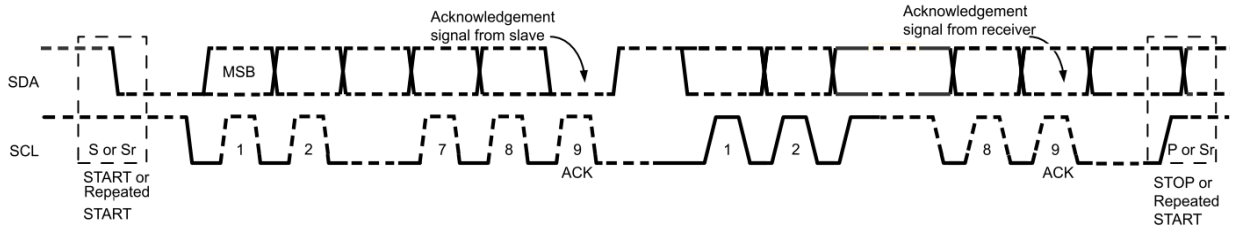


Figure 5. Data Transfer on the I²C Bus

Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledged 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the high period of this clock pulse.

When SDA remains high during the 9th clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

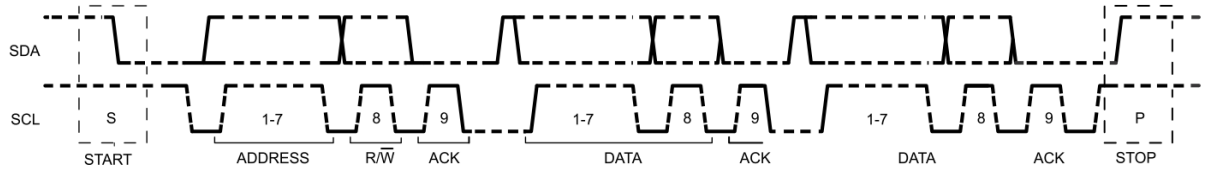


Figure 6. Complete Data Transfer

Single Read and Write

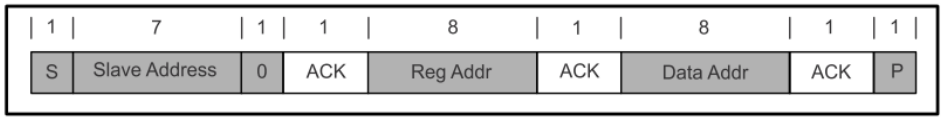


Figure 7. Single Write

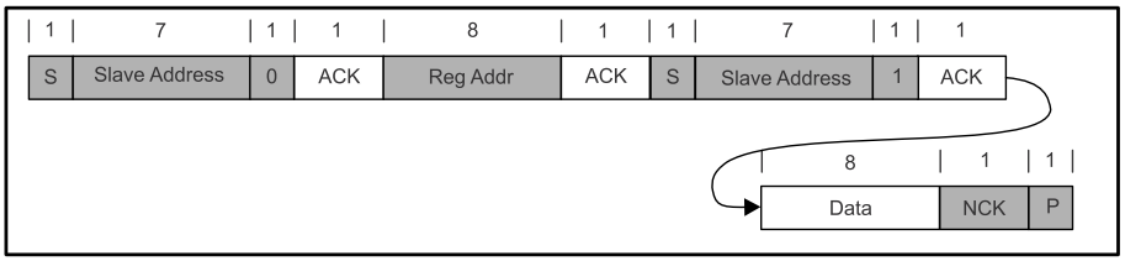


Figure 8. Single Read

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

Multi-Read and Multi-Write

The charger device supports multi-read and multi-write on REG00 through REG08.

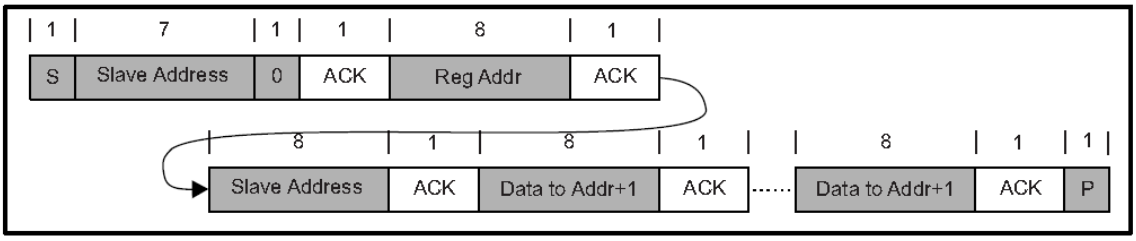


Figure 9. Multi-Write

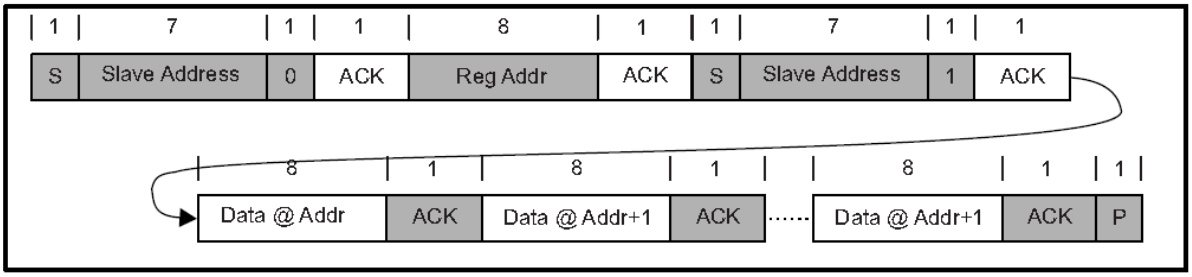


Figure 10. Multi-Read

The fault register REG0C locks the previous fault and only clears it after the register is read. For example, if charge safety timer expiration fault occurs but recovers later, the fault register REG0C will report the fault when it is read the first time, but will return to normal when it is read the second time. To verify real time fault, the fault register REG0C should be read twice to get the real condition. In addition, the fault register REG0C does not support multi-read or multi-write.

Applications Information

The following battery charger design refers to the "Application Schematic". This section describes how to select the external components including the inductor, the input and output capacitors.

Inductor Selection

Higher switching frequency allows the using of the smaller inductor and the capacitor values. The inductor saturation current should be higher than the load current (I_{LOAD}) plus half of the ripple current (I_{Ripple}):

$$I_{SAT} \geq I_{LOAD} + \frac{1}{2} \times I_{Ripple}$$

The inductor ripple current depends on the input voltage (V_{IN}), the duty cycle (D = V_{OUT}/V_{IN}), the switching frequency (F_{SW}) and the inductance (L):

$$I_{Ripple} = \frac{V_{IN} \times D \times (1-D)}{F_{SW} \times L}$$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. Usually the inductor ripple is designed in the range of (20-40%) maximum charging current as a trade-off between the inductor size and efficiency for a practical design.

Output Capacitor Selection

The output capacitor in parallel with the battery is used for absorbing the high frequency switching ripple current and smoothing the output voltage. The RMS value of the output ripple current I_{RMS} is calculated as follow:

$$I_{RMS} = \frac{V_{IN} \times D \times (1-D)}{\sqrt{12} L \times F_{SW}}$$

Where the duty cycle D is the ratio of the output voltage (battery voltage) over the input voltage for CCM mode which is the typical operation for the battery charger. During the battery charge period, the battery voltage varies from its initial battery voltage to the rated voltage. A typical 10μF ceramic capacitor is a good choice to absorb this current and also has a very small size.

Input Capacitor Selection

The input capacitor absorbs input ripple current from the Buck converter, which is given by the below equation:

$$I_{RMS} = \frac{I_{LOAD} \times \sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

This RMS ripple current must be smaller than the rated RMS current in the capacitor datasheet. At the same time, the input capacitor is also as the output capacitor when Boost works. At this condition, the input capacitor can be calculated as below:

$$C_{IN} = \frac{I_{BUS} \times (V_{BUS} - V_{BAT})}{F_{SW} \times V_{BUS} \times V_{RIPPLE}}$$

Usually V_{RIPPLE} is designed less than 0.5% of the Boost output voltage. A typical 10μF ceramic capacitor is a good choice to absorb this current and also has a very small size. For best performance, VBUS should be decoupled to PGND with 1μF capacitance. The remaining input capacitor should be place on PMID.

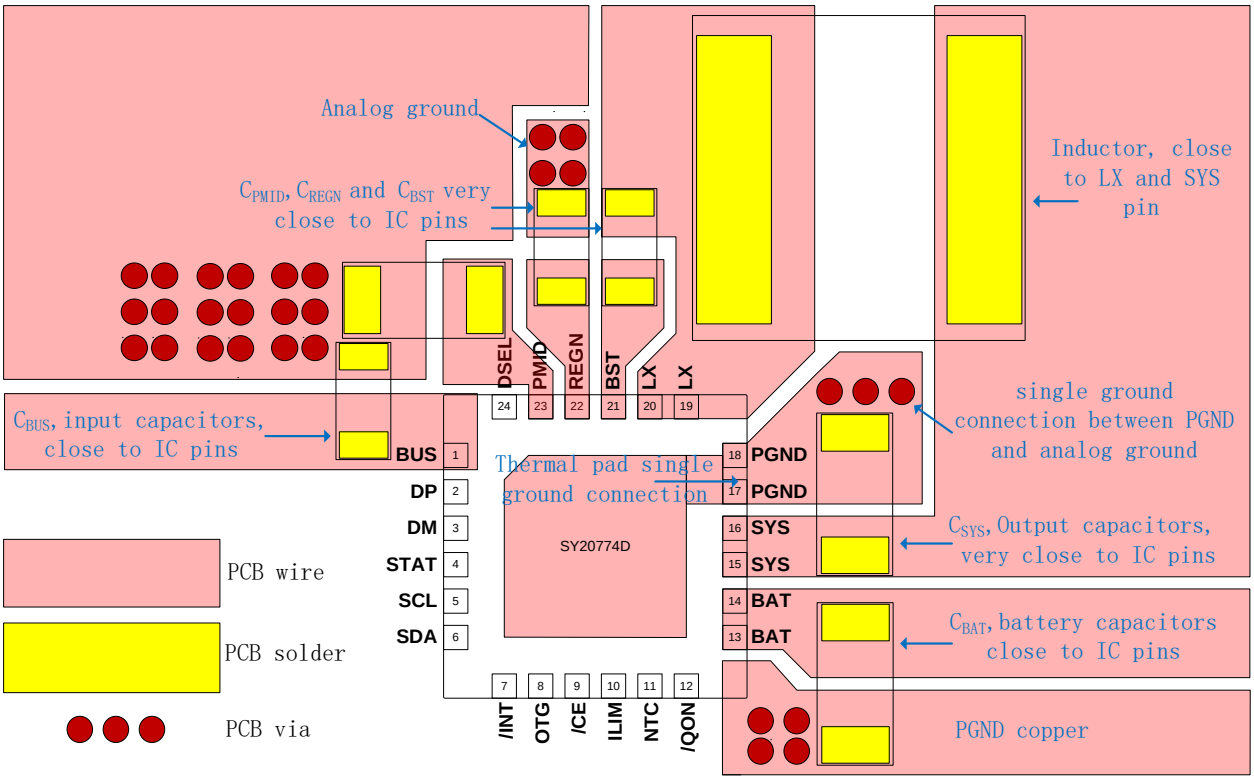
Layout Design

The layout design of the SY20774D regulator is relatively simple. For the best efficiency and to minimize noise problems, we should place the following components close to the IC: C_{PMID}, C_{REGN}, C_{BST}, C_{SYS} and C_{BAT}.

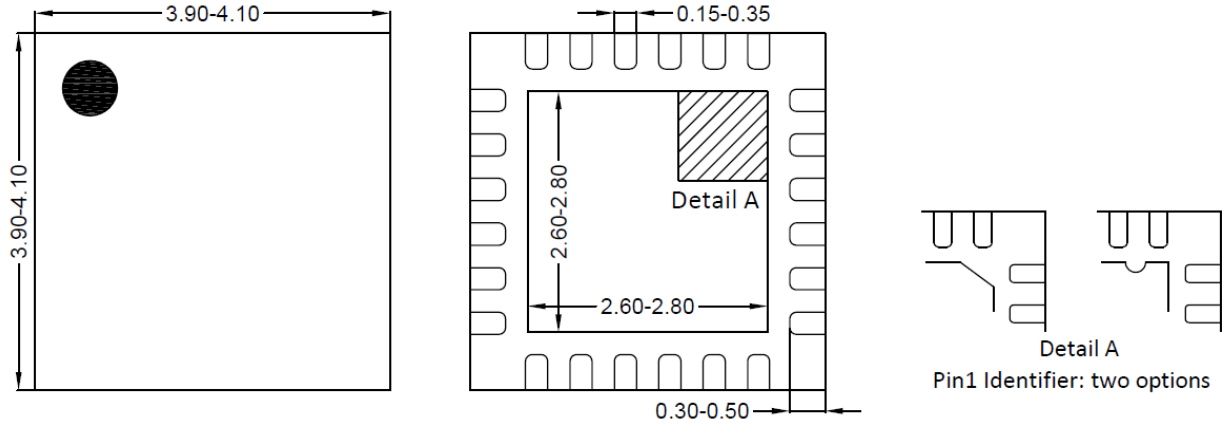
1) It is desirable to maximize the PCB copper area adjacent to PGND pin to achieve the best thermal and noise performance. If the board space allows, a ground plane is highly desirable.

2) C_{PMID}, C_{REGN}, C_{BST}, C_{SYS} and C_{BAT} must be close to the IC.

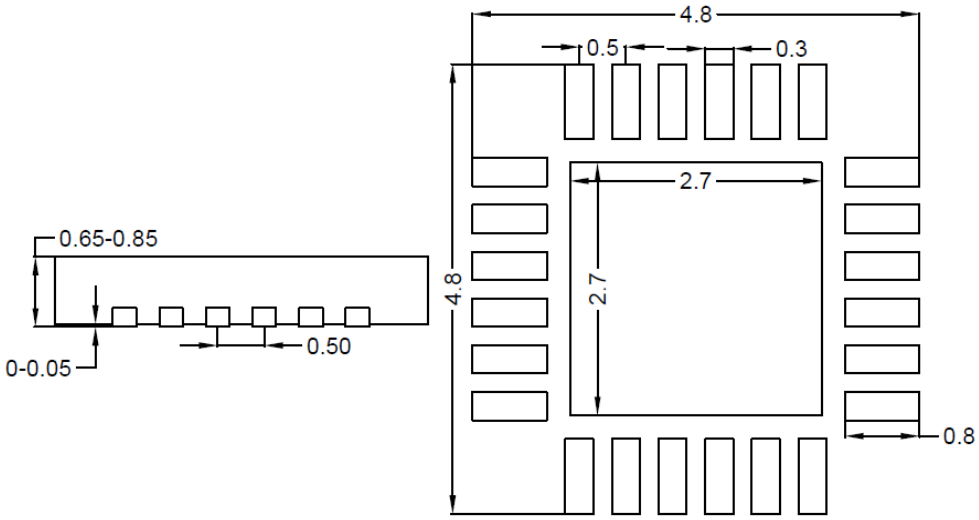
3) The loop area formed by C_{PMID} and PGND must be minimized. The PCB copper area adjacent to LX pin must be minimized to avoid the potential noise problem. The following picture is the recommended layout design of LX, C_{PMID}, C_{REGN}, C_{BST}, C_{SYS} and C_{BAT}.



QFN4×4-24 Package outline & PCB Layout



Top View **Bottom View**

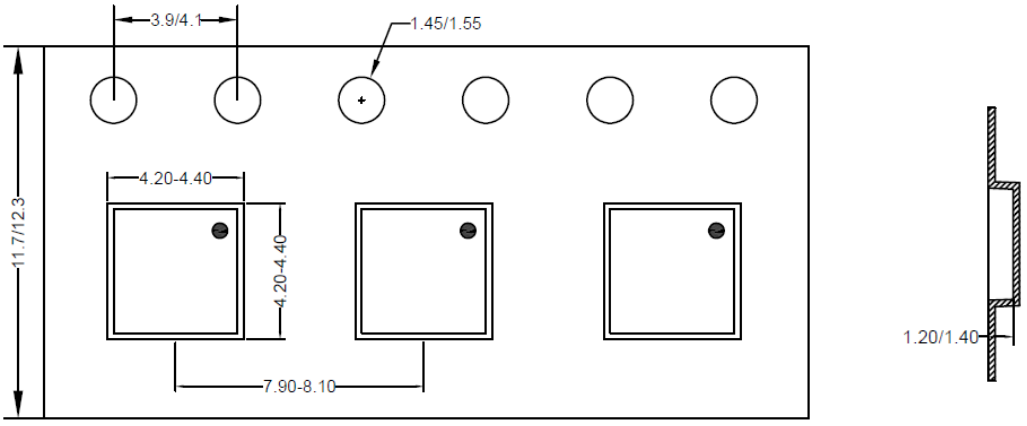


Front View **PCB layout (Recommended)**

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

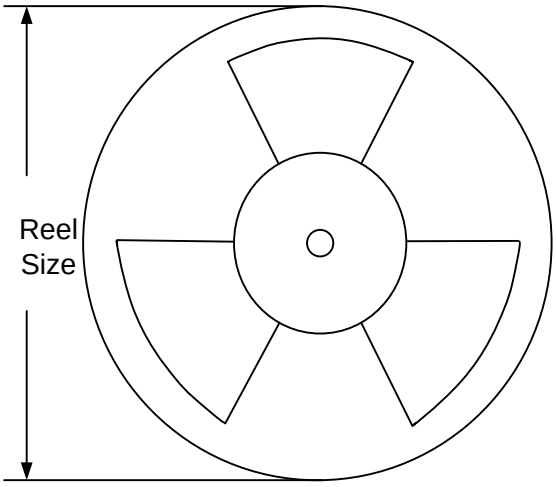
Taping & Reel Specification

1. QFN4x4 taping orientation



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel (pcs)
QFN4x4	12	8	13"	400	400	5000

3. Others: NA

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