SY7T612+U3 / SY7T612+I3

Single-Phase, Three-Outlet, Energy Measurement IC

General Description

The SY7T612 is an energy measurement processor (EMP), in a 32QFN package, designed specifically for BOM optimized applications such as smart-plugs, smart appliances, lighting and home/building automation.

The analog front end (AFE) provides configurable analog inputs for interfacing to current sensors and voltage sensors respectively. Scaled voltages from the sensors are fed to a high-resolution delta-sigma converter. A low power 24-bit energy measurement processor (EMP) with embedded firmware performs all the necessary computation, compensation, and data formatting for interfacing to any host controller. With integrated flash memory for storing nonvolatile data such as calibration coefficients and input configuration settings, the device provides an autonomous solution that simplifies system integration.

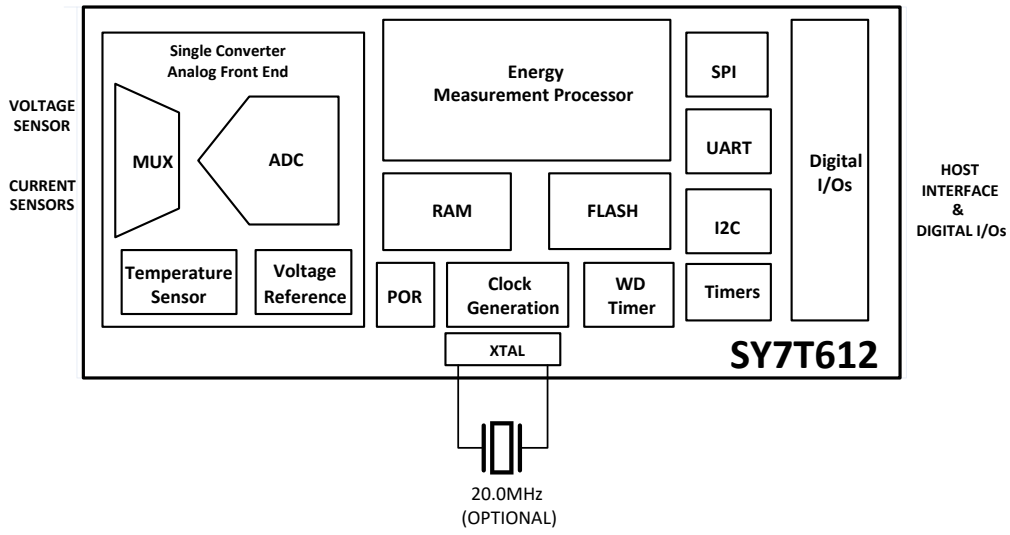
This document describes the SY7T612+U3/I3 solutions, designed for single-phase applications with energy measurement of up to three outlets.

Features

- Small 32-pin QFN Package
- High Resolution Delta-Sigma ADC with Configurable Analog Inputs for Sampling One Voltage and Four Current Sensor Signals.
- Precision Internal Voltage and Timing References Minimize External Components
- 24-Bit Energy Measurement Processor
- SPI, UART, I^2C Host Interface Options
- Configurable DIOs for Alarm Signaling, Relay Control, Address Pins, Energy Pulse Output, or User Control.
- Nonvolatile Storage of Calibration and Configuration Data.
- Provision for Optional External 20MHz Crystal.

Applications

- Metered Power Distribution Units (PDUs)
- Distribution Panels
- Power-Strips
- Smart Appliances



Ordering Information

Ordering Number	Carrier Type	Host Interface	Temperature Range	Package	Top Marking (1)	Firmware Revision
SY7T612B+U3/A0	Tray (Bulk)	UART/SPI	-40℃ to +85℃	TQFN-32	BNExyz	0xA36506
SY7T612T+U3/A0	Tape & Reel					
SY7T612B+I3/A0	Tray (Bulk)	I^2C/SPI	-40℃ to +85℃	TQFN-32	BNExyz	0xAB6506
SY7T612T+I3/A0	Tape & Reel					

Pinout (top view)

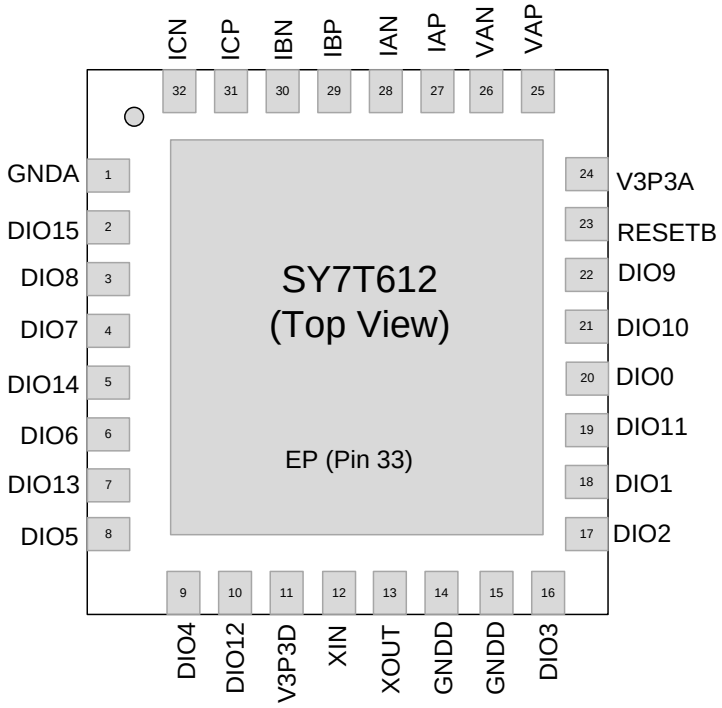


Table 1. SY7T612+U3/I3 Pin Description/Assignment

Pin Number	Pin Name	Pin Description / Assignment
1	GNDA	Ground (Analog)
2	DIO15	Digital I/O
3	DIO8	Digital I/O, Interface Select (1)
4	DIO7	Digital I/O
5	DIO14	Digital I/O
6	DIO6	Digital I/O, ADDRSEL0
7	DIO13	Digital I/O
8	DIO5	Digital I/O, SPI SSB, UART TXEN, SCL(1)
9	DIO12	Digital I/O
10	DIO4	Digital I/O
11	V3P3D	3.3VDC Supply (Digital)
12	XIN	Crystal Oscillator Input
13	XOUT	Crystal Oscillator Output
14	GNDD	Ground (Digital)
15	GNDD	Ground (Digital)
16	DIO3	Digital I/O, SPI MISO, UART TX, SDAo(1)
17	DIO2	Digital I/O, SPI MOSI, UART RX, SDAi(1)

Table 1 (Cont.). SY7T612+U3/I3 Pin Description

18	DIO1	Digital I/O, SPI SCK(1), ADDRSEL1
19	DIO11	Digital I/O
20	DIO0	Digital I/O
21	DIO10	Digital I/O
22	DIO9	Digital I/O
23	RESETB	Reset Input (Active Low)
24	V3P3A	3.3VDC Supply (Analog)
25	VAP	Voltage Sensor Input (pos)
26	VAN	Voltage Sensor Input (neg)
27	IAP	Channel A Current Sensor Input (pos)
28	IAN	Channel A Current Sensor Input (neg)
29	IBP	Channel B Current Sensor Input (pos)
30	IBN	Channel B Current Sensor Input (neg)
31	ICP	Channel C Current Sensor Input (pos)
32	ICN	Channel C Current Sensor Input (neg)
33	EP	Thermal Pad - Tie to GND (Optional) (2)

Note 1: For SY7T612+U3, SPI or UART mode is selected at device startup based upon sampled DIO8. For SY7T612+I3, SPI or I^2C mode is selected at device startup based upon sampled DIO8. See DIO section for details.

Note 2: The exposed thermal pad is connected to the device substrate. It can be connected to GND, however it cannot be used to replace the GND connection. The GND must be connected through GNDD (digital) and GNDA (analog) ground pins.

Block Diagram

The SY7T612 hardware integrates all the functional blocks required for solid-state power and energy measurement. Only a few external resistors and capacitors are required. Included on the device are:

- Temperature compensated oscillator and clock management logic
- Integrated power-on reset and watchdog timer
- High-accuracy analog front-end (AFE) with trimmed voltage reference and temperature sensor
- 24-bit energy measurement processor with RAM and flash memory
- Peripheral interfaces (UART, I^2C or SPI) and Digital I/O pins – *usage varies with firmware*

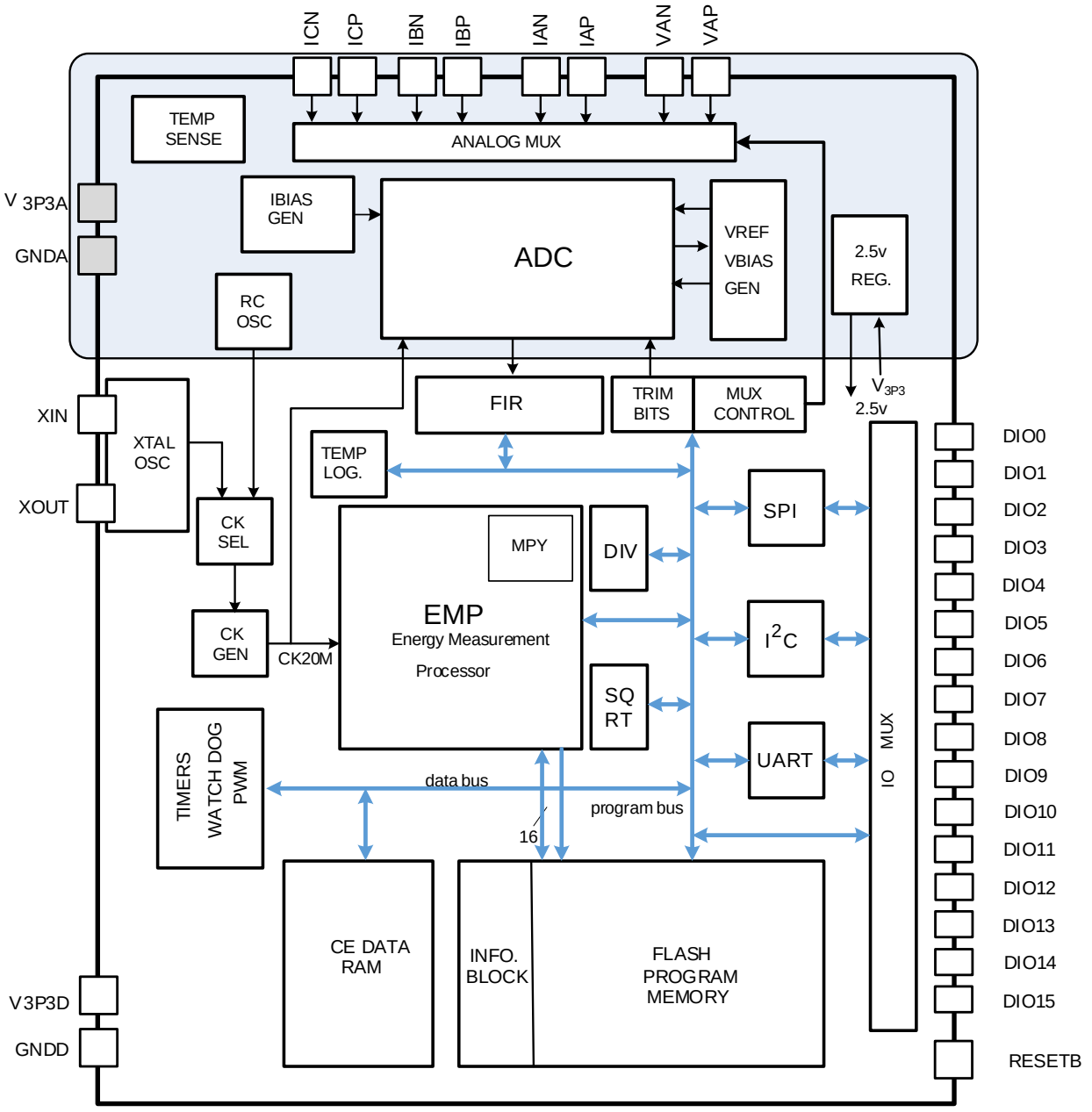


Figure 1. SY7T612+U3/I3 Functional Block Diagram

Electrical Specifications

Absolute Maximum Ratings

Supplies and Ground Pins:	
V_{3P3D}, V_{3P3A}	-0.5V to 4.6V
GNDD, GNDA	-0.5V to +0.5V
Analog Input Pins:	
AIN1N, AIN1P, AIN2N, AIN2P, AIN3N, AIN3P, AIN4N, AIN4P	-10mA to +10mA -0.5V to (V_{3P3} + 0.5V)
Digital Pins:	
DIO15, DIO14, DIO13, DIO12, DIO11, DIO10, DIO9, DIO8, DIO7, DIO6, DIO5, DIO4, DIO3, DIO2, DIO1, DIO0	-30mA to +30mA, -0.5V to (V_{3P3D}+ 0.5V)
Temperatures:	
Operating Junction Temperature (peak, 100ms)	+140 ℃
Operating Junction Temperature (continuous)	+125 ℃
Storage Temperature	-45 ℃ to +165 ℃
Soldering Temperature (10-second duration)	+250 ℃
ESD Stress on All Pins	±4kV

Stresses beyond Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND.

Recommended Operating Conditions

Parameter	Condition	Min	Typ	Max	Unit
3.3V Supply Voltage (V_{3P3})	Normal Operation	3.0	3.3	3.6	V
Operating Temperature		-40	–	+85	℃

Performance Specifications

Production tests are performed at room temperature.

Input Logic Levels

Parameter	Condition	Min	Typ	Max	Unit
Digital high-level input voltage, V_{IH}		2	–	–	V
Digital low-level input voltage, V_{IL}		–	–	0.8	V

Output Logic Levels

Parameter	Condition	Min	Typ	Max	Unit
Digital high-level output voltage V_{OH}	I_{LOAD} = 1 mA	V_{3P3} –0.4	–	–	V
	I_{LOAD} = 10 mA	V_{3P3}- 0.6	–	–	V
Digital low-level output voltage V_{OL}	I_{LOAD} = 1 mA	0	–	0.4	V
	I_{LOAD} = 10 mA	–	–	0.5	V

Supply Current

Parameter	Condition	Min	Typ	Max	Unit
V_{3P3D} and V_{3P3A} current (compounded)	Normal Operation, V3P=3.3V	–	8.1	10.3	mA

Internal RC Oscillator

Parameter	Condition	Min	Typ	Max	Unit
Nominal Frequency	V3P=3.3V, 25℃	–	20.000	–	MHz
Accuracy		–	±1.5	–	%

ADC Converter, V3P3 Referenced

LSB values do not include the 9-bit left shift at processor input.

Parameter	Condition	Min	Typ	Max	Unit
Usable Input Range (Vin-V_{3P3})		-250	–	250	mV peak
THD (First 10 harmonics)	Vin=65Hz, 64kpts FFT, Blackman-Harris window	–	-85	–	dB
Input Impedance	Vin=65Hz	30	–	90	kΩ
Temperature coefficient of Input Impedance	Vin=65Hz	–	1.7[1]	–	Ω/°C
ADC Gain Error vs %Power Supply Variation $\frac{10^6\,\Delta Nout_{PK}\,357\,nV/V_{IN}}{100\,\Delta V3P3A/3.3}$	Vin=200mVpk, 65Hz V_{3P3}=3.0V, 3.6V	–	–	50	ppm/%
Input Offset (Vin-V_{3P3})		-10		10	mV

Note 1: Guaranteed by design, not subject to test.

Timing Specifications

SPI Slave Port

Parameter		Condition	Min	Typ	Max	Unit
t_{SPIcyc}	SPCK cycle time		1	–	–	μs
$t_{SPILead}$	Enable lead time		15	–	–	ns
t_{SPILag}	Enable lag time		0	–	–	ns
t_{SPIW}	SPCK pulse width: High Low		 250 250	–	–	 ns ns
t_{SPISCK}	SSB to first SPCK fall	Ignore if SPCK is low when SSB falls.	–	2[1]	–	ns
t_{SPIDIS}	Disable time		–	0[1]	–	ns
t_{SPIEV}	SPCK to Data Out (MISO)			–	25	ns
t_{SPISU}	Data input setup time (MOSI)		10	–	–	ns
t_{SPIH}	Data input hold time (MOSI)		5	–	–	ns

Note 1: Guaranteed by design, not subject to test.

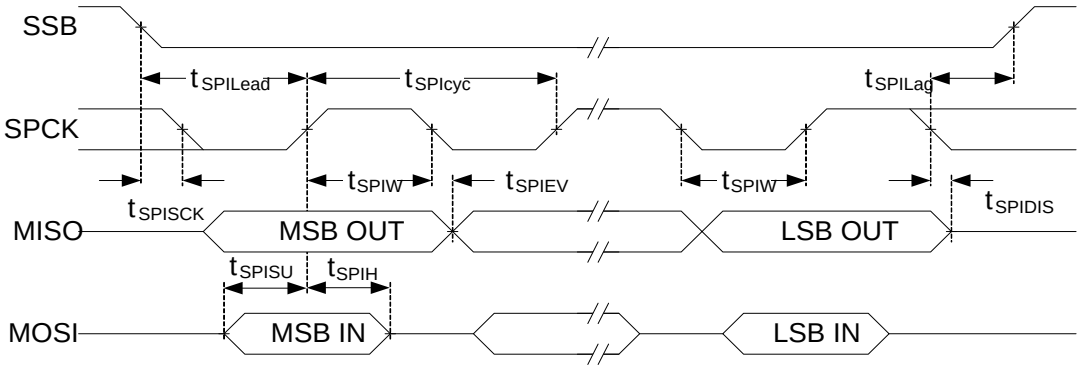


Figure 2. SPI Slave Port Timing

I²C Slave Port

I²C Slave Port Timing[2]

Parameter	Condition	Min	Typ	Max	Unit
t_{BUF} Bus Idle (Free) time between transmissions (STOP/START)		1500	-	–	ns
t_{ICF} I²C input Fall Time		20[1]	–	300	ns
t_{ICR} I²C input Rise Time		20[1]	–	300	ns
t_{STH} I²C START or repeated START condition hold time		500	–	–	ns
t_{STS} I²C START or repeated START condition setup time		600	–	–	ns
t_{SCH} I²C clock high time		600	–	–	ns
t_{SCL} I²C clock low time		1300	–	–	ns
t_{SDS} I²C serial data setup time		100	–	–	ns
t_{SDH} I²C serial data hold time		10	–	–	ns
t_{VDA} I²C Valid data time: - SCL low to SDA output valid - ACK signal from SCL low to SDA (out) low		–	–	900	ns

Note 1: Dependent on bus capacitance.

Note 2: Guaranteed by design, not subject to test.

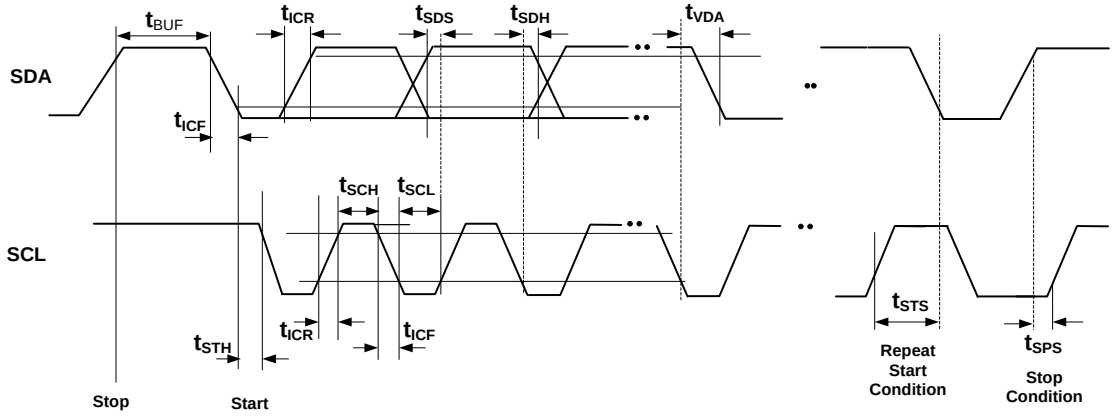


Figure 3. I²C Port Timing

Hardware Resources Overview

Power-On Reset (POR)

An on-chip Power-On Reset (POR) block monitors the supply voltage (V_{3P3D}) and initializes the internal digital circuitry at power-on. Once V_{3P3D} is above the minimum operating threshold, the POR circuit triggers and initiates a reset sequence. It will also issue a reset to the digital circuitry if the supply voltage falls below the minimum operating level.

Watchdog Timer (WDT)

A Watchdog Timer (WDT) block detects any software processing errors. The embedded software periodically refreshes the free-running watchdog timer to prevent it from timing out. If the WDT times out, it is an indication that software is no longer being executed in the intended sequence; thus, a system reset is initiated.

External Reset Pin (RESETB Pin)

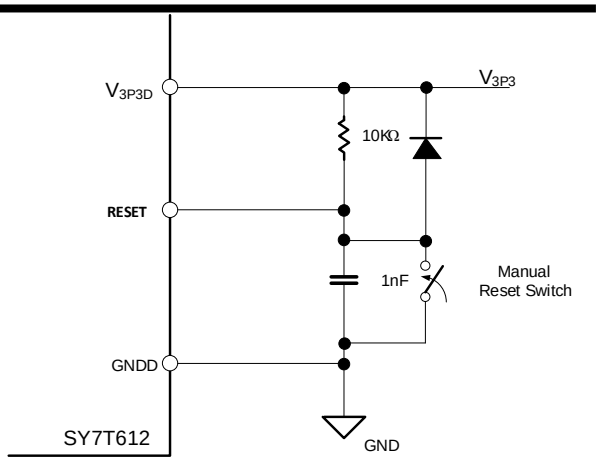
In addition to the internal reset sources, a reset can be forced by applying a low level to the RESETB pin.

If the RESETB pin is pulled low, all digital activities in the device stop, except the clock management circuitry and oscillators, which continue to run. The external reset input is filtered to prevent spurious reset events in noisy environments. The reset does not occur until RESETB has been held low for at least 1 μs.

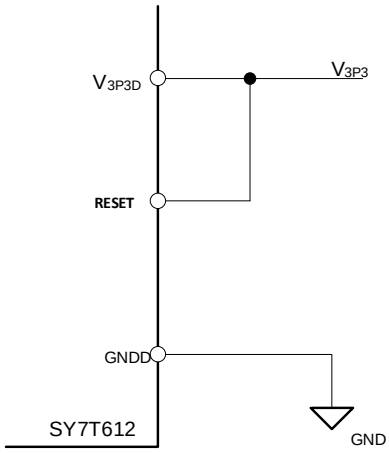
Once initiated, the reset mode persists until the RESETB is set high and the reset timer times out (4096 clock cycles). At the completion of the reset sequence, the internal reset is released and the processor (EMP) begins executing from address 0.

RESETB pin can be driven by a host processor or connected to a pushbutton as indicated in Figure 4.

If not used, the RESETB pin can be connected either directly or through a pull-up resistor to V_{3P3D} supply.



a) RESETB External Connection Example



b) Unused RESETB Connection Example

Figure 4. Reset Pin Connections Examples

Clock Management

The SY7T612 integrates a trimmed and temperature compensated RC oscillator. The device also includes the circuitry to handle an external crystal or ceramic resonator. The clock management unit of the SY7T612 automatically handles the clock sources logic and distributes the clock to the rest of the device.

Upon reset or power-on, the SY7T612 starts up on the internal RC oscillator. After 1024 clock cycles of the internal RC oscillator, the clock management logic will switch to the external 20MHz clock (if available), allowing the external crystal an adequate start-up time. If no valid external clock is detected,
the clock management logic will keep clocking the device using the internal RC oscillator. If the device is normally clocked using the external 20MHz crystal, the clock management logic continuously monitors the status of the clock. The clock management logic

of the SY7T612 will automatically switch to the internal oscillator in the event of a failure of the external oscillator.

The internal RC oscillator is factory-trimmed and temperature-compensated. It provides an accurate clock source, however for applications requiring highest accuracy of the time-based measurements (i.e. line frequency, energy, etc.), the use of an external crystal is recommended.

The SY7T612 external clock circuitry requires a 20.000MHz crystal. The circuitry includes two 18pF ceramic capacitors. Figure 5 shows the typical connection of the external crystal. This oscillator is self-biasing and therefore an external resistor should NOT be connected across the crystal.

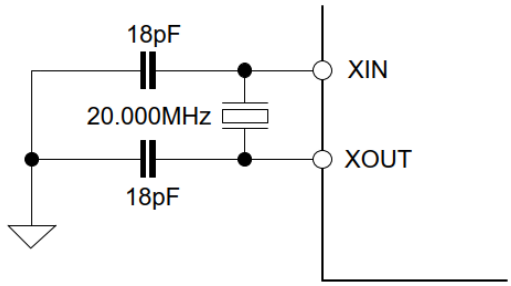


Figure 5. XTAL Connection

Alternatively, an external clock signal can be utilized instead of the crystal. In this case, the external clock should be connected to the XOUT pin while the XIN pin should be connected to GNDD.

If the external crystal is not utilized (not mounted), the XOUT pin should be connected to GNDD and the XIN pin left unconnected.

Analog Front-End and Conversion

The SY7T612's Analog Front-End (AFE) includes an input multiplexer, delta-sigma A/D converter, voltage reference, bias current reference, temperature sensor, voltage fault comparators, and POR circuitry.

Delta-Sigma A/D Converter

A second-order delta-sigma converter digitizes the analog inputs. The converted data is then filtered and decimated through a FIR filter.

Voltage Reference

The device includes an on-chip precision bandgap voltage reference that incorporates auto-zero techniques as well as production trims to minimize errors caused by component mismatch and drift. The voltage reference is digitally compensated over temperature.

Die Temperature Measurement

The device includes an on-chip die temperature sensor used for digital compensation of the voltage reference. It is also used to report temperature information to the user.

Voltage and Current Inputs

The external voltage and current sensors are connected to analog input pins. The full-scale signal level that can be applied to the voltage input pins is V3P3A ±250 mVpk. With a sinusoidal waveform, the maximum RMS voltage is:

$$Vrms(MAX) = \frac{250mVpk}{\sqrt[2]{2}} = 176.78mVRMS$$

A common-mode voltage of less than ±25 mV is recommended in order to fully utilize the available dynamic range.

Energy Measurement Processor

The SY7T612 integrates a dedicated 24-bit processor that performs all the digital signal processing necessary for measurement, calibration, compensation, analysis, alarms generation, relay control, etc.

Flash and RAM

The SY7T612 includes on-chip flash memory for storing program code, coefficients, calibration data, and configuration settings. The SY7T612 also includes on-chip RAM which is used to store the values of input and output registers and utilized by the firmware for its operations.

Digital I/O

The SY7T612 features 16 general purpose digital I/Os. The digital I/Os are either managed directly by the user, by the embedded firmware, or multiplexed with the serial communication interfaces. The device also includes the necessary hardware to generate free-running PWM signals at either DIO7 or DIO8 with configurable period and pulse width (PWM functionality is not supported in this firmware revision). The following table summarizes the multiplexing and pin assignment on the SY7T612.

Table 2. Digital I/O Assignments

Pin Name	Pin #	Function at Power-On Reset	Function by Interface		
			SPI	UART	I²C
DIO15	2	--	DIO15		
DIO14	5	--	DIO14/RelayOutC0(1)		
DIO13	7	--	DIO13/RelayOutC1		
DIO12	10	--	DIO12/RelayOutB0		
DIO11	19	--	DIO11/RelayOutB1		
DIO10	21	--	DIO10/RelayOutA0		
DIO9	22	--	DIO9/RelayOutA1		
DIO8	3	Interface Selection	DIO8/ALARM1		
DIO7	4	--	DIO7/ALARM0		
DIO6	6	ADDRSEL0	DIO6/PULSE		
DIO5	8	--	SSB	DIO5/DIR	SCL
DIO4	9	--	DIO4		
DIO3	16	--	MISO	TX	SDAo
DIO2	17	--	MOSI	RX	SDAi
DIO1	18	ADDRSEL1	SCK	DIO1	
DIO0	20	--	DIO0		

Note 1: Relay outputs can be configured (assigned to different DIO pins, for single and dual coil relays) and unused relay outputs can be used as general purpose DIOs.

Warning: Where applicable, pins should be configured via pull-up and pull-down resistors as these pins could become outputs after initialization. Therefore, direct connection to GNDD/GNDA or V3P3D/V3P3A supplies must be avoided.

Serial Interfaces

The SY7T612 provides UART, I²C, and SPI interface options, but only one interface can be active at a time. In the SY7T612+U3 solution, pin DIO8 is sampled following a power-on reset to select between SPI or UART interface.
In the SY7T612+I3 solution, pin DIO8 is sampled following a power-on reset to select between SPI or I²C interface.
The user should allow at least 10ms from a power-on reset event for the selection pin status to be latched and the serial interface selected. During this time the status of DIO8 must not change.

Selected Interface	DIO8
SPI	**0**
UART (SY7T612+U3) Or **I²C** (SY7T612+I3)	**1**

UART Interface

The SY7T612 features a UART interface with a data rate ranging from 2400 up to 115k Baud. The UART interface has a fixed configuration supporting: 8-bit, one start bit, one stop bit and no-parity. The UART interface hardware does not provide handshaking hardware signals (i.e. RTS, CTS etc.).
Once the UART interface is activated, it utilizes the following digital I/Os:

- **DIO3**: Transmit (TX) output
- **DIO2**: Receive (RX) input.
- **DIO5**: Optional (DIR) output, to drive a RS-485 transceiver's direction pin

The communication protocol is described in the UART Protocol Description (SY7T612+U3) section.

The UART clock is derived from the 20MHz system clock. The error due to the clock division is reported in the following Table.

Table 3. UART Baud Rate Error

Baud Rate	Actual Baud Rate	Error [percent]
2400	2399.808	0.008
4800	4800.768	0.016
9600	9596.929	-0.032
19200	19193.858	-0.032
38400	38461.538	0.160
57600	57541.264	-0.223
115200	114942.529	-0.223

SPI Interface

The SPI featured in the SY7T612 is slave only. Once the SPI interface is activated, it utilizes the following digital I/O as the SPI interface:

- **DIO5**: Slave select (SSB) is an active low input.

- **DIO1**: Serial Data Clock (SCK) input.
- **DIO3**: Master Input, Slave Output (MISO), serial data output.
- **DIO2**: Master Output, Slave Input (MOSI), serial data input.

The SPI interface allows read and write accesses to the data RAM specified in the command bit field ADDR [5:0]. The command limits the access to RAM locations 0x00 through 0x3F. Refer to the SPI Indirect Access Protocol Description section for details on accessing other RAM locations.

SPI Mode

The device operates in mode 3 (CPOL=1, CPHA=1) and as such the data is captured on the rising edge and propagated on the falling edge of the serial data clock (SCK). The figure below shows a single-byte transaction on the SPI bus. Bytes are transmitted/received MSB first.

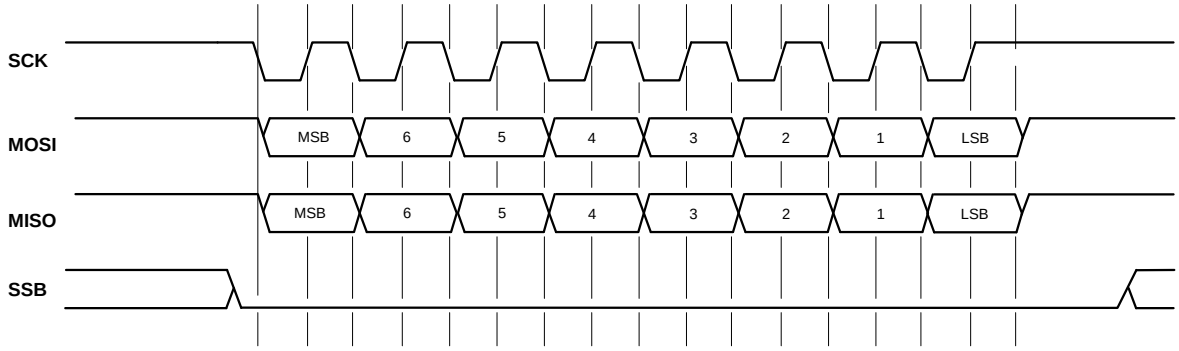


Figure 6. Signal Timing on the SPI Bus (Single Byte Transaction)

Single Word SPI Reads

The device supplies direct read access to the device RAM memory. To read the RAM the master device must send a read command to the slave device and then clock out the resulting read data. SSB must be kept active low for the entire read transaction (command and response). SCK may be interrupted as long as SSB remains low. ADDR [5:0] is filled with the word address of the read transaction. RAM data contents are transmitted most significant byte first. ADDR [5:0] cannot exceed 0x3F. RAM words, and therefore the results, are natively 24 bits (3 bytes) long.

Table 4: Single-Word Read Command (MOSI)

Byte #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0		ADDR[5:0]					0x0	
1		0						
2		0						
3		0						

The slave responds with the data contents of the requested RAM addresses.

Table 5: Single-Word Read Response (MISO)

Byte #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Hi-Z (during Read Command)							
1	DATA[23:16] @ ADDR							
2	DATA[15:8] @ ADDR							
3	DATA[7:0] @ ADDR							

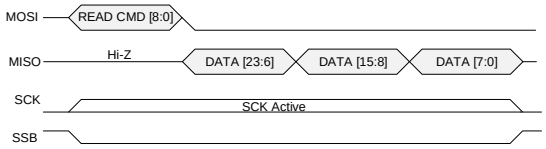


Figure 7. Single Word Read Access Timing

Single Word SPI Writes

The device supplies direct write access to the device RAM memory. To write the RAM the master device must send a write command to the slave device and then clock out the write data. SSB must be kept active low for the entire write transaction (command and data). SCK may be interrupted as long as SSB

remains low. ADDR [5:0] is filled with the word address of the write transaction. RAM data contents are transmitted most significant byte first. ADDR [5:0] cannot exceed 0x3F. RAM words are natively 24 bits (3 bytes) long.

Table 6: Single-Word Write Command (MOSI)

Byte #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	ADDR[5:0]						0x02	
1	DATA[23:16] @ ADDR							
2	DATA[15:8] @ ADDR							
3	DATA[7:0] @ ADDR							

The slave SDO remains Hi-Z during a write access.

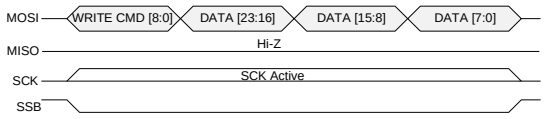


Figure 8. Single Word Write Access Timing

I²C Interface

The SY7T612+U3/I3 has an I²C interface available at the DIO2, DIO3, and DIO5 pins. The interface supports I²C slave mode with a 7-bit address and operates at a data rate up to 400kHz (Fast-mode).

The SY7T612 has separate SD (serial data) input and output pins to allow the use of digital isolators/opto-couplers to isolate the serial bus. The configuration in Figure 9 (standard) has the I²C data pins (SDAi and SDAo) shorted.

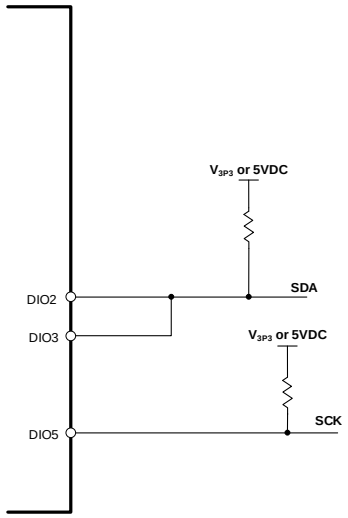


Figure 9: I²C Bus Connection (Standard Configuration)

It is possible to isolate the I²C interface utilizing the configuration indicated in Figure 10. In this case the bus is isolated using optocouplers (any other open drain isolator type can be used).

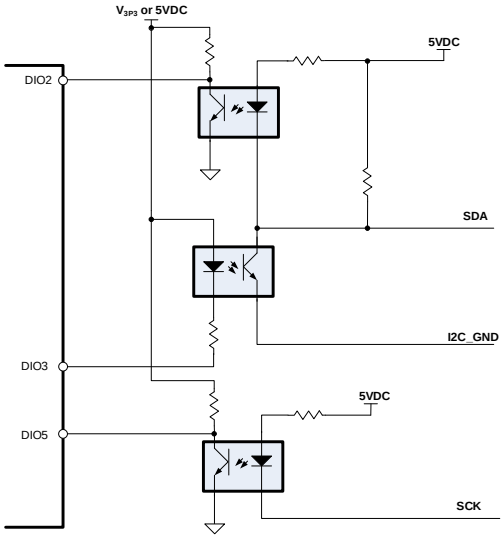


Figure 10: I²C Bus Connection (Isolated Configuration)

The I²C interface allows access to read and write registers contained in a 256-word (24-bit) area of the on-chip RAM.
The Register Map section contains the address and assignment of each register.

Bus Characteristics

- A data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Bus Conditions

- **Bus not Busy (I):** Both data and clock lines are HIGH indicating an Idle Condition.
- **Start Data Transfer (S):** a HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.
- **Stop Data Transfer (P):** a LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

- **Data Valid:** The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition.
- **Acknowledge (A):** Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse, which is associated with this Acknowledge bit. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by not generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave SY7T612 will leave the data line HIGH to enable the master to generate the STOP condition.

-

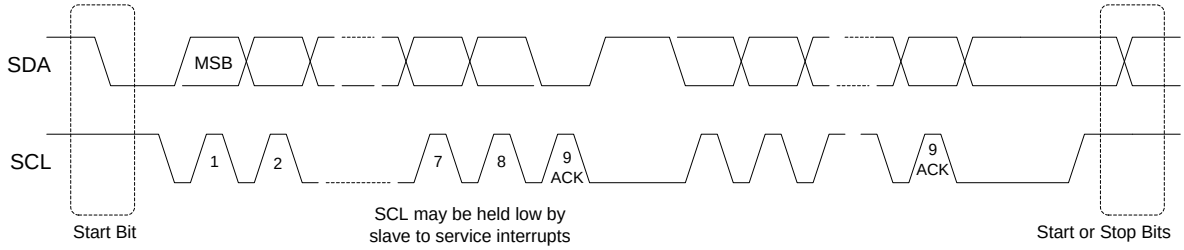
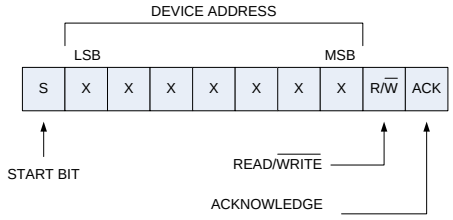


Figure 11: I²C Bus Conditions

Device Addressing



The control byte consists of a seven-bit address and a bit (LSB) indicating the type of access (0=write; 1=read).

Write Operations

Following the START (S) condition from the master, the device address (7-bits) and the R/W bit (logic low for write) are clocked onto the bus by the master. This indicates to the addressed slave receiver that the register address will follow after it has generated an acknowledge bit (A) during the ninth clock cycle.
Therefore, the next byte transmitted by the master is the register address and will be written into the address pointer of the SY7T612. After receiving another acknowledge (A) signal from the 78M6610+PSU the master device will transmit the data byte(s) to be written into the addressed memory location. The data transfer ends when the master generates a STOP (P) condition. This initiates the internal write cycle. The example in Figure 12 shows a 3-byte data write (24-bit register write).
Upon receiving a STOP (P) condition, the internal register address pointer will be incremented.
The write access can be extended to multiple sequential registers. Figure 13 shows a transaction where multiple register are written sequentially.

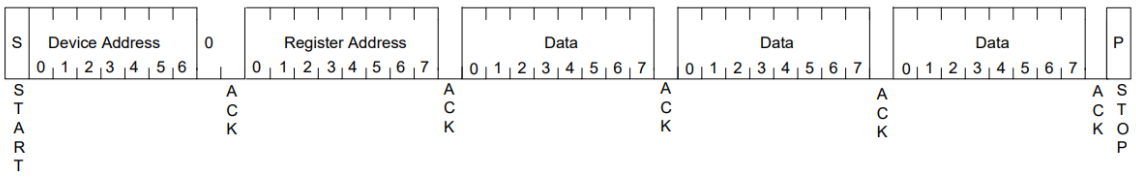


Figure 12: I²C Bus 3-byte Data Write

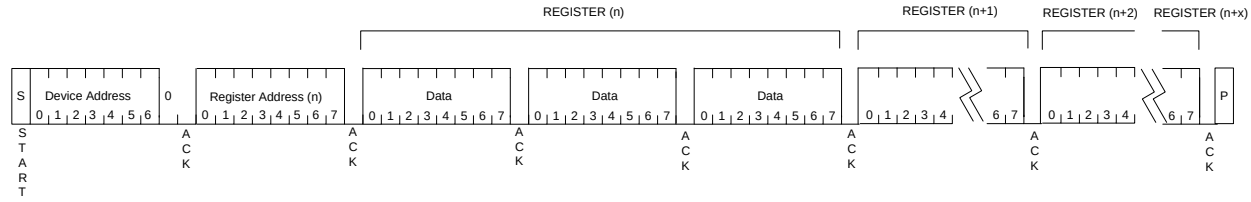


Figure 13: I²C Bus Multiple Sequential Register Write

Read Operations

Read operations are initiated in the same way as write operations with the exception that the R/W bit of the control byte is set to one. There are two basic types of read operations: current address read and random read.
Current Address Read:
The SY7T612 contains an address counter that maintains the address of the last register accessed, internally incremented by one when the STOP bit is received. Therefore, if the previous read access was to register address n, the next current address read operation would access data from address n + 1.

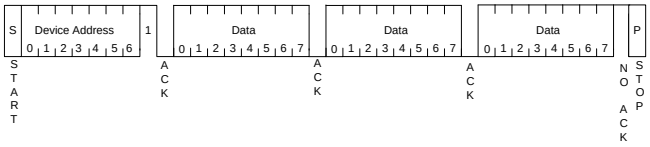


Figure 14: I²C Bus 3-byte Data Read

This read operation is not limited to 3 bytes but can be extended until the register address pointer reaches its maximum value.
If the register address pointer has not been set by previous operations, it is necessary to set it issuing a command as follows:

Upon receipt of the control byte with R/W bit set to one, the SY7T612 issues an acknowledge (A) and transmits the eight-bit data byte. The master will not acknowledge the
Random read operations allow the master to access any register in a random manner. To perform this operation, the register address must be set as part of the write operation. After the address is sent, the master generates a START condition following the acknowledge response. This sequence completes the write operation. The master should issue the control byte again this time, with the R/W bit set to 1 to indicate a read operation. The SY7T612 will issue the acknowledge response and transmit the data.

At the end of the transaction the master will not acknowledge the transfer and generate a STOP condition.
Random read operations are not limited to 3 bytes but can be extended until the register address pointer reaches its maximum value.

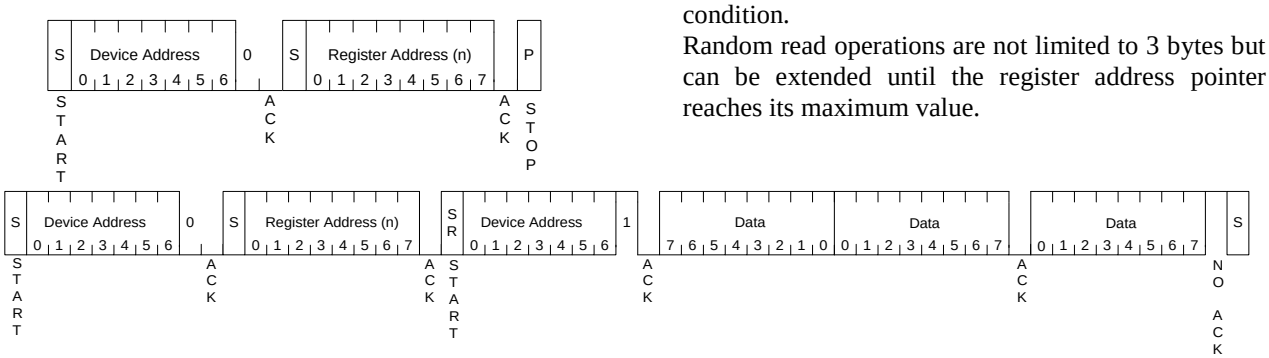


Figure 15: I²C Bus 3-byte Random Data Read

Functional Description

This section describes the operation and configuration of the device, mainly implemented by the embedded FW. It includes the flow of measurement data, relevant calculations, alarm monitoring, I/O control, and user configurations.

Note: For brevity, variables and parameters may be shown as **Ix**, **Px** etc. in this section, instead of the three individual names (**IA, IB, IC)**. The full list is shown in section Register Map.

Measurement Interface

The device incorporates a flexible measurement interface for simplified integration into any single-phase system. This section describes the configuration and signal conditioning of the analog inputs.

Settings and calibration parameters described in this section can be saved to flash memory and automatically initialized upon power on or reset.

AFE Input Multiplexer

The device samples four external sensors with an effective sample rate of 4,010 samples/second (“Fsample”) for each multiplexer slot. Two analog input pins are defined as the common voltage differential input pair for all three phases, and six analog input pins are defined as three pairs of differential current inputs (IA, IB, IC), as shown in Figure 16.

Voltage and Current Inputs Conditioning

The sensor input voltages are digitized using a single integrated second-order delta-sigma A/D converter. The analog front-end includes a temperature sensor whose output is digitized and used for temperature (gain) compensation. Samples are then processed for gain, offset and phase correction as described below and shown in Figure 17

Gain Correction

The device provides individual calibrated gain correction for each of the Voltage and Current sensors as well as common gain correction for the temperature effects on the gain of the ADC.

Offset Correction

The fixed offsets and high-pass filters (HPF) in Figure 3.2 can remove any DC from the signal paths and consequently from power and RMS calculated values. The offset registers (**VA_offs**, **Ix_offs**) are designed to remove any fixed ADC or system. DC offsets can be set by the user, by an automatic calibration routine, or adjusted dynamically by the FW.

Phase Compensation

A phase compensation register is provided to compensate phase errors introduced by current transformers (CT) or external filters. The amount of phase shift is set by the **IA_phasecomp** registers as a fractional number of ADC samples with a total range of -1 to +4 ADC samples (roughly -5 to +20 degrees for a 60Hz line frequency).

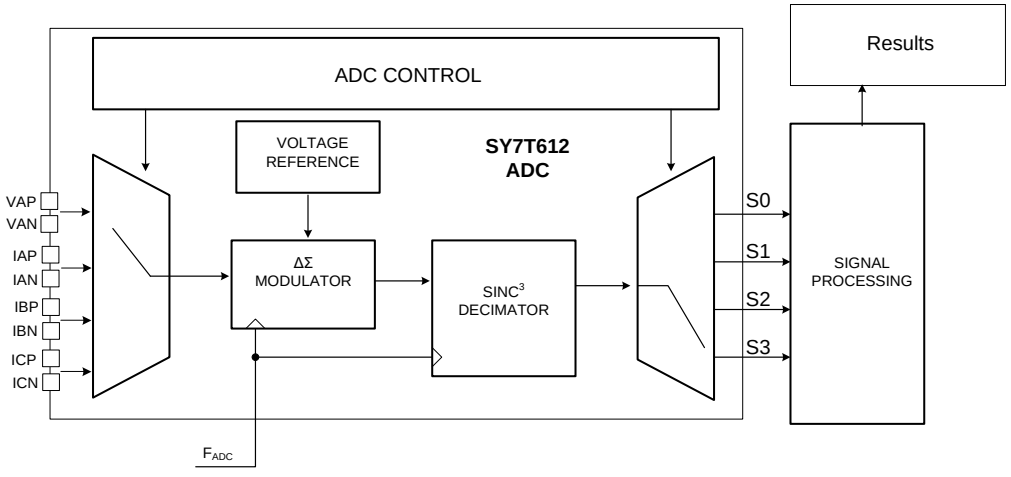


Figure 16. SY7T612 Analog Front-End

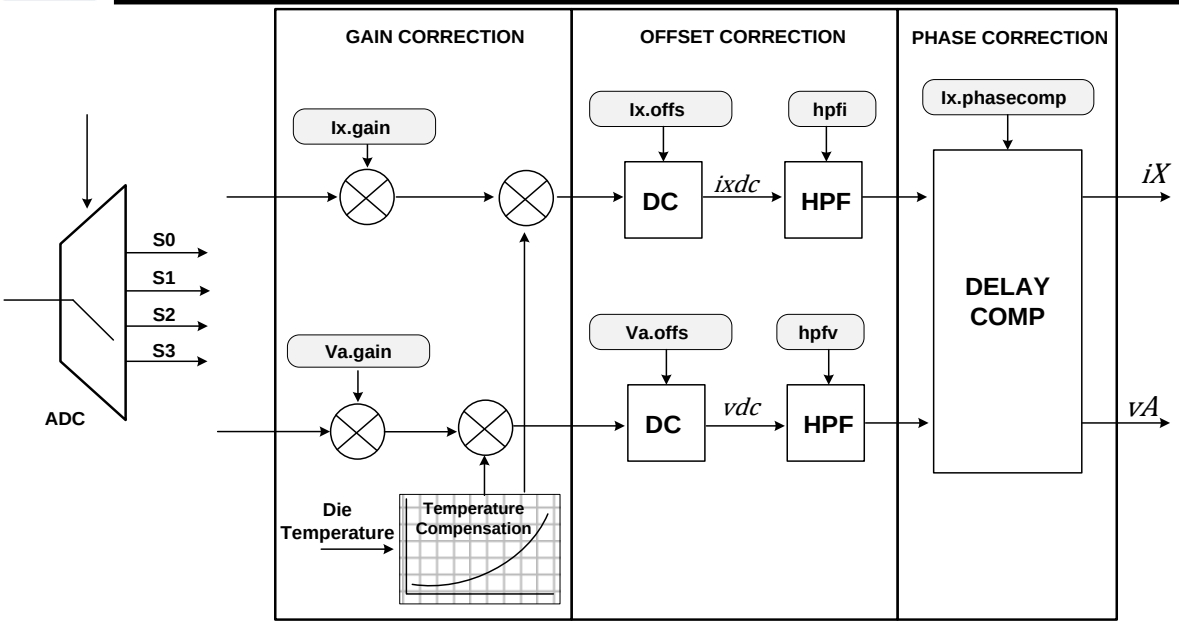


Figure 17: Analog Input Signal Conditioning

Accumulation Interval

The accumulation interval (frame) is the amount of time over which the device calculates and how often the device will update its measurements. The accumulation interval is configurable by the user through the **cycles.MaxSampleCount** ("MaxSampleCount") and **cycles.AccumNumLineCyc** ("AccumNumLineCyc") registers. The **cycles.Divisor** register reports the actual number of samples used within any given accumulation interval. A 48-bit counter **cycles.Frame** reports the number of accumulation intervals that have been processed since the last reset event.

Fixed Interval

When the **AccumNumLineCyc** register is 0 then the device will operate on a fixed time accumulation interval set by the **MaxSampleCount** register. The **MaxSampleCount** register contains an unsigned integer values representing the accumulation interval (time) expressed in number of high-rate samples.

$$\text{Accumulation Interval} = \frac{\text{MaxSampleCount}}{\text{Fsample}}$$

Line Locked Interval

The accumulation interval can also be locked to the incoming line voltage cycles. When the **AccumNumLineCyc** register is set to a non-zero value, the accumulation interval will end after **AccumNumLineCyc** low-to-high zero crossings of the Reference AC Voltage (see Zero-Crossing Detection) unless the maximum accumulation time, set as number of samples in **MaxSampleCount,** has elapsed. This will cause the device to use an accumulation interval of **AccumNumLineCyc** line cycles regardless of the line frequency.

$$\text{Accumulation Interval} = \text{MIN}\left(\frac{AccumNumLineCyc}{\text{Line Frequency}}, \frac{\text{MaxSampleCount}}{\text{Fsample}}\right)$$

Zero-Crossing Detection

The SY7T612+U3/I3 includes a zero-crossing detection feature on the AC input channels. The zero-crossing detection allows measurements and relay operations to be synchronized to the frequency of the incoming waveforms. There is an internal time delay of the zero-crossing detection from the external zero crossing of approximately 3±1 ADC samples (0.5-1.0ms).

The zero-crossing information can be redirected to a Digital I/O pin. The zero-crossing signal is a pulse with a 250 μs width.

Current and Voltage RMS Calculations

The SY7T612+U3/I3 provides true RMS measurements (**VA_rms**, **Ix_rms**) for voltage and current inputs. The RMS is obtained by performing the square sum of the instantaneous samples of voltage and current over the accumulation interval and then performing a square root of the result after dividing by the number of samples in the interval. Optional RMS offset controls (**VA_rmsoffs**, **Ix_rmsoffs**) are available for each reported value to help compensate for an uncorrelated system noise floor. The values in these registers are squared and subtracted from the accumulated/divided squares. If the resulting RMS value is negative, zero is used. Figure 18 provides an overview of this process.

$$VRMS = \sqrt[2]{\frac{\sum_{n=0}^{N-1} Vn^2}{N}} \qquad IRMS = \sqrt[2]{\frac{\sum_{n=0}^{N-1} In^2}{N}}$$

Current and Voltage Average Calculations

The SY7T612+U3/I3 provides average/DC measurements (**VA_average**, **Ix_average**) for voltage and current inputs. The average is obtained by performing the sum of the instantaneous samples of voltage and current over the accumulation interval and then dividing by the number of samples in the interval. Figure 19 provides an overview of this process.

Power Calculations and Power Factor

The SY7T612+U3/I3 computes the active, reactive, and apparent power, as well as the power factor, for each outlet. Refer to Figure 20 for an overview of the operations described in the following paragraphs.

Active Power Calculation

Active power is calculated as the product of the voltage and current waveforms. The resulting waveform is the instantaneous power signal, and it is equal to the rate of energy flow at every instant of time. The unit of power is the watt or joules/sec. The instantaneous power is then averaged over N samples (accumulation time) for the computation of the active power available at register **Px_WATT**.

$$Px\_watt = \frac{\sum_{n=1}^{N-1} vA_n\, ix_n}{N}$$

Reactive Power

The reactive power is calculated as multiplication of instantaneous samples of current (ix) and the instantaneous quadrature voltage (VAq). The quadrature voltage is obtained through a 90 °phase shift (quadrature delay) of the voltage samples. The samples are then averaged over the accumulation time interval and updated in the **Px_VAR** register.

$$\text{Px\_VAR} = \sqrt{\sum_{n=0}^{N-1} ix_n \times vAq_n}$$

Apparent Power

The apparent power (S) is the product of RMS voltage (VRMS) and current (IRMS). The apparent power results, also referred as Volt-Amps, are available at the register **Px_VA**.

$$\textbf{Px\_VAR} = IX_{RMS} * VA_{RMS}$$

Power Factor

The power factor (**Px_PF**) is calculated as active power divided by the apparent power. The sign of the power factor is determined by the active power sign.

$$\text{Px\_PF} = \frac{\text{Px\_WATT}}{\text{Px\_VA}}$$

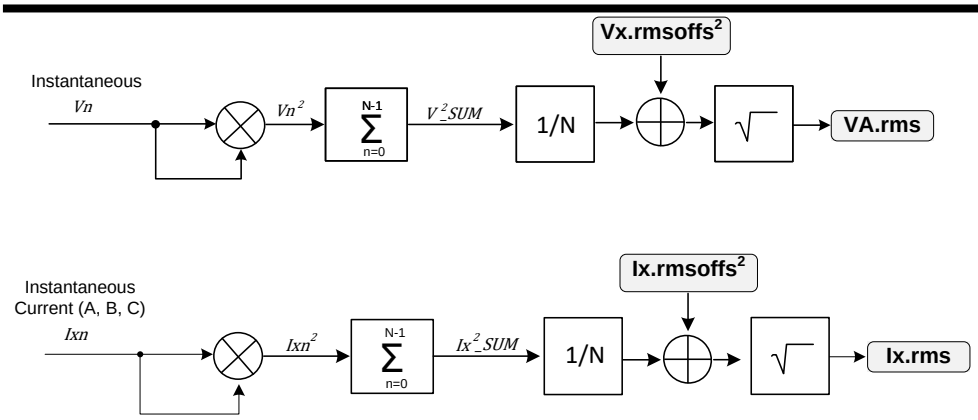


Figure 18: RMS Calculations

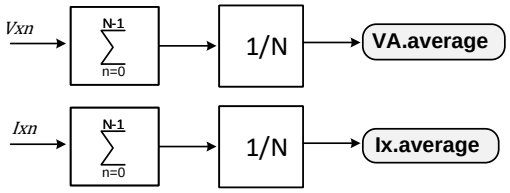


Figure 19: Average Calculations

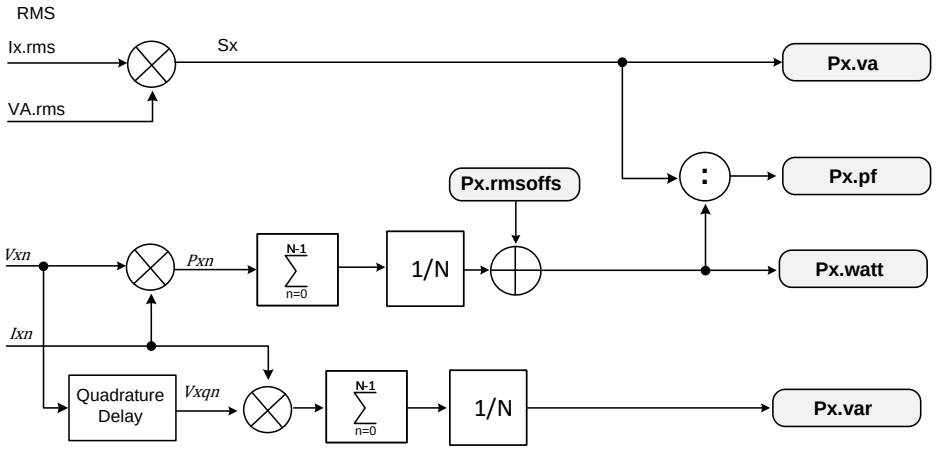


Figure 20: Power (Active, Reactive, and Apparent) and Power Factor Calculation

Fundamental and Harmonics Calculations

Fundamental and Harmonics

The SY7T612+U3/I3 provides measurements of fundamental and individual harmonics of voltage and currents.

Fundamental and Harmonic Selection

The SY7T612+U3/I3 allows extraction and calculation of a single selected harmonic. The **harmonics.order** register is used to select the single harmonic to extract. By default, the fundamental (first harmonic) is selected for voltage and current, calculations.

The resulting harmonic component of voltage and currents is available in the **VA_harm.rms** and **Ix_harm.rms** registers.

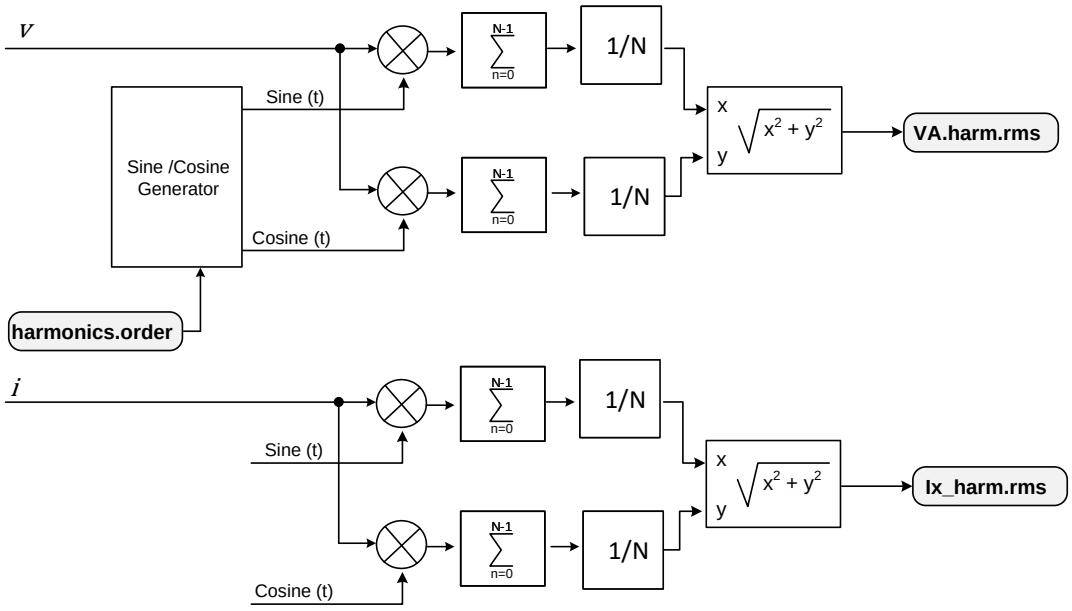


Figure 21: Voltage and Current Fundamental and Harmonic Calculations

Net Energy Accumulation

Energy calculations are included to minimize the traffic on the host interface and simplify system design. The (signed) energy in the accumulation intervals are summed together until a user defined "bucket size" is reached. When a bucket of energy is reached, the value in the energy counter register is incremented or decremented by one. All energy counter registers are low-rate 24-bit output registers that contain values calculated over multiple accumulation intervals. The net results are provided in the **Px_enet.Wh** and **Px_enet.Varh** registers for active and reactive energy, respectively.

Energy results are cleared upon any power down or reset and can be manually cleared by the user using the command register. The **cycles.Frame** register can be used to detect device resets (loss of energy data) or to track time between energy reads.

Bucket Size for Energy Counters

The **energy.bucket.L/H** register pair ("**bucketH**" and "**bucketL**") allows the user to define the unit of measure for the energy counter registers. It is an unsigned 48-bit fixed-point number with 24 bits for the integer part and 24 bits for the fractional part (U24.24). The bucket size can be saved to flash memory as the register default.

$$BUCKET = bucketH + \frac{bucketL}{2^{24}}$$

$$Bucket\ in\ Wh = BUCKET * \frac{3600s * Fsample}{FSI * FSV}$$

Bucket calculation example

If FSV=667Vpk, FSI=62Apk, and the energy counters incrementing in steps of 1.0 watt-hours, the value in BUCKET should be:

$$Bucket\ in\ Wh = 1.0 * \frac{3600s * 4010sps}{667 * 62} = 349.08352275$$

bucketH=349 (0x00015D)
bucketL= 0. 08352275 * 2^{24}= 1,401,279 (0x1561BF)

Voltage and Current Peak Values

The SY7T612+U3/I3 records the highest voltage and current measured during an accumulation interval. These values are updated at each accumulation interval and available in the output registers **VA_peak** and **Ix_peak**, for voltage and current, respectively.

Voltage Sag and Surge Detection

The SY7T612+U3/I3 device implements a voltage sag and surge detection function on the line voltage VA input. The sag/surge detection function generates an alarm when the line voltage drops below or exceeds the relevant programmable thresholds.
This function performs cycle-by-cycle monitoring of the AC line voltage. The RMS value of the line voltage is calculated over a full line cycle (or at most 25msec if no more zero crossings are detected) and compared with sag and surge thresholds. Registers **sag.Limit** and **surge.Limit** contain the values of the sag and surge thresholds parameters.
The sag and/or detection can be used to monitor or record the quality of the power line or generate a signal on one of the ALARM DIO pins to notify external devices. For instance, a sag signal would immediately inform a host microprocessor of a pending power-down. The external device could then enter a power-down mode (and save data or record the event) before a power outage. Refer to the Alarms section for more information.
This function also counts such sag and surge events and provides them in the **sag.Count** the **surge.Count** result registers. Note that only new events increment the counters, i.e. multiple consecutive line cycles in a sag or surge condition only increment the appropriate counter once. The following figure shows a typical sag event.

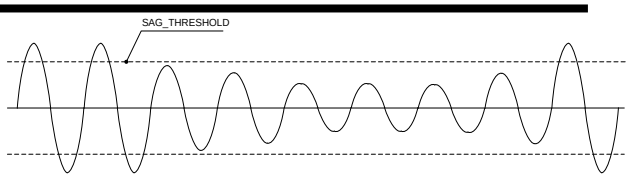


Figure 22. Voltage Sag

Alarms and Status

The SY7T612+U3/I3 monitors device status and user configurable signal conditions. This information is reported as "alarms" and managed via a set of registers described in this section.
Most alarms have a corresponding register to store the threshold above which (in the case of "max" limits), or below which (in the case of "min" limits) an alarm condition is generated.
The alarm bit will continue to be set as long as the alarm condition persists, even if the user clears it.

Alarm Bit Definitions and Configuration Registers

The bit definitions in Table 7 apply to the **Alarms.Status**, **Alarms.Sticky**, **Alarms.Set**, **Alarms.Reset**, **Alarms.Mask_A** and **Alarms.Mask_B** registers. Also shown are the corresponding limit registers (thresholds).

Table 7: Alarms Register and Corresponding Configuration Registers

Bit	Alarms (bit)	Limit Register [Alarms.xxx]	Function
23	DataReady		Low-Rate results have been updated
22	Reset		Reset occurred
21	OverTemp	**DieTemp.Max**	Die Temperature is Over Limit
20	UnderTemp	**DieTemp.Min**	Die Temperature is Under Limit
19	Not Used	--	Not Used
18	IC.PF-under	**PF.Min**	Power Factor is Under Limit
17	IB.PF-under		
16	IA.PF-under		
15	Not Used	--	Not Used
14	IC. OverCurrent	**I.Max**	RMS Current went above limit RMS Voltage went above upper limit
13	IB. OverCurrent		
12	IA. OverCurrent		
11	OverVolt	**VA.Max**	RMS Voltage went above upper limit
10	UnderVolt	**VA.Min**	RMS Voltage fell below lower limit
9	OverFreq	**Freq.Max**	Line Frequency went above upper limit

8	UnderFreq	**Freq.Min**	Line Frequency fell below lower limit
7	Not Used	--	Not Used
6	IC. Zero-cross	--	Current low-to-high Zero Crossing Detected
5	IB. Zero-cross		
4	IA. Zero-cross		
3	Not Used	--	Not Used
2	VA.Surge	**surge.Limit**	Voltage Surged above limit
1	VA.Sag	**sag.Limit**	Voltage Dropped below limit
0	VA.Zero-cross	--	Voltage low-to-high Zero Crossing Detected

Alarms.Status Register

The **Alarms.Status** register is an output register (read-only) that contains the status of the alarms and other conditions.

Alarms.Sticky

The **Alarms.Sticky** register is an input register that allows configuring individual bits into the Alarms register to hold the alarm status ("sticky") until an **Alarms.Reset** command is issued by the host. Each alarm can otherwise be set to auto-reset at the removal of the offending condition. The **Alarms.Sticky** register is non-volatile.

Alarms.Set and Alarms.Reset

By setting the bit **Alarms.Set**[#] or **Alarms.Reset**[#] to **1** (one) the user can set the state of the corresponding Alarm register bit (**Alarms.Status**[#]) to 1 or 0 respectively. **Alarms.Set**[#] or **Alarms.Reset**[#] will return to 0 upon completion.

Alarms. Mask_A and Alarms. Mask_B

The **Alarms.Mask_A** and **Alarms.Mask_B** registers are associated with the digital I/O pins **DIO7/ALARM0/SAG** and **DIO8/ALARM1**, respectively. They allow the user to select which alarm will activate the respective associated DIO pin. For example, to select Alarms **VA.Sag** and **VA.surge** to drive the **DIO7/ALARM0/SAG** pin, the **Alarms.Mask_A** register should be set to 0x000006. The value of the Mask registers can be saved into flash memory. Note that the polarity (active high or active low) for the alarm signals is determined by the DIO polarity configuration bits as described in Digital I/O Pins Polarity.
If the mask register is 0x000000 or the associated DIO pin is configured as an input then the alarm signal is not driven and the DIO is left to direct user control.

Digital Input Output Usage and Control

The SY7T612 has a set of digital I/O's that are multi-function and user-configurable. The digital I/O pins can be driven through the relevant registers or assigned to a particular alarm or function. Their assignment depends on the interface that is selected and the firmware configuration, as shown in Table 8. The bit assignments apply to registers: **dio.dio_dir**, **dio.dio_pol**, **dio.dio_state**, **dio.dio_set** and **dio.dio_rst**.

Table 8: Digital I/O Function and Pin Mapping

		SY7T612+U3			SY7T612+I3		
Pin Name	**DIO register Bit #**	**Function at Power-On Reset**	**Function(s) at Runtime**		**Function at Power-On Reset**	**Function(s) at Runtime**	
			SPI	**SSI/UART**		**SPI**	**I²C**
	23:16						
DIO15	15						
DIO14	14		RelayOutC0			RelayOutC0	
DIO13	13		RelayOutC1			RelayOutC1	
DIO12	12		RelayOutB0			RelayOutB0	
DIO11	11		RelayOutB1			RelayOutB1	
DIO10	10		RelayOutA0			RelayOutA0	
DIO9	9		RelayOutA1			RelayOutA1	

DIO8	8	SPI/SSI sel	ALARM1		SPI/I²C sel	ALARM1	
DIO7	7		ALARM0/SAG			ALARM0/SAG	
DIO6	6	ADDRSEL0	PULSE		ADDRSEL0	PULSE	
DIO5	5		SSB	DIR		SSB	SCL
DIO4	4		DIO4			DIO4	
DIO3	36		MISO	TX		MISO	SDAo
DIO2	2		MOSI	RX		MOSI	SDAi
DIO1	1	ADDRSEL1	SCK	DIO1	ADDRSEL1	SCK	DIO1
DIO0	0		DIO0			DIO0	

Digital I/O Pins Direction

The **dio.dio_dir** register sets the direction of the pins, where "1" is input and "0" is output. For pins used as part of the selected serial interface, the **dio.dio_dir** register has no effect. If a DIO is defined as an input, a weak internal pull-up is active.

Digital I/O Pins Polarity

For digital DIOs configured as outputs (DIO#), the **dio.dio_pol**[#] determines the active state polarity, and thus the logic state in relation to the physical state. For **dio.dio_pol[#]** = 1, the corresponding DIO output level 1 = logic high and 0= logic low. For **dio.dio_pol[#]** = 0, the corresponding DIO output level 1 = logic low, 0 = logic high.

Digital I/O Pins Input State

The **dio.dio_state** register contains the current physical state of the DIOs. Note that the logic state is determined also by the polarity setting.

Digital I/O Pins Output State

The digital I/O pins can be set to logic high or low through two separate registers.
By setting the a bit **dio.dio_set**[#] to 1 the user can set the state of the corresponding DIO# pin to logic high if configured as an output. Note that if the polarity setting for that bit is 0, the physical state of the DO# pin is 0. **dio.dio_state**[#] will also reflect this change. **dio.dio_set**[#] will return to 0 upon completion of the command.
By setting the bit **dio.dio_rst**[#] to 1 the user can set the state of the corresponding DIO# pin to low if configured as an output. Note that if the polarity setting for that bit is 0, the physical state of the DO# pin is 1. **dio.dio_state**[#] will also reflect this change. **dio.dio_rst**[#] will return to 0 upon completion of the command.

Relay Control

The SY7T612+U3/I3 includes a flexible relay control scheme. Up to three relays can be switched. Supported relay types are single-coil non-latching, single-coil latching and dual-coil latching. The SY7T612+U3/I3 generates appropriate control levels or pulses, with mechanisms to try to align switching to zero-crossings of voltage and currents.

Relay configuration: types and DIO assignment

This section describes how to set basic configuration parameters, such as DIO assignments, relay type and options for synchronization to zero crossings of voltage and currents.

The main configuration registers are **relay.configAB** and **relay.configC**. Each register controls two relays as shown in the following table.

Table 9: relay.configAB bit fields

Bit	Field/Function
23:22	REL_B_LOCK
21:20	REL_B_TYPE
19:16	REL_B_DIO_OFF
15:12	REL_B_DIO_ON
11:10	REL_A_LOCK
9:8	REL_A_TYPE
7:4	REL_A_DIO_OFF
3:0	REL_A_DIO_ON

Table 10: relay.configC bit fields

Bit	Field/Function
23:12	Not Used
11:10	REL_C_LOCK
9:8	REL_C_TYPE
7:4	REL_C_DIO_OFF
3:0	REL_C_DIO_ON

Where:

REL_x_TYPE (x = ABCD)	
00	Relay x = single-coil, non-latching Relay
10	Relay x = single-coil, latching Relay
11	Relay x = dual-coil, latching Relay

REL_x_DIO_ON (x = ABCD)	
0xN	DIO N is a control output for Relay x as follows: the ON signal for dual-coil relays the sole (ON/OFF) signal for single-coil relays

REL_x_DIO_OFF (x = ABCD)	
0xN	DIO N is a control output for Relay x as follows: the OFF signal for dual-coil relays not used for single-coil relays

REL_x_LOCK (x = ABCD)	
00	ON and OFF signals for Relay x are not locked to zero crossings
01	ON and OFF signals for Relay x are both locked to voltage VA zero-crossings
11	The ON signal for Relay x is locked to voltage VA zero crossings, and the OFF signal locked to current Ix zero crossings

Note that the polarity of the control signals is determined by the **dio.dio_pol** register as described in section Digital I/O Pins Polarity.
A relay OFF (open) transition can be aligned with zero-crossings of either the line voltage VA, or the current associated with the relay (i.e. Relay A to IA, etc).

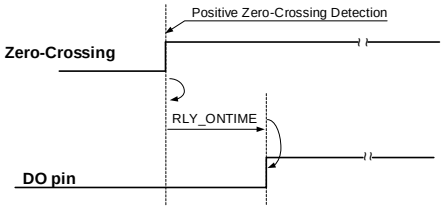
Relay configuration: timing

This section describes how to set timing parameters such as switching delays and control pulses.

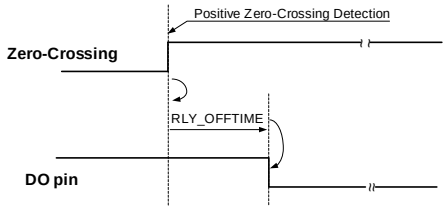
Timing of the control signals after a relay ON or OFF command is sent to the SY7T612+U3/I3 can be broken down into three parts:

1) If so configured, signal is delayed until the next positive zero crossing of the voltage or current is found. If no zero-crossing is configured, this part is skipped.
2) A user configurable delay is then applied before toggling the control signal. Separate delay parameters are available for ON and OFF operations. This allows the user take known mechanical delays of the relays into account and align the actual closing/opening with subsequent zero crossings. Note that this is an empirical process and there is no feedback or close loop control of the mechanical delay.
3) If a latching relay type is configured, the control signal generates a pulse whose width is user configurable.

The following two figures show an example of relay switching in the case of a single-coil non-latching and single-coil latching relay. All signals are shown as active high. In the case of dual-coil latching relay the DIO pin numbers in the ON and OFF operations are different, but timing is identical to the single-coil diagram.

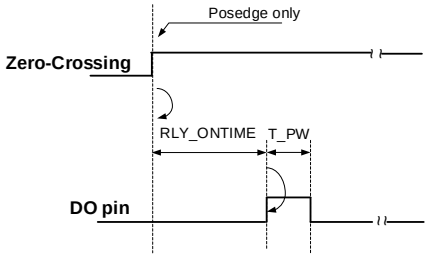


a. Relay Activation (ON Command)

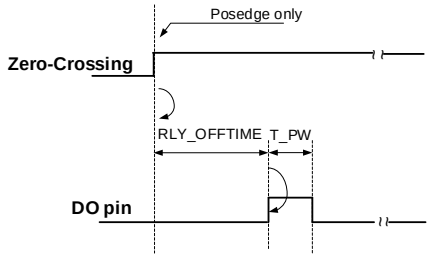


b. Relay De-activation (OFF Command)

Figure 23: Relay Commands (non-latching)



a. Relay Activation (ON Command)



b. Relay De-activation (OFF Command)

Figure 24: Relay Commands (latching)

The delays are configured in the **relay.delay** register:

Table 11: relay.delay bit fields

Bit	Field/Function
23:12	RELAYON[11:0]
11: 0	RELAYOFF[11:0]

Where

RELAYON	
[11:0]	Relay ON delay in number of samples. 0 = 0 samples; 0xFFF/4095 = 4095 samples; (~1.021sec @ Fsample =4010Hz)

RELAYOFF	
[11:0]	Relay OFF delay in number of samples. 0 = 0 samples; 0xFFF/4095 = 4095 samples; (~1.021 @ Fsample =4010Hz)

Note that all relays for all channels have the same delays, unless they are switched one-by-one and this register is configured dynamically.

The signal pulse width for latching relays is configured in the **relay.pulsewidth** register:

Table 12: relay.delay bit fields

Bit	Field/Function
23:13	reserved
12: 0	PULSEWIDTH [12:0]

Where

PULSEWIDTH	
[12:0]	Latch pulse width in number of samples, for latching relay types. 0 = 0 samples; 0x1FFF/8191 = 8191 samples; (~2.043sec @ Fsample =4010Hz)

Note that all latching relays for all channels have the same pulse width, unless they are switched one-by-one and this register is configured dynamically

Relay commands

Relay activation/deactivation commands are issued by the host via writes to the **Command** register. The principle is that the command contains a mask field specifying which relays should be controlled (1 = set new state, 0 = do not change), and the corresponding new state of the relays specified in the mask (1 = relay ON/close, 0 = relay OFF/open). Refer to section Relay Control Command: 0xDExxxx for details.

Energy Counter Pulse Output

The SY7T612+U3/I3 can optionally output a pulse train on the DIO6/PULSE output at a programmable rate.

Pulse configuration

There are three configuration register controlling pulse generation. **pulsegen.addr** controls which of the energy counters should be monitored, and whether pulses should be generated. The counter is selected by writing its register address into this register. The following table shows the possible configurations:

Table 13: pulsegen.addr bit fields

Bit	Field/Function
23:12	reserved
11: 0	CNTR_ADDR

Where:

CNTR_ADDR	
0x000	Disable Pulse Generation
0x018/0x022/0x02C	Generate pulse for active energy (based on PA.watt/PB.watt/PC.watt)
0x019/0x023/0x02D	Generate pulse for reactive energy (based on PA.var/PB.var/PC.var)
0x01A/0x024/0x02E	Generate pulse for apparent energy (based on PA.va/PB.va/PC.va)

Register **pulsegen.pulsewidth** defines the desired pulse-width of the generated pulse train, in number of samples.

Table 14: pulsegen. pulsewidth bit fields

Bit	Field/Function
23:13	reserved
12: 0	PULSEWIDTH [12:0]

Where

PULSEWIDTH	
[12:0]	Energy pulse width in number of samples 0 = 0 samples; 0x1FFF/8191 = 8191 samples; (~2.042sec @ Fsample =4010Hz)

Register **pulsegen.wrate** specifies pulse rate and meter constant (Kh) setting for power pulse output as follows:

$$WRATE = 2^{25} * \frac{FSV * FSI}{\left(\frac{watt \times sec}{pulse}\right) * Fsample} = \frac{2^{25}}{3{,}600} * \frac{FSV * FSI}{\left(\frac{Wh}{pulse}\right) * Fsample} = \frac{2^{25}}{3{,}600{,}000} * \frac{FSV * FSI}{\left(\frac{KWh}{pulse}\right) * Fsample}$$

Where

- FSV is the full-scale peak voltage,
- FSI is the full-scale peak current,

Example: Generate a pulse every Wh (Kh =1Wh/pulse) The system configuration is assumed to be set as follows:
FSV = $667V_{peak}$; FSI = $125A_{peak}$, Fsample = 4010Hz

To set the meter constant to 1 Wh/pulse:

$$WRATE = \frac{2^{25}}{3{,}600} * \frac{FSV * FSI}{\left(\frac{Wh}{pulse}\right) * Fsample} = \frac{2^{25}}{3{,}600} * \frac{667V * 125A}{1 * 4010Hz} = 193{,}793 = 0x02F501$$

On-Chip Calibration Routines

The SY7T612+U3/I3 includes current and voltage and temperature calibration routines. These routines modify gain and offset coefficients.

The user can set up and initiate a calibration routine through the Command register. When the calibration process completes, command register bits 23:16 (set to 0xCA to issue a calibration command) are cleared along with bits associated with channels that calibrated successfully. Any channels that failed will have their corresponding bit left set. After completion of the calibration, the new coefficients can be saved into flash memory as defaults by issuing the Save to Flash Command (0xACC200).
The duration of a calibration cycle is determined by two user parameters. The measurements from the signal to be calibrated are averaged over the number of measurement cycles set by the register **calib.cyclecount**. At the end of this interval (one "iteration") gains are calculated. This process is repeated for a number of iterations specified in register **calib.iterations**. Therefore, given the time of one accumulation interval, the duration is approximately

$$t_{calibration} = t_{accum} * calib.cyclecount * calib.iterations$$

Note that for best results, the accumulation interval should be locked to the line cycle.

Voltage Gain Calibration using VRMS target

In order to calibrate the voltage gain, a stable reference AC signal must be applied to the channel to be calibrated. The value corresponding to the applied supply (usually obtained from a power meter) must be entered in the relevant target register (**calib.target.voltage**). Considering that calibration is done with low-rate RMS results, the value of the target register should never be set to a value above 70.7% of full-scale.
To start the calibration, the calibration command (0xCAxxxx) with the **cmnd.calib.vrms.A** bit (0x001000) set must be written to the Command register.
The new gain is calculated by dividing the target register value by the averaged measured value. It is then written to the **VA_gain** register unless an error occurred.

Current Gain Calibration using IRMS target

In order to calibrate the current gain(s), a stable reference AC signal must be applied to the channel to be calibrated. The value corresponding to the applied supply (usually obtained from a power meter) must be entered in the relevant target register (**calib.target.current**). Considering that calibration is done with low-rate RMS results, the value of the target register should never be set to a value above 70.7% of full-scale.
To start the calibration, the calibration command (0xCAxxxx) with the **cmnd.calib.irms.x** bit(s) (0x0000x0) set must be written to the Command register. In addition, the **cmnd.calib.power** bit must be set to **zero**.
The new gain(s) are calculated by dividing the target register value by the averaged measured value. It is then written to the **Ix_gain** register(s) unless an error occurred.

Current Gain Calibration using power target

In order to calibrate the current gain(s) based on a power target, a stable reference AC signal must be applied to the channel to be calibrated. The value corresponding to the applied supply (usually obtained from a power meter) must be entered in the relevant target register (**calib.target.power**).
To start the calibration, the calibration command (0xCAxxxx) with the **cmnd.calib.irms.x** bit(s) (0x0000x0) set must be written to the Command register. In addition, the **cmnd.calib.power** bit must be set to **one**.
The new gain(s) are calculated by dividing the target register value by the averaged measured value. It is

then written to the **Ix_gain** register(s) unless an error occurred.

Voltage Offset Calibration using vavg target

In order to calibrate the voltage offset, a stable reference DC voltage must be applied to the channel to be calibrated. The value corresponding to the applied supply (usually obtained from a power meter) must be entered in the relevant target register (**calib.target.voltage.offset**).
To start the calibration, the calibration command (0xCAxxxx) with the **cmnd.calib.voffs.A** bit (0x002000) set must be written to the Command register.
At the end of each iteration, the delta between measured and target voltage is added to the existing offset.

$$voffsnew = voffsold + (vavg - vavgtarget$$

The new offset is then written to the **VA_offs** register unless an error occurred.

Current Offset Calibration using iavg target

In order to calibrate the current offset(s), a stable reference DC signal must be applied to the channel to be calibrated. The value corresponding to the applied supply (usually obtained from a power meter) must be entered in the relevant target register (**calib.target.current.offset**).
To start the calibration, the calibration command (0xCAxxxx) with the **cmnd.calib.ioffs.x** bit(s) (0x000x00) set must be written to the Command register.
At the end of each iteration, the delta between measured and target current(s) is added to the existing offset.

$$ixoffsnew = ixoffsold + (ixavg - iavgtarget$$

The new offset(s) are then written to the **Ix_offs** register(s) unless an error occurred.

On-Chip Temperature Calibration

In order to calibrate the on-chip temperature sensor, the user must write the known chip temperature value to **DieTemp.Target**. To start the calibration, the calibration command (0xCAxxxx) with the **cmnd.calib.DieTemp** bit (0x000001) set must be written to the Command register. This will cause the **DieTemp.Offset** parameter to be updated with a new offset based on the known temperature supplied by the user.

Data Access and Configuration

All user registers are contained in a 256-word (24-bits each) area of the on-chip RAM and can be accessed through the UART, SPI, or I²C interfaces. These registers are byte-addressable via the UART interface and word-addressable via the SPI, and I²C interfaces. These registers consist of read (output), write (input), and read/write in the case of the Command Register.

Note: Writing to reserved registers or to unspecified memory locations could result in device malfunction or unexpected results.

Data Types

The input and output registers have different data types, depending on their assignment and functions. The notation used, indicates whether the number is signed, unsigned or bit-mapped and the location of the binary point. U indicates an unsigned value, S indicated a signed value. The following notation indicates whether the number is signed, unsigned, or bit-mapped and the location of the binary point.

(S|U|B)(xx)(.yy)	
S|U|B	Indicates a **S**igned, **U**nsigned or **B**it Mapped Value, respectively
xx	(optional) Indicates a number with xx total bits. Defaults to 24 bits if absent.
.yy	(optional) Indicates a fixed-point number with yy bits to the right of the binary point. Defaults to 0 bits if absent

Example:

S24.21 and S.21 are notations for a signed 24-bit number with 21 bits to the right of the decimal point.

Bit Position											
23	22	21	.	20	19	18	17	…	2	1	0
S·(-22)	21	20		2-1	2-2	2-3	2-4	…	2-19	2-20	2-21

Table 15: Data Types

Data Type	Description
S24	A 24-bit signed integer with a range of -8,388,608 to +8,388,607
U.24	A 24-bit unsigned fixed-point value with the binary point to the left of bit 23 with a range of 0 to $(1-2^{-24})$
U.23	A 24-bit unsigned fixed-point number with the binary point to the left of bit 22 and with a range of 0 to $(2-2^{-23})$
U.22	A 24-bit unsigned fixed-point number with the binary point to the left of bit 21 and with a range of 0 to $(4-2^{-22})$
U.21	A 24-bit unsigned fixed-point number with the binary point to the left of bit 20 and with a range of 0 to $(8-2^{-21})$
S.23	A 24-bit signed fixed point number with the binary point to the left of bit 22 and with a range of -1.0 to $(+1-2^{-23})$
S.21	A 24-bit signed fixed-point number with a binary point to the left of bit 20 and with a range of -4.0 to $(+4-2^{-21})$
S.16	A 24-bit signed fixed-point number with a binary point to the left of bit 15 and with a range of -128.0 to $(+128-2^{-16})$
B24	A variable containing 24 independent single-bit values
U38.24	A 48-bit unsigned fixed-point value with the binary point to the left of bit 24. See section Bucket Size for Energy Counters

Register Map

	Word Address	Register Name	Data Type	Description
Basic info and Commands				
	0x000	Command	B24	See section: Command Register
	0x001	FWversion	U24	Firmware release date in hex format (0x00YMDD)
	0x002	protocol.indirect.wr.data	N/A	See section: SPI Indirect Access Protocol Description
	0x003	protocol.indirect.wr.addr	U24	
	0x004	protocol.indirect.rd.addr	U24	
	0x005	protocol.indirect.rd.data	N/A	
Results				
	0x006	cycles.Divisor	U24	Number of samples used in last accumulation interval
	0x007	cycles.Frame.L	U0.24	Accumulation interval (Frame) counter[23:0]
	0x008	cycles.Frame.H	U24.0	Accumulation interval (Frame) counter[47:24]
	0x009	VA.LineFreq	S.16	Line Frequency
	0x00a	Alarms.Status	B24	Alarms/Status Register
	0x00b	VA.sag.Count	U24	Number of times a SAG event has been detected
	0x00c	VA.surge.Count	U24	Number of times a SURGE event has been detected
	0x00d	dio.dio_state	B24	State of DIO Outputs
	0x00e	DieTemp	S.10	Chip/Die Temperature
	0x00f	VA.rms	S.23	RMS Voltage (common for all outlets)
	0x010	VA.average	S.23	Average Voltage (common for all outlets)
	0x011	VA.peak	S.23	Peak Voltage for (common for all outlets)
	0x012	VA.harm.rms	S.23	Harmonic RMS Voltage (common for all outlets)
	0x013	Itotal.rms	S.23	Total RMS current for all outlets (divided by 4 to prevent overflow)
	0x014	IA.rms	S.23	RMS Current Outlet A
	0x015	IA.average	S.23	Average CurrentOutlet A
	0x016	IA.peak	S.23	Peak Current Outlet A
	0x017	IA.harm.rms	S.23	Harmonic RMS Current Outlet A
	0x018	PA.watt	S.23	Active Power Outlet A
	0x019	PA.var	S.23	Reactive Power Outlet A
	0x01a	PA.va	S.23	Apparent Power Outlet A
	0x01b	PA.pf	S.22	Power Factor Outlet A
	0x01c	PA.enet.Wh	S24	Active Energy Counter Outlet A
	0x01d	PA.enet.Varh	S24	Reactive Energy Counter Outlet A
	0x01e	IB.rms	S.23	RMS Current Outlet B
	0x01f	IB.average	S.23	Average CurrentOutlet B

	0x020	IB.peak	S.23	Peak Current Outlet B
	Word Address	**Register Name**	**Data Type**	**Description**
	0x021	IB.harm.rms	S.23	Harmonic RMS Current Outlet B
	0x022	PB.watt	S.23	Active Power Outlet B
	0x023	PB.var	S.23	Reactive Power Outlet B
	0x024	PB.va	S.23	Apparent Power Outlet B
	0x025	PB.pf	S.22	Power Factor Outlet B
	0x026	PB.enet.Wh	S24	Active Energy Counter Outlet B
	0x027	PB.enet.Varh	S24	Reactive Energy Counter Outlet B
	0x028	IC.rms	S.23	RMS Current Outlet C
	0x029	IC.average	S.23	Average CurrentOutlet C
	0x02a	IC.peak	S.23	Peak Current Outlet C
	0x02b	IC.harm.rms	S.23	Harmonic RMS Current Outlet C
	0x02c	PC.watt	S.23	Active Power Outlet C
	0x02d	PC.var	S.23	Reactive Power Outlet C
	0x02e	PC.va	S.23	Apparent Power Outlet C
	0x02f	PC.pf	S.22	Power Factor Outlet C
	0x030	PC.enet.Wh	S24	Active Energy Counter Outlet C
	0x031	PC.enet.Varh	S24	Reactive Energy Counter Outlet C
Additional Commands				
	0x03c	harmonics.order	U24	Harmonic selector (1=fundamental)
	0x03d	Alarms.Set	B24	Alarm Set Register
	0x03e	Alarms.Reset	B24	Alarm Reset Register
	0x03f	dio.dio_set	B24	DIO Set Logic High Register
	0x040	dio.dio_rst	B24	DIO Set Logic Low Register
Configuration				
	0x041	Control	B24	See section: Control Register
	0x042	Config.FSV	U24	Voltage full scale register [667 = 667Vpeak]
	0x043	Config.FSI	U24	Current full scale register [62 = 62Apeak]
	0x044	Serial.DevAddr	U24	SSI target address for multiple target systems
	0x045	Serial.Baud	U24	Baud rate for UART interface
	0x046	cycles.AccumNumLineCyc	U24	Number of AC line cycles in an accumulation interval (line locked mode)
	0x047	cycles.MaxSampleCount	U24	Maximum number of ADC sample times in an accumulation interval
	0x048	Alarms.Sticky	B24	Status bits to hold until cleared by host. Alarms 1 = Holding; 0 = Not Holding
	0x049	Alarms.Mask_A	B24	Alarm mask bits for ALARM0/SAG/DIO7 pin
	0x04a	Alarms.Mask_B	B24	Alarm mask bits for ALARM1/DIO8 pin
	0x04b	Alarms.VA.Max	S.23	Voltage threshold above which OVERVOLT alarm will be activated.
	0x04c	Alarms.VA.Min	S.23	Voltage threshold below which VDROPOUT alarm will be activated.

Word Address	Register Name	Data Type	Description
0x04d	Alarms.Ix.Max	S.23	Current High Alarm Limit.
0x04e	Alarms.PFx.Min	S.22	Power Factor Low Alarm Limit.
0x04f	Alarms.DieTemp.Max	S.10	Die temperature threshold below which the UNDERTEMP alarm will be activated.
0x050	Alarms.DieTemp.Min	S.10	Die temperature threshold above which the OVERTEMP alarm will be activated.
0x051	Alarms.Freq.Max	S.16	Line Frequency threshold below which the UNDERFREQ alarm will be activated.
0x052	Alarms.Freq.Min	S.16	Line frequency threshold above which the OVERFREQ alarm will be activated.
0x053	sag.Limit	S.23	Voltage Sag Threshold
0x054	surge.Limit	S.23	Voltage Surge Threshold
0x055	dio.dio_dir	B24	Direction of DIO pins. 1 = Input ; 0 = Output
0x056	dio.dio_pol	B24	Polarity of DIO pins. 1 = Active High ; 0 = Active Low
0x057	app.relay.configAB	B24	Configuration register for Relay A and B
0x058	app.relay.configCD	B24	Configuration register for Relay C and D
0x059	app.relay.delay	U12:U12	Relay ON and OFF delay
0x05a	app.relay.pulsewidth	U14	Latching Relay Pulsewidth
0x05b	energy.bucket.L	U0.24	Energy Bucket Size – Low word
0x05c	energy.bucket.H	U24.0	Energy Bucket Size – High word
0x05d	calib.target.cyclecount	U24	Number of Frames to Average for calibration
0x05e	calib.target.iterations	U24	Number of Iterations for calibration
0x05f	calib.target.voltage	S.23	RMS Voltage target for gain calibration
0x060	calib.target.voltage.offset	S.23	Voltage target for offset calibration
0x061	calib.target.current	S.23	RMS Current target for gain calibration
0x062	calib.target.current.offset	S.23	Current target for offset calibration
0x063	calib.target.power	S.23	Active Power target for current gain calibration
0x064	DieTemp.Target	S.10	Chip/Die temperature calibration target
0x065	DieTemp.Offset	S.10	Chip/Die temperature offset
0x066	VA.rmsoffs	S.23	RMS Voltage offset for VA (Positive values only)
0x067	VA.gain	S.21	VA Gain (Positive values only)
0x068	VA.offs	S.23	VA Sample Offset
0x069	VA.phasecomp	S.21	VA Phase compensation
0x06a	Itotal.rmsoffs	S.23	RMS offset for Total Current (Positive values only)
0x06b	IA.rmsoffs	S.23	RMS Current offset for IA (Positive values only)
0x06c	PA.rmsoffs	S.23	Power Offset Adjust for Outlet A
0x06d	IA.gain	S.21	IA Gain (Positive values only)
0x06e	IA.offs	S.23	IA Sample Offset
0x06f	IA.phasecomp	S.21	IA Phase compensation
0x070	IB.rmsoffs	S.23	RMS Current offset for IB (Positive values only)
0x071	PB.rmsoffs	S.23	Power Offset Adjust for Outlet B

Word Address	Register Name	Data Type	Description
0x072	IB.gain	S.21	IB Gain (Positive values only)
0x073	IB.offs	S.23	IB Sample Offset
0x074	IB.phasecomp	S.21	IB Phase compensation
0x075	IC.rmsoffs	S.23	RMS Current offset for IC (Positive values only)
0x076	PC.rmsoffs	S.23	Power Offset Adjust for Outlet C
0x077	IC.gain	S.21	IC Gain (Positive values only)
0x078	IC.offs	S.23	IC Sample Offset
0x079	IC.phasecomp	S.21	IC Phase compensation
0x07A	pulsegen.sourcevar.addr	U12	Energy pulse output: address of energy counter to monitor
0x07B	pulsegen.pulsewidth	U14	Energy pulse output: pulse-width
0x07C	pulsegen.rate	U24	Energy pulse output: pulse-rate

Configuration Register Defaults

Address	Register Name	Default [hex]	Default [scaled]	Description
0x041	Control	0x000037		Enable HPFs, SSI single target mode, RS485, and Temperature Compensation
0x042	Config.FSV	0x00029D	667	Full Scale Peak Voltage [V]
0x043	Config.FSI	0x00007D	125	Full Scale Peak Current [A]
0x044	Serial.DevAddr	0x000000	0	
0x045	Serial.Baud	0x01C200	115,200	UART/SSI baud rate
0x046	cycles.AccumNumLineCyc	0x00001E	30	Accumulation interval locked to line cycles, duration of 30 cycles (0.5 sec @60Hz)
0x047	cycles.MaxSampleCount	0x0007D4	2004	Maximum accumulation interval of 2004 samples at 4009sps = 0.5 sec
0x048	Alarms.Sticky	0x400000		Reset alarm bit is sticky
0x049	Alarms.Mask_A	0x800000		Output DataReady signal on DIO7/ALARM0
0x04a	Alarms.Mask_B	0x000001		Output VA zerocrossings on DIO8/ALARM1
0x04b	Alarms.VA.Max	0x18F291	130.000	low rate over voltage threshold in Vrms
0x04c	Alarms.VA.Min	0x1330BE	100.000	low rate under voltage threshold in Vrms
0x04d	Alarms.Ix.Max	0x010624	1.000	low rate over current threshold in Arms
0x04e	Alarms.PFx.Min	0x2CCCCC	0.700	power factor threshold (abs value)
0x04f	Alarms.DieTemp.Max	0x011800	70.000	low rate over temperature threshold in ℃
0x050	Alarms.DieTemp.Min	0xFFB000	-20.000	low rate under temperature threshold in ℃

Address	Register Name	Default [hex]	Default [scaled]	Description
0x051	Alarms.Freq.Max	0x3E8000	62.500	low rate over frequency threshold in Hz
0x052	Alarms.Freq.Min	0x398000	57.500	low rate under frequency threshold in Hz
0x053	sag.Limit	0x114578	90.000	high rate Surge threshold in Vrms
0x054	surge.Limit	0x1ADDD7	140.000	high rate Sag threshold in Vrms
0x055	dio.dio_dir	0x00AA3B		Alarm0/1 and 2 relay controls are outputs
0x056	dio.dio_pol	0x00FFBF		All active high, except DIO6/PULSE
0x057	app.relay.configAB	0xCBCC9A		single-coil, non-latching relays, lock closing to V and opening to I, DIO10 and 12 controls
0x058	app.relay.configCD	0xC22CDE		single-coil, non-latching relay C, lock closing to V and opening to I, DIO14 control output (upper half is don't care)
0x059	app.relay.delay	0x05003C		ondelay=20.0 msec, offdelay=15.0 msec
0x05a	app.relay.pulsewidth	0x0000C8		pulsewidth= 50.0 msec (don't care for non-latching relays)
0x05b	energy.bucket.L	0x501B37		BucketH/L = 0.1Wh at nominal clock
0x05c	energy.bucket.H	0x000011		
0x05d	calib.target.cyclecount	0x00000A	10	each iteration = 10 accumulation intervals = 5sec @ 60Hz
0x05e	calib.target.iterations	0x000004	4	4 iterations = 20sec @ 60Hz
0x05f	calib.target.voltage	0x17074B	120.000	in Vrms
0x060	calib.target.voltage.offset	0x000000	0.000	
0x061	calib.target.current	0x010625	1.000	in Arms
0x062	calib.target.current.offset	0x000000	0.000	
0x063	calib.target.power	0x002F2A	120.000	in Watt
0x064	DieTemp.Target	0x006400	25.000	in ℃
0x065	DieTemp.Offset	0xFFA800	-22.000	in ℃
0x066	VA.rmsoffs	0x000000	0.000	
0x067	VA.gain	0x200000	0.250	
0x068	VA.offs	0x000000	0.000	
0x069	VA.phasecomp	0x000000	0.000	
0x06a	Itotal.rmsoffs	0x000000	0.000	
0x06b	IA.rmsoffs	0x000000	0.000	
0x06c	PA.rmsoffs	0x000000	0.000	
0x06d	IA.gain	0x200000	0.250	
0x06e	IA.offs	0x000000	0.000	
0x06f	IA.phasecomp	0x000000	0.000	
0x070	IB.rmsoffs	0x000000	0.000	

Address	Register Name	Default [hex]	Default [scaled]	Description
0x071	PB.rmsoffs	0x000000	0.000	
0x072	IB.gain	0x200000	0.250	
0x073	IB.offs	0x000000	0.000	
0x074	IB.phasecomp	0x000000	0.000	
0x075	IC.rmsoffs	0x000000	0.000	
0x076	PC.rmsoffs	0x000000	0.000	
0x077	IC.gain	0x200000	0.250	
0x078	IC.offs	0x000000	0.000	
0x079	IC.phasecomp	0x000000	0.000	
0x07A	pulsegen.sourcevar.addr	0x000000	0.000	Address 0, pulse generation disabled
0x07B	pulsegen.pulsewidth	0x000028	40	Pulse-width = 10.0 msec
0x07C	pulsegen.rate	0x02F501	193,793	Kh = 1 Wh/pulse

Control Register

This register is used to control the basic operating modes of the solution.

Bit(s)	Name	Description
23:18	rsvd	Reserved (set to 0)
17	ICPOL	Swap Current Channel IC Polarity 0= Normal; 1=Reversed
16	IBPOL	Swap Current Channel IB Polarity 0= Normal; 1=Reversed
15	IAPOL	Swap Current Channel IA Polarity 0= Normal; 1=Reversed
14	VPOL	Swap Voltage Channel Polarity 0= Normal; 1=Reversed
13:11	rsvd	Reserved (set to 0)
10	CTEMP	Stop chip/die temperature update: 1=stop update; 0=update.
9	ARRST	Enable auto-reporting at reset. 0=Disabled; 1=Enabled)
8	rsvd	Reserved (set to 0)
7	CHOP	1 = disable chopping 0 = enable chopping (default)
6	FREQ	1 = disable Line Frequency update 0 = enable Line Frequency update
5	DIR.EN	1: DIO5/DIR pin is used in UART mode to indicate the device is transmitting data. 0: DIO5/DIR is not driven in UART mode
4	TC	Enable Gain/Temperature compensation 1=enable; 0=disable. This bit allows the firmware to modify the system gain based on measured chip temperature.
3	AR	Enable auto-reporting of all result registers once ever accumulation interval. 0=Disabled; 1=Enabled
2	STRG	Single-Target SSI Mode: SSI ignores the **Serial.DevAddr** and ADDRSEL0/1 pins. Will respond to all SSI commands. Only checked during initialization.
1	HPFI	High-Pass Filter Current Channels (All) 0=Disabled; 1=Enabled
0	HPFV	High-Pass Filter Voltage Channel 0=Disabled; 1=Enabled

Command Register

This register is used to issue commands to perform specific tasks.

Save to Flash Command: 0xACC200

Use this command to save the calibration coefficients and user parameters registers to flash memory. Upon reset or power-on, the values stored in flash will become new system defaults. Upon completion of the command, the **Command** register is cleared.

Clear Flash Storage Command: 0xACC000

Use this command to clear the flash coefficients (nonvolatile system defaults). Upon reset or power-on, the values revert to factory system defaults. Upon completion of the command, the **Command** register is cleared.

Soft Reset: 0xBD0000

Use this command to invoke a reset. Note that it resets the program counter only and not the HW. Upon completion, the **Command** register is cleared.

Clear Energy Counters: 0xEC0000

Use this command to clear all energy counters. Upon completion, the **Command** register is cleared.

Enable/Disable Auto-reporting: 0xAE000x

Use this command to enable or disable auto reporting mode. When the device is in Auto Reporting mode a read-modify-write of the Control register to stop auto reporting is generally unreliable. This command provides a way to set/clear the ar bit without directly accessing the Control register. Bit 0 of the value determines whether auto-reporting should be enabled (1) or disabled (0). Upon completion, the **Command** register is cleared.

Calibration Command: 0xCAxxxx

The Calibration Command starts the calibration process. It is assumed that appropriate input signal(s) are applied, and target values set before starting calibration. Refer to section On-Chip Calibration Routines for more details on calibration.

When the calibration process completes, bits 23:16 are cleared. If the calibration has completed without a detected error then bits 15:0 (with the exception of the **cmnd.calib.power** bit) are also cleared. If an error is detected during the calibration the bit associated with the unsuccessful calibration routine remains set.

The following table describes the command bits:

Table 16: Command Register, Calibration Command

Bit(s)	Value	Description
23:16	0xCA	"Calibrate" Command.
15:14	reserved	Set to 0.
13	Voffs.A	Calibrate voltage offset
12	Vrms.A	Calibrate voltage
11	Not used	Write as zero
10	Ioffs.C	Calibrate current offset for Phase C.
9	Ioffs.B	Calibrate current offset for Phase B.
8	Ioffs.A	Calibrate current offset for Phase A.
7	Not used	Write as zero
6	Irms.C	Calibrate current gain for Phase C.
5	Irms.B	Calibrate current gain for Phase B.
4	Irms.A	Calibrate current gain for Phase A.
3	Power	0: Use current target for I gain calibration 1: Use power target for I gain calibration
2:1	reserved	Set to 0.
0	DieTemp	Calibrate chip/die temperature

Relay Control Command: 0xDExxxx

The Relay Command sets and resets one or several relays. Refer to section Relay Control for more details on this function.
The following table describes the command bits:

Table 17: Command Register, Calibration Command

it(s)	alue	escription
23:16	0xDE	Relay Control" Command.
15:11	reserved	et to 0.
10	Cmd.C	reset, 1 set Relay C.
9	Cmd.B	reset, 1 set Relay B.
8	Cmd.A	reset, 1 set Relay A.
7:3	reserved	et to 0.
2	Mask.C	issue Cmd.C, 0: Relay C unaffected.
1	Mask.B	issue Cmd.B, 0: Relay B unaffected.
0	Mask.A	issue Cmd.A, 0: Relay A unaffected.

UART Protocol Description (SY7T612+U3)

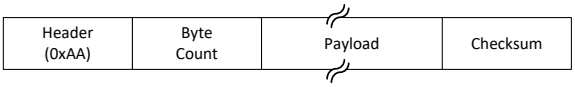
The SY7T612+U3 firmware implements a "SSI protocol on the UART interface. While the protocol supports multi-point communications, the SY7T612+U3 firmware sets the device for single point (Single Target Mode) by default. The protocol includes data integrity check.

The protocol also includes an auto-report mode. This mode allows the SY7T612+U3 to autonomously send packets at the completion of the accumulation intervals.

Command-Response Mode

In this protocol, the host is the master and must initiate communications. The master should first set the device's register address pointer before performing read or write operations.

After sending the synchronization header code (0xAA), the master sends (in the following order) the byte counts (bytes in payload), the payload and then the checksum that provides data integrity check. The following figure shows a generic command packet generated from the master:



The payload contains commands, registers address, data etc. The payload can contain either a single command or multiple commands. The protocol allows for reading or writing one up to 255 bytes in a single operation. The following paragraphs describe the data access method for both read and write. Only the payload is shown.

Register Address Pointer Selection

The following message sets the address pointer to the register (or set of registers) to read or write:

PAYLOAD	
0xA3 Command	Register Address (2 Bytes)

The SY7T612+U3 replies with an acknowledge message.

Read Command

It is possible to read data from the SY7T612+U3 using the 0xE command. To read 0 to 15 bytes, the command byte is completed with the number of bytes to read. For example, to read 3 bytes:

PAYLOAD
0xE3 Command

In order to read a larger number of bytes (up to 255), the command 0xE0 must be used. In this case, the command 0xE0 must be followed by a byte containing the number of bytes to be read. For example, to read 31 bytes:

PAYLOAD	
0xE0 Command	0x1F (Number of Bytes to Read)

Write Command

It is possible to write data to the SY7T612+U3 using the 0xD command. To write 1 to 15 bytes, the command byte must be completed with the number of bytes of data to write. For example to write 3 bytes:

PAYLOAD	
0xD3 Command	Data (Number of Bytes = 3)

In order to write a larger number of bytes (up to 255), the command 0xD0 must be used. In this case, the number of data bytes to follow is determined by the Byte Count. For example, to write 31 bytes:

PAYLOAD	
0xD0 Command	Data (Number of Bytes = Byte Count – 4)

After each read or write operation, the internal address pointer is incremented to point to the address that followed the target of the previous read or write operation.

Summary of Commands

Table 18: Host SSI Commands

Command	Parameters	Description
0 - 7F		(invalid)
80 - 9F		(not used)
A0		Clear address
A1	[byte-L]	Set Read/Write address bits [7:0]
A2	[byte-H]	Set Read/Write address bits [15:8]
A3	[byte-L][byte-H]	Set Read/Write address bits [15:0]
A4 - AF		(reserved for larger address targets)
B0 - BF		(not used)
C0		De-select Target (target will Acknowledge)
C1 - CE		Select target 1 to 14
CF	[byte]	(reserved for multi-point communications)
D0	[data...]	Write bytes set by remainder of Byte Count
D1 - DF	[data...]	Write 1 to 15 bytes
E0	[byte]	Read 0 to 255 bytes
E1 – EF		Read 1 to 15 bytes
F0 - FF		(not used)

Slave Packets

The SY7T612+S1 replies to the host processor either with an acknowledge (either ACK or NACK) or with data. The format of slave packets depends upon the type of response to the master device. The table below lists the reply codes and their meanings.

Table 19: Slave Reply Codes

Code	Definition
0xAA	Acknowledge with data.
0xAE	Auto Reporting Header (with data).
0xAD	Acknowledge without data.
0xB0	Negative Acknowledge (NACK).
0xBC	Command not implemented.
0xBD	Checksum failed.
0xBF	Buffer overflow (or packet too long).
- timeout -	Any condition too difficult to handle with a reply.

SPI Indirect Access Protocol Description

The indirect access method supplies a set of memory locations in a user accessible address space which allows reliable access to a larger memory space using any serial interface than might otherwise be available.

Registers

The indirect method is implemented using several registers in user accessible space. The location of these registers may be solution dependent.

Table 20: Indirect Access Registers

Register Name (protocol.)	Access Type	Description
indirect.rd.addr	RD/WR	Indirect Read Address and Control
indirect.rd.data	R	Indirect Read Data
indirect.wr.data	W	Indirect Write Data
indirect.wr.addr	RD/WR	Indirect Write Address and Control

Indirect Read Access

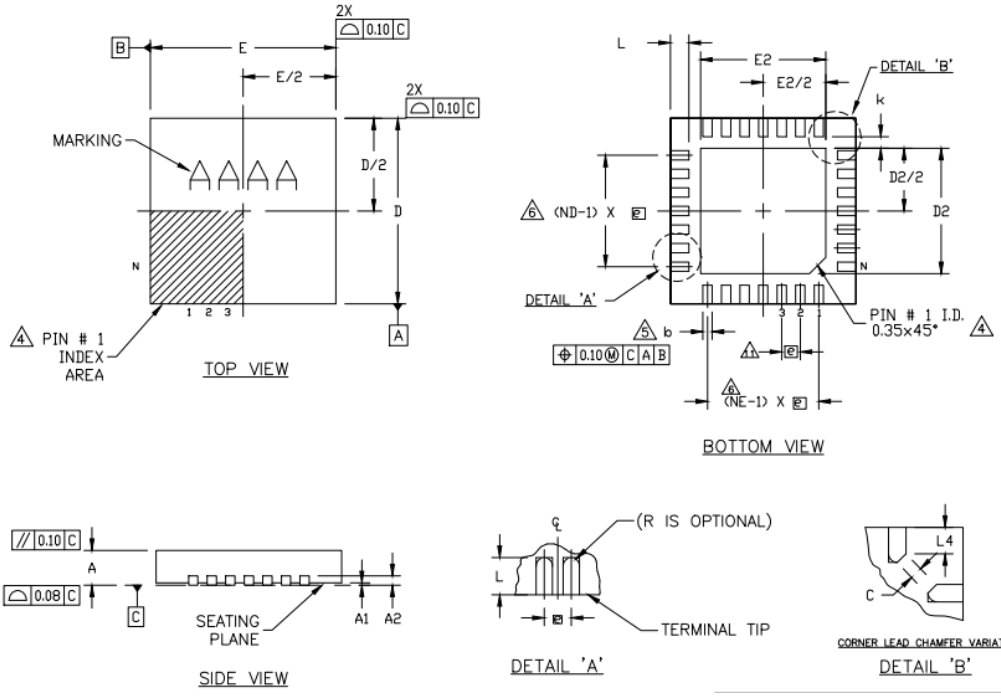
The solution supplies a method for indirect read access to the device memory. The firmware will put the content of the device's RAM memory at the word address determined by (**protocol.indirect.rd.addr** mod(256)) into the output register **protocol.indirect.rd.data.** This potentially modified address value is also written back into **protocol.indirect.rd.addr**. The firmware performs this check and updates the output data register once every high rate sample.

Indirect Write Access

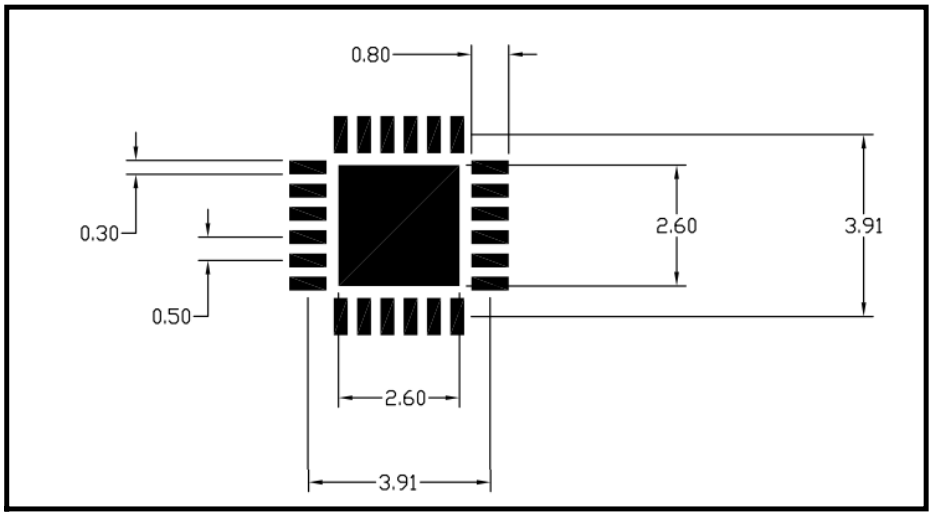
The solution supplies a method for indirect write access to the device memory. If any of the upper 8 bits of **protocol.indirect.wr.addr** are nonzero, the firmware writes the contents of **protocol.indirect.wr.data** into the word address determined by (**protocol.indirect.wr.addr** mod(256)). This modified address value is also written back into **protocol.indirect.wr.addr** to indicate that the write has completed. The firmware performs this check and updates the output registers once every high rate sample.

Packaging

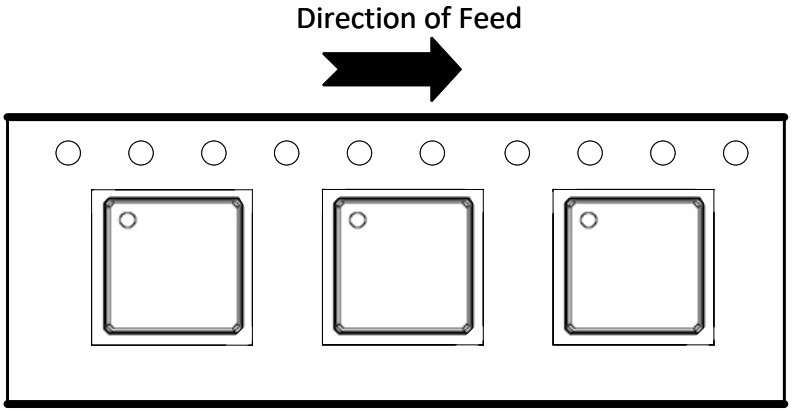
Package Outline and Land Pattern



COMMON DIMENSIONS			
PKG	24L 4x4		
REF.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.0	0.02	0.05
A2	0.20 REF		
b	0.18	0.23	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
e	0.50 BSC.		
k	0.25	–	–
L	0.30	0.40	0.50
N	24		
ND	6		
NE	6		
Jedec Var.	WGGD-2		



Tape & Reel Orientation



Contact Information

For more information about the SY7T612, contact support.em@silergy.com

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0.3	05/18/2022	First Issue	-
0.4	05/22/2022	Corrected pin assignment table	4

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