SY26512A

High Efficiency, 16V, Synchronous Step-Up Regulator With 10A Programmable Current Limit

General Description

The SY26512A high efficiency, high power density, synchronous step-up regulator operates using adaptive constant off-time and current mode control, a wide input voltage range from 2.9V to 16V. It integrates switches with low $R_{DS(ON)}$ to minimize conduction loss.

The SY26512A features selectable PFM/PWM light load operation mode, cycle-by-cycle peak current limit, and internal soft-start to limit inrush current. The programmable pseudo-constant frequency reduces output voltage ripple and enables using smaller external capacitors and inductor.

The programmable peak current limit enables using smaller inductor sizes for applications that require lower output current.

The SY26512A is available in a compact QFN, 3mm×3mm 20 pin package.

Features

- 2.9V to 16V Input Voltage Range
- 16V Maximum Output Voltage
- 1.5 µA Shutdown Current (Typ.)
- 200 µA Quiescent Current (Typ.)
- Low $R_{DS(ON)}$ for Internal N-Channel MOSFET: 10mΩ Main, 20mΩ Rectifier
- Programmable Peak Current Limit
- Programmable Pseudoconstant 400kHz-2MHz Frequency
- PFM/PWM Selectable Light Load Operation Mode
- Internal Loop Compensation
- Internal Soft-Start Limits Inrush Current
- Input Voltage UVLO
- Output Overvoltage Protection
- Overtemperature Protection
- RoHS-Compliant and Halogen-Free
- Compact QFN3mm×3mm-20 Package

Applications

- Power Banks
- E-cigarettes
- Bluetooth Speakers

Typical Application

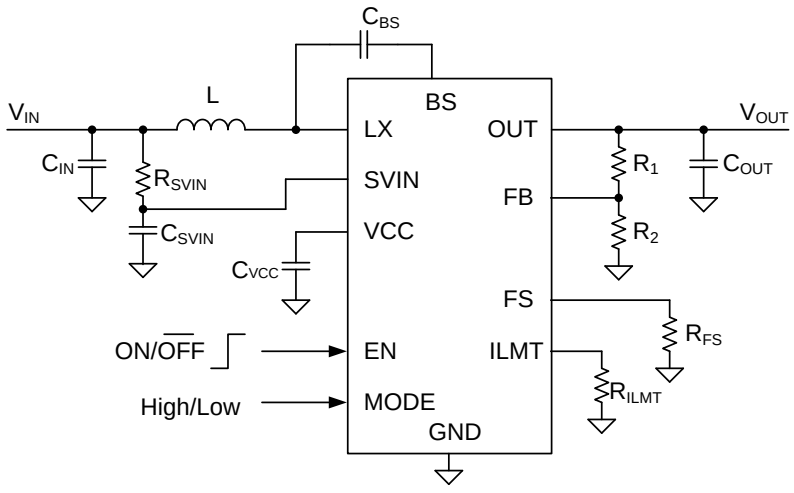

Figure 1. Typical Application Circuit

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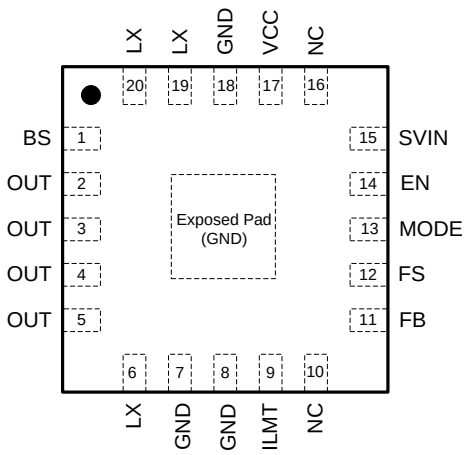
Ordering Information

Ordering Part Number	Package type	Top Mark
SY26512ARAC	QFN3×3-20 RoHS-Compliant and Halogen-Free	**EQR*xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin Number	Pin Name	Pin Description
1	BS	Bootstrap pin. Rectifier FET's gate driver supply. Connect a 0.1µF ceramic capacitor between the BS and LX pins. Do not connect a resistor in series with the capacitor.
2,3,4,5	OUT	Boost converter output pin.
6,19,20	LX	Inductor node. Connect an inductor from the power input to the LX pin.
7,8,18, EP	GND	Ground pin. Connect to system GND.
9	ILMT	Switch peak current limit setting. Connect a resistor from this pin to GND. When MODE pin is low (PFM light load mode), $I_{LMT}(A) = 1200/R_{ILMT}(k\Omega) - 2$. When MODE pin is high (PWM mode), $I_{LMT}(A) = 1200/R_{ILMT}(k\Omega) - 3$.
10,16	NC	Not connected.
11	FB	Feedback pin. Connect to the center of the resistor voltage divider to program the output voltage: $V_{OUT} = 1V \times (R_1/R_2+1)$.
12	FS	Switching frequency setting pin. Connect a resistor from this pin to ground to program the switching frequency. Leave this pin open for default 300kHz switching frequency. $f_S(kHz) = 73565/R_{FS}(k\Omega) + 300$
13	MODE	Operating mode selection under light load. Pull this pin low for PFM operation, or pull this pin high for PWM operation. Do not leave floating.
14	EN	Enable control. Pull this pin high to turn on the IC. Do not leave floating.
15	SVIN	Power supply input pin. Decouple this pin to the GND pin with a ceramic capacitor of at least 1µF.
17	VCC	Output of the internal LDO regulator. Decouple this pin to the GND with a ceramic capacitor of at least 1µF.

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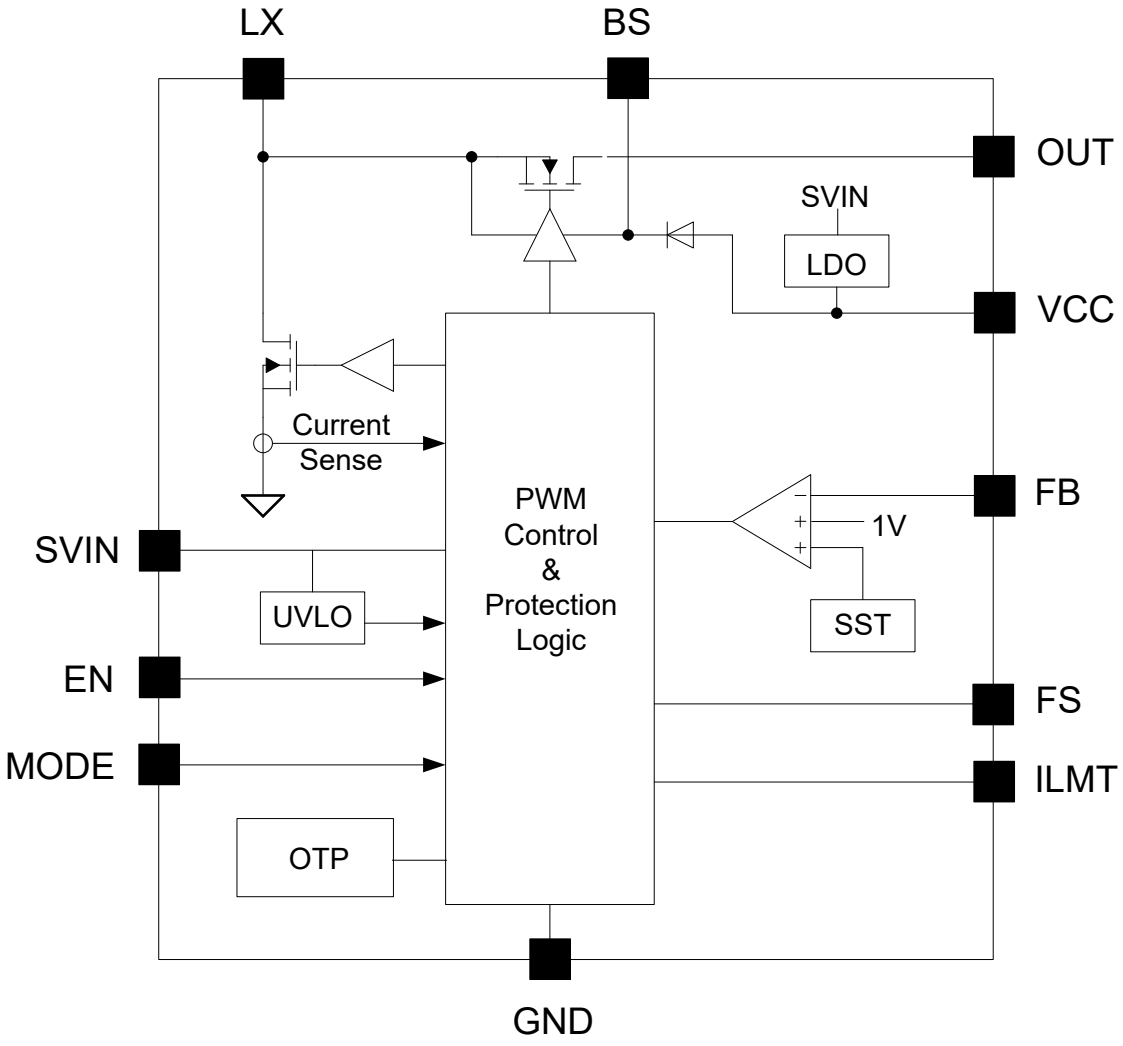
Block Diagram



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Absolute Maximum Ratings

Parameter (Note1)	Min	Max	Unit
SVIN, LX, OUT, ILMT, FS, MODE, EN	-0.3	18	V
FB, VCC, BS-LX	-0.3	4	
LX, 10ns Duration	-3.5	22	
Lead Temperature (Soldering, 10 sec.)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	32	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	4	
P_D Power Dissipation T_A= 25°C	3.1	W

ESD Ratings

Parameter	Min	Max	Unit
HBM (Human Body Mode)	-2	2	kV
CDM (Charged Device Mode)	-750	750	V

Recommended Operating Conditions

Parameter (Note3)	Min	Max	Unit
SVIN	2.9	16	V
OUT	4	16	
Junction Temperature, Operating	-40	125	°C
Ambient Temperature	-40	85	

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Electrical Characteristics

(V_{IN} = 5V, V_{OUT} = 12V, I_{OUT} = 100mA, T_A = -40°C–125°C, unless otherwise specified; values are guaranteed by test, design, or statistical correlation.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{SVIN}		2.9		16	V
Quiescent Current	I_Q	FB = 1.1 V		200	250	μA
Shutdown Current	I_{SHDN}	EN = 0		1.5	3.5	μA
FB Leakage Current	I_{FB}	V_{FB} = 3.3V	-50		50	nA
Main N-FET R_{ON}	$R_{DS(ON)\_M}$			10	25	mΩ
Rectifier N-FET R_{ON}	$R_{DS(ON)\_R}$			20	45	mΩ
Feedback Reference Voltage	V_{REF}	T_A = 25°C	0.99	1	1.01	V
		T_A = -40°C to 125°C	0.98	1	1.02	V
SVIN UVLO Rising Threshold	$V_{SVIN,UVLO}$				2.9	V
SVIN UVLO Hysteresis	$V_{SVIN,HYS}$			0.25		V
Output OVP Threshold	$V_{OUT,OVP}$		16	17	18	V
Main N-FET Current Limit	I_{LMT}	R_{ILMT} = 100kΩ, MODE = Low	8	10	12	A
		R_{ILMT} = 100kΩ, MODE = High	7	9	11	A
Main N-FET Current Limit Program Range	$I_{LMT,RNG}$		2		10	A
I_{LMT} Reference Voltage	V_{ILMT}			0.6		V
EN/MODE Input Voltage High	$V_{EN/MODE,H}$		1.2			V
EN/MODE Input Voltage Low	$V_{EN/MODE,L}$				0.35	V
Bottom FET Reverse Current Limit	$I_{LMT,\ RVS}$	MODE = High	-3.8	-5.5	-7.2	A
Minimum Peak Current	I_{MIN}	MODE = High			0	A
Switching Frequency Programing Range	$f_{SW,RNG}$	R_{FS} = 43kΩ–735kΩ	400		2000	kHz
Switching Frequency Accuracy	f_{SW}	R_{FS} = 360kΩ	400	500	600	kHz
Minimum On-Time	$t_{ON,MIN}$	(Note 4)		130	160	ns
Minimum Off-Time	$t_{OFF,MIN}$	(Note 4)		120	150	ns
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Package thermal resistance is measured in the natural convection at T_A = 25°C on a four-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Based on simulation result.

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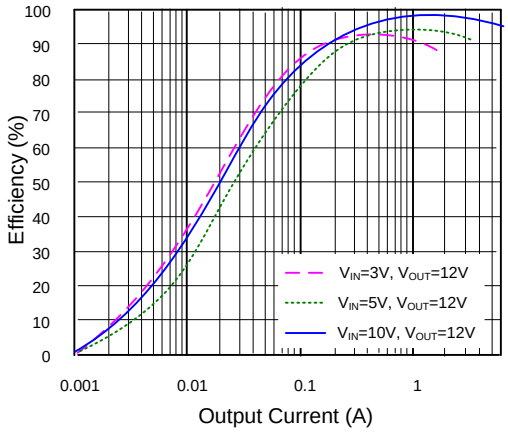
Typical Performance Characteristics

(T_A= 25℃, V_{OUT} = 12V, f_{SW}=500kHz, L = 2.2μH, C_{OUT}= 66μF, unless otherwise specified.)

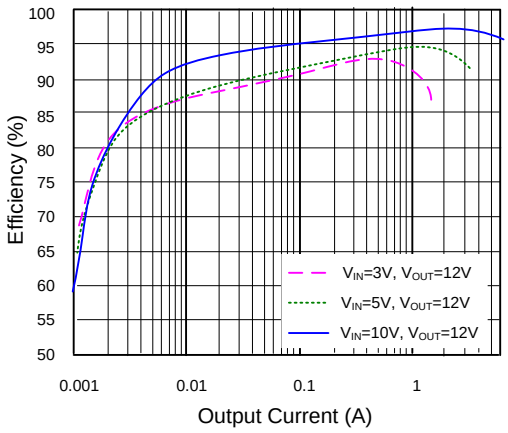
Efficiency vs. Load Current

Mode=high



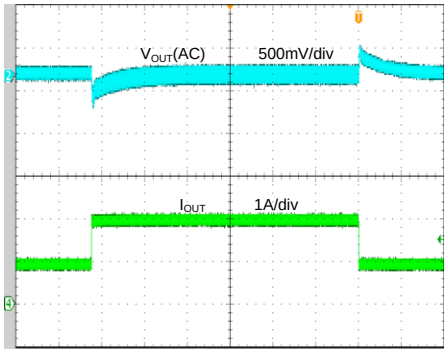
Efficiency vs. Load Current

Mode=low



Load Transient

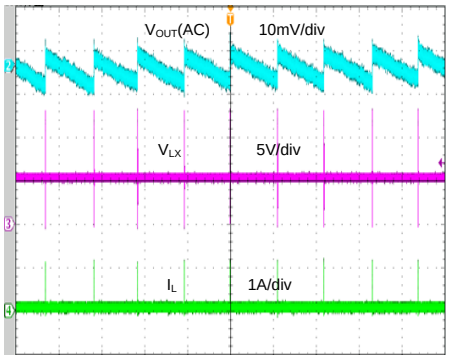
(V_{IN}=5V, V_{OUT}=12V, I_O=1 ~ 2A)



Time (200μs/div)

Output Ripple

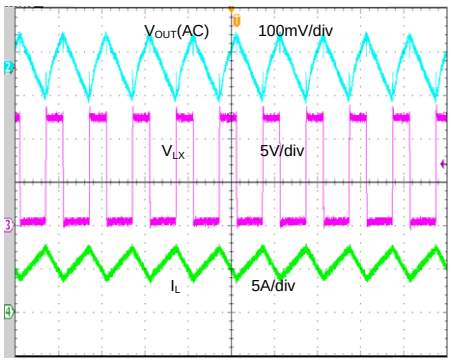
(V_{IN}=5V, V_{OUT}=12V, I_O=0A, Mode=Low)



Time (800μs/div)

Output Ripple

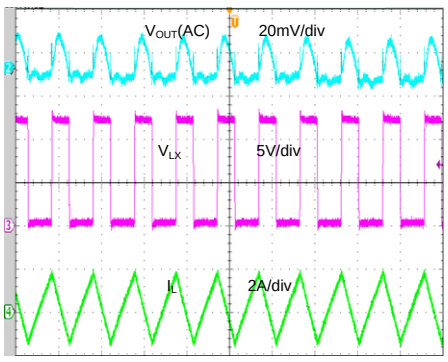
(V_{IN}=5V, V_{OUT}=12V, I_O=2A)



Time (2μs/div)

Output Ripple

(V_{IN}=5V, V_{OUT}=12V, I_O=0A, Mode=High)



Time (2μs/div)

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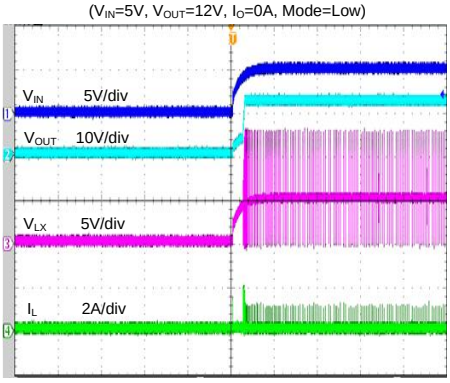
Startup from V_{IN}

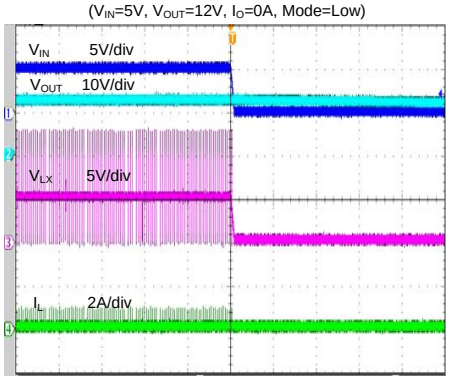
(V_{IN}=5V, V_{OUT}=12V, I_O=0A, Mode=Low)



Time (20ms/div)

Shutdown from V_{IN}

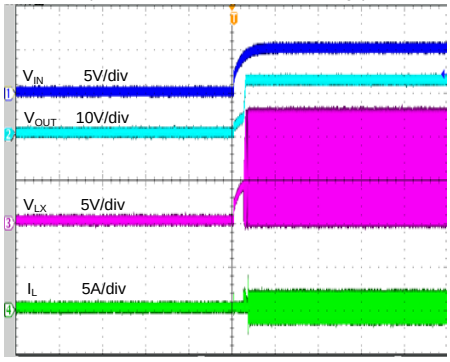
(V_{IN}=5V, V_{OUT}=12V, I_O=0A, Mode=Low)



Time (20ms/div)

Startup from V_{IN}

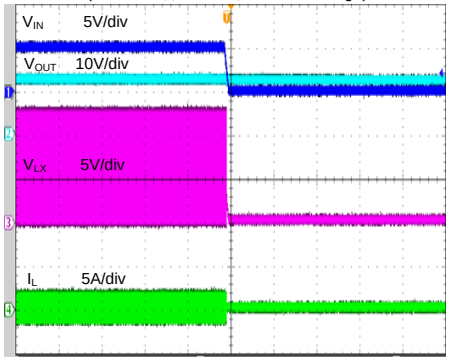
(V_{IN}=5V, V_{OUT}=12V, I_O=0A, Mode=High)



Time (20ms/div)

Shutdown from V_{IN}

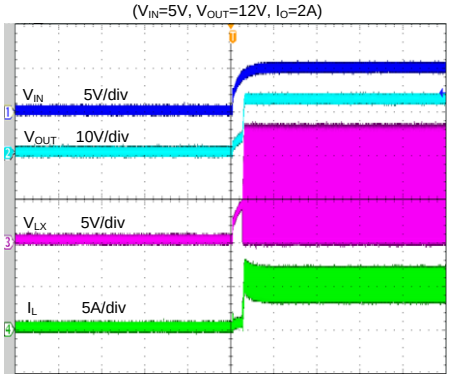
(V_{IN}=5V, V_{OUT}=12V, I_O=0A, Mode=High)



Time (10ms/div)

Startup from V_{IN}

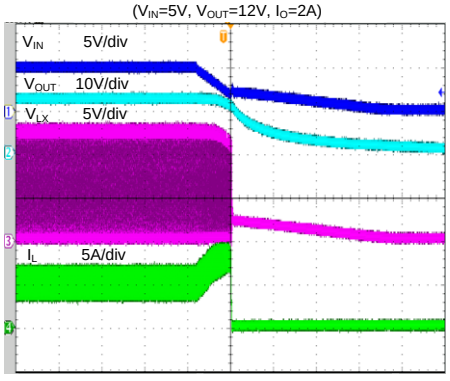
(V_{IN}=5V, V_{OUT}=12V, I_O=2A)



Time (20ms/div)

Shutdown from V_{IN}

(V_{IN}=5V, V_{OUT}=12V, I_O=2A)



Time (200µs/div)

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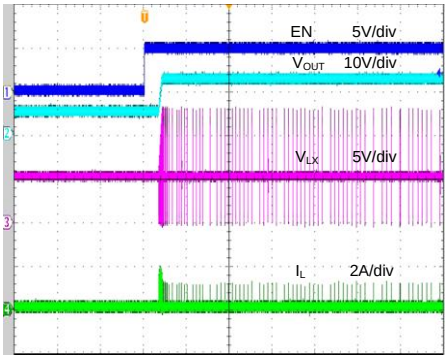
Startup from Enable

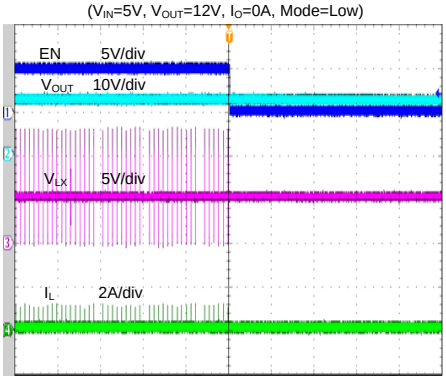
(V_{IN}=5V, V_{OUT}=12V, I_O=0A, Mode=Low)



Time (10ms/div)

Shutdown from Enable

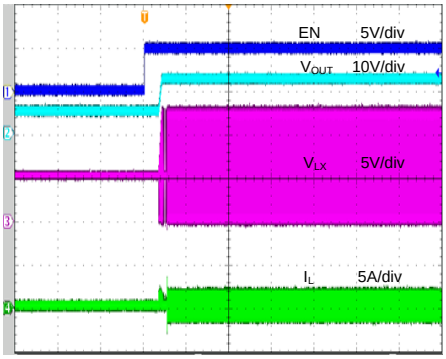
(V_{IN}=5V, V_{OUT}=12V, I_O=0A, Mode=Low)



Time (10ms/div)

Startup from Enable

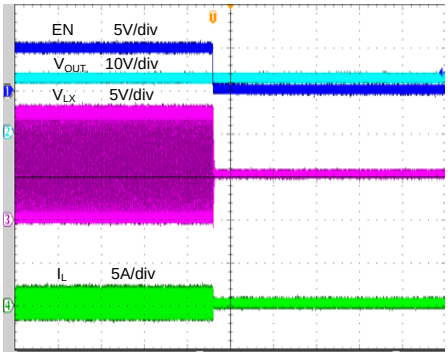
(V_{IN}=5V, V_{OUT}=12V, I_O=0A, Mode=High)



Time (10ms/div)

Shutdown from Enable

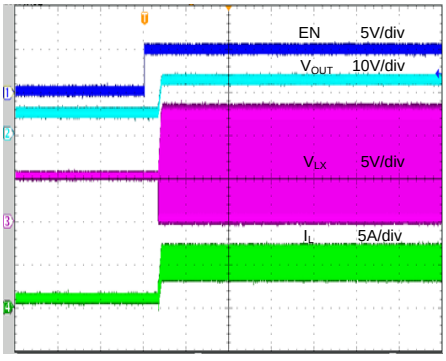
(V_{IN}=5V, V_{OUT}=12V, I_O=0A, Mode=High)



Time (10ms/div)

Startup from Enable

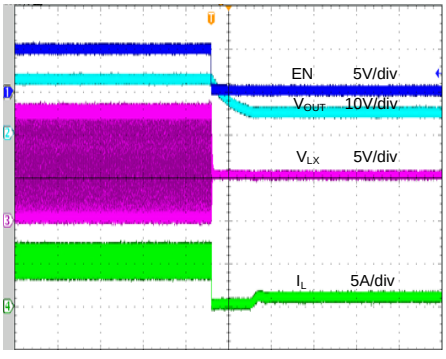
(V_{IN}=5V, V_{OUT}=12V, I_O=2A)



Time (10ms/div)

Shutdown from Enable

(V_{IN}=5V, V_{OUT}=12V, I_O=2A)



Time (200µs/div)

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Detailed Description

The SY26512A high efficiency, high power density, synchronous step-up regulator operates using adaptive constant off-time and current mode control, over a wide input voltage range from 2.9V to 16V. It integrates switches with low $R_{DS(ON)}$ to minimize conduction loss.

The SY26512A features selectable PFM/PWM light load operation mode, cycle-by-cycle peak current limit, and internal soft-start to limit inrush current. The programmable pseudo-constant frequency reduces output voltage ripple and permits smaller external capacitors and inductor.

Enable Operation

Driving the EN pin high (>1.2V) enables normal operation. Driving the EN pin low (<0.4V) places the device in shutdown mode. During shutdown, the SY26512A current drops to less than 3.5μA.

Switching Frequency

The SY26512A switching frequency in CCM can be programmed by adjusting the external resistor R_{FS} connected to the FS pin:

$$f_{SW}\,(kHz) = 73565/R_{FS}(k\Omega) + 300$$

Under PFM light load conditions, the SY26512A linearly folds back the frequency, maintaining high-efficiency.

Light Load Operation Mode Selection

PFM or PWM light load operation is selected using the MODE pin. Pull the MODE pin low (<0.4V) for PFM operation, or high (>1.2V) for PWM operation.

Light Load Operation

If PFM light load operation is selected, under light load conditions, the output of the error amplifier (V_{COMP}) naturally decreases and reduces the peak current. When the COMP voltage further decreases with the reduced load and reaches the preset low threshold, the SY26512A stops switching to decrease the switching power loss and reduce quiescent current to further improve light load efficiency. Switching resumes once V_{COMP} rises above the threshold.

If PWM light load operation is selected, the SY26512A keeps the switching frequency constant for the entire load range. When the load current decreases, the output of the internal error amplifier decreases as well to lower the inductor peak current and deliver less power from input to output. The high-side FET is not turned off, even if the current through the FET goes negative, in order to keep the switching frequency equal to that of the heavy load.

Peak Current Limit Setting

The peak current limit can be programmed using resistor R_{ILMT}:

- Pull the MODE pin low (PFM light load mode), $I_{LMT}(A) = 1200/R_{ILMT}(k\Omega) - 2$
- Pull the MODE pin high (PWM light load mode), $I_{LMT}(A) = 1200/R_{ILMT}(k\Omega) - 3$

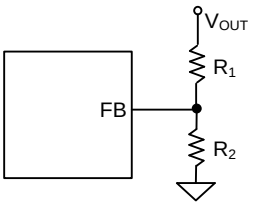
Application Information

The following paragraphs describe the selection process for the feedback resistor divider (R1 and R2), input capacitor C_{IN}, output capacitor C_{OUT}, boost inductor L, and external bootstrap capacitor.

Feedback Resistor Divider R1 and R2

Choose R1 and R2 to program the proper output voltage. Choose large resistance values between 10kΩ and 1MΩ for both R1 and R2 to minimize power consumption under light loads. If a value is chosen for R1, then R2 can be calculated as:

$$R_2 = \frac{R_1}{V_{OUT} - 1}(\Omega)$$



Input Capacitor C_{IN}

Input filter capacitors reduce the ripple voltage on the input, filter the switched current drawn from the input supply, and reduce EMI. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating higher than the system requirements. X5R series ceramic capacitors are most often selected due to their small size, low cost, surge-current capability, and high RMS current ratings over a wide temperature and voltage range. However, systems that are powered by a wall adapter or other long and therefore inductive cabling may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum, or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic

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capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = \frac{V_{IN} \cdot (V_{OUT} - V_{IN})}{2\sqrt{3} \cdot L \cdot F_{SW} \cdot V_{OUT}}$$

For the best performance, use at least two X5R or better grade low ESR 10μF ceramic capacitors and place them as close as possible to the V_{IN} and GND pins. Minimize the loop area formed by C_{IN}, V_{IN}, and the GND pin.

The SVIN capacitor must be placed as close as possible to the SVIN and GND pins. Minimize the loop area formed by C_{SVIN} and the SVIN/SGND pins. A 1μF low ESR ceramic capacitor is recommended for most applications.

Output Capacitor C_{OUT}

The output capacitor is selected to handle the output ripple requirements. Both steady state ripple and transient requirements must be considered when selecting these capacitors. For the best performance, it is recommended to use at least three X5R or a better grade ceramic capacitors with a 25V rating and 22μF capacitance each.

Boost Inductor L

Consider the following when choosing this inductor:

1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{V_{OUT} - V_{IN}}{f_{SW}\, I_{OUT,MAX} \times 0.4}$$

where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY26512A is tolerant to ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

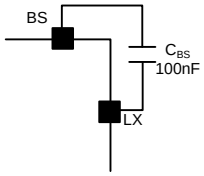
2) The inductor's saturation current rating must be greater than the peak inductor current under full load:

$$I_{SAT,MIN} = \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT,MAX} + \frac{V_{IN}(V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Choose an inductor with DCR less than 10mΩ to achieve good overall efficiency.

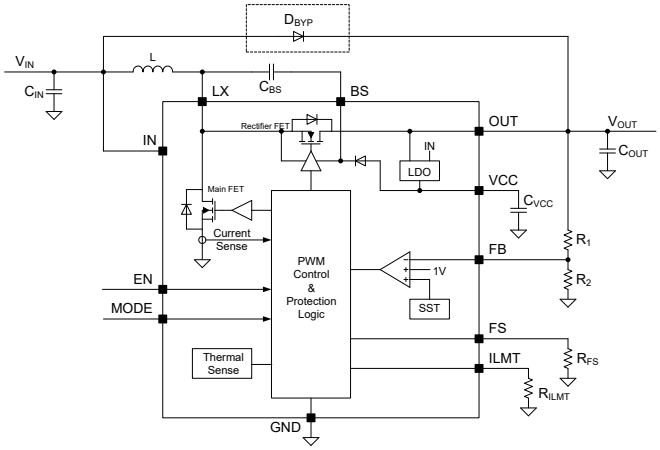
External Bootstrap Capacitor

This capacitor provides the gate driver voltage for the internal rectifier. A 100nF low ESR ceramic capacitor connected between the BS pin and the LX pin is recommended. Do not connect a resistor in series with the capacitor.



Application with Output Short Circuit

The SY26512A does not have short-circuit protection. When OUT is shorted to ground and $V_{OUT} < V_{IN} - V_{DIODE}$, ($V_{DIODE}$ is the forward voltage drop of the rectifier MOSFET body diode), the short-circuit current will directly flow through L and the rectifier MOSFET body diode. This current is mainly determined by the input voltage and short-circuit resistance. The high short-circuit current may damage the device. In order to bypass the short-circuit current in case of output short circuit, place a regular diode with a high current rating from input to output.



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Over Voltage Protection

The SY26512A includes an output over voltage protection. If the output voltage exceeds V_{OVP} (typ. 17V), the part stops switching, and the main switch is turned off. When the output voltage returns to the normal operating range, the device resumes operation.

Thermal Protection

The SY26512A includes over temperature protection circuitry to prevent overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds 150°C. When the junction temperature cools down by approximately 15°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the thermal protection threshold.

Over Current Protection

The SY26512A provides a cycle-by-cycle overcurrent protection and turns off the main power MOSFET once the inductor current reaches the overcurrent limit threshold. During the overcurrent protection, the output voltage drops as a function of the load. If the output voltage drops below the input voltage, the body diode of the MOSFET becomes forward biased, and this diode cannot be turned off. In this case the current is only limited by the DC resistance in the path during the event. As soon as the overload condition is removed, the converter resumes operation.

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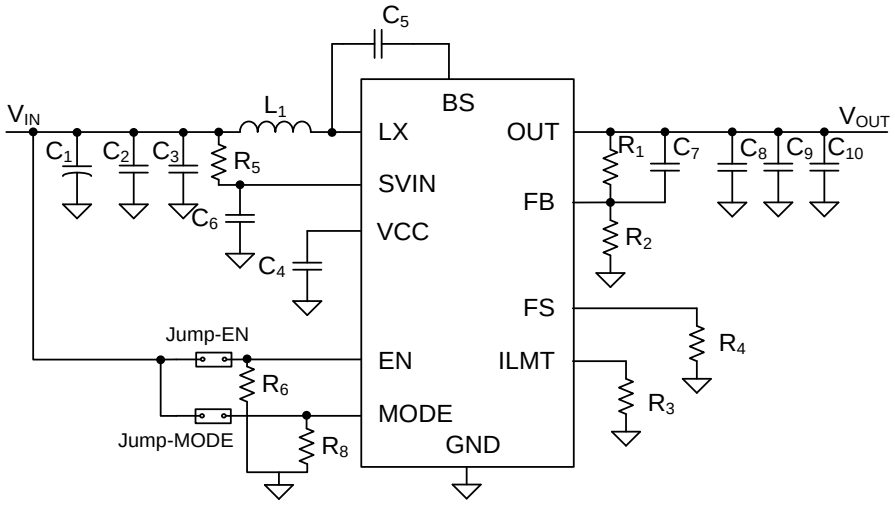
Application Schematic



Design Specifications

Input Voltage (V)	Output Voltage (V)	Input Current Limit (A)
2.9-10	12	1

BOM List

Designator	Description	Part Number	Manufacturer
C1	100μF/25V, Electrolytic Capacitor		
C2, C3	10μF/25V,1206	C3216X5R1E106KT	TDK
C4	2.2μF/16V,0603	C3216X7R1E225K	TDK
C5	100nF/50V,0603	C1608X7R1H104K	TDK
C6	4.7μF/25V,0603	C1608X5R1E475M	TDK
C8,C9,C10	22μF/16V,1206	C3216X5R1C226M	TDK
L1	2.2μH/18A	PCMB104T-2R2MS	CYNTEC
R1	110k , 1%,0603		
R2	10k , 1%, 0603		
R3	100k , 1%, 0603		
R4	300k		
R5	10Ω, 1%, 0603		
R6,R8	1MΩ, 1%, 0603		

Recommended Components for Typical Applications

V_{OUT}(V)	R_H(kΩ)	R_L(kΩ)	L(μH)	C_{OUT}
12	110	10	2.2	3×22μF/16V/X7R,1206
9	80.6	10	1.5	3×22μF/16V/X7R,1206
5	80.6	20	0.68	3×22μF/16V/X7R,1206

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Layout Design

To achieve optimal design, follow these PCB layout considerations:

- Place C_{IN}, C_{SVIN}, C_{VCC}, C_{OUT}, L, R1, and R2 close to the IC
- To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. A ground plane is highly recommended if cost allows.
- C_{SVIN} must be close to pins SVIN and GND. Minimize the loop area formed by C_{SVIN}, S_{VIN}, and GND.
- C_{OUT} must be close to pins OUT and GND. Minimize the loop area formed by C_{OUT}, OUT, and GND.
- To reduce switching noise, minimize the PCB copper area connected to the LX pin.
- In order to reduce crosstalk, R1, R2, and the trace connected to the FB pin must not be adjacent to the LX net on the PCB layout.
- If the system chip interfacing with the EN pin has a high impedance state during shutdown mode, and the SVIN pin is connected directly to a power source such as a Li-ion battery, add a 1MΩ pulldown resistor between the EN and GND pins to prevent noise from falsely triggering the regulator during shutdown mode.

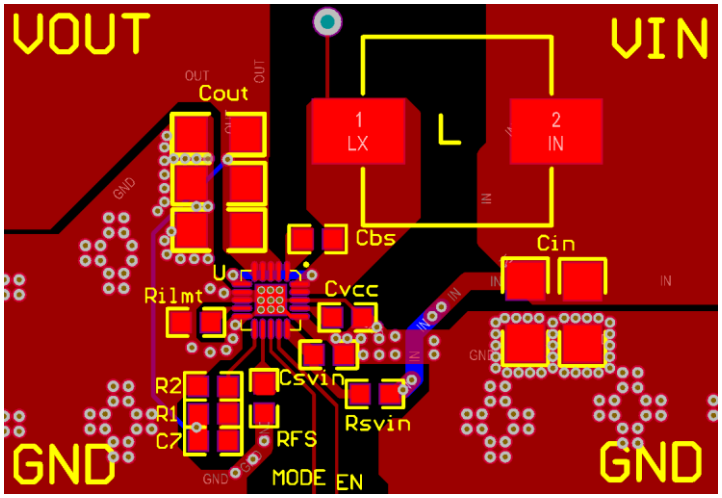

Figure 4. Suggested PCB Layout

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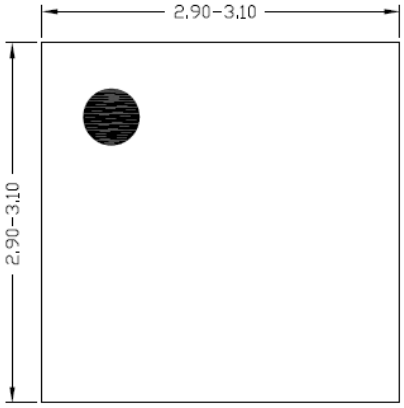
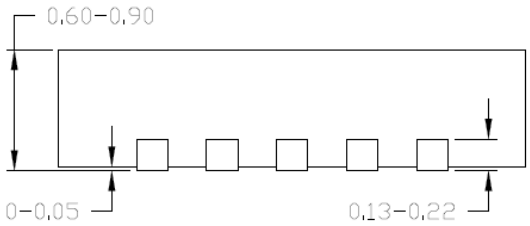
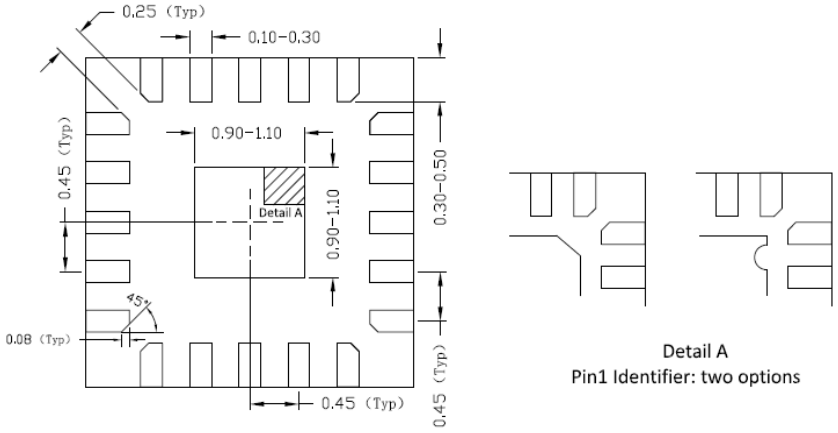
QFN3×3-20 Package Outline and PCB Layout



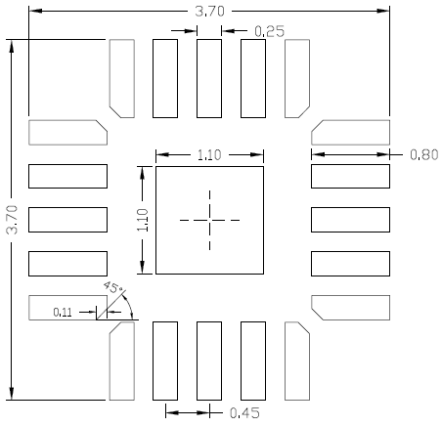
Top view



Side view



Bottom view



Recommended PCB layout (reference only)

Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

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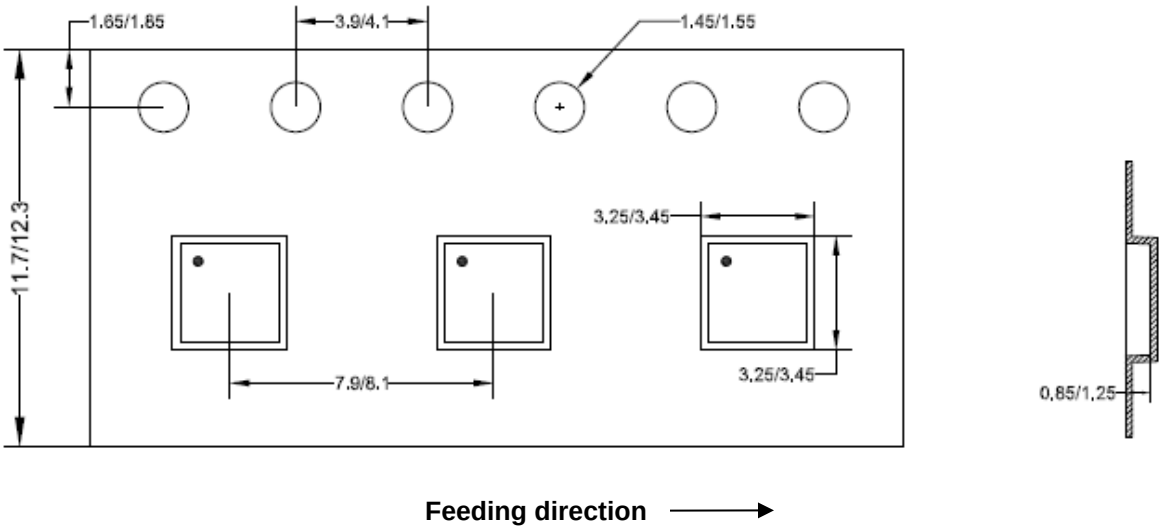
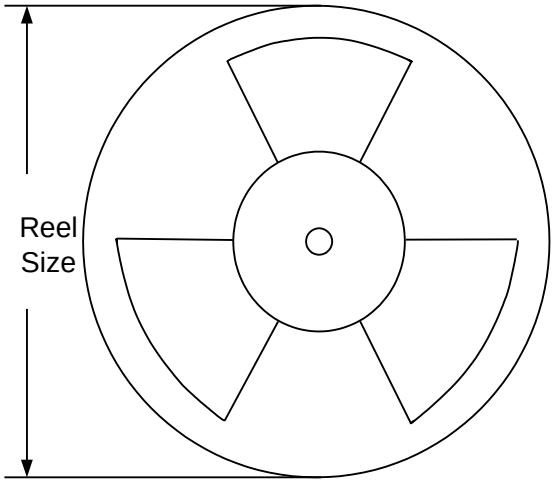
Taping and Reel Specification

QFN3×3 taping orientation



Carrier tape and reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3×3	12	8	13"	400	400	5000

Others: NA

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Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
June 12, 2025	Revision 1.0A	Add the following description to the BS pin description (Page2) and the **External Bootstrap Capacitor** application information (page 10): ---- Do not connect a resistor in series with the capacitor.
Apr.20, 2023	Revision 1.0	Language improvements for clarity.
Jan.24, 2022	Revision 0.9	Initial Release

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