

General Description

The SY28846A is a highly integrated smart switch and power management device with a full suite of protection functions, including a low-power device sleep (DevSleep) mode. Its wide operating input voltage range of 2.7V to 18V makes it ideal for the control of many popular DC BUS voltages.

Integrated back-to-back FETs provide bidirectional current control, making the device well-suited for systems with load-side energy reservoirs that must not drain back to a failed supply BUS.

The device provides many programmable features, including over current, dVo/dt ramp, over-voltage, and under-voltage thresholds using very few external components. The device provides PGOOD, /FLT and precise current monitor output for system status monitoring and downstream load control. Precise programmable and the low I_Q DevSleep mode simplify SSD power management design.

The SY28846A provides true reverse current blocking by monitoring $V_{IN} < (V_{OUT} - 25mV)$. This function supports swift change over to a boosted voltage energy storage element in systems with higher backup voltage than the BUS voltage.

Features

- 2.7V to 18V Operating Voltage, 30V (Max)
- Ultra Low $R_{DS(ON)}$: 42 mΩ R_{ON} (Typical)
- 0.6A to 5.3A Adjustable Current Limit ($\pm 8\%$)
- IMON Current Indicator Output ($\pm 8\%$)
- Operating I_Q : 115μA ($V_{IN} = 12V$, typ.)
- Shutdown Current: 15 μA ($V_{IN} = 12V$, typ.)
- Reverse Current Blocking
- Programmable dV/dt Control
- Power Good and Fault Outputs
- -40°C to 125°C Junction Temperature Range
- QFN3x4-20 package

Applications

- PCIe/SATA/SAS HDD and SSD Drives
- Enterprise and Micro Servers
- Set-Top-Box (STB), DTVs and Game Consoles
- RAID Cards - Holdup Power Management
- Telecom Switches and Routers
- Adapter Powered Devices

Typical Application

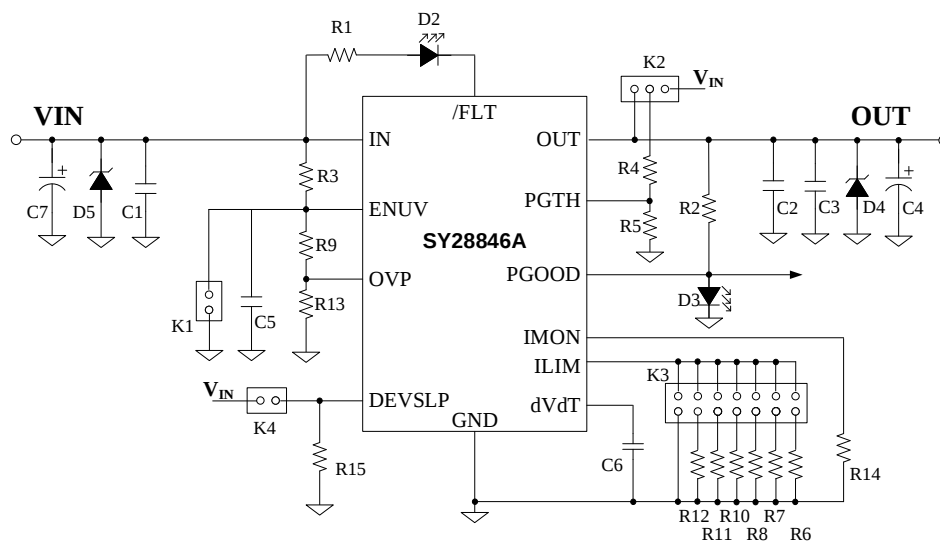


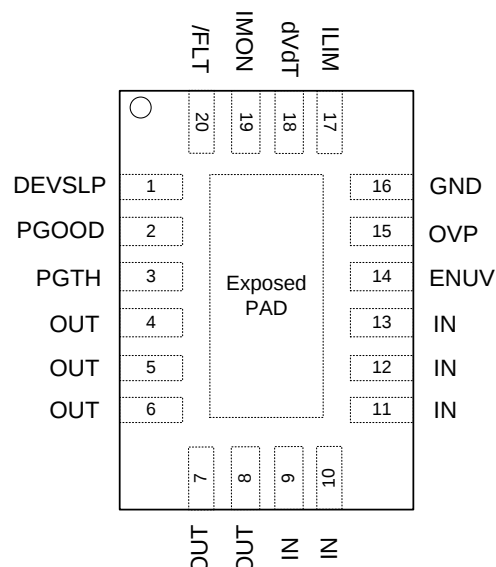
Figure 1. Schematic Diagram

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY28846AQSC	QFN3×4-20 RoHS Compliant and Halogen Free	CTWxyz

x=year code, y=week code, z= lot number code

Pinout (top view)



Pin Name	Pin NO.	I/O	Pin Description
DEVSLP	1	I	Active High. DevSleep mode control. A high level on this pin activates the DevSleep mode (low power mode).
PGOOD	2	O	Open Drain Output. A high impedance state indicates that output voltage has crossed the PGTH pin voltage level.
PGTH	3	I	Positive input of PGOOD comparator.
OUT	4-8	O	Power output of the device.
IN	9-13	I	Power input and supply voltage of the device.
ENUV	14	I	Input for setting programmable under-voltage lockout threshold. An under-voltage event opens internal FET and asserts FLT to indicate power failure.
OVP	15	I	Input for setting programmable over-voltage protection threshold. An over-voltage event opens the internal FET and asserts FLT to indicate over-voltage.
GND	16	-	Ground pin.
ILIM	17	I/O	A resistor from this pin to GND sets the overload and short-circuit current limit.
dVdT	18	I/O	A capacitor from this pin to GND sets the output voltage ramp rate.
IMON	19	O	This pin sources a scaled-down ratio of current through the internal FET. A resistor from this pin to GND converts the current to a proportional voltage, used as an analog current monitor.
/FLT	20	O	Open Drain Output. Fault event indicator, active low to indicate a fault condition due to under-voltage, Over-voltage, Reverse voltage, or thermal shutdown events.
Exposed pad	-		The GND terminal must connect to the exposed PAD. This exposed PAD must be connected to a PCB ground plane using multiple vias for good thermal performance.

Block Diagram

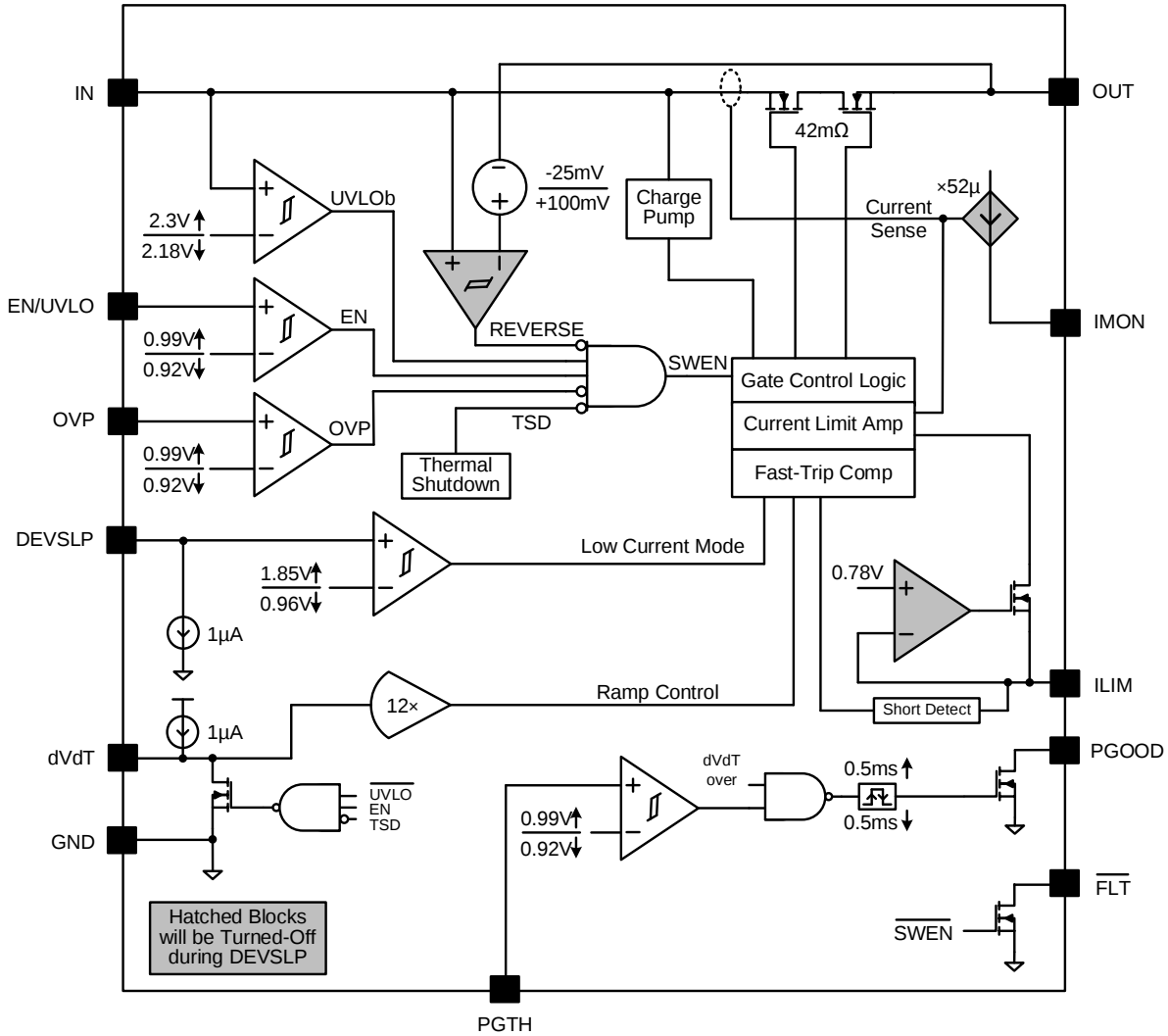


Figure 2. Block Diagram

Absolute Maximum Ratings (1)	Min	Max	Unit
IN, PGTH, PGOOD, ENUV, OVP, DEVSLP, /FLT	-0.3	30	V
OUT	-1	20	
dVdT, ILIM, IMON	-0.3	7	
PGOOD, /FLT, dVdT Sink Current		10	mA
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering,10sec.)		260	
Storage Temperature	-65	150	

Thermal Information (2)	Typ	Unit
θ_{JA} Junction-to-ambient Thermal Resistance	31.5	°C/W
θ_{JC} Junction-to-case Thermal Resistance	26	
P_D Power Dissipation $T_A=25^\circ\text{C}$	3.17	W

Recommended Operating Conditions (3)	Min	Max	Unit
IN	2.7	18	V
OUT, PGTH, PGOOD, ENUV, OVP, DEVSLP, /FLT	0	18	

Recommended Operating Conditions(cont.) (3)	Min	Max	Unit
dVdT, ILIM, IMON	0	6	V
R _{ILIM}	16.9	150	kΩ
R _{IMON}	1		
C _{OUT}	0.1		μF
C _{dVdT}		470	nF
Junction Temperature	-40	125	°C
Ambient Temperature Range	-40	105	°C

Electrical Characteristics

(-40°C ≤ T_J=T_A ≤ 125°C, 2.7V ≤ V_{IN} = 18V, V_{EN/UVLO} = 2V, V_{OVP} = V_{DEVSLP} = V_{PGTH} = 0V, R_{ILIM} = 150kΩ, C_{OUT} = 1μF, C_{dVdT} = OPEN, PGOOD = /FLT = IMON = OPEN. Positive current reaches terminals. All voltages referenced to GND, unless otherwise specified. The values are guaranteed by test, design, or statistical correlation.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage and Internal Under-Voltage Lockout						
Input Voltage Range	V _{IN}		2.7		18	V
Input UVLO Threshold	V _{UVLO}		2.2	2.3	2.4	V
UVLO Hysteresis	V _{HYS}		112	122	132	mV
Shutdown Current	I _{SHDN}	V _{EN/UVLO} = 0 V, V _{IN} = 3 V	3	8.6	15	μA
		V _{EN/UVLO} = 0 V, V _{IN} = 12 V	3	15	20	
		V _{EN/UVLO} = 0 V, V _{IN} = 18 V	3	18.5	25	
Quiescent Current	I _Q	V _{EN/UVLO} = 2 V, V _{IN} = 3 V	60	110	160	μA
		V _{EN/UVLO} = 2 V, V _{IN} = 12 V	65	115	165	
		V _{EN/UVLO} = 2 V, V _{IN} = 18 V	65	115	165	
DevSleep Mode Current	I _{Q_DEVSLP}	V _{DEVSLP} = 0 V, V _{IN} = 2.7V to 18V	60	100	140	μA
Enable And Under-Voltage Lockout (En/UVLO) Input						
EN/UVLO Logic High	V _{ENH}		0.97	0.99	1.01	V
EN/UVLO Logic Low	V _{ENL}		0.9	0.92	0.94	V
EN Threshold Voltage for Low I _Q Shutdown, Falling	V _{SHUTF}		0.3	0.47	0.63	V
EN Hysteresis for Low I _Q Shutdown				66		mV
EN Input Leakage Current	I _{EN}	0 V ≤ V _{EN/UVLO} ≤ 18 V	-100	0	100	nA
Over Voltage Protection (OVP) Input						
Over-voltage Threshold Voltage, Rising.	V _{OVP}		0.97	0.99	1.01	V
Over-voltage Threshold Voltage, Falling.	V _{OVPF}		0.9	0.92	0.94	V
OVP Input Leakage Current	I _{OVP}	0 V ≤ V _{OVP} ≤ 5 V	-100	0	100	nA
Devslp Mode Input (Devslp): Active High						
DEVSLP Threshold Voltage, Rising.	V _{DEVSLPR}		1.6	1.85	2	V
DEVSLP Threshold Voltage, Falling.	V _{DEVSLPF}		0.8	0.96	1.1	V
DEVSLP Input Leakage Current	I _{DEVSLP}	0.2 V ≤ V _{DEVSLP} ≤ 18 V	0.6	1	1.25	μA
Output Ramp Control (dVdt)						
dVdT Charging Current	I _{dVdT}	V _{dVdT} = 0 V	0.85	1	1.15	μA
dVdT Discharging Resistance	R _{dVdT}	V _{EN/UVLO} = 0V, I _{dVdT} = 10mA sinking		16	35	Ω
dVdT to OUT Gain	G _{dVdT}	ΔV _{OUT} /ΔV _{dVdT}	11.65	11.9	12.05	V/V
dVdT Maximum Capacitor Voltage	V _{dVdT_MAX}		1.4	2.5	3.1	V
MOSFET – Power Switch						

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
IN to OUT - ON Resistance	R _{DS(ON)}	1A ≤ I _{OUT} ≤ 5A, T _J = 25°C	34	42	49	mΩ
		1A ≤I _{OUT} ≤ 5A, -40°C ≤T _J ≤85°C	26		58	
		1A ≤I _{OUT} ≤5A, -40°C ≤T _J ≤125°C	26		66	
CURRENT LIMIT PROGRAMMING (ILIM)						
ILIM Bias Voltage	V _{ILIM}			0.87		V
Current Limit	I _{LIM}	R _{LIM} = 150 kΩ, (V _{IN} - V _{OUT}) = 1V	0.53	0.58	0.63	A
		R _{LIM} = 88.7 kΩ, (V _{IN} - V _{OUT}) = 1V	0.9	0.99	1.07	
		R _{LIM} = 42.2 kΩ, (V _{IN} - V _{OUT}) = 1V	1.92	2.08	2.25	
		R _{LIM} = 24.9 kΩ, (V _{IN} - V _{OUT}) = 1V	3.25	3.53	3.81	
		R _{LIM} = 20 kΩ, (V _{IN} - V _{OUT}) = 1V	4.09	4.45	4.81	
		R _{LIM} = 16.9 kΩ, (V _{IN} - V _{OUT}) = 1V	4.78	5.2	5.62	
		R _{LIM} = OPEN	0.35	0.45	0.55	
		R _{LIM} = SHORT	0.55	0.67	0.8	
DevSleep Mode Current Limit	I _{DEVSLP(LIM)}		0.55	0.67	0.8	A
Short-circuit Current Limit	I _{OS}	R _{LIM} = 42.2 kΩ, V _{IN} =12V, (V _{IN} - V _{OUT}) = 5V	1.91	2.07	2.24	A
		R _{LIM} = 24.9 kΩ, V _{IN} =12V, (V _{IN} - V _{OUT}) = 5V	3.21	3.49	3.77	
		R _{LIM} = 16.9 kΩ, V _{IN} =12V, (V _{IN} - V _{OUT}) = 5V, -40°C ≤T _J ≤85°C	4.7	5.11	5.52	
Fast-Trip Comparator Threshold	I _{FASTRIP}		1.4 × I _{LIM} +2			A
Current Monitor Output (IMON)						
Gain Factor I _{MON} /I _{OUT}	G _{IMON}	1 A ≤ I _{OUT} ≤ 5 A	47.78	52.3	57.23	μA/A
Pass Fet Output (OUT)						
OUT Leakage Current in OFF State	I _{LKG_OUT}	V _{IN} =18V, V _{EN/UVLO} = 0V, V _{OUT} = 0V (Sourcing)	-2	0	2	μA
		V _{IN} =2.7V, V _{EN/UVLO} =0V, V _{OUT} = 18V (Sinking)	3	13	20	
V _{IN} -V _{OUT} Threshold for Reverse Protection Comparator, Falling	V _{REVTH}		-40	-25	-10	mV
V _{IN} -V _{OUT} Threshold for Reverse Protection Comparator, Rising	V _{FWDTH}		84	100	116	mV
FAULT FLAG (/FLT): ACTIVE LOW						
/FLT Internal Pull-Down Resistance	R _{/FLT}	V _{OVP} = 2 V, I _{/FLT} = 5 mA sinking	15	30	55	Ω
/FLT Input Leakage Current	I _{/FLT}	0V ≤ I _{/FLT} ≤ 18V	-1	0	1	μA
POSITIVE INPUT for POWER-GOOD COMPARATOR (PGTH)						
PGTH Threshold Voltage, Rising	V _{PGTHR}		0.97	0.99	1.01	V
PGTH Threshold Voltage, Falling	V _{PGTHF}		0.9	0.92	0.94	V
PGTH Input Leakage Current	I _{PGTH}	0 V ≤ V _{PGTH} ≤ 18 V	-100	0	100	nA
POWER-GOOD COMPARATOR OUTPUT (PGOOD): ACTIVE HIGH						
PGOOD Internal Pull-down Resistance	R _{PGOOD}	V _{PGTH} =0V, I _{PGOOD} = 5 mA sinking	15	30	55	Ω
PGOOD input leakage current	I _{PGOOD}	0 V ≤ V _{PGOOD} ≤ 18 V	-1	0	1	μA
THERMAL SHUTDOWN (TSD)						
TSD Threshold	T _{TSD}			160		°C
TSD Hysteresis	T _{TSDhys}			12		°C
OVER-VOLTAGE PROTECTION INPUT (OVP)						
OVP Disable Delay	t _{OVP(dly)}	OVP↑ (100mV above V _{OVPR}) to /FLT↓		2		μs

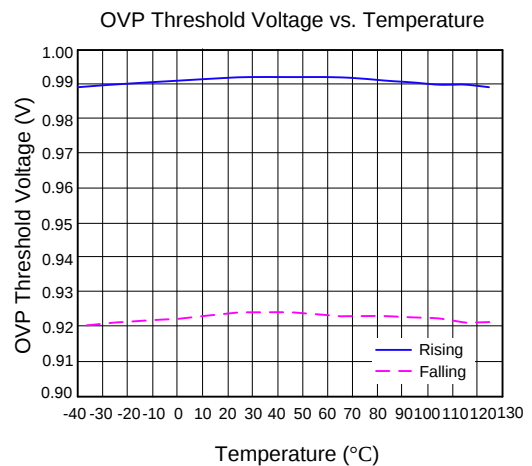
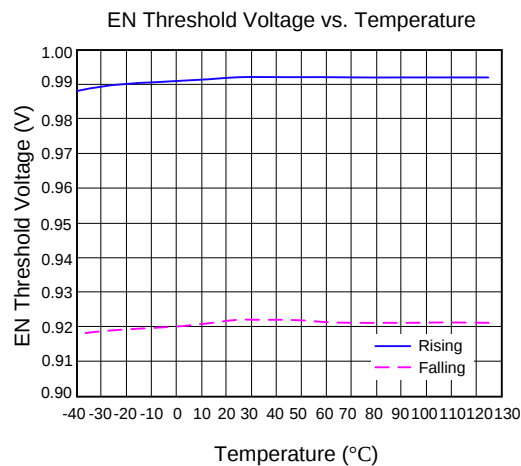
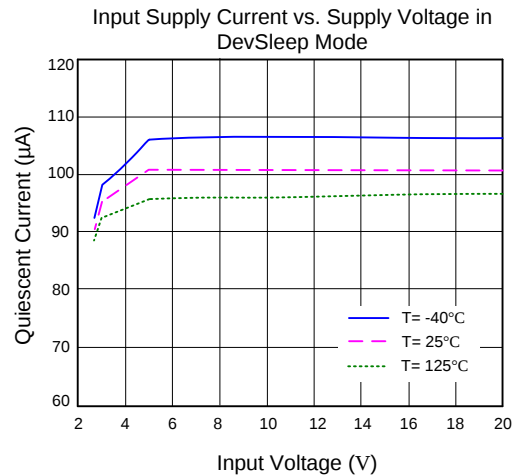
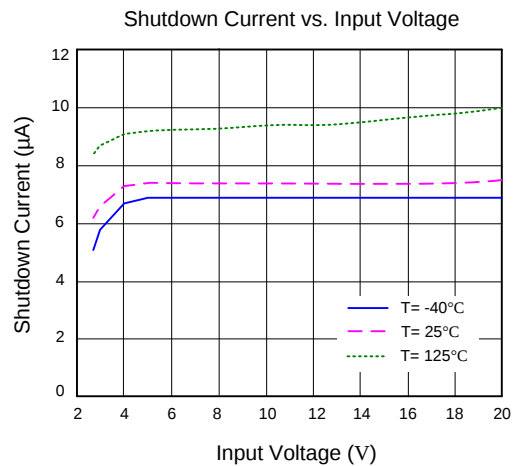
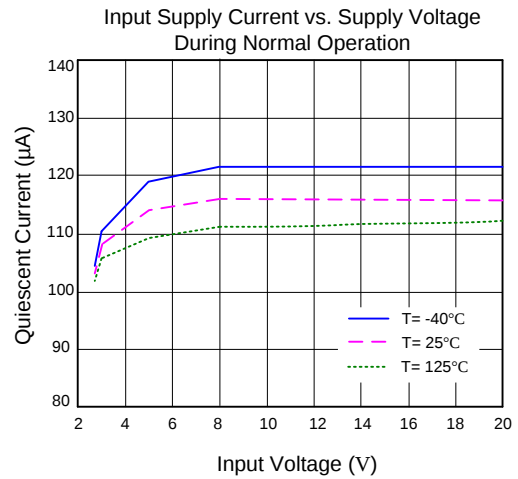
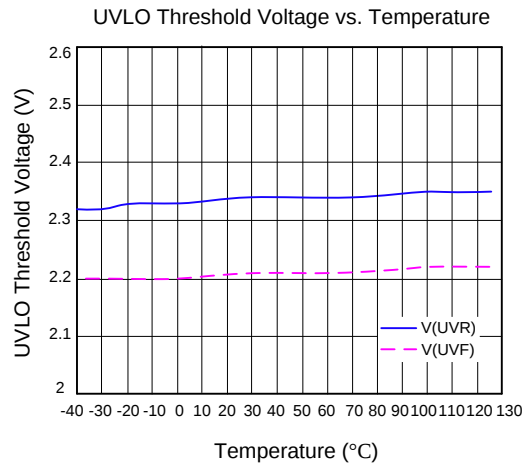
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Enable and UVLO Input						
EN Turn ON Delay	t _{ON(dly)}	EN/UVLO↑ (100mV above V _{ENR}) to V _{OUT} = 100 mV, C _{dVdT} < 0.8 nF		220		μs
		EN/UVLO↑ (100mV above V _{ENR}) to V _{OUT} = 100 mV, C _{dVdT} ≥ 0.8 nF	100 + 150 x C _{dVdT}			μs
EN Turn OFF Delay	t _{OFF(dly)}	EN/UVLO↓ (100mV below V _{ENF}) to /FLT↓		2		μs
Output Ramp Control (dV/dT)						
Output Ramp Time	t _{dVdT}	EN/UVLO ↑ to V _{OUT} = 4.5 V, with C _{dVdT} = open		0.2		ms
		EN/UVLO ↑ to V _{OUT} = 11 V, with C _{dVdT} = open	0.25	0.37	0.5	
		EN/UVLO ↑ to V _{OUT} = 11 V, with C _{dVdT} = 1nF		0.97		
Current Limit						
Fast-Trip Comparator Delay	t _{FASTRIP(dly)}	I _{OUT} > I _{FASTRIP}		200		ns
Reverse Protection Comparator						
Reverse Protection Comparator Delay	t _{REV(dly)}	(V _{IN} - V _{OUT})↓(1 mV overdrive below V _{REVTH}) to /FLT↓		10		μs
		(V _{IN} - V _{OUT})↓(10 mV overdrive below V _{REVTH}) to /FLT↓		1		
	t _{FWD(dly)}	(V _{IN} - V _{OUT})↑(10 mV overdrive below V _{FWDTH}) to /FLT↑		3.1		
Power-Good Comparator Output (PGOOD): Active High						
PGOOD Delay (De-glitch) Time	t _{PGOODR}	Rising edge	0.42	0.54	0.66	ms
	t _{PGOODF}	Falling edge	0.42	0.54	0.66	ms
Thermal Shut Down (TSD)						
Retry Delay in TSD				128		ms

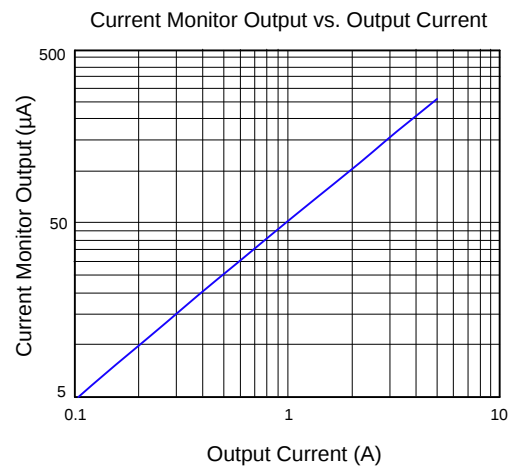
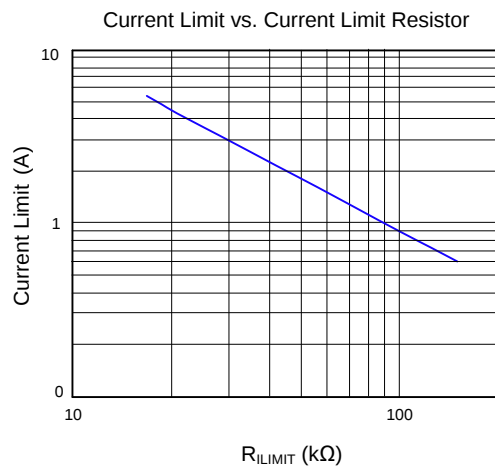
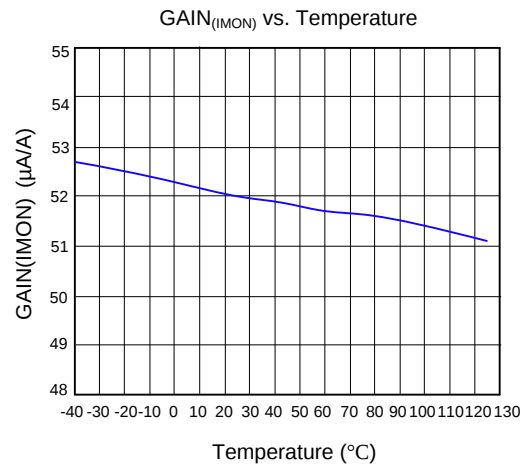
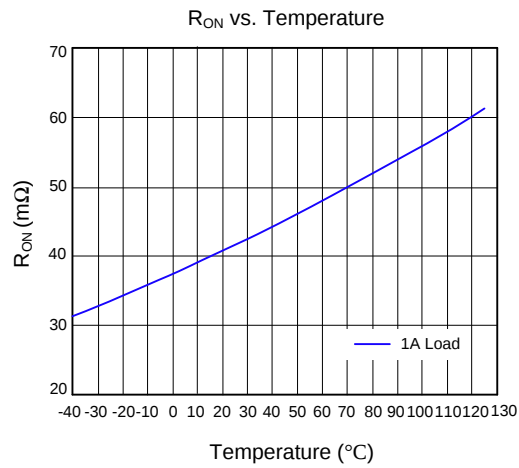
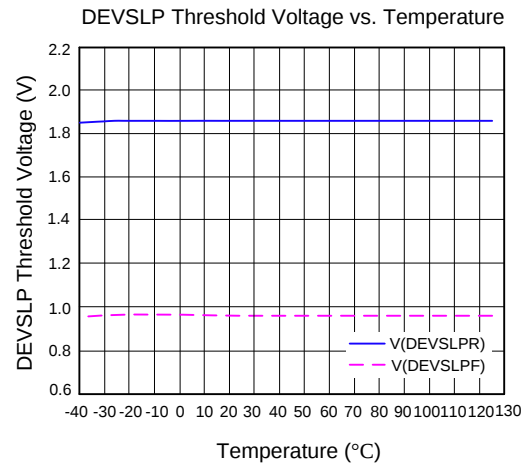
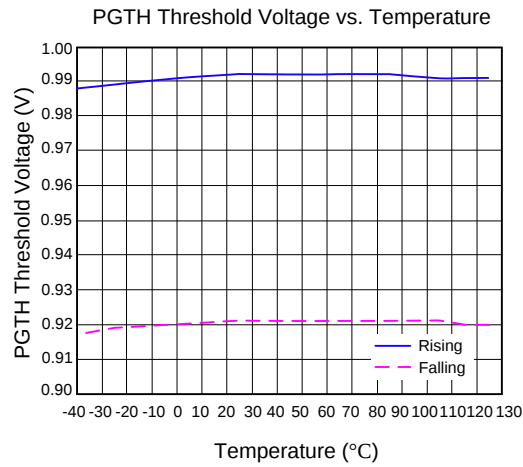
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

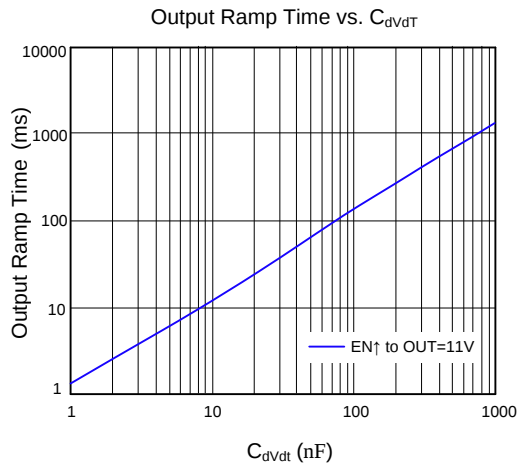
Note 2: θ_{JA} is measured in the natural convection at $T_A = 25^\circ\text{C}$ on a highly effective four-layer thermal conductivity test board of JESD5-2, -5, -7 thermal measurement standards.

Note 3: The device is not guaranteed to function outside its operating conditions.

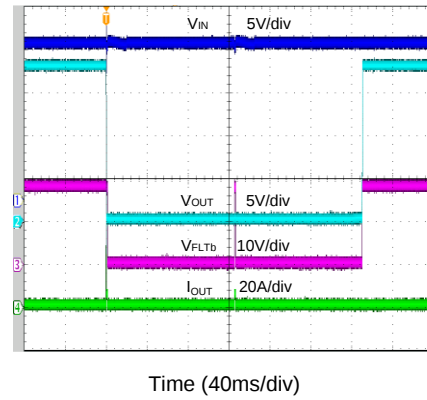
Typical Performance Characteristics



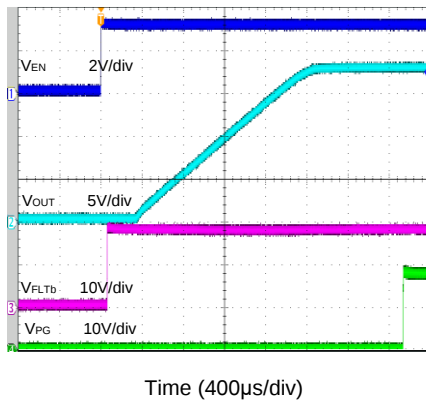




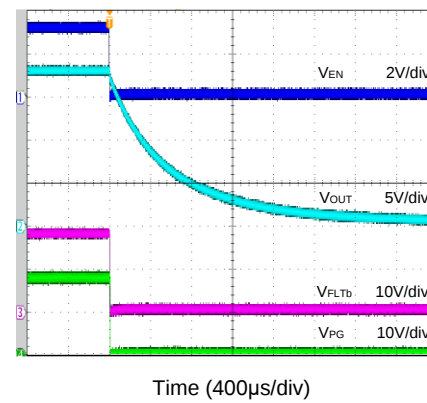
Hard-short: Auto-retry and Recovery from Short ($V_{IN}=18V$, $C_{IN}=C_{OUT}=10\mu F$, $R_{ILIM}=16.9k\Omega$)



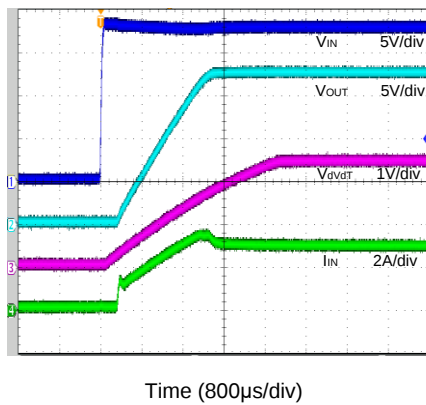
Turn ON with Enable
($V_{IN}=18V$, $C_{dVdt}=1nF$, $C_{OUT}=100\mu F$, 6 Ω Load)



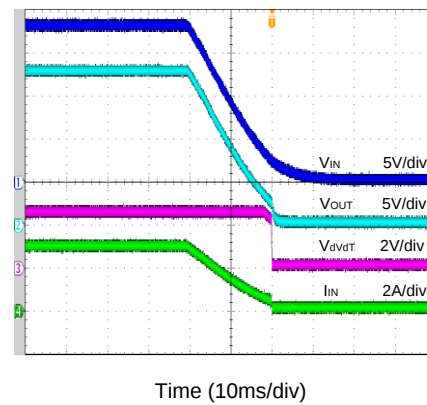
Turn OFF with Enable
($V_{IN}=18V$, $C_{dVdt}=1nF$, $C_{OUT}=100\mu F$, 6 Ω Load)



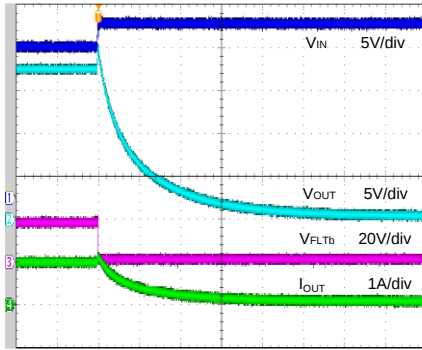
V_{IN} Startup
($V_{IN}=18V$, EN ON, $C_{dVdt}=1nF$, $C_{OUT}=100\mu F$, 6 Ω Load)



V_{IN} Shutdown
($V_{IN}=18V$, EN ON, $C_{dVdt}=1nF$, $C_{OUT}=100\mu F$, 6 Ω Load)

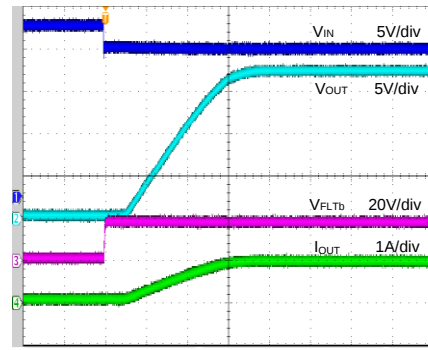


Over-voltage Shutdown
($V_{IN}=18V \rightarrow 20V$, $R_{FLTb}=100k\Omega$, 18 Ω Load)



Time (40 μ s/div)

Over-voltage Recovery
($V_{IN}=20V \rightarrow 18V$, $R_{FLTb}=100k\Omega$, 18 Ω Load)



Time (100 μ s/div)

Operation

The SY28846A is a smart protection switch. It integrates back-to-back FETs and enhanced built-in protection circuitry. It is ideal for power management systems and applications powered from 2.7V to 5V.

For hot-plug applications, the device provides hot-swap power management with an in-rush current limit during a programmable soft-start. The device is equipped with a precision over-current limit used to minimize over design of the input power supply. The device also integrates a short circuit protection that helps protect both the part and system from a sudden high-current event when a short circuit is detected. The over-current limit can be programmed between 0.6A and 5.3A using an external resistor.

Under-Voltage Lockout and Over-Voltage Set Point:

The trip points can be programmed for under-voltage and over-voltage protection. An external resistor network divides the supply voltage for monitoring. Figure 3 illustrates the UVLO and OVP Threshold settings. The values required are calculated by solving the following equations:

$$V_{OVPR} (V) = \frac{R_3}{R_1 + R_2 + R_3} \times V_{OV}$$

$$V_{ENR} (V) = \frac{R_2 + R_3}{R_1 + R_2 + R_3} \times V_{UV}$$

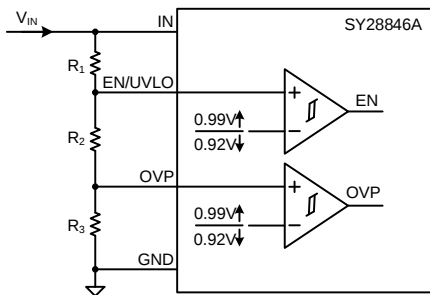


Figure 3.

UVLO and OVP Thresholds Set By R_1 , R_2 and R_3

It is recommended to use larger values of resistance for R_1 , R_2 , and R_3 to minimize the input current drawn from the power supply.

However, this can add errors in these calculations due to leakage currents from external devices connected to the resistor string. Using a resistor string current 20× larger than the expected leakage current is recommended to improve the thresholds accuracy.

Overload Protection:

The device continuously monitors the load current and keeps it limited to the value programmed by R_{ILIM} . During overload events, the current limit is set to I_{LIM} (over-load current limit), as shown in the following equation:

$$I_{LIM} = \frac{89}{R_{ILIM}}$$

Where:

- I_{LIM} is overload current limit in Amperes.
- R_{ILIM} is the current limiting resistor value, in kΩ.

The internal current-limit amplifier regulates the output current to I_{LIM} in the current-limiting state. The output voltage drops, resulting in increased power dissipation for the internal FET, leading to a thermal shutdown, if the condition persists for an extended period. In this case, the device is turned off. During thermal shutdown, the SY28846A enters an auto-retry cycle 128 ms after $T_J < [T_{TSD} - 12^\circ\text{C}]$, and the fault pin /FLT pulls low to signal a fault condition.

Short Circuit Protection:

The device features a separate high-bandwidth current sense comparator with a fast-trip threshold ($I_{FASTrip}$). $I_{FASTrip}$ is adjusted based on the selected current limit:

$$I_{FASTrip} = 1.4 \times I_{LIM} + 2$$

The device's current increases rapidly during a transient short circuit event. As the current-limit amplifier cannot respond quickly to this event due to its limited bandwidth, the fast-trip circuit ensures that the device can respond to and control the current within 1 μs when detecting a short circuit event ($I_{OUT} > I_{FASTrip}$). The fast-trip circuit holds the internal FET off for a few microseconds, after which the current limit amplifier regulates the output current to I_{LIM} . Then, the device behaves similar to an overload condition.

Current Monitoring:

The device provides a current mirror at the IMON pin proportional to the output current. A resistor R_{IMON} connected from the IMON pin to the GND is used to convert the sensed current to a voltage. The sense voltage at IMON pin is calculated from equation:

$$V_{IMON} = (I_{OUT} \times GAIN_{IMON} + I_{IMON_{OS}}) \times R_{IMON}$$

Where:

- $GAIN_{IMON}$ = Gain factor $I_{MON}:I_{OUT} = 52 \mu\text{A/A}$
- I_{OUT} = Load current
- $I_{IMON_{OS}} = 0.8 \mu\text{A (typ)}$

This can be connected to a downstream ADC for system health monitoring. The R_{IMON} needs to be configured based on the maximum input voltage range of the ADC used. R_{IMON} is set using:

$$R_{IMON} = \frac{V_{IMONmax}}{I_{LIM} \times 52 \times 10^{-6}} \text{ k}\Omega$$

If the IMON pin voltage is not digitized with an ADC, R_{IMON} can be selected to produce a 1V/1A voltage at the IMON pin, using the above equation. Choose the closest 1% standard value: 20 k Ω .

This pin should not have a bypass capacitor to avoid delay in the current monitoring information.

IN, OUT, and GND Pins

The device has multiple input (IN) and output (OUT) pins.

All the IN pins should be connected together and to the power source. C_{IN} is a bypass capacitor that helps control transient voltages, limit emissions, and local power supply noise. Where acceptable, a value in the range of 0.1 μ F to 10 μ F is recommended for C_{IN} . The voltage rating should be 20% higher than the maximum expected input voltage.

The GND terminal is the most negative voltage in the circuit and is used as a reference unless otherwise specified.

Device Operation Modes

The SY28846A features a dedicated DevSleep interface pin (DEVSLP) to control the device and help it enter low-power mode. The DEVSLP pin is compatible with standard hardware signals asserted from the host controller. When DEVSLP pin is pulled high, the device starts operating in low-power DevSleep mode. During this mode, the quiescent current is decreased to less than 130 μ A (95 μ A typical), the output voltage remains active, the current limit is set to $I_{DEVSLP(LIM)}$, and the reverse blocking comparator and the current monitor are disabled. All other protections remain active to ensure the system's safety even in DevSleep mode.

Hot Plug-in and In-Rush Current Control

The device has a controlled output slew rate, providing soft start functionality. This limits the inrush current caused by the output capacitor(s) charging and enables these devices to be used in hot-swap applications. The slew rate can be decreased with an external capacitor added between the dVdT pin and the ground (as shown in Figure 4). With an external capacitor present, the slew rate can be determined by the following equation:

$$I_{dVdT} = \left(\frac{C_{dVdT}}{GAIN_{dVdT}} \right) \times \left(\frac{dV_{OUT}}{dt} \right)$$

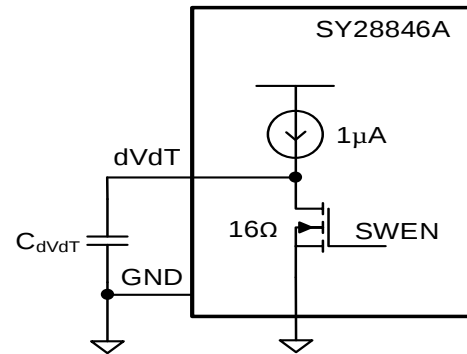


Figure 4.
Output Ramp up Time t_{dVdT} Set by C_{dVdT}

Where:

- $I_{dVdT} = 1\mu\text{A}$ (typical)
- $\frac{dV_{OUT}}{dt}$ = Desired output slew rate
- $GAIN_{dVdT}$ = dVdT to OUT gain = 12

The total ramp time (t_{dVdT}) of V_{OUT} for 0 to V_{IN} can be calculated using the equation:

$$t_{dVdT} = 8.3 \times 10^4 \times V_{IN} \times C_{dVdT}$$

The dVdT pin can be left floating if the slew rate is not decreased. When left floating, the device uses the default value of 48V/ms for the output slew rate.

FAULT Response

The /FLT pin asserts (active low) when one of the following fault conditions are detected: under-voltage, over-voltage, reverse block, and thermal shutdown. The /FLT signal remains asserted until the fault conditions are addressed and the device resumes regular operation. An internal "deglitch" circuit for under-voltage and over-voltage (2.2 μ s typical) filters unexpected false faults during transients on the input bus. Using this pin requires an external pull-up resistor to an external voltage rail. If the /FLT reporting feature is not used in the application, the /FLT pin may be left open or tied to the ground. VIN falling below $V_{UVF} = 2.1 \text{ V}$ resets the /FLT pin status.

Power Good Comparator

The power-good (PGOOD) output can indicate whether the output voltage is above a user-defined threshold and can, therefore, be considered within the acceptable range by downstream DC-DC converters or system monitoring circuits. A resistor divider connected to the PGTH pin sets an accurate power-good threshold for the output voltage. The PGOOD pin is an open-drain output

that is high-impedance when the voltage at the PGTH pin is higher than 0.99 V.

The PGOOD signal has deglitch time incorporated to ensure that internal FET is fully biased before downstream converters apply heavy load. Rising deglitch delay is determined by using the equation:

$$t_{PGOOD(deg)} = \text{Maximum}\{(3.5 \times 10^6 \times C_{dVdT}), t_{PGOODR}\}$$

It requires an external pull-up resistor to the input or output voltage rails. If the PGOOD reporting feature is not used, PGOOD may be left open or tied to the ground.

Thermal Shutdown

Internal over-temperature shutdown turns off the FET when $T_J > 160^\circ\text{C}$ (typical). The SY28846A starts an auto-retry cycle 128ms after T_J drops below $[T_{TSD} - 12^\circ\text{C}]$. During the thermal shutdown, the fault pin /FLT pulls low to signal a fault condition.

PCB Layout Guide

1. A 0.1μF or greater ceramic decoupling capacitor is recommended for all applications between the IN terminal and the GND. For hot-plug applications,

where input power path inductance is negligible, this capacitor can be eliminated or its value reduced.

2. The optimum placement of the decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the device.
3. Place all external components: R_{LIM} , C_{dVdT} , R_{IMON} , and resistors for UVLO and OVP, close to their connection pins. Connect the components to the SGND with the shortest trace length to reduce parasitic effects.
4. Connect the SGND plane to the PGND (main power ground) at a single point, near the input capacitor's negative terminal.
5. Protection devices such as TVS, snubbers, capacitors, or diodes should be placed physically close to the device they intend to protect and routed with short traces to reduce the parasitic inductance. For example, a Schottky diode across the output can be used to absorb negative spikes.

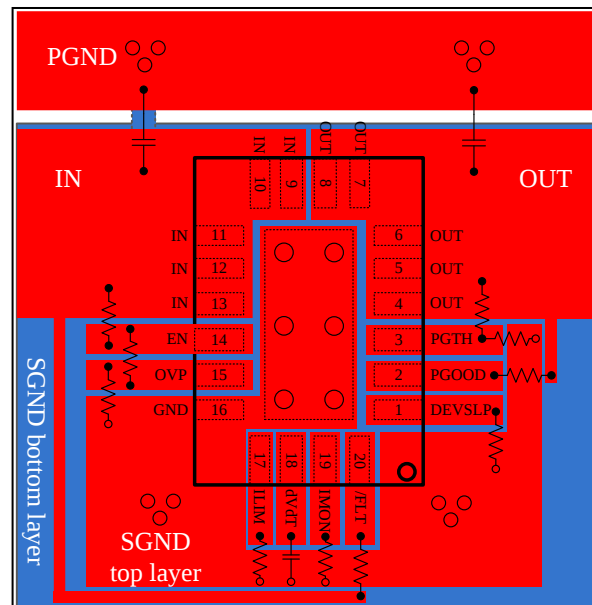
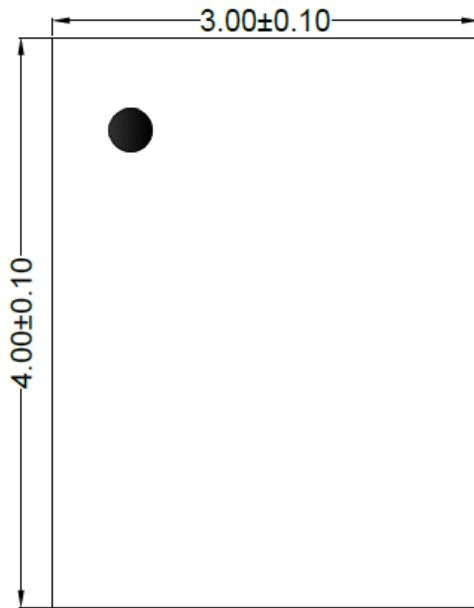
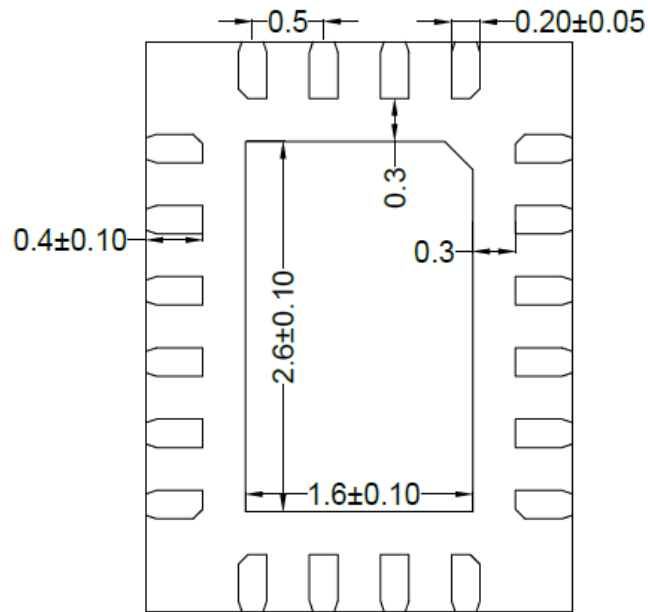


Figure 5. PCB Layout Suggestion

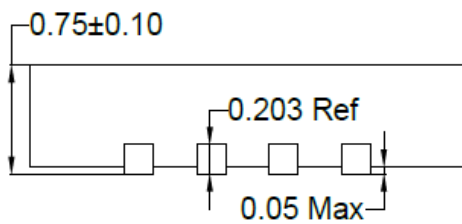
QFN3×4-20 Package Outline Drawing



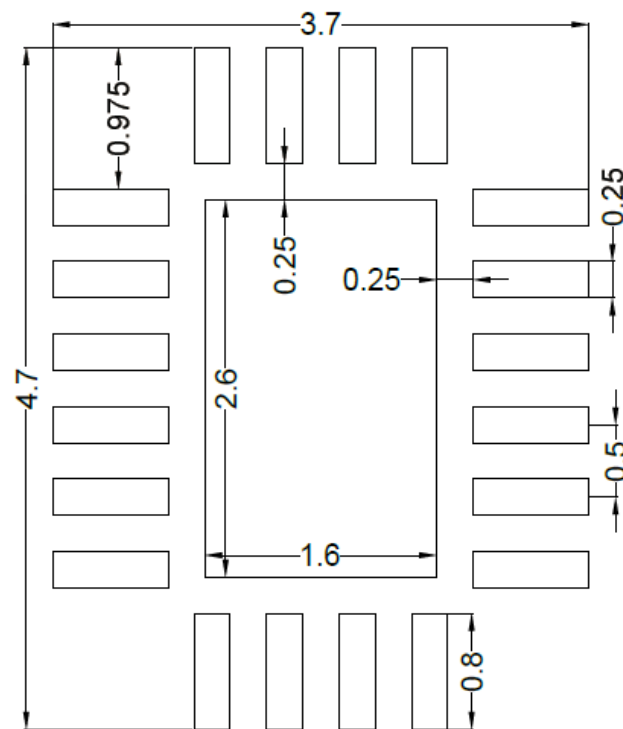
Top View



Bottom View



Side View

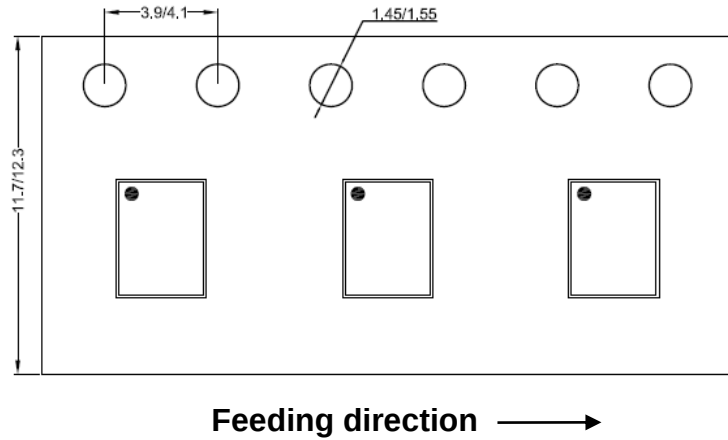


Recommended PCB Layout
(Reference Only)

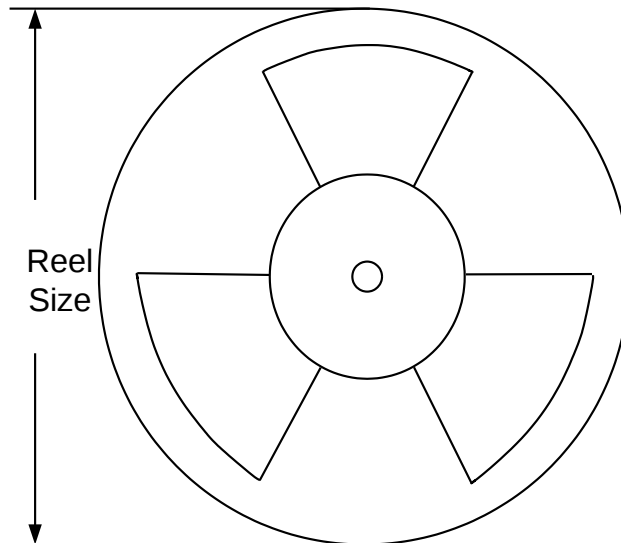
Note: All dimensions are in millimeters and exclude mold flash and metal burr.

Taping & Reel Specification

QFN3×4 Taping Orientation



Carrier Tape & Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3×4	12	8	13"	400	400	5000

Revision History

Date	Revision	Change
Mar.27, 2023	Revision 1.0	Upgraded the version code to Rev1.0 for Production Release. (No change in specification.)
Dec.16, 2020	Revision 0.9A	1. Changed the reverse blocking threshold from -10mV to -25mV in Figure 2 (page 3) 2. Updated /FLT logic circuit in Figure 2 (page 3) 3. Changed OUT absolute maximum ratings from (-0.3V to 20V) to (-1V to 20V) in page 3; 4. Changed "a low effective single layer thermal conductivity test board" to "a high effective four-layer thermal conductivity test board" in Note 2 (page 6) 5. Changed "an internal ramp rate of 12V/ms for output (VOUT) ramp" to "an internal ramp rate of 48V/ms for output (VOUT) ramp".(page 12)
Jun.22, 2020	Revision 0.9	Initial Release

The revision history provided is for informational purposes only and is believed to be accurate; however, it is not warranted. Please make sure that you have the latest revision.

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