SY26741

Switcher for Auxiliary Power Supply

General Description

The SY26741 is a peak current mode flyback/buck switcher that integrates 800V MOS and controller together. It features pseudo fixed frequency control which can avoid sub-harmonic oscillation at CCM and duty>50%. Frequency fold back control is adopted to achieve high efficiency at medium/light load condition. It will enter burst mode at very light or no load condition. When used in flyback topology, IC can be configured to be either PSR or SSR mode. SY26741 has wide VCC operating range from 4.5V to 25.5V, which can support buck converter with as low as 5V output. SY26741 integrates HV start up to achieve fast start up.

The SY26741 also provides comprehensive and reliable protections including VCC OVP, OLP, OTP, input/output OVP (through ENB pin).

The SY26741 is available with compact SSOP10 package.

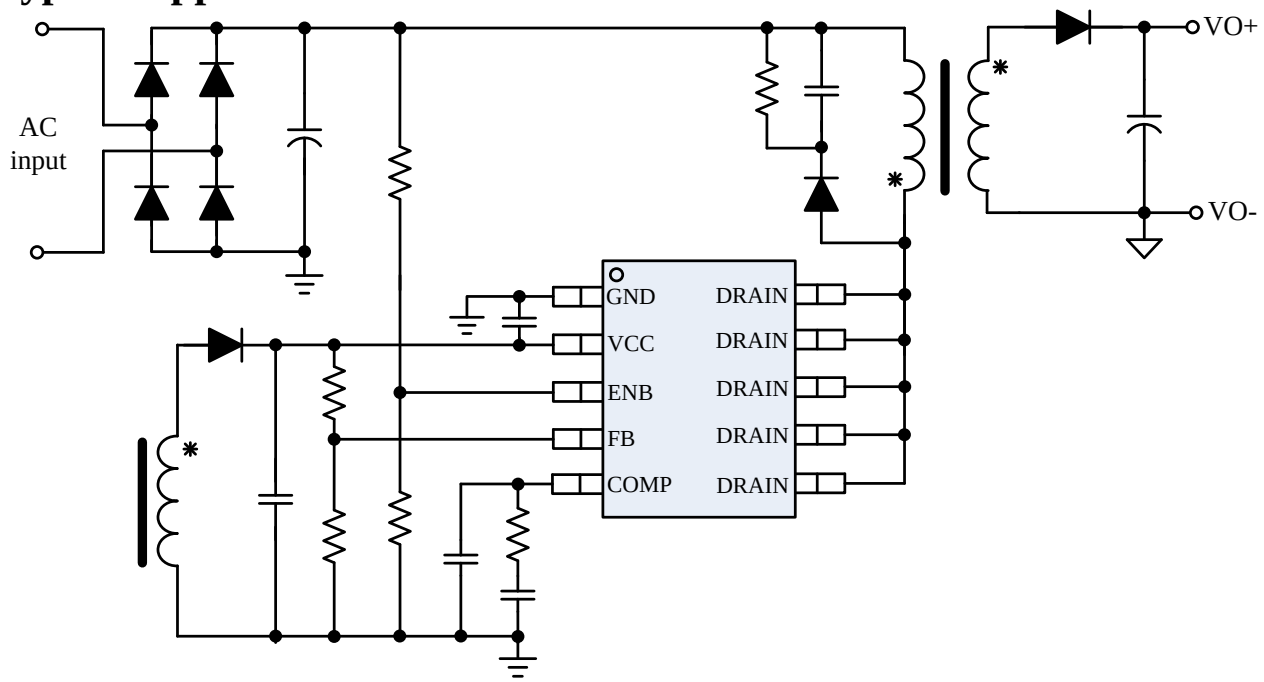
Features

- 800V Power MOS Integrated
- Pseudo Fixed Frequency Control
- Rated Switching Frequency: 60kHz
- Frequency Fold Back and Burst Mode Control
- F_{SW} Modulation to Reduce EMI Noise
- Support Both Flyback and Buck Topology
- PSR/SSR Optional for Flyback Topology
- HV Start Up from DRAIN
- Peak Current Limit: 345mA
- Wide VCC Operating Range: 4.5V~25.5V
- VCC OVP, OLP, OTP, Input OVP (through ENB pin)
- Internal Soft Start Process
- Compact Package: SSOP10

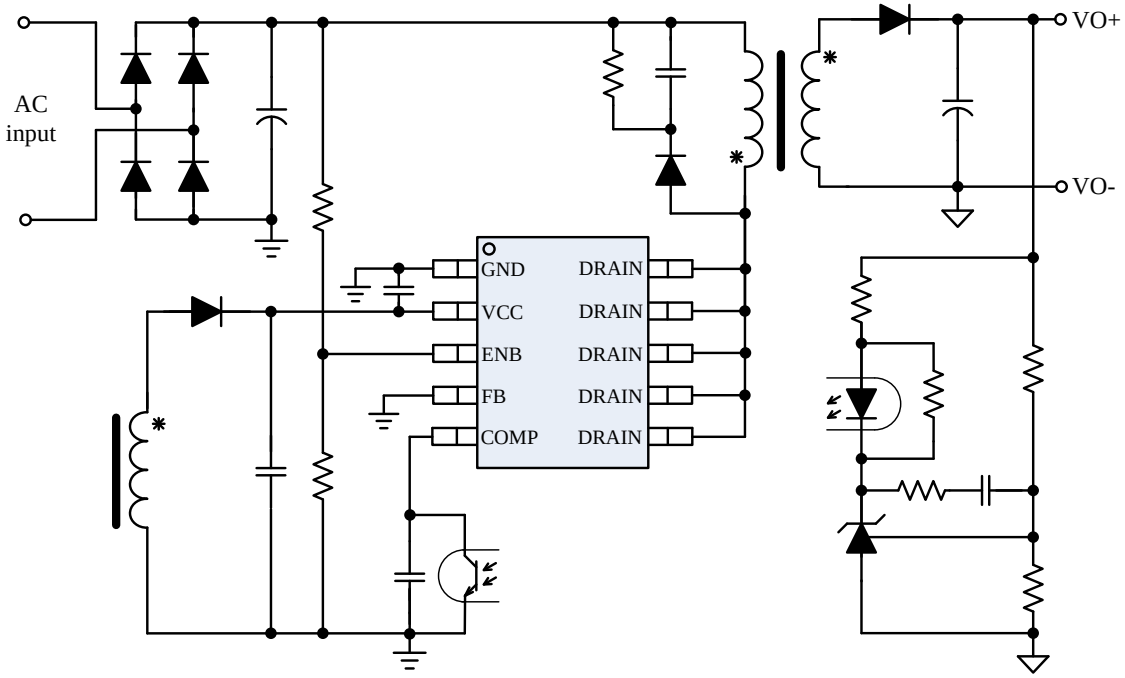
Applications

- Auxiliary Power Supply

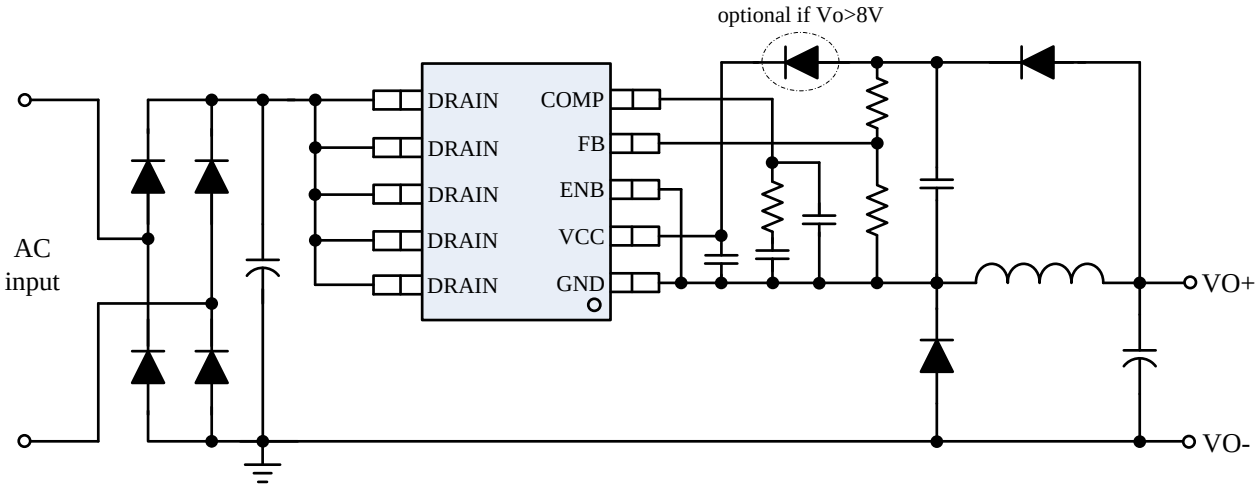
Typical Applications



PSR Flyback



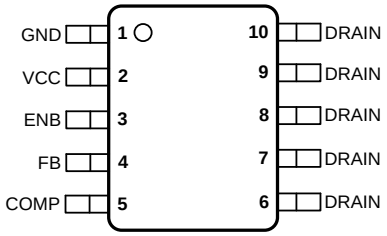
SSR Flyback



Buck

Ordering Information

SY26741□(□□□)
- Package Code
- Optional Spec Code



Pinout (top view)

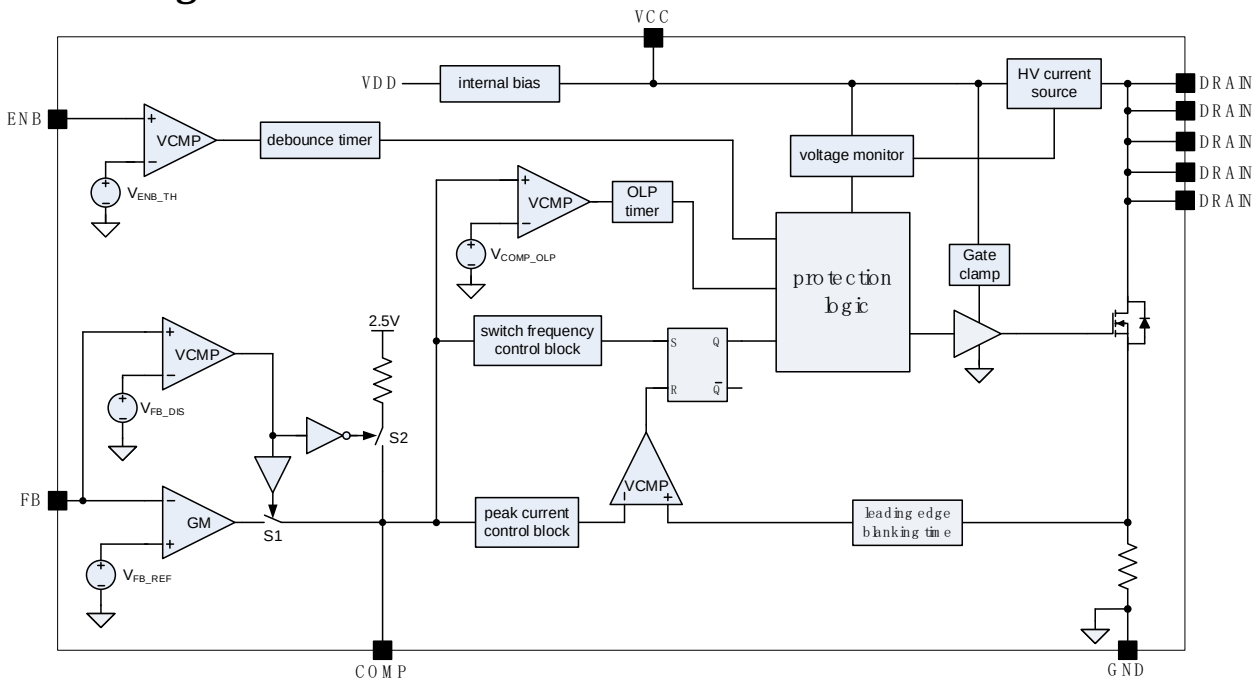
Ordering Number	Package type	Note
SY26741FHP	SSOP10	DEM*xyz*

x=year code, y=week code, z= lot number code

Pinout

Pin Number	Pin Name	Pin Description
1	GND	Ground pin
2	VCC	Supply pin of IC
3	ENB	Disable pin. If voltage on this pin is pulled up to above 1.2V, IC will stop switching. Pull this pin down below 1.2V will enable switching.
4	FB	Output voltage feedback pin. The middle point of a resistor divider between VCC and GND is connected to this pin for output voltage feedback; When SSR flyback is selected, this pin is connected to GND
5	COMP	Loop compensation pin. Connect a loop compensation network between this pin and GND for loop compensation.
6~10	DRAIN	DRAIN of internal power MOSFET and HV start up.

Block Diagram



Block Diagram

F

Absolute Maximum Ratings (Note 1)

DRAIN---------- -0.3~800V
I_{DRAIN} (Pulsed DRAIN current) ---------- 2A
VCC---------- -0.3~28.5V
I_{VCC} (Current sink to clamp VCC) ---------- 12.6mA
ENB---------- -0.3~3.6V
FB---------- -0.3~3.6V
COMP---------- -0.3~3.6V
P_{TOT} (Power dissipation at T_A=25℃) ---------- 1.1W
Junction temperature operating range---------- -45~150℃
Storage temperature---------- -65~150℃
Lead temperature (Soldering, 10sec.) ---------- 260℃
Package thermal resistance (note2)
R_{JP} (junction-pin) ---------- 24℃/W
R_{JA}(junction-ambient)---------- 139℃/W
Avalanche current (note3) ---------- 1.5A
Single pulse avalanche energy (note4) ---------- 1.1mJ

Recommended Operating Conditions

V_{VCC}---------- 4.5V~25.5V
Junction Temperature Range ---------- -40℃ to 125℃
Ambient Temperature Range ---------- -40℃ to 105℃

Electrical Characteristics

(T_J=-40 to 125℃, V_{VCC}=9V (unless otherwise specified))

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
DRAIN Pin						
Break down Voltage	V_{BVDSS}	I_{DRAIN}=250μA, V_{COMP}=GND, T_J=25℃	800			V
Drain-source Leakage Current	I_{DSS}	V_{DS}=400V, V_{COMP}=GND, T_J=25℃			1	μA
OFF-state Drain Current	I_{OFF}	V_{DRAIN}=800V, V_{COMP}=GND, T_J=25℃			1	μA
On Resistance of Power MOS	R_{DSON}	I_{DRAIN}=50mA, T_J=25℃		17	20	Ω
		I_{DRAIN}=50mA, T_J=125℃		34	40	Ω
Equivalent Output Capacitance	C_{OSS_EQ}	V_{GS}=0, V_{DS}=0 to 640V, T_J=25℃		7		pF
Break down Voltage of Start- up JFET	V_{BVDSS_SU}	T_J=25℃	800			V
Drain-source Start up Voltage	V_{HV_START}	V_{VCC}=0V, I_{CHARGE}=500μA			6	V
Leakage Current of start-up Circuit	I_{DRAIN_LK}	V_{DRAIN}=800V, V_{COMP}=GND			3	μA
VCC Charging Current at Start up	I_{CH1}	V_{DRAIN}=100V, V_{VCC}=0V	0.8	1.6	2.4	mA
VCC Charging Current at Start up	I_{CH2}	V_{DRAIN}=100V, V_{VCC}=6V	2.5	4.5	7.2	mA
Max. VCC Charging Current in Self Supply	I_{CH3}	V_{DRAIN}=100V, V_{VCC}=6V	2.5	4.5	7.2	mA
VCC Pin						
Operating Voltage Range	V_{VCC}	V_{GND}=0V	4.5		25.5	V
VCC OVP Threshold	V_{VCC_OVP}		25.5	27	28.5	V
Current Sink to Clamp VCC	I_{VCC_SINK}	V_{VCC}=V_{CC_OVP}	7.4	10	12.6	mA
VCC OVP Debounce Time	T_{VCCOVP_DBC}		190	250	310	μs
VCC ON Threshold	V_{VCC_ON}		7.5	8	8.5	V
HV Current Source Turn on Threshold	V_{CS_ON}	V_{VCC} Falling	4	4.25	4.5	V
VCC UVLO Threshold	V_{VCC_OFF}		3.75	4	4.25	V
Quiescent Current	I_{VCC_Q}	No Switching, V_{FB}>V_{FB_REF}		0.2	0.25	mA
Operating Current	I_{VCC_OP}	V_{DS}=150V, V_{COMP}=1.2V, F_{SW}=60kHz		1.1	1.25	mA
FB Pin						
Reference Voltage	V_{FB_REF}		1.175	1.2	1.225	V
Current Source to Select PSR/SSR Mode	I_{FB_SELECT}	T_J=25℃	80	90	105	μA
EA Disable Voltage	V_{FB_DIS}		250	300	350	mV
Transconductance of EA	G_M	V_{COMP}=1.5V, V_{FB}>V_{FB_REF}	350	500	650	μA/V
Max. Source Current	I_{COMP1}	V_{COMP}=1.5V, V_{FB}=0.5V	70	100	130	μA
Max. Sink Current	I_{COMP2}	V_{COMP}=1.5V, V_{FB}=1.5V	70	100	130	μA

COMP Pin						
Internal Pull up Resistor	R_{COMP}	V_{FB}=GND, I_{COMP}=40uA	32	40	48	kΩ
Current Limitation Threshold	V_{COMP_H}			1.9		V
PFM Threshold	V_{COMP_L}			1.1		V
Threshold to Enter Sleep Mode	V_{COMP_SLPIN}			500		mV
Hysteresis to Exit Sleep Mode	V_{COMP_SLPOUT}			100		mV
OLP Threshold	V_{COMP_OLP}		2.1	2.2	2.3	V
OLP Debounce Time	T_{OLP_DBC}		50	70	90	ms
OLP and Timing						
DRIAN Current Limitation	I_{D_MAX}	T_J=25℃	328	345	362	mA
Power Coefficient	I^2f	$I_{D\_MAX\_TYP}^2 \times F_{SW\_TYP}$	0.9×I^2f	I^2f	1.1×I^2f	A^2×kHz
Min. DRAIN Current at Light Load	I_{D_MIN}	T_J=25℃	75	95	115	mA
Disable Threshold Voltage	V_{DIS_TH}		1.15	1.2	1.25	V
Debounce Time before DIS Protection Tripping	T_{DIS_DBC}		0.5	0.7	0.9	ms
Restart Time after DIS Protection Tripping	$T_{DIS\_RESTART}$		610	760	910	ms
Soft Start Time	T_{SS}		4.9	6	7.1	ms
Min. ON Time	T_{ON_MIN}	V_{COMP}=0.7V, V_{FB}=V_{FB_REF}, T_J=25℃	230	305	380	ns
Restart Time after Fault	$T_{RESTART}$		0.5	0.7	0.9	s
Switching Frequency						
Nominal Switching Frequency	F_{SW_NOM}	T_J=25℃, V_{COMP}=1.5V	55	60	65	kHz
Min. Switching Frequency	F_{SW_MIN}	T_J=25℃, V_{COMP}=0.8V	20	23.5	27	kHz
Modulation Depth (Note5)	F_D			±7F_{SW_NOM}		%
Modulation Frequency (Note5)	F_M			250		Hz
Max. Duty Cycle	D_{MAX}		70		85	%
Thermal Shutdown						
OTP Threshold (Note5)	T_{OTP}		155	163		℃
Hysteresis to resume Operating (Note5)	T_{HYS}			20		℃

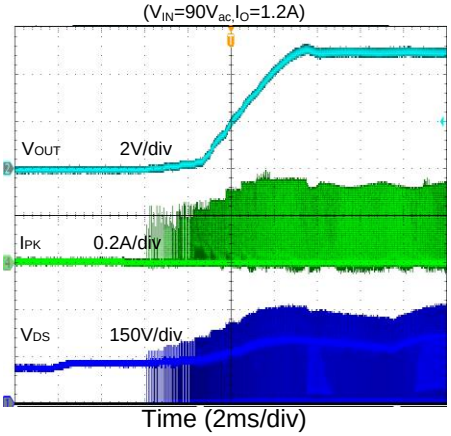
Note1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Note2: R_{JA} is test under still air at T_A=25℃ and chip mounted on a single layer PCB following JESD51-3.
Note3: Repetitive and non-repetitive, pulse width limited by T_{JMAX}.
Note4: Test condition: L=1mH, I_{AS}=1.5A, V_{DS}=50V, R_G=47ohm, starting T_J=25℃.
Note5: Guaranteed by design.

Typical Performance Characteristics

(Test condition: PSR flyback, V_{IN}: 90~264Vac; output spec: 5V/1.2A; T_A=25±5 ℃)

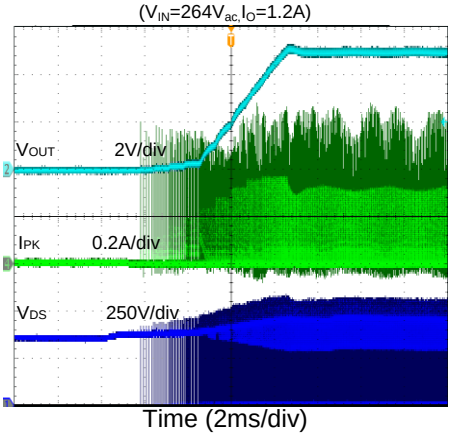
Startup

(V_{IN}=90V_{ac},I_O=1.2A)



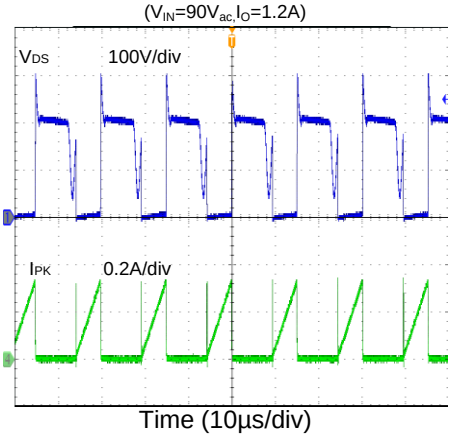
Startup

(V_{IN}=264V_{ac},I_O=1.2A)



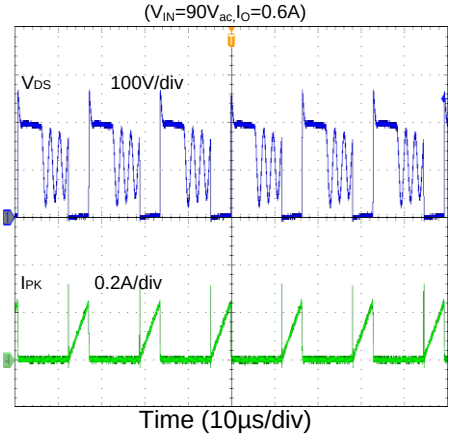
Steady States

(V_{IN}=90V_{ac},I_O=1.2A)



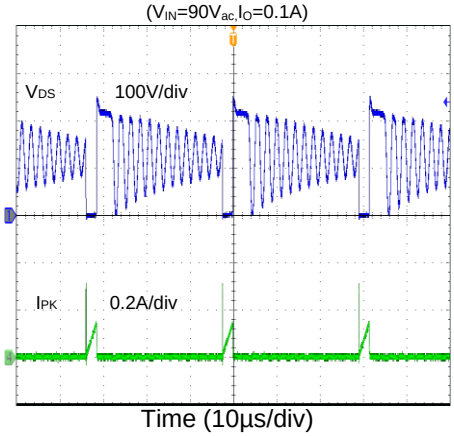
Steady States

(V_{IN}=90V_{ac},I_O=0.6A)



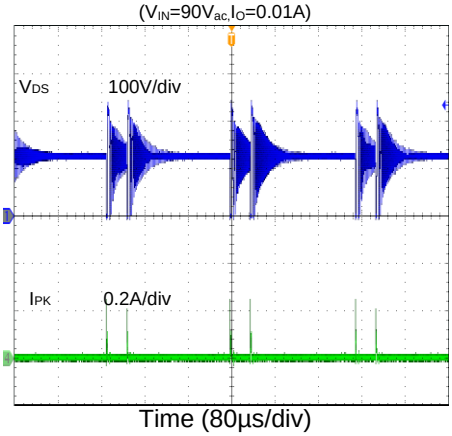
Steady States

(V_{IN}=90V_{ac},I_O=0.1A)



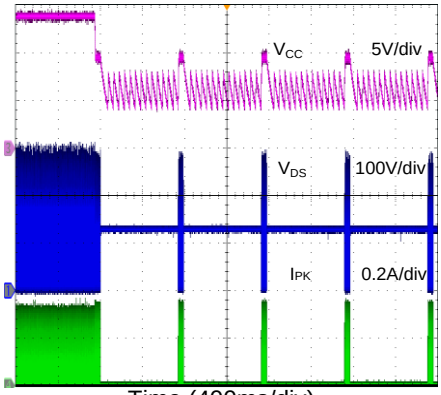
Steady States

(V_{IN}=90V_{ac},I_O=0.01A)



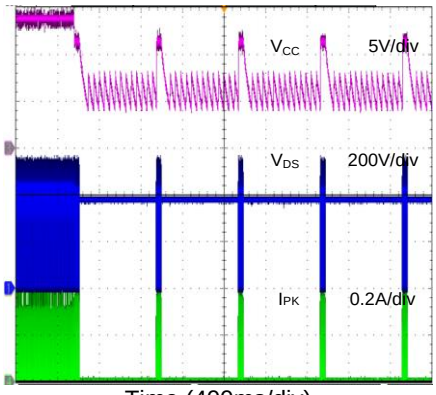
OLP

(Vin=90V_{ac}, Io jump from 1.2A to 2A)



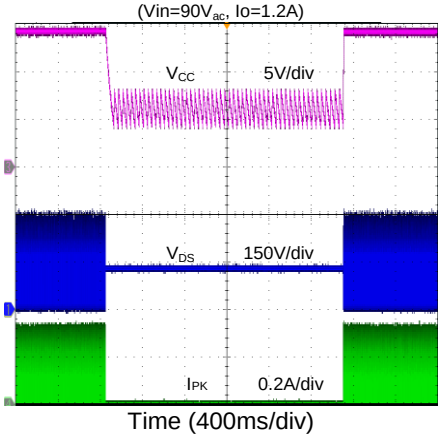
OLP

(Vin=264V_{ac}, Io jump from 1.2A to 2A)



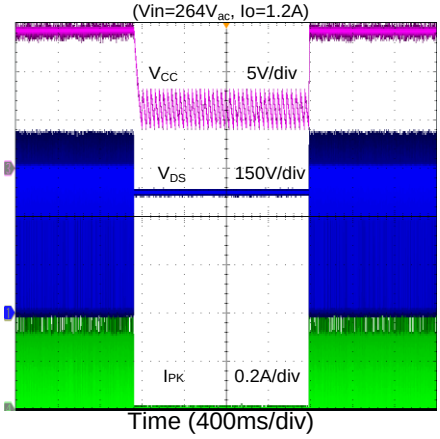
OTP

(Vin=90V_{ac}, Io=1.2A)

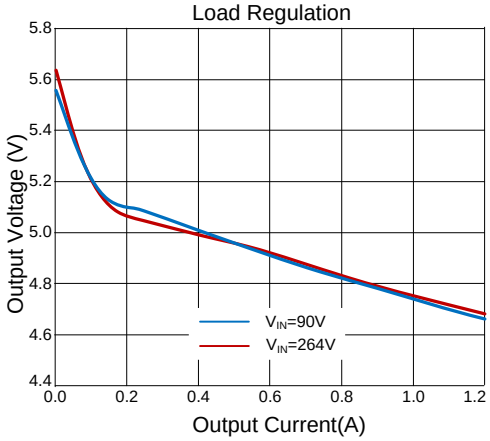


OTP

(Vin=264V_{ac}, Io=1.2A)



Load Regulation



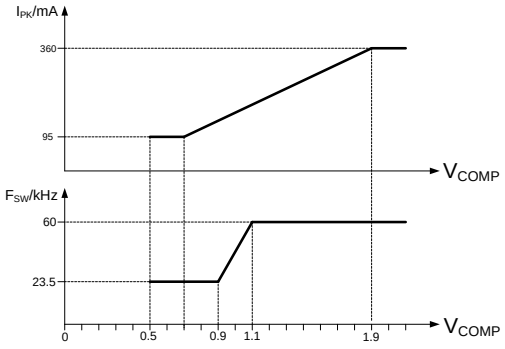
Operation Principles

Pseudo Fixed Frequency Control

The SY26741 adopts pseudo fixed frequency control (Silergy proprietary) to avoid sub-harmonic oscillation when converter works under CCM and D>50%. Sub-harmonic oscillation is an inherent issue under peak current control method. Traditionally, slope compensation is used to avoid this issue. The SY26741 do not need slope compensation to solve the sub-harmonic issue, so application design is simplified.

Frequency Fold Back Control

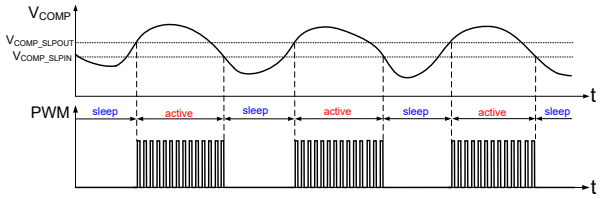
The SY26741 adopts frequency fold back control to improve medium and light load efficiency. When load get lighter and lighter, COMP pin voltage will become lower and lower. When COMP pin voltage drops below 1.1V, IC begins to decrease switching frequency. When COMP pin voltage drops to 0.9V, switching frequency reaches minimum 23.5kHz. When load further decreases, IC will enter burst mode. The switching frequency control curve is shown in below figure:



Burst Mode

The SY26741 adopts burst mode control under very light load or no-load condition. When load get lighter and lighter, COMP pin voltage will become lower and lower, and when COMP pin voltage drops below a threshold (typical=0.5V), IC will enter sleep mode. Under sleep mode, power MOS will not switch, and most part of internal control blocks will be shut down to save energy. As there is no switching, output voltage will gradually drop, due to the closed loop, COMP pin voltage will rise again, and when COMP pin voltage rises above another threshold (typical=0.6V), IC will awake from sleep mode and resume normal operating again. Due to this control method, IC will alternatively work under sleep mode and active mode, optimized light load efficiency will be achieved.

Notice: To achieve unified peak current level and switching frequency under burst mode, when COMP is between 0.7V and 0.5V, peak current and switching frequency is kept constant. As a result, the output regulation strength is zero when COMP is between 0.7V and 0.5V, the output voltage ripple will become a little larger.

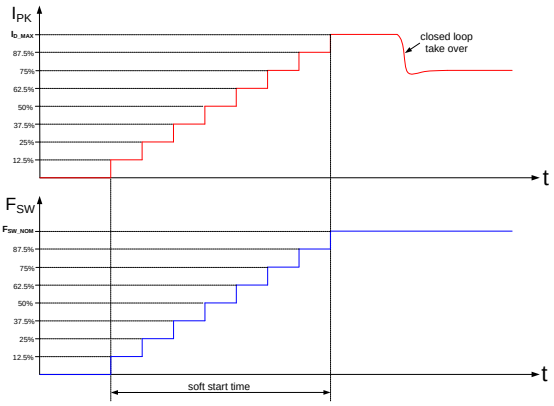


HV Start up

The SY26741 integrates high voltage start up from DRAIN pin. The HV current source to charge VCC pin capacitor is I_{CH2}, high start up speed is achieved. Before VCC is charged above 1.5V, the HV current source is limited to I_{CH1}. As a result, if VCC pin is shorted to GND by fault, the power dissipation inside IC is limited to safe level, and there is no risk of IC to be over heated.

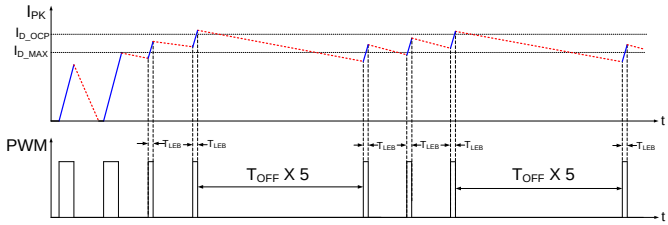
Internal Soft Start Process

The SY26741 integrates soft start process during start up to achieve smooth output voltage rise up and keep peak current of power MOS within safe level. IC will gradually increase peak current setpoint step by step until it reaches maximum value (typical=345mA), and also gradually increase switching frequency step by step until it reaches maximum value (typical=60kHz). The soft start process is formed by 8 small steps as shown in below figure:



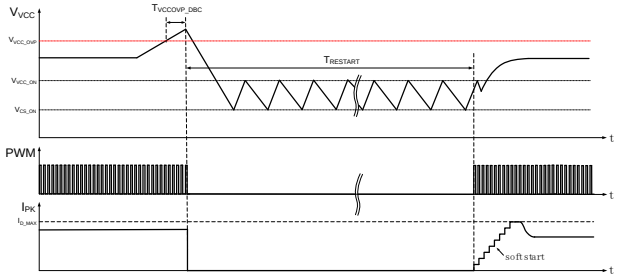
Peak Current Reduction under Abnormal Condition

Under normal operating condition, peak current will not exceed maximum setpoint value (typical=345mA). However, under abnormal conditions, like output short circuit, the peak current will rise up to higher than the maximum setpoint value (since there is a leading-edge blanking time before peak current sense when power MOS is turned on, during this blanking time, peak current will rise up without limit). To keep the peak current within safety level, the SY26741 just let the OFF time of power MOS to be 5 times of that under normal condition as soon as peak current reaches another threshold which is higher than maximum setpoint under normal condition. Due to this control method, the transformer current (Flyback) or inductor current (Buck) will have enough time to drop down. The maximum peak current level under abnormal condition will be limited. The peak current reduction process under abnormal condition is shown as below figure:



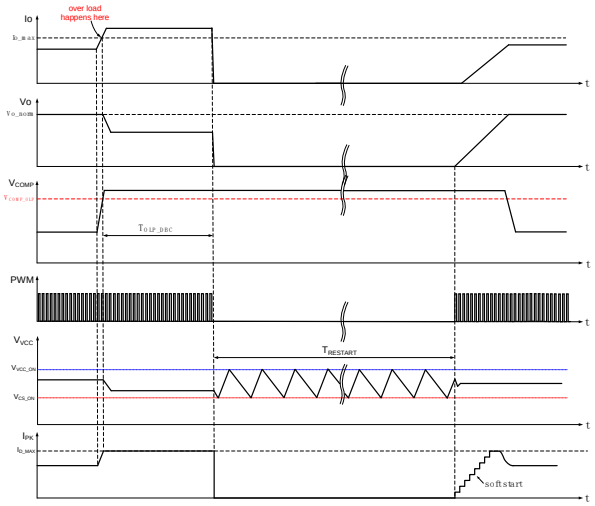
VCC OVP

Under abnormal conditions, such as opto-coupler open circuit or failure (SSR flyback), output voltage will rise higher and higher, and VCC will become higher and higher (when IC is supplied by auxiliary winding). To avoid IC damage caused by VCC pin over voltage condition, SY26741 adopts a VCC OVP threshold V_{VCC_OVP}, when V_{VCC} exceeds V_{VCC_OVP} threshold, IC will stop switching and enter auto-recovery mode. Before V_{VCC} reaches V_{VCC_OVP} threshold, a 10mA current sink into VCC pin will try to clamp VCC pin voltage. When the auto-recovery timer elapse, IC will try to resume operating.



OLP

When over load condition happens, COMP pin voltage will be pulled up to high level, and peak current will reach the maximum setpoint (typical=345mA). The SY26741 will compare COMP pin voltage with an OLP threshold, when COMP pin voltage is higher than the OLP threshold, a timer will begin to count, and if COMP pin voltage is continuously higher than OLP threshold which result in OLP timer elapse, OLP will be triggered, IC will stop switching and enter auto-recovery mode. When the auto-recovery timer elapse, IC will try to resume operating. If over load condition still exists, IC will again trigger OLP and another auto-recovery cycle will begin. If over load condition disappear when IC is try to resume operating, then the converter will resume normal working again. Every time when auto-recovery timer elapse and IC try to resume operating, soft start process will be active. The OLP process is shown as below figure:

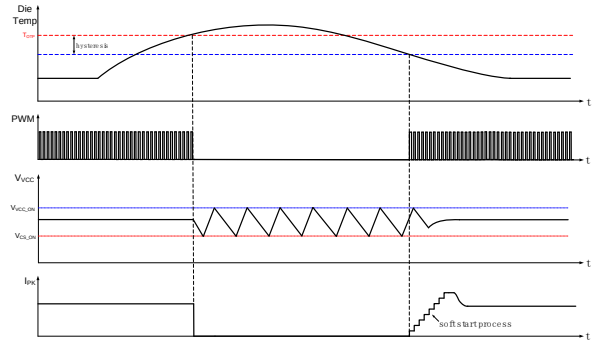


Under some special cases (big bus capacitor and big VCC capacitor), during Vin shut down, OLP will be triggered due to max T_{ON} limit. Once OLP is triggered, IC will wait for auto-recovery timer elapse to resume operating, so under Vin fast on-off test, output voltage can't response immediately. To solve this problem,

during Vin shut down, if IC works under max T_{ON} condition, the OLP timer will be disabled even if COMP pin voltage is higher than OLP threshold. Due to this procedure, OLP will not be triggered during Vin shut down, output voltage can achieve fast response to fast Vin on-off test.

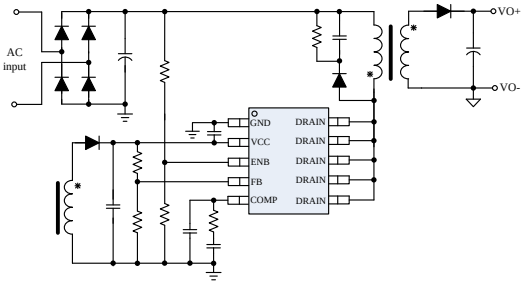
OTP

SY26741 monitors IC's die temperature under normal operating mode. Once die temperature rises above internal OTP threshold (typical=163℃), IC will stop switching. It will resume normal operating as noon as die temperature drops below the OTP recovery temperature (typical=143℃). Due to this protection, IC's temperature will be guaranteed within safe level.

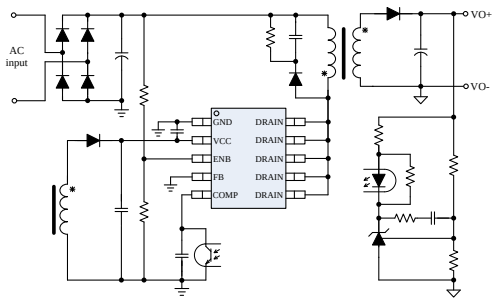


PSR/SSR configuration for flyback topology

For isolated flyback topology, both PSR and SSR mode is available. The PSR/SSR mode is configured by FB pin. When start up, FB pin will source a current to sense the FB pin impedance. If FB pin voltage is HIGH, IC will work under PSR mode, and internal error amplifier will be active. If FB pin voltage is LOW, IC will work under SSR mode, and internal error amplifier will be disabled. If SSR mode is selected, it is recommended to directly connect FB pin to GND.



Isolated Flyback topology with PSR configuration



Isolated Flyback topology with SSR configuration

Loop Compensation Network Design (Flyback)

The small signal transfer function of flyback power stage that operating in CCM is shown as below equation:

$$G_{vc2vo}(s)=\frac{\hat{v}_o(s)}{\hat{v}_c(s)}=\frac{N_{PS}\cdot R_L}{R_{CS}}\cdot\frac{D'}{1+D}\cdot\frac{(1-\frac{s}{\omega_a})\cdot(1+\frac{s}{\omega_{zc}})}{(1+\frac{s}{\omega_p})\cdot(1+\frac{s}{Q_p\omega_n}+\frac{s^2}{\omega_n{}^2})}$$

The RHP (right half plane) zero:

$$\omega_a=\frac{N_{PS}{}^2\cdot D'^2\cdot R_L}{D\cdot L_m}$$

The output capacitor ESR zero:

$$\omega_{zc}=\frac{1}{C_O\cdot R_C}$$

The main pole (low frequency):

$$\omega_p=\frac{1+D+\frac{N_{PS}{}^2\cdot R_L\cdot T_S}{L_m}\cdot D'^3\cdot(m_c-0.5)}{R_L\cdot C_O}$$

The double pole that located at half the switching frequency:

$$\omega_n=\frac{\pi}{T_S},\ \text{quality factor}\ Q_P=\frac{1}{\pi(m_c D'-0.5)}$$

Where N_{PS} is primary/secondary turns ratio of the transformer

R_{CS} is primary current sense resistor, $R_{CS}=1.39\Omega$ for SY26741

R_L is the equivalent load resistance, which can be derived as $R_L=\frac{V_O}{I_O}$

D is duty cycle under steady state

D' is defined as $D' = 1 - D$

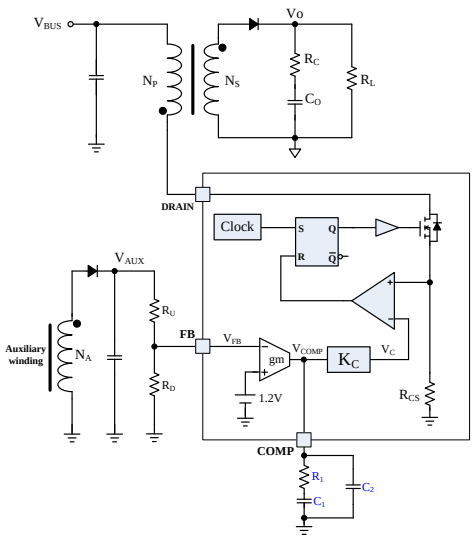
m_c is defined as: $m_c = 1 + \frac{S_e}{S_n}$

S_e is the external ramp compensation, $S_e = 0$ for SY26741

S_n is the sensed primary inductor current rising slope:

$$S_n = \frac{V_{BUS}}{L_m} \cdot R_{CS}$$

The double pole ω_n is located at half the switching frequency, for a practical design, the bandwidth of closed loop is always set at 1/10~1/6 switching frequency, so the double pole ω_n is far away from the bandwidth, it can be neglected when design the compensation network. The right half plane zero ω_a of power stage is very difficult to compensate, the best way is to choose the bandwidth of closed loop to be far away (lower) from that RHP zero location. As a result, the compensation network only needs to consider the lower frequency pole ω_p and the output capacitor ESR zero ω_{zc} . A simple type II compensation network is most suitable for single pole system. Type II compensation includes one integral, one zero and one pole. The integral is aimed to achieve very small static error under steady state, the zero is aimed to compensate the power stage low frequency pole ω_p , and the pole is aimed to compensate the output capacitor ESR zero. A type II compensation network can be achieved by COMP pin network formed by capacitor C_1 , C_2 and resistor R_1 .



The transfer function from V_{FB} to V_{COMP} is shown as below equation:

$$G_{fb2comp}(s) = \frac{\hat{v}_{COMP}}{\hat{v}_{FB}} = \frac{G_m}{C_1 + C_2} \cdot \frac{1}{s} \cdot \frac{1 + \frac{s}{\omega_{z\_comp}}}{1 + \frac{s}{\omega_{p\_comp}}}$$

Where G_m is the transconductance of internal error amplifier of SY26741, $G_m = 500uA / V$

The zero of compensation network: $\omega_{z\_comp} = \frac{1}{C_1 R_1}$

The pole of compensation network:

$$\omega_{p\_comp} = \frac{1}{R_1 \cdot \frac{C_1 C_2}{C_1 + C_2}}$$

The basic compensation principle is that compensation zero ω_{z_comp} locates at the same frequency as the pole ω_p of power stage, the compensation pole ω_{p_comp} locates at the same frequency as the ESR zero ω_{zc} of the power stage.

The transfer function from v_o to v_C is:

$$G_{vo2vctrl} = \frac{\hat{v}_C}{\hat{v}_o} = K_C \cdot \frac{N_A}{N_S} \cdot \frac{R_D}{R_U + R_D} \cdot \frac{G_m}{C_1 + C_2} \cdot \frac{1}{s} \cdot \frac{1 + \frac{s}{\omega_{z\_comp}}}{1 + \frac{s}{\omega_{p\_comp}}}$$

Where K_C is the decay factor from V_{COMP} to V_C , $K_C = 0.25$ for SY26741

Loop Compensation Network Parameter Calculation (Flyback)

The open loop transfer function is derived as below equation:

$$G_{openloop} = K_C \cdot \frac{N_A}{N_S} \cdot \frac{R_D}{R_U + R_D} \cdot \frac{G_m}{C_1 + C_2} \cdot \frac{N_{PS} \cdot R_L}{R_{CS}} \cdot \frac{D'}{1 + D} \cdot \frac{1}{s} \cdot \frac{(1 + \frac{s}{\omega_{z\_comp}})(1 - \frac{s}{\omega_a})(1 + \frac{s}{\omega_{zc}})}{(1 + \frac{s}{\omega_{p\_comp}})(1 + \frac{s}{\omega_p})(1 + \frac{s}{Q_p \omega_n} + \frac{s^2}{\omega_n^2})}$$

Based on compensation principle: $\omega_{z\_comp} = \omega_P$, $\omega_{p\_comp} = \omega_{zc}$, and ω_a , ω_n is far away from the cross over frequency, then the transfer function can be simplified as below equation:

$$G_{openloop} = K_C \cdot \frac{N_A}{N_S} \cdot \frac{R_D}{R_U + R_D} \cdot \frac{G_m}{C_1 + C_2} \cdot \frac{N_{PS} \cdot R_L}{R_{CS}} \cdot \frac{D'}{1 + D} \cdot \frac{1}{s}$$

The cross over frequency ω_c of the open loop bode plot should be decided firstly, and then according the Gain equation:

$20\log\left|G_{openloop}\right| = 0$ or

$$K_C \cdot \frac{N_A}{N_S} \cdot \frac{R_D}{R_U + R_D} \cdot \frac{G_m}{C_1 + C_2} \cdot \frac{N_{PS} \cdot R_L}{R_{CS}} \cdot \frac{D'}{1+D} \cdot \frac{1}{\omega_c} = 1$$

$C_1 + C_2$ is derived, under normal design, $C_1 \gg C_2$, so $C_1 + C_2 \approx C_1$, C_1 will be decided firstly:

$$C_1 \approx K_C \cdot \frac{N_A}{N_S} \cdot \frac{R_D}{R_U + R_D} \cdot G_m \cdot \frac{N_{PS} \cdot R_L}{R_{CS}} \cdot \frac{D'}{1+D} \cdot \frac{1}{\omega_c}$$

According to $\omega_{z\_comp} = \omega_P$, or

$$\frac{1}{C_1 R_1} = \frac{1 + D + \frac{N_{PS}^2 \cdot R_L \cdot T_S}{L_m} \cdot D'^3 \cdot (m_c - 0.5)}{R_L \cdot C_O}$$, R_1 can be decided secondly:

$$R_1 = \frac{1}{C_1} \cdot \frac{R_L \cdot C_O}{1 + D + \frac{N_{PS}^2 \cdot R_L \cdot T_S}{L_m} \cdot D'^3 \cdot (m_c - 0.5)}$$

According to $\omega_{p\_comp} = \omega_{zc}$, or $\frac{1}{R_1 \cdot \frac{C_1 C_2}{C_1 + C_2}} = \frac{1}{C_O \cdot R_C}$,

C_2 can be decided thirdly:

$$C_2 = \frac{C_1 \cdot R_C \cdot C_O}{R_1 \cdot C_1 - R_C \cdot C_O}$$

Until now, all the compensation network parameters have been decided.

Loop Compensation Network Design（Buck）

The small signal transfer function of power stage for peak current mode buck converter which operating in CCM is shown as below equation:

$$G_{vc2vo}(s) = \frac{\tilde{v}_o(s)}{\tilde{v}_c(s)} = \frac{R_L}{R_{CS}} \cdot \frac{1}{1 + \frac{R_L \cdot T_S}{L} \cdot (m_c D' - 0.5)} \cdot \frac{(1 + \frac{s}{\omega_{zc}})}{(1 + \frac{s}{\omega_p}) \cdot (1 + \frac{s}{Q_P \cdot \omega_n} + \frac{s^2}{\omega_n^2})}$$

The output capacitor ESR zero:

$$\omega_{zc} = \frac{1}{C_O \cdot R_C}$$

The main pole (low frequency):

$$\omega_p = \frac{1 + \frac{R_L \cdot T_S}{L} \cdot (m_c D' - 0.5)}{R_L \cdot C_O}$$

The double pole:

$\omega_n = \frac{\pi}{T_S}$, quality factor $Q_P = \frac{1}{\pi(m_c D' - 0.5)}$

Where R_{CS} is primary current sense resistor, $R_{CS} = 1.39\Omega$ for SY26741

R_L is the equivalent load resistance, which can be derived as $R_L = \frac{V_O}{I_O}$

L is the inductance of buck inductor

T_S is the switching period

D is duty cycle under steady state

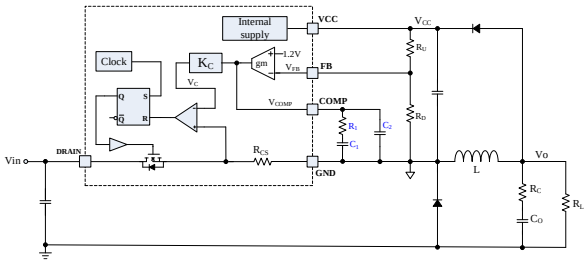
D' is defined as $D' = 1 - D$

m_c is defined as: $m_c = 1 + \frac{S_e}{S_n}$

S_e is the external ramp compensation, $S_e = 0$ for SY26741

S_n is the sensed inductor current rising slope: $S_n = \frac{V_{BUS} - V_O}{L} \cdot R_{CS}$

The double pole ω_n is located at half switching frequency, for a practical design, the bandwidth of closed loop is always set at 1/10~1/6 switching frequency, so the double pole ω_n is far away from the bandwidth, it can be neglected when design the compensation network. As a result, the compensation network only needs to consider the lower frequency pole ω_p and the output capacitor ESR zero ω_{zc}. A simple type II compensation network is most suitable for single pole system. Type II compensation includes one integral, one zero and one pole. The integral is aimed to achieve very small static error under steady state, the zero is aimed to compensate the power stage low frequency pole ω_p, and the pole is aimed to compensate the output capacitor ESR zero. A type II compensation network can be achieved by COMP pin network formed by capacitor C_1, C_2 and resistor R_1.



The transfer function from V_{FB} to V_{COMP} is shown as below equation:

$$G_{fb2comp}(s)=\frac{\hat{v}_{COMP}}{\hat{v}_{FB}}=\frac{G_m}{C_1+C_2}\cdot\frac{1}{s}\cdot\frac{1+\frac{s}{\omega_{z\_comp}}}{1+\frac{s}{\omega_{p\_comp}}}$$

Where G_m is the transconductance of internal error amplifier of SY26741, $G_m=500uA/V$

The zero of compensation network: $\omega_{z\_comp}=\frac{1}{C_1R_1}$

The pole of compensation network:

$$\omega_{p\_comp}=\frac{1}{R_1\cdot\frac{C_1C_2}{C_1+C_2}}$$

The basic compensation principle is that compensation zero ω_{z_comp} locates at the same frequency as the pole ω_p of power stage, the compensation pole ω_{p_comp} locates at the same frequency as the ESR zero ω_{zc} of the power stage.

The transfer function from v_o to v_C is:

$$G_{vo2vctrl}=\frac{\hat{v}_C}{\hat{v}_o}=K_C\cdot\frac{R_D}{R_U+R_D}\cdot\frac{G_m}{C_1+C_2}\cdot\frac{1}{s}\cdot\frac{1+\frac{s}{\omega_{z\_comp}}}{1+\frac{s}{\omega_{p\_comp}}}$$

Where K_C is the decay factor from V_{COMP} to V_C, $K_C=0.25$ for SY26741.

Loop Compensation Network Parameter Calculation (Buck)

The open loop transfer function is derived as below equation:

$$G_{openloop}=K_C\cdot\frac{R_D}{R_U+R_D}\cdot\frac{G_m}{C_1+C_2}\cdot\frac{R_L}{R_{CS}}\cdot\frac{1}{1+\frac{R_L\cdot T_S}{L}\cdot(m_c D'-0.5)}\cdot\frac{1}{s}\cdot\frac{(1+\frac{s}{\omega_{z\_comp}})(1+\frac{s}{\omega_{zc}})}{(1+\frac{s}{\omega_{p\_comp}})(1+\frac{s}{\omega_p})(1+\frac{s}{Q_p\omega_n}+\frac{s^2}{\omega_n^2})}$$

Based on compensation principle: $\omega_{z\_comp}=\omega_P$, $\omega_{p\_comp}=\omega_{zc}$, and ω_n is far away from the cross over frequency, then the transfer function can be simplified as below equation:

$$G_{openloop}=K_C\cdot\frac{R_D}{R_U+R_D}\cdot\frac{G_m}{C_1+C_2}\cdot\frac{R_L}{R_{CS}}\cdot\frac{1}{1+\frac{R_L\cdot T_S}{L}\cdot(m_c D'-0.5)}\cdot\frac{1}{s}$$

The cross over frequency ω_c of the open loop bode plot should be decided firstly, and then according the Gain equation:

$$20\log\left|G_{openloop}\right|=0 \text{ or}$$

$$K_C\cdot\frac{R_D}{R_U+R_D}\cdot\frac{G_m}{C_1+C_2}\cdot\frac{R_L}{R_{CS}}\cdot\frac{1}{1+\frac{R_L\cdot T_S}{L}\cdot(m_c D'-0.5)}\cdot\frac{1}{\omega_c}=1$$

C_1+C_2 is derived, under normal design, C_1 is much larger than C_2, so $C_1+C_2\approx C_1$, C_1 will be decided firstly:

$$C_1\approx\frac{K_CR_DG_mR_L}{R_{CS}(R_U+R_D)(1+\frac{R_L\cdot T_S}{L}\cdot(m_c D'-0.5))\cdot\omega_c}$$

According to $\omega_{z\_comp}=\omega_P$ or $\frac{1}{C_1R_1}=\frac{1+\frac{R_L\cdot T_S}{L}\cdot(m_c D'-0.5)}{R_L\cdot C_O}$

R_1 can be decided secondly:

$$R_1=\frac{1}{C_1}\cdot\frac{R_L\cdot C_O}{1+\frac{R_L\cdot T_S}{L}\cdot(m_c D'-0.5)}$$

According to $\omega_{p\_comp}=\omega_{zc}$, or $\frac{1}{R_1\cdot\frac{C_1C_2}{C_1+C_2}}=\frac{1}{C_O\cdot R_C}$,

C_2 can be decided thirdly:

$$C_2=\frac{C_1C_OR_C}{C_1R_1-C_OR_C}$$

Until now, all the compensation network parameters have been decided.

Layout Considerations

A good PCB layout is helpful for correct operating, strong noise immunity and good EMI performance. Customer is recommended to follow below tips:

(a)Three power loops that feature fast switching behavior should be kept as close as possible, or the area of the loops should be kept as small as possible:

Loop1: formed by BUS capacitor, primary winding of transformer and SY26741 (DRAIN→GND);

Loop2: formed by secondary winding of transformer, rectification diode D_1 and output capacitor C_O;

Loop3: formed by auxiliary winding of transformer, rectification diode D_2 and capacitor C_2;

(b) Analog ground and power ground should be separated clearly, the two ground should only be connected by single trace.

Analog ground includes ground of COMP pin compensation network, ground of FB pin resistor divider, ground of ENB pin resistor divider and VCC pin capacitor. All analog ground should be connected together with trace as short as possible.

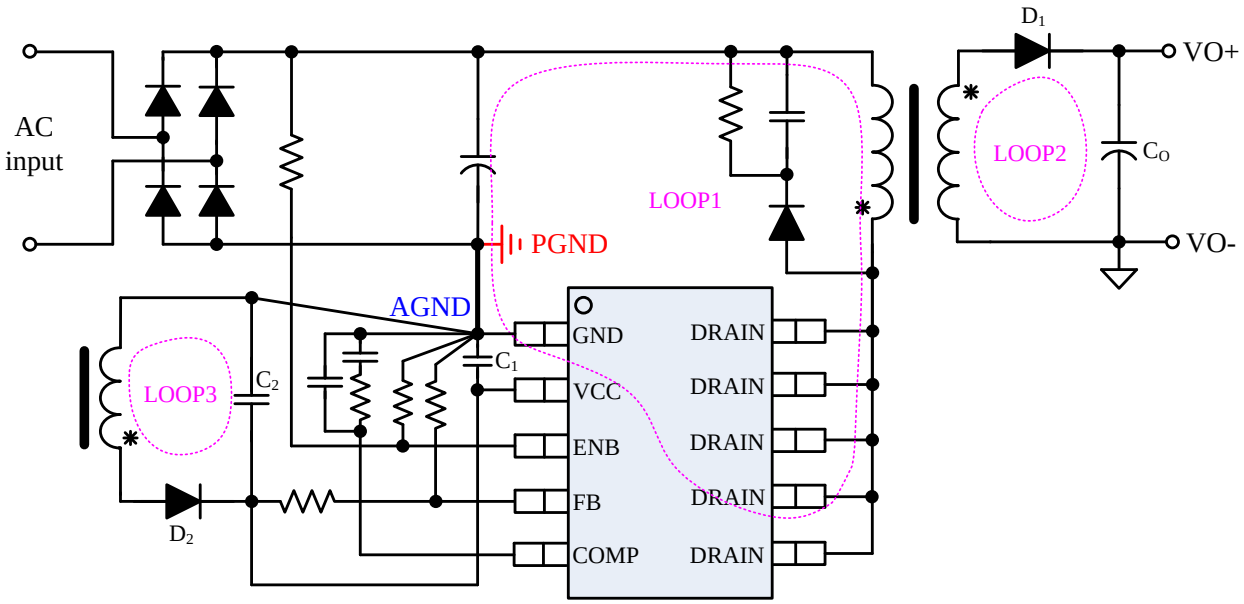
Power ground includes negative terminal of bus capacitor and GND pin of SY26741. All power ground should be connected together with trace as short as possible.

(c) A ceramic capacitor C_1 with 0.1uF~1uF should be located beside IC as close as possible for decoupling of noise.

(d)FB pin resistor divider (especially lower resistor) should be located beside IC as close as possible for noise immunity.

(e)COMP pin loop compensation network should be located beside IC as close as possible for noise immunity.

(f)ENB pin resistor divider (especially lower resistor) should be located beside IC as close as possible for noise immunity.



PSR Flyback PCB Layout Consideration

Design Example (Flyback)

A design example of typical application is shown below step by step.

Input/output specification

Parameter	Symbol	Value
Input voltage range	V_{IN}	100Vdc~480Vdc
Rated output power	P_O	6W
Rated output voltage	V_O	5V
Output OVP level	$V_{O,OVP}$	6V
Rated output current	I_O	1.2A
OCP proportion	K_{OCP}	120%

Preset parameter

Parameter	Symbol	Value
Break down voltage of power MOS	$V_{MOS,BR}$	800V
V_{DS} de-rating factor of power MOS	K_{DR}	85%
Spike on V_{DS} during power MOS turn off	ΔV_{SN}	100V
Converter efficiency	η	78%
Secondary diode forward voltage drop	$V_{D,F}$	0.6V
Transformer effective cross-sectional area (EE16 safety)	A_E	19.8 mm^2
Primary inductance	L_m	2.4mH
Output capacitance	C_O	470uF
Output capacitance ESR	R_C	50mΩ
Upper resistor divider on FB pin	R_U	200kΩ
Lower resistor divider on FB pin	R_D	20kΩ

1) BUS capacitor selection

Calculate input power at rated output power

$$P_{IN}=\frac{P_O}{\eta}=\frac{6}{78\%}=7.69W$$

Minimum BUS capacitor: $C_{BUS,MIN}=1.5\cdot 7.69=11.54uF$

Maximum BUS capacitor: $C_{BUS,MAX}=2\cdot 7.69=15.39uF$

Select BUS capacitor: $C_{BUS}=11.5uF$

2) Transformer design

(a)Calculate primary/secondary turns ratio: N_{PS}

$$N_{PS}\le\frac{V_{MOS,BR}\cdot K_{DR}-V_{BUS,MAX}-\Delta V_{SN}}{V_O+V_{D,F}}=\frac{800\cdot 0.85-480-100}{5+0.6}=17.86$$

N_{PS} is selected to: $N_{PS}=16$

(b)Calculate primary winding turns: N_P

Transformer core effective cross-sectional area: $A_E=19.8mm^2$

Maximum allowed flux density: $B_{MAX}=0.275T$

$$N_P=\frac{L_M\cdot I_{PK}}{B_{MAX}\cdot A_E}=\frac{2.4\cdot10^{-3}\cdot0.36}{0.275\cdot19.8\cdot10^{-6}}=158.68$$

Select primary winding turns: $N_P=160$

(c) Calculate secondary winding turns: N_S

$$N_S=\frac{N_P}{N_{PS}}=\frac{160}{16}=10$$

Select secondary turns: $N_S=10$

(d) Calculate auxiliary winding turns: N_A

VCC supply voltage from auxiliary winding is set to: $V_{CC}=12V$

$$N_A=\frac{V_{CC}\cdot N_S}{V_O}=\frac{12\cdot10}{5}=24$$

Select auxiliary winding turns: $N_A=24$

(e) If other transformer core type is selected, then recalculate (b)~(d).

3) Secondary diode selection

(a)Maximum reverse voltage calculation:

$$V_{D,R,MAX}=\frac{V_{BUS,MAX}}{N_{PS}}+V_{O,OVP}=\frac{480}{16}+6=36V$$

Considering the voltage spike, reverse voltage rating of the diode is recommended to be 60V~100V.

(b)Maximum instantaneous forward current:

$$I_{D,PK,MAX}=N_{PS}\cdot I_{PK,MAX}=16\cdot0.36=5.76A$$

(c)Maximum average forward current:

$$I_{D,AVG,MAX}=I_O\cdot K_{OCP}=1.2\cdot120\%=1.44A$$

4) Boundary primary inductance calculate at Vin=100Vdc

$$L_{M,BCM}=\frac{V_{BUS}\cdot\frac{N_{PS}\cdot V_O}{V_{BUS}+N_{PS}\cdot V_O}\cdot T_S}{I_{PK}}=\frac{100\cdot\frac{16\cdot5}{100+16\cdot5}\cdot1.667\cdot10^{-5}}{0.36}=2.058\cdot10^{-3}H$$

$L_m(2.4\cdot10^{-3}H)>L_{M,BCM}(2.058\cdot10^{-3}H)$, therefore the circuit operates in continuous mode

5) Compensation design

(a) Control to output transfer function simplified:

$$G_{vc2vo}(s)=\frac{\hat{v}_o(s)}{\hat{v}_c(s)}=\frac{N_{PS}\cdot R_L}{R_{CS}}\cdot\frac{D'}{1+D}\cdot\frac{(1-\frac{s}{\omega_a})\cdot(1+\frac{s}{\omega_{zc}})}{(1+\frac{s}{\omega_p})\cdot(1+\frac{s}{Q_P\omega_n}+\frac{s^2}{\omega_n{}^2})}$$

Where N_{PS} is primary/secondary turns ratio of the transformer, $N_{PS}=16$

R_{CS} is primary current sense resistor, $R_{CS}=1.39\Omega$ for SY26741

R_L is the equivalent load resistance, which can be derived as $R_L=\frac{V_O}{I_O}=\frac{5}{1.2}=4.17\Omega$

D is duty cycle under steady state $D=\frac{N_{PS}\cdot V_O}{V_{BUS}+N_{PS}\cdot V_O}=\frac{16\cdot 5}{100+16\cdot 5}=0.444$

D' is defined as $D'=1-D=1-0.444=0.556$

m_c is defined as: $m_c=1+\frac{S_e}{S_n}=1$

S_e is the external ramp compensation, $S_e=0$ for SY26741

S_n is the sensed primary inductor current rising slope:

$$S_n=\frac{V_{BUS}}{L_m}\cdot R_{CS}=\frac{100}{2.4\cdot 10^{-3}}\cdot 1.39=57.92\cdot 10^3$$

The RHP (right half plane) zero:

$$\omega_a=\frac{N_{PS}{}^2\cdot D'^2\cdot R_L}{D\cdot L_m}=\frac{16^2\cdot 0.556^2\cdot 4.17}{0.444\cdot 2.4\cdot 10^{-3}}=309.69\cdot 10^3$$

The output capacitor ESR zero:

$$\omega_{zc}=\frac{1}{C_O\cdot R_C}=\frac{1}{50\cdot 10^{-3}\cdot 470\cdot 10^{-6}}=42.55\cdot 10^3$$

The main pole (low frequency):

$$\omega_p=\frac{1+D+\frac{N_{PS}{}^2\cdot R_L\cdot T_S}{L_m}\cdot D'^3\cdot(m_c-0.5)}{R_L\cdot C_O}=\frac{1+0.444+\frac{16^2\cdot 4.17\cdot 1.667\cdot 10^{-5}}{2.4\cdot 10^{-3}}\cdot 0.556^3\cdot(1-0.5)}{4.17\cdot 470\cdot 10^{-6}}=1.06\cdot 10^3$$

The double pole that located at half the switching frequency:

$$\omega_n=\frac{\pi}{T_S}=\frac{\pi}{1.667\cdot 10^{-5}}=188.5\cdot 10^3$$

Quality factor $Q_P=\frac{1}{\pi(m_c\cdot D'-0.5)}=\frac{1}{\pi(1\cdot 0.556-0.5)}=5.684$

Loop Compensation Network Parameter Calculation (Flyback)

The open loop transfer function is derived as below equation:

$$G_{openloop} = K_C \cdot \frac{N_A}{N_S} \cdot \frac{R_D}{R_U + R_D} \cdot \frac{G_m}{C_1 + C_2} \cdot \frac{N_{PS} \cdot R_L}{R_{CS}} \cdot \frac{D'}{1+D} \cdot \frac{1}{s} \cdot \frac{(1+\frac{s}{\omega_{z\_comp}})(1-\frac{s}{\omega_a})(1+\frac{s}{\omega_{zc}})}{(1+\frac{s}{\omega_{p\_comp}})(1+\frac{s}{\omega_p})(1+\frac{s}{Q_P\omega_n}+\frac{s^2}{\omega_n{}^2})}$$

Based on compensation principle: $\omega_{z\_comp} = \omega_P$, $\omega_{p\_comp} = \omega_{zc}$, and ω_a , ω_n is far away from the cross over frequency, then the transfer function can be simplified as below equation:

$$G_{openloop} = K_C \cdot \frac{N_A}{N_S} \cdot \frac{R_D}{R_U + R_D} \cdot \frac{G_m}{C_{COMP} + C_2} \cdot \frac{N_{PS} \cdot R_L}{R_{CS}} \cdot \frac{D'}{1+D} \cdot \frac{1}{s}$$

The cross over frequency ω_c of the open loop bode plot is defined as: $\omega_c = \frac{1}{10} \cdot f_S \cdot 2 \cdot \pi = \frac{1}{10} \cdot 60 \cdot 10^3 \cdot 2 \cdot \pi = 37.70 \cdot 10^3$

and then according the Gain equation:

$$K_C \cdot \frac{N_A}{N_S} \cdot \frac{R_D}{R_U + R_D} \cdot \frac{G_m}{C_1 + C_2} \cdot \frac{N_{PS} \cdot R_L}{R_{CS}} \cdot \frac{D'}{1+D} \cdot \frac{1}{\omega_c} = 1$$

$C_1 + C_2$ is derived, under normal design, $C_1 \gg C_2$, so $C_1 + C_2 \approx C_1$, C_1 will be decided firstly:

$$C_1 \approx K_C \cdot \frac{N_A}{N_S} \cdot \frac{R_D}{R_U + R_D} \cdot G_m \cdot \frac{N_{PS} \cdot R_L}{R_{CS}} \cdot \frac{D'}{1+D} \cdot \frac{1}{\omega_c}$$

$$C_1 = 0.25 \cdot \frac{24}{10} \cdot \frac{20 \cdot 10^3}{200 \cdot 10^3 + 20 \cdot 10^3} \cdot 500 \cdot 10^{-6} \cdot \frac{16 \cdot 4.17}{1.39} \cdot \frac{0.556}{1+0.444} \cdot \frac{1}{37.70 \cdot 10^3} = 1.337 \cdot 10^{-8} \text{F}$$

According to $\omega_{z\_comp} = \omega_P$, $\frac{1}{C_1 R_1} = \frac{1 + D + \frac{N_{PS}{}^2 \cdot R_L \cdot T_S}{L_m} \cdot D'^3 \cdot (m_c - 0.5)}{R_L \cdot C_O}$, R_1 can be decided secondly:

$$R_1 = \frac{1}{C_1} \cdot \frac{R_L \cdot C_O}{1 + D + \frac{N_{PS}{}^2 \cdot R_L \cdot T_S}{L_m} \cdot D'^3 \cdot (m_c - 0.5)} = \frac{1}{1.337 \cdot 10^{-8}} \cdot \frac{4.17 \cdot 470 \cdot 10^{-6}}{1 + 0.444 + \frac{16^2 \cdot 4.17 \cdot 1.667 \cdot 10^{-5}}{2.4 \cdot 10^{-3}} \cdot 0.556^3 \cdot (1 - 0.5)} = 70.43 \cdot 10^3 \Omega$$

According to $\omega_{p\_comp} = \omega_{zc}$, $\frac{1}{R_1 \cdot \frac{C_1 C_2}{C_1 + C_2}} = \frac{1}{C_O \cdot R_C}$, C_2 can be decided thirdly:

$$C_2 = \frac{C_1 \cdot R_C \cdot C_O}{R_1 \cdot C_1 - R_C \cdot C_O} = \frac{1.337 \cdot 10^{-8} \cdot 50 \cdot 10^{-3} \cdot 470 \cdot 10^{-6}}{70.43 \cdot 10^3 \cdot 1.337 \cdot 10^{-8} - 50 \cdot 10^{-3} \cdot 470 \cdot 10^{-6}} = 3.422 \cdot 10^{-10} \text{F}$$

Until now, all the compensation network parameters have been decided.

Design Example (Buck)

A design example of typical application is shown below step by step.

Input/output specification

Parameter	Symbol	Value
Input voltage range	V_{IN}	100Vdc~480Vdc
Rated output power	P_O	1W
Rated output voltage	V_O	5V
Rated output current	I_O	0.2A

Preset parameter

Parameter	Symbol	Value
Inductance	L	2mH
Output capacitance	C_O	100uF
Output capacitance ESR	R_C	100mΩ
Upper resistor divider on FB pin	R_U	36kΩ
Lower resistor divider on FB pin	R_D	10kΩ

1）Boundary inductance calculate at Vin=100Vdc

$$L_{BCM}=\frac{(V_{BUS}-V_O)\cdot R_L}{2\cdot V_{BUS}\cdot F_S}=\frac{(100-5)\cdot 25}{2\cdot 100\cdot 60\cdot 10^3}=1.979\cdot 10^{-4}H$$

$L(2\cdot 10^{-3}H)>L_{BCM}(1.979\cdot 10^{-4}H)$, therefore, the circuit operates in CCM

2） Compensation design

Control to output transfer function simplified:

$$G_{vc2vo}(s)=\frac{\hat{v}_o(s)}{\hat{v}_c(s)}=\frac{R_L}{R_{CS}}\cdot\frac{1}{1+\frac{R_L\cdot T_S}{L}\cdot(m_c D'-0.5)}\cdot\frac{(1+\frac{s}{\omega_{zc}})}{(1+\frac{s}{\omega_p})\cdot(1+\frac{s}{Q_p\cdot\omega_n}+\frac{s^2}{\omega_n{}^2})}$$

Where R_{CS} is primary current sense resistor, $R_{CS}=1.39\Omega$ for SY26741

R_L is the equivalent load resistance, which can be derived as $R_L=\frac{V_O}{I_O}=\frac{5}{0.2}=25\Omega$

D is duty cycle under steady state $D=\frac{V_O}{V_{BUS}}=\frac{5}{100}=0.05$

D' is defined as $D'=1-D=1-0.05=0.95$

m_c is defined as: $m_c=1+\frac{S_e}{S_n}=1$

S_e is the external ramp compensation, $S_e = 0$ for SY26741

S_n is the sensed primary inductor current rising slope:

$$S_n = \frac{V_{BUS} - V_O}{L} \cdot R_{CS} = \frac{100-5}{2 \cdot 10^{-3}} \cdot 1.39 = 66.03 \cdot 10^3$$

The output capacitor ESR zero:

$$\omega_{zc} = \frac{1}{C_O \cdot R_C} = \frac{1}{100 \cdot 10^{-6} \cdot 100 \cdot 10^{-3}} = 100 \cdot 10^3$$

The main pole (low frequency):

$$\omega_p = \frac{1 + \frac{R_L \cdot T_S}{L} \cdot (m_c D' - 0.5)}{R_L \cdot C_O} = \frac{1 + \frac{25 \cdot 1.667 \cdot 10^{-5}}{2 \cdot 10^{-3}} \cdot (1 \cdot 0.95 - 0.5)}{25 \cdot 100 \cdot 10^{-6}} = 437.5$$

The double pole that located at half the switching frequency:

$$\omega_n = \frac{\pi}{T_S} = \frac{\pi}{1.667 \cdot 10^{-5}} = 188.5 \cdot 10^3$$

Quality factor $Q_P = \frac{1}{\pi(m_c \cdot D' - 0.5)} = \frac{1}{\pi(1 \cdot 0.95 - 0.5)} = 0.707$

Loop Compensation Network Parameter Calculation（Buck）

The open loop transfer function is derived as below equation:

$$G_{openloop} = K_C \cdot \frac{R_D}{R_U + R_D} \cdot \frac{G_m}{C_1 + C_2} \cdot \frac{R_L}{R_{CS}} \cdot \frac{1}{1 + \frac{R_L \cdot T_S}{L} \cdot (m_c D' - 0.5)} \cdot \frac{1}{s} \cdot \frac{(1 + \frac{s}{\omega_{z\_comp}})(1 + \frac{s}{\omega_{zc}})}{(1 + \frac{s}{\omega_{p\_comp}})(1 + \frac{s}{\omega_p})(1 + \frac{s}{Q_P \omega_n} + \frac{s^2}{\omega_n{}^2})}$$

Based on compensation principle: $\omega_{z\_comp} = \omega_P$, $\omega_{p\_comp} = \omega_{zc}$, and ω_n is far away from the cross over frequency, then the transfer function can be simplified as below equation:

$$G_{openloop} = K_C \cdot \frac{R_D}{R_U + R_D} \cdot \frac{G_m}{C_1 + C_2} \cdot \frac{R_L}{R_{CS}} \cdot \frac{1}{1 + \frac{R_L \cdot T_S}{L} \cdot (m_c D' - 0.5)} \cdot \frac{1}{s}$$

The cross over frequency ω_c of the open loop bode plot is defined as:

$$\omega_c = \frac{1}{10} \cdot f_S \cdot 2 \cdot \pi = \frac{1}{10} \cdot 60 \cdot 10^3 \cdot 2 \cdot \pi = 37.70 \cdot 10^3$$

and then according the Gain equation:

$$K_C \cdot \frac{R_D}{R_U + R_D} \cdot \frac{G_m}{C_1 + C_2} \cdot \frac{R_L}{R_{CS}} \cdot \frac{1}{1 + \frac{R_L \cdot T_S}{L} \cdot (m_c D' - 0.5)} \cdot \frac{1}{\omega_c} = 1$$

$C_1 + C_2$ is derived, under normal design, $C_1 \gg C_2$, so $C_1 + C_2 \approx C_1$, C_1 will be decided firstly:

$$C_1 \approx \frac{K_C R_D G_m R_L}{R_{CS}(R_U + R_D)(1 + \frac{R_L \cdot T_S}{L} \cdot (m_c D' - 0.5)) \cdot \omega_c}$$

$$C_1=\frac{0.25\cdot10\cdot10^3\cdot500\cdot10^{-6}\cdot25}{1.39\cdot\left(10\cdot10^3+36\cdot10^3\right)\cdot\left(1+\frac{25\cdot1.667\cdot10^{-5}}{2\cdot10^{-3}}\cdot\left(1\cdot0.95-0.5\right)\right)\cdot37.70\cdot10^3}=1.185\cdot10^{-8}\,\mathrm{F}$$

According to $\omega_{z\_comp}=\omega_p$, $\frac{1}{C_1R_1}=\frac{1+\frac{R_L\cdot T_S}{L}\cdot(m_c\,D'-0.5)}{R_L\cdot C_O}$, R_1 can be decided secondly:

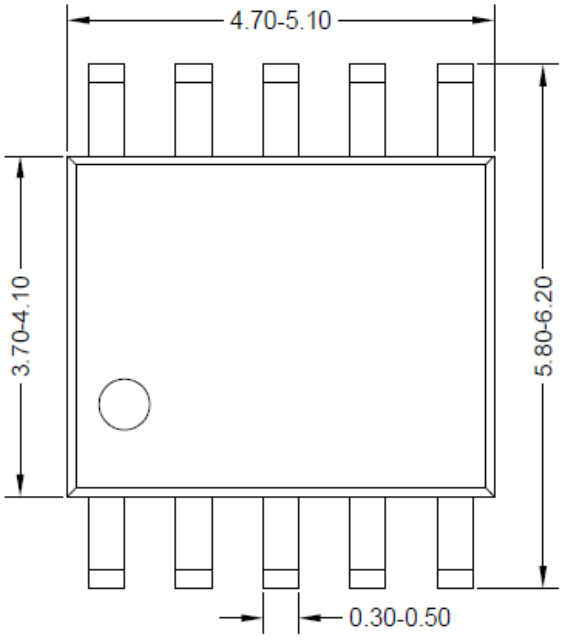
$$R_1=\frac{1}{C_1}\cdot\frac{R_L\cdot C_O}{1+\frac{R_L\cdot T_S}{L}\cdot(m_c\,D'-0.5)}=\frac{1}{1.185\cdot10^{-8}}\cdot\frac{25\cdot100\cdot10^{-6}}{1+\frac{25\cdot1.667\cdot10^{-5}}{2\cdot10^{-3}}\cdot\left(1\cdot0.95-0.5\right)}=192.88\cdot10^3\,\Omega$$

According to $\omega_{p\_comp}=\omega_{zc}$, $\frac{1}{R_1\cdot\frac{C_1C_2}{C_1+C_2}}=\frac{1}{C_O\cdot R_C}$, C_2 can be decided thirdly:

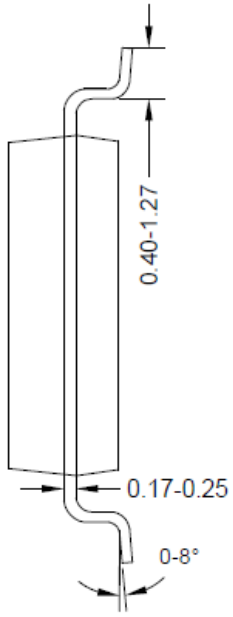
$$C_2=\frac{C_1C_OR_C}{C_1R_1-C_OR_C}=\frac{1.185\cdot10^{-8}\cdot100\cdot10^{-6}\cdot100\cdot10^{-3}}{1.185\cdot10^{-8}\cdot192.88\cdot10^3-100\cdot10^{-3}\cdot100\cdot10^{-6}}=5.207\cdot10^{-11}\,\mathrm{F}$$

Until now, all the compensation network parameters have been decided.

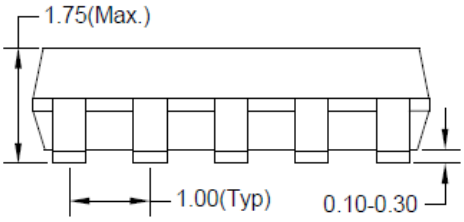
SSOP10 Package Outline Drawing



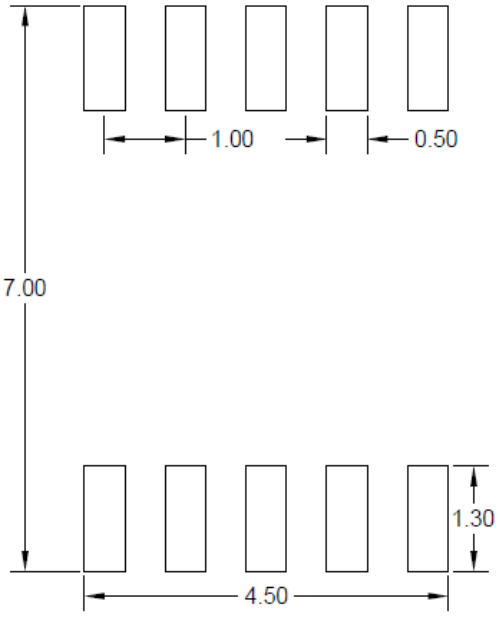
Top view



Side view



Front view



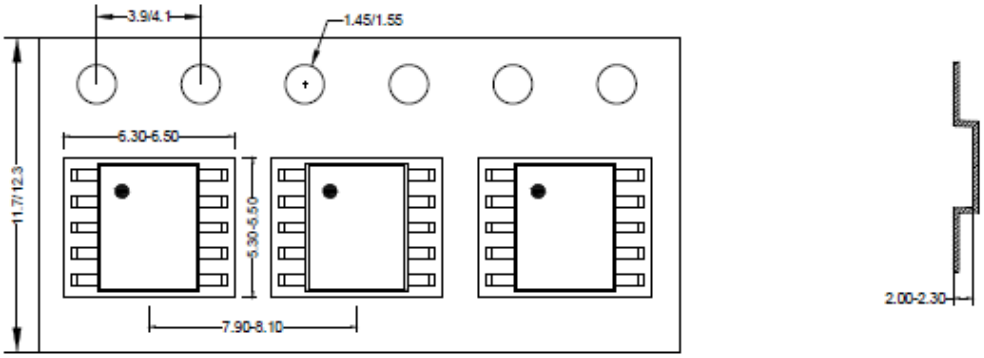
Recommended PCB layout

(Reference only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

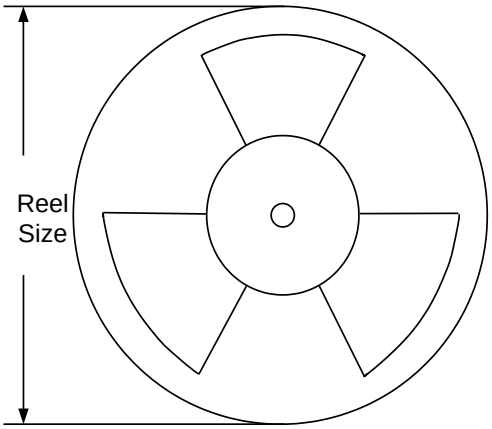
Taping & Reel Specification

1. Taping orientation for packages（SSOP10）



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
SSOP10	12	8	13"	400	400	2500

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
February 28, 2024	Revision 1.0A	Update the EC table
December 27, 2023	Revision 0.9	Initial Release

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