SY23421

Secondary Side Synchronous Rectification

General Description

The SY23421 is a synchronous rectification switcher with high performance capabilities, ideal for use in flyback converters operating in CCM (Continuous Conduction), DCM (Discontinuous Conduction), and QR (Quasi-Resonant) modes.

To prevent false turn-on by parasitic ringing under DCM or QR mode, the device uses the DRAIN voltage falling slope rate detection.

The SY23421 features a DRAIN high-voltage blanking time detection function that enhances system ESD performance, preventing external noise from false turn-on of the SR (Synchronous Rectifier) MOSFET.

Under CCM operating mode, it has an extremely short turn-off delay time, while the DRAIN voltage regulation fully utilizes the conduction time of the SR MOSFET for optimizing the efficiency under DCM and QR modes.

During light load conditions, the device enters power saving mode to improve light load efficiency.

Features

- Suitable for CCM, DCM and QR Mode Flyback Converter
- DRAIN Falling Slope Rate Detecting to Avoid False Turn On of SR MOSFET by Parasitic Ring
- DRAIN High Voltage Blanking Time detecting to enhance system ESD performance
- Dual Power Supply Channel for 3.3V to 12V Output Systems
- Compact Package: SO8

Applications

- AC/DC Adapters
- USB Type-C and Power Delivery AC Adapters
- Server and Telecom Power Supply
- Auxiliary Power Supplies

Typical Application

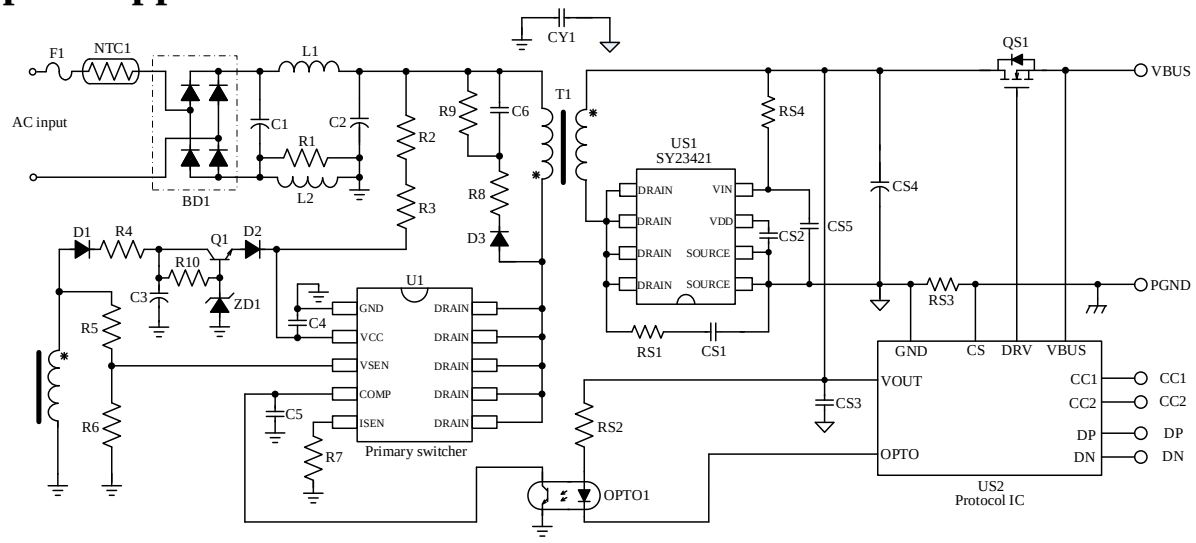


Fig. 1 Typical Application Circuit (SR MOSFET location: Low Side)

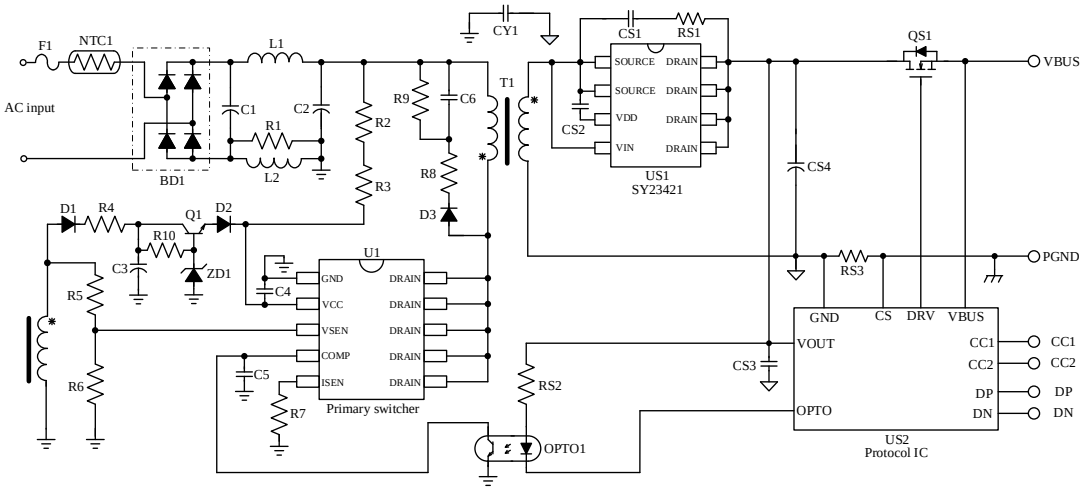


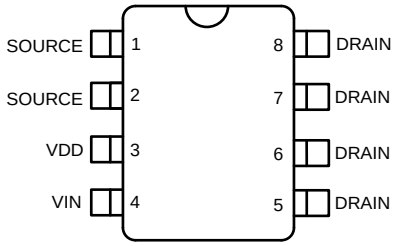
Fig. 2 Typical Application Circuit (SR MOSFET location: High Side)

Ordering Information

SY23421□(□□□)

Package Code

Optional Spec Code



SO8

Pinout (top view)

Ordering Number	Package	Top Mark
SY23421FAP	SO8	EFWxyz

x=year code, y=week code, z= lot number code

Pinout (top view)

Pin number	Pin Name	Pin Description
1,2	SOURCE	Source terminal of integrated SR MOS, also the analog GND
3	VDD	Output of internal LDO, power supply for control unit and drive circuit. Connect a 0.1μF or larger ceramic capacitor between VDD and SOURCE pin
4	VIN	Power supply pin, connect it to the output of converter when SR MOSFET is located at low side. Connect it to SOURCE pin when SR MOSFET is located at high side
5,6,7,8	DRAIN	DRAIN terminal of integrated SR MOSFET, also used for self-supply

Block Diagram

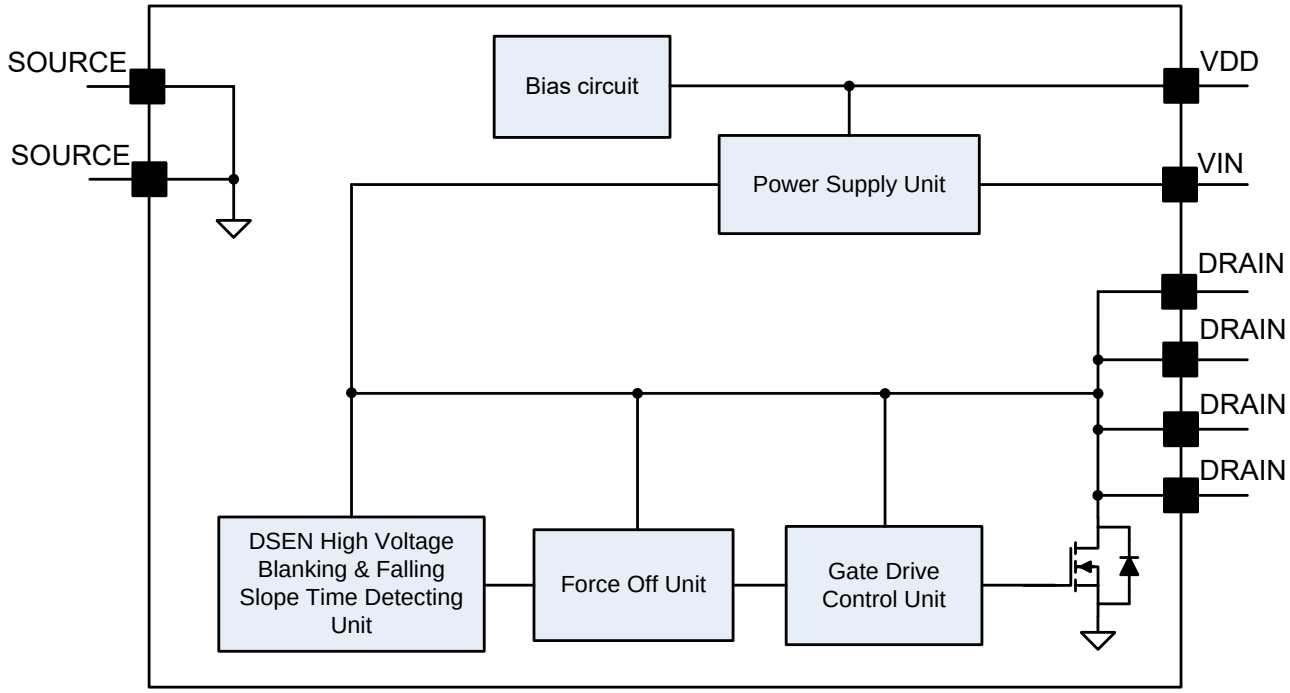


Fig.3 Block diagram

Absolute Maximum Ratings (Note 1)

VIN ---------- -0.3V~28V
VDD ---------- -0.3V~16V
DRAIN ---------- -1V~65V
Power Dissipation, @ T_A = 25°C SO8----------1.1W
Package Thermal Resistance (Note 2)
SO8, θ_{JA}----------150°C/W
SO8, θ_{JC}----------60°C/W
Junction Temperature Range ---------- -45°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions

VIN ---------- 3.3V~12V
VDD ---------- 3V~9.5V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 105°C

Electrical Characteristics

(V_{VIN}=12V, T_A=25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VIN Pin						
Threshold of Switching to VIN Supply Channel	V_{VIN_VINSPY}	V_{IN} is rising	4.35	4.6	4.85	V
Threshold of Switching to DRAIN Supply Channel	$V_{VIN\_DRAINSPY}$	V_{IN} is falling	4.3	4.55	4.8	V
VDD Pin						
ON Threshold	V_{VDD_ON}		5	5.26	5.52	V
UVLO Hysteresis	V_{VDD_HYS}		1.9	2.15	2.4	V
VDD Regulation Voltage when VIN Pin is Active to Supply IC	$V_{VDD\_REG\_VIN}$		8.5	9.0	9.4	V
VDD Regulation Voltage when DRAIN Pin is Active to Supply IC	$V_{VDD\_REG\_DRAIN}$		8.5	9.0	9.4	V
Maximum VDD Pin Capacitor Charging Current	$I_{VDD\_CHARGE\_MAX}$	VIN pin is active to charge VDD capacitor	12	17		mA
		DRAIN pin is active to charge VDD capacitor	40	50		mA
Quiescent Current	I_{VDD_STBY}	Under Standby Mode		230	280	μA
DRAIN Pin						
Blanking Time for Sample PVS Pin Voltage	T_{PVS_BLK}		210	310	410	ns
Low Level Threshold to Sense VDRAIN Falling Time	V_{DRAIN_LTH}	V_{DRAIN} is falling	10	20	30	mV
Closed Loop V_{DRAIN} Regulation Voltage Level	V_{DS_REG}	SR MOSFET is conducting	-55	-40	-25	mV
SR MOSFET Turn off Threshold	V_{OFF_TH}	V_{DRAIN} is rising	-10	0	10	mV
Time Threshold IC Go into Sleep(Note 3)	$T_{STANDBY}$		15	20	25	us
MOSFET Section						
MOSFET Break down Voltage	$V_{DSS(BR)}$	V_{GS}=0V, I_D=0.25mA	65			V
MOSFET On-state Resistor	$R_{DS(ON)}$	V_{GS}=10V, I_D=10A		8.7	9.5	mΩ
Continuous Drain Current(Note 3)	I_D				10	A
Pulsed Drain Current(Note 3)	I_{DM}				40	A
Blanking Time Section						
Minimum ON Time	T_{ON_MIN}		500	700	900	ns
Minimum OFF Time	T_{OFF_MIN}		400	565	730	ns
OTP						
Thermal Shutdown Temperature(Note 3)	T_{SD}			160		°C
Hysteresis to Resume Operating(Note 3)	T_{OTP_HYS}			20		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

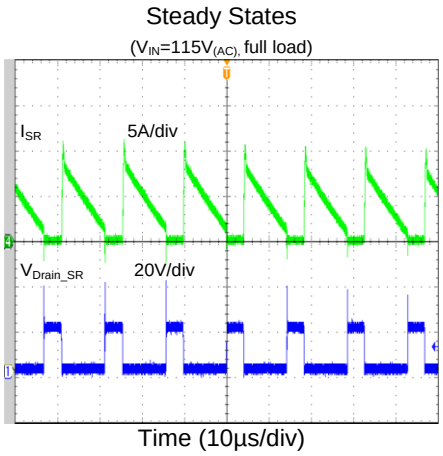
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on "2x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal via to bottom layer ground plane.

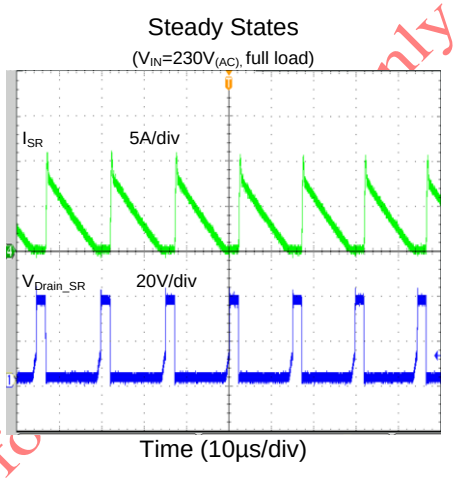
Note 3: Guarantee by design.

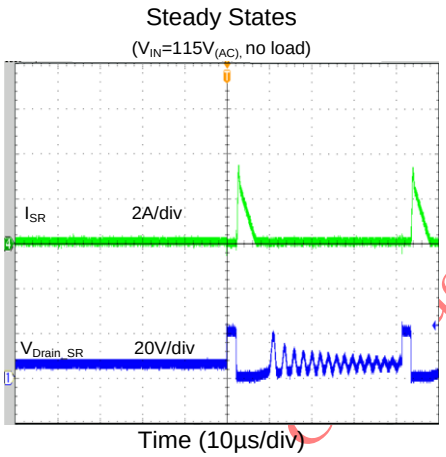
Typical Performance Characteristics

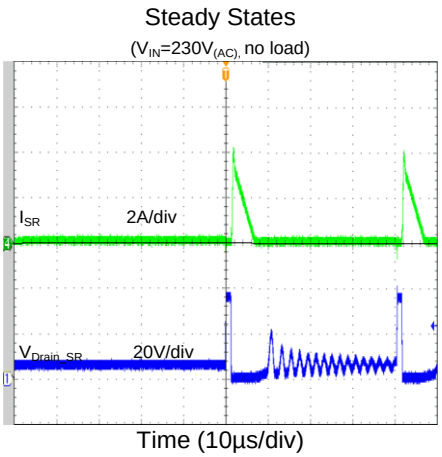
(Test condition: input voltage: 90Vac~264Vac; output spec: 5Vdc_3A, 12Vdc_2.08A; Ambient temperature: 25±5 ℃; Ambient humidity: 65±25 %.)

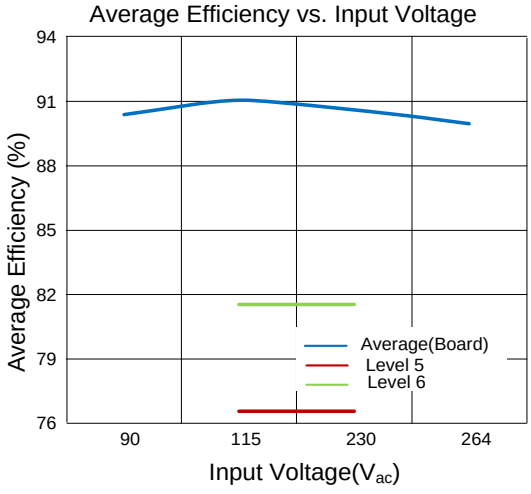
5Vdc_3A output





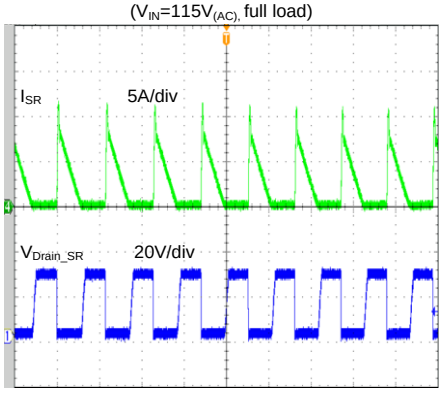






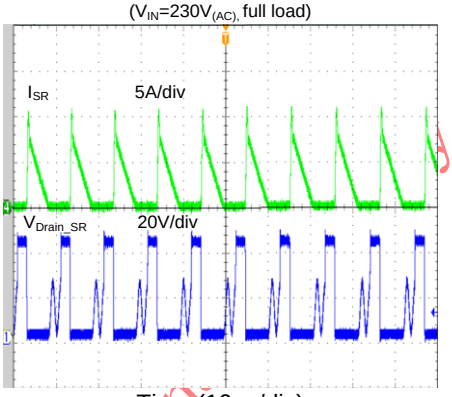
12Vdc_2.08A output

Steady States
(V_{IN}=115$V_{(AC)}$, full load)



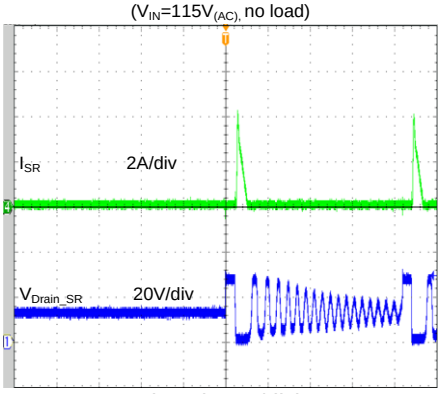
Time (10µs/div)

Steady States
(V_{IN}=230$V_{(AC)}$, full load)



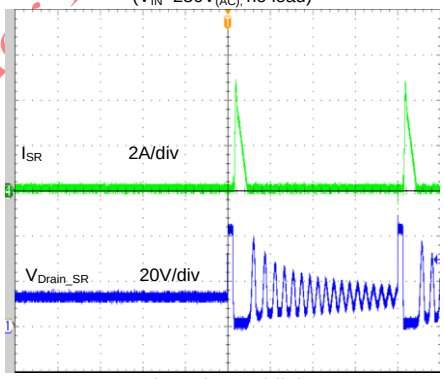
Time (10µs/div)

Steady States
(V_{IN}=115$V_{(AC)}$, no load)



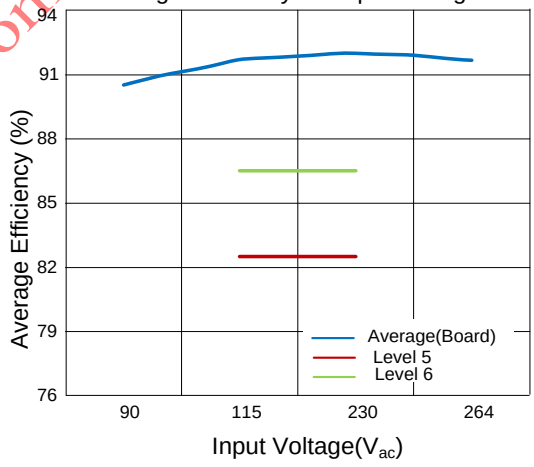
Time (10µs/div)

Steady States
(V_{IN}=230$V_{(AC)}$, no load)



Time (10µs/div)

Average Efficiency vs. Input Voltage



Detailed Description

General Features

GATE Drive

For proper operation, while V_{VDD}<V_{VDD_ON} the SR MOSFET gate is pulled down. The circuit in the diagram below is used for this purpose:

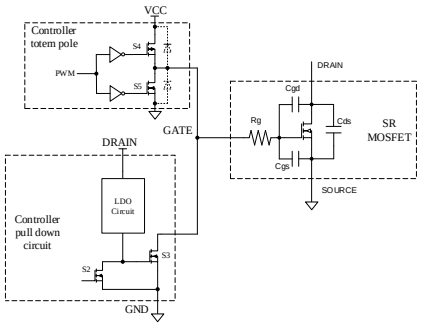


Fig. 3 Circuit Used for SR MOSFET Control during Start-up

When V_{VDD}<V_{VDD_ON}, switch S2 is Open and the DRAIN voltage will charge the Cgs capacitance for the S3 switch. When S3 turns ON, it will pull down the gate of the SR MOSFET. The pull down current of S3 is 200mA (@Vgs=1V for the POWER MOSFET) to optimize the performance.

While V_{VDD}>V_{VDD_ON}, the S2 switch is closed, leading to S3 being turned OFF (switch open). The GATE pin will be controlled only by the driver circuit consisting of S4 and S5, as shown in Fig.3 & Fig.4.

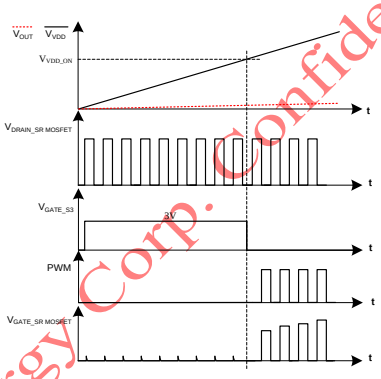


Fig. 4 GATE Pin Timing diagram

SR MOSFET GATE Control

The traditional method of turning ON the SR MOSFET is to use a set turn-on threshold V_{ON_TH}.

When the DRAIN voltage falls and reaches V_{ON_TH}, the SR MOSFET is turned ON after a short delay.

While in DCM or QR operating modes, a resonant waveform may appear after the transformer secondary current decreases to zero. Sometimes, the amplitude of this resonant waveform can be large enough to cause the DRAIN voltage to drop below the turn-on threshold V_{ON_TH}, which may lead to the false turn-on of the SR MOSFET. To address this issue, a circuit to detect the falling slope rate of V_{DRAIN} is used.

When the primary MOSFET Q1 is turned off, the V_{DRAIN} falling slope rate is very high, and the SR MOSFET will turn on. During the resonant phase, the V_{DRAIN} falling slope rate is relatively low, and the SR MOSFET will not turn on. The SY23421 uses a resistor divider circuit to sense the DRAIN voltage, where V_{PVS} is 0.02 x V_{DRAIN}.

Two thresholds are set to sense the V_{PVS} falling slope rate. △T is the time duration measured when V_{PVS} is falling between the high-level threshold V_{PVS_HTH} and the low-level threshold V_{DRAIN_LTH} (0mV). △T is compared with a falling slope reference time T_{REF} using a counter.

A blanking period is used to prevent external noise (such as ESD noise) from falsely turning on the SR MOSFET.

If V_{PVS} is above V_{PVS_HTH}, lasts for T_{PVS_BLK} (300ns) and the falling slope time △T <T_{REF}, the IC considers this action as a primary MOSFET turn-off event, and will turn ON the SR MOSFET after a short delay. In all other cases the SR MOSFET will not be turned ON.

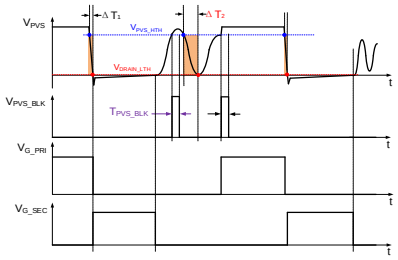


Fig. 5 SR MOSFET Turn ON Time Diagram

V_{PVS_HTH} is a dynamically adjusted value, and it has a value of 0.85 x V_{DRAIN}. The falling slope ref time threshold T_{REF} is 170ns (Typical value).

In DCM mode, the current through the SR MOSFET will decrease before the primary MOSFET is turned on. The closed-loop V_{DS} regulation circuit will gradually reduce V_{GATE} once V_{DS} is above the V_{DS_REG} (-40mV) level. As the current through the SR MOSFET decreases, V_{GATE} drops close to the turn-off threshold of the SR MOSFET. At this point, the product of the (I_D x R_{DSON}) can no longer be regulated to V_{DS_REG}, causing V_{DS} to increase beyond V_{OFF_TH}. After a short delay time T_{OFF_DLY} (10ns), a large sink current will pull down the gate voltage to zero to turn OFF the SR MOSFET.

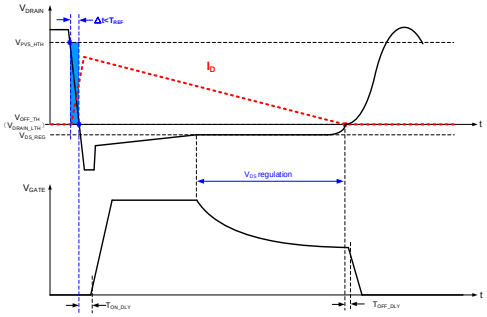


Fig. 6 SR MOSFET Control in DCM Mode

During the CCM mode, the primary MOSFET will be turned ON before secondary current decreases to ZERO, and V_{DRAIN} will rapidly increase. The device will compare V_{DRAIN} with another threshold V_{OFF_TH}, and once V_{DRAIN} is rising and crossing V_{OFF_TH}, after a short delay time T_{OFF_DLY}, the gate voltage will be pulled down by a large sink current to achieve fast turn off. The turn off delay time T_{OFF_DLY} (10ns) is designed to be very short to minimize the power loss caused by primary and secondary MOSFET overlap.

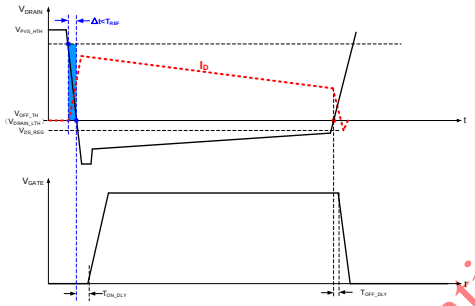


Fig. 7 SR MOSFET in CCM Mode

Min ON Time & Min OFF Time

When primary MOSFET is turned off, the DRAIN voltage of the secondary SR MOSFET will drop rapidly to about -700mV, due to the circuit parasitic resonance. To void false turn off of the SR MOSFET, a blanking time T_{ON_MIN} is applied after the SR MOSFET is turned ON. During this blanking time, the GATE pin output is latched off.

After SR MOSFET is turned OFF, a ringing will appear on DRAIN voltage waveform. To avoid the internal logic circuit false trigger, a blanking time T_{OFF_MIN} used.

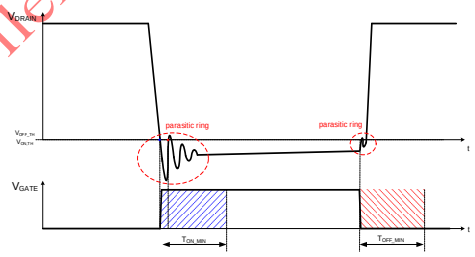


Fig. 8 Timing Diagram of Min ON/OFF Time

Power Supply

The device optimizes the overall efficiency by using two possible power sources during normal operation.

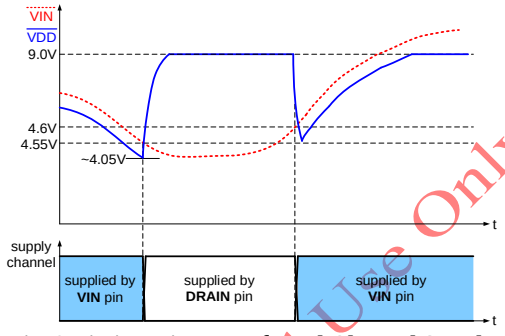


Fig. 9 Timing Diagram of Dual Channel Supply

Before VDD voltage reaches the V_{VDD_ON} threshold, the voltage is supplied by DRAIN pin. When the voltage exceeds the V_{VIN_VINSPY} threshold, the VIN pin will be used instead.

As VIN increases, VDD will follow VIN (with about 0.5V voltage drop). When the voltage goes above 9V, the rail is regulated internally to this value.

When VIN is decreasing and crossing $V_{VIN\_DRAINSPY}$, the device will switch to using the DRAIN pin, and VDD will be regulated to 9V. The timing diagram is shown in Fig. 9.

Power Saving Mode

Under light load conditions, the SY23421 will enter power saving mode to improve light load efficiency.

During the switching cycle, a timer will start to count after SR MOSFET is turned off. If the timer counts to 20us before next SR turn ON, the device will enter the power saving mode to

reduce the power consumption. The SY23421 will exit power saving mode on the next SR MOSFET turn ON event.

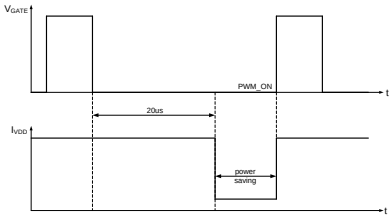


Fig. 10 Timing Diagram of Power Saving Mode

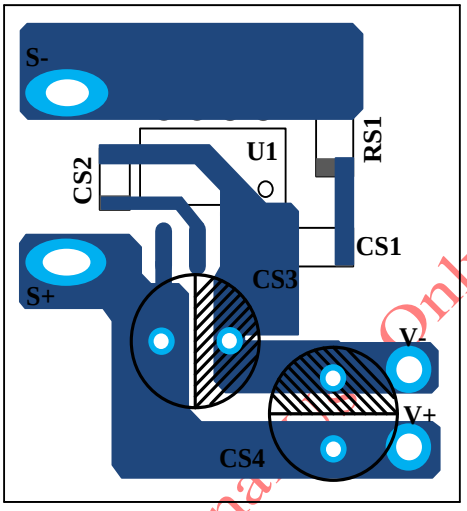
Over Temperature Protection

IC die temperature is monitored, if the die temperature rises above 160℃, IC will stop driving SR MOSFET and the keep gate voltage to 0V. When die temperature drops below 140℃, IC will resume normal operating again.

Layout

Follow the follwing PCB layout guidelines for optimal performance and thermal dissipation:

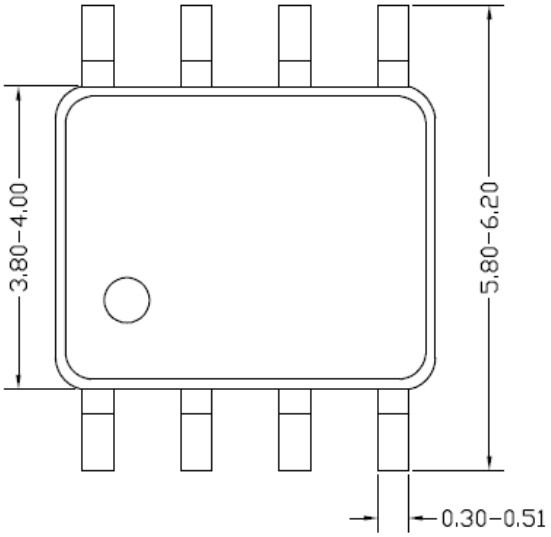
- Minimize the size of the switching loops: secondary power loop, secondary RC snubber circuit loop and IC power supply loop.
- To achieve better EMI and Efficiency performance, use a decoupling capacitor between the output connector and the SR MOSFET output.
- To reduce ringing the parasitic inductance should be reduced by optimizing the layout, and/or increasing the RC snubber.



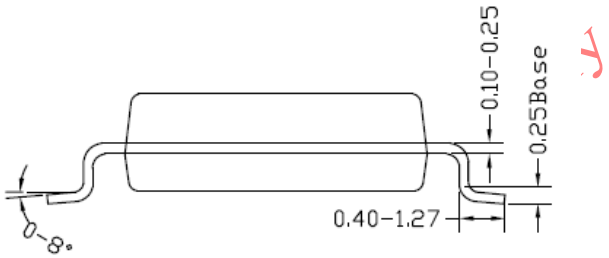
Design Notice

1. To prevent SR turn off later at no load, the SR freewheeling time should be more than the minimum ON time.
2. To improve the system ESD performance, a 10Ω~51Ω resistor should be used in series between VIN pin and output terminal, and at least 100nF cap should be used in parallel between VIN pin and SOURCE pin.

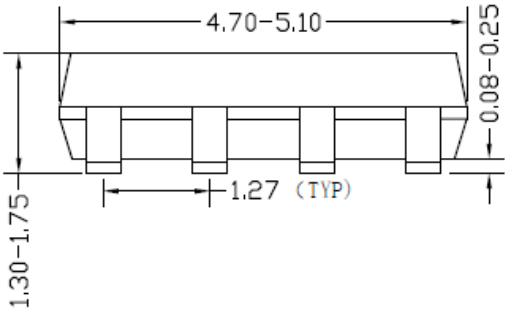
SO8 Package outline & PCB layout design



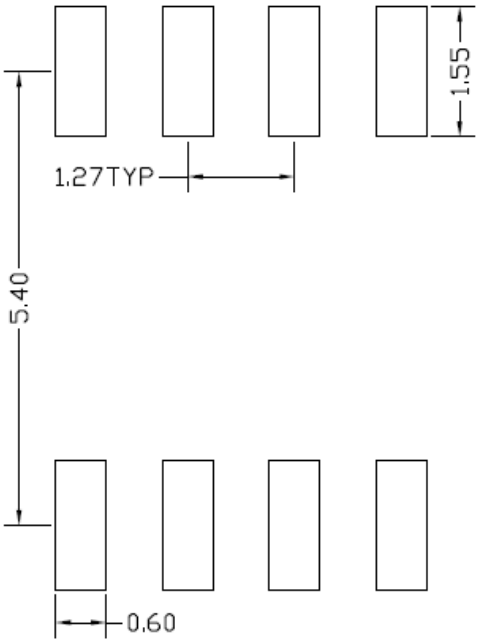
Top view



Side view



Front view

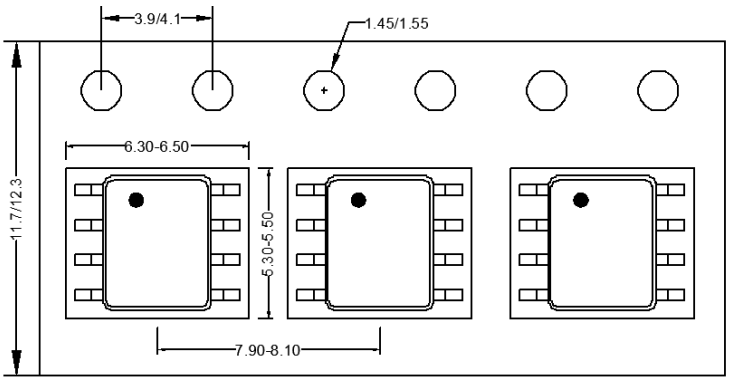


Recommended Pad Layout (Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

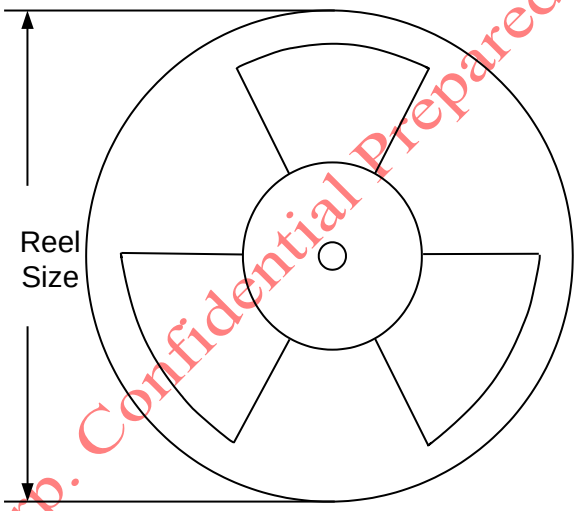
Taping & Reel Specification

1. Taping orientation for packages（SO8）



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SO8	12	8	13"	400	400	2500

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
January 18, 2024	Revision 1.0A	Update the EC table Modify the function description
December 17, 2021	Revision 0.9	Initial Release

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