SY5601

IEEE 802.3 af/at POE compliant Powered Device (PD) Controller

General Description

SY5601FCP is an IEEE 802.3 af/at POE compliant Powered Device (PD) controllers. It includes detection and classification modes as well as a 100V output pass switch. Thermal protection is built in to accommodate both transient and/or overload conditions, shutting down the pass switch and protecting the input source. Inrush current limiting is included to slowly charge the input capacitor without interruption due to die heating.

Features

- Meets IEEE 802. 3 af/at Specifications
- 100V, 0.45Ω Integrate PASS Switch
- 100mA Inrush Current Limit
- 600mA Operation Current Limit
- Open Drain Power Good Output
- SO8E Package Support Flexible Topology Design

Applications

- VoIP Telephones
- Network Cards
- Security Camera Systems
- Safety Backup Power
- Remote Internet Power Eras

Ordering Information

SY5601 □(□□□)

Package Code

Optional Spec Code

Ordering Number	Package type	Note
SY5601FCP	SO8E	----

Typical Applications

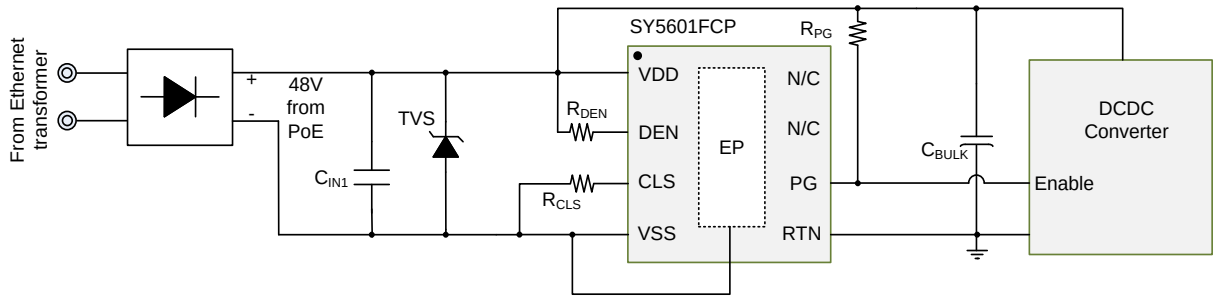
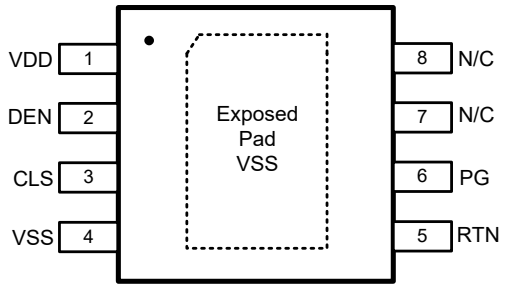


Fig.1 Schematic Diagram

Pinout (top view)



(SO8E)

Top Mark: EMG*xyz* (device code: EMG, ***x=year code, y=week code, z= lot number code***)

Pin number	Pin Name	Pin Description
1	VDD	Positive power supply terminal for PoE and controller input power rail.
2	DEN	Detection. Connect a 24.9kΩ resistor between VDD and DEN for PoE detection.
3	CLS	Classification. Connect a resistor from CLS to VSS to program the classification current.
4, EP	VSS	Negative power supply terminal from PoE input power rail.
5	RTN	Drain of PD hot-swap MOSFET and negative rail input of the DCDC converter.
6	PG	Power Good Indicator. Active low, open-drain converter disable output, referenced to RTN.
7,8	N/C	Not connected internally.

Absolute Maximum Ratings (1)

Pins Voltage Respects to VSS:

VDD---------- -0.3V to +100V
DEN, RTN, PG---------- 0.3V to VDD+0.7V
CLS(2) ---------- -0.3V to +5.5V

Pins Voltage Respects to RTN:

VDD, PG---------- -0.3V to +100V

Pins Current:

PG Sink Current---------- 0.5mA(3)
Package Thermal Resistance (4)
SO8E, θ_{JA} ---------- TBD
SO8E, θ_{JC} ---------- TBD
Junction Temperature Range ---------- -45°C to 150°C

Recommended Operating Conditions

Supply Voltage VDD---------- 0V to 57V
Maximum PG Sink Current---------- 0.1mA (3)
Operating Junction Temperature(T_J)---------- ---------- -40℃to +125℃

Notes:

(1) Exceeding these ratings may damage the device.
(2) Voltage should not be externally applied to this pin.
(3) If PG is pulled up to higher than 5V externally, the pull up current should be limited.
(4) JESD 51-2，-5，-7，-8，-14 standard.

Block Diagram

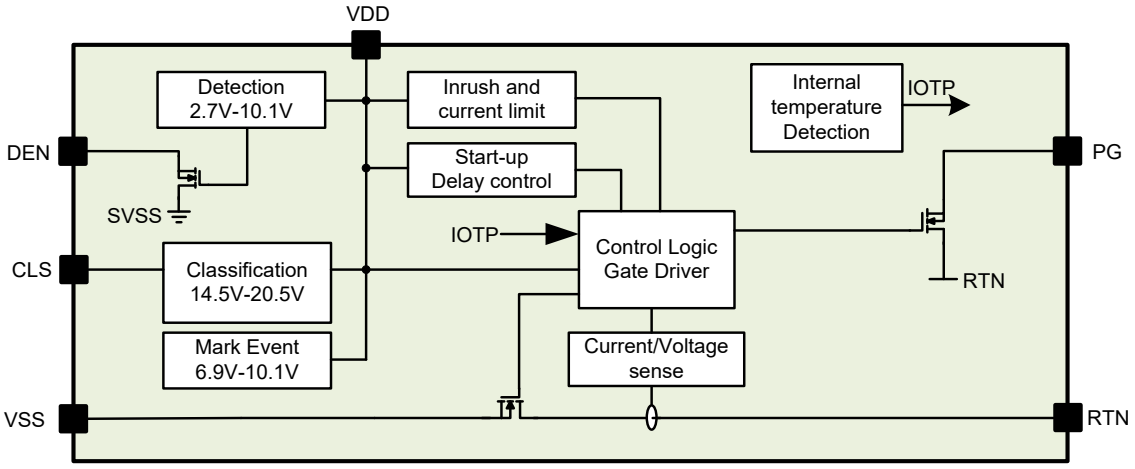


Fig.2 Block Diagram

Electrical Characteristics

VDD, CLS, DEN and RTN voltages are referred to VSS, PG voltage is referred to RTN. VDD-VSS=48V, R_{DEN}=24.9 kΩ, R_{CLS}=90.9 Ω,T_J=-40℃ to +125℃(5),typical values are tested at T_J=25℃,unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Detection						
Detection on	V_{DET_ON}	V_{DD} rising		1.1	1.4	V
Detection off	V_{DET_OFF}	V_{DD} rising		11		V
DEN Leakage Current	V_{DET_LK}	V_{DET}=V_{DD} =57V, measure I_{DET}		0.1	5	μA
Bias Current		V_{DD} =10.1 V, float DET pin, not in Mark event, measure I_{SUPPLY}			12	μA
Detection Current	I_{DET}	V_{DD}=1.4V, measure I_{SUPPLY}	53.8	55.6	58.3	μA
		V_{DD}=10.1V, measure I_{SUPPLY}	395	410	425	μA
Classification						
Classification Stability Time				90		μs
V_{CLASS} Output Voltage	V_{CLASS}	13V<VDD<21V, 1mA<I_{CLASS}<42mA	2.37	2.5	2.63	V
Classification Current	I_{CLASS}	13 V ≤ V_{DD}≤ 21 V, Guaranteed by V_{CLASS}				
		R_{CLASS} = 1270 Ω, 13 V ≤ V_{DD}≤ 21 V	1.8	2	2.4	mA
		R_{CLASS} = 243 Ω, 13 V ≤ V_{DD}≤ 21 V	9.9	10.55	11.3	
		R_{CLASS} = 137 Ω, 13 V ≤ V_{DD}≤ 21 V	17.7	18.7	19.8	
		R_{CLASS} = 90.9 Ω, 13 V ≤ V_{DD}≤ 21 V	26.6	28.15	29.7	
		R_{CLASS} =63.4 Ω, 13 V ≤ V_{DD}≤ 21 V	38.2	40.4	42.6	

Classification Lower Threshold	V_{CL_ON}	V_{DD} rising, Class regulator turns on	11	12	13	V
Classification upper Threshold	V_{CL_OFF}	V_{DD} rising, Class regulator turns off	21	22	23	
Classification Hysteresis	V_{CL_H}	Low side hysteresis		0.94		
		High side hysteresis		0.5		
Mark Event Reset Threshold	V_{MARK_L}		4	5	6	V
Max Mark Event Voltage	V_{MARK_H}		11	12	13	V
Mark Event Resistance	R_{MARK}	2-point measure at 7V and 10V			12	kΩ
IC Supply Current during Classification	I_{IN_CLASS}	V_{DD}=17.5V, CLASS floating		200	270	μA
Class Leakage Current	I_{LK}	V_{DD}=57V, V_{CLASS}=0V			1	μA
PD UVLO						
VDD Turn on Threshold	$V_{DD\_VSS\_R}$	V_{DD} rising	33	35	37	V
VDD Turn off Threshold	$V_{DD\_VSS\_F}$	V_{DD} falling	29	31	33	V
VDD UVLO Hyteresis	$V_{DD\_VSS\_HYS}$			4		V
IC Supply Current during Operation	I_{IN}			380		μA
PG						
ON Resistance	R_{DS-PG}	I_{PG} = 0.5mA		2.5	5	kΩ
Output High Leakage Current		V_{PG}=48V			1	μA
PASS Device and Current Limit						
ON Resistance	R_{DS-RTN}	I_{RTN}=100mA		0.45		Ω
Leakage Current	I_{RTN-LK}	V_{DD}=V_{RTN}=57V		1	15	μA
Current Limit	I_{LIMIT}	V_{RTN}=1 V	530	600	670	mA
Inrush Current Limit	I_{INRUSH}	V_{RTN}=2 V		100		mA
Inrush Current Termination		V_{RTN} falling		1.2		V
Inrush to Operation Mode Delay	T_{DELAY}		80	100	120	ms
Current Fold-back Threshold		V_{RTN} rising		10		V
Fold-back Deglitch Time		V_{RTN} rising to inrush current fold-back		1.1		ms
Protection						
Thermal Shutdown Temperature	T_{SD}			150		℃
Thermal Shutdown Hysteresis	T_{HYS}			20		℃

Notes:
(5) Not tested in production. Guaranteed by over-temperature correlation.

Operation Principles

DEN Detection and Enable

DEN pin implements two separate functions.

A resistor connected between VDD and DEN generates a detection signature whenever the voltage differential between VDD and VSS lies from approximately 1.4 to 10.9 V. Beyond this range, the controller disconnects this resistor to save power. The IEEE 802.3af/at standard specifies a detection signature resistance, R_{DEN} from 23.75 kΩ to 26.25 kΩ, or 25 kΩ ± 5%. Silergy recommends a resistor of 24.9 kΩ ± 1% for R_{DEN}.

Pulling DEN down to VSS during powered operation causes the internal PASS Switch and class regulator to turn off. The falling threshold to disable PASS Switch is 3.7V, the debounce time is 3ms to prevent wrongly triggered in Surge test.

Classification

In the classification mode, the PSE will classify the PD for one of five power levels or classes. This allows the PSE to efficiently manage power distribution. The five different classes is shown in Table 1, it determine the class the PD must advertise. An external resistor (R_{CLS}) connected from CLS to VSS sets the classification current. The PSE may disconnect a PD if it draws more than its stated Class power. During hardware Classification, the PSE presents a fixed voltage between 15.5 V and 20.5 V to the PD, which in turn draws a fixed current set by R_{CLS}. PD current is measured by the PSE to determine which of the five available classes is advertised (see Table 1). The SY5601 disables classification while the input voltage is above 22V to avoid excessive power dissipation.

Table 1. Class Resistor Selection

Class	Power at PD(W)	Class current (mA)	Resistor(Ω)
0	0.44~12.95	0~4	1270
1	0.44~3.84	9~12	243
2	3.84~6.49	17~20	137
3	6.49~12.95	26~30	90.9
4	-	36~44	63.4

2-Events Classification

The SY5601 can be used as a Type-1 PD class 0-3 (as shown in Table 1). It also distinguishes class 4 with 2-event classification.

In 2-event classification, the Type-2 PSE reads the power classification twice. Figure 2 shows an example of a 2-event classification. The first classification event occurs when the PSE presents a voltage between 14.5V to 20.5V to the SY5601, and SY5601 presents a class-4 load current. The PSE then drops the input voltage into the mark voltage range of 6.9V to 10.1V, signaling the first mark event. The SY5601 presents a load current between 0.5mA to 2mA in the mark event voltage range.

The PSE repeats this sequence, signaling the second classification and second mark event. The PSE then applies power to the SY5601, which charges up the DC/DC input capacitor with a controlled inrush current.

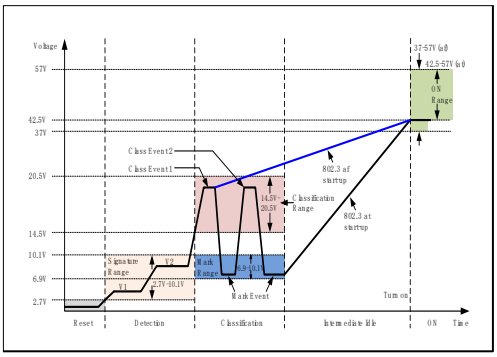


Fig.3 PD Interface Operation Description

PD Interface UVLO and Inrush Current Limit

When PD is powered by PSE, and VDD is higher than the turn-on threshold, the hot-swap switch begins passing a limited current (I_{INRUSH}) to charge the downstream DC/DC converter's input capacitor The start-up charging current I_{INRUSH} is limited to around 100mA to comply with the IEEE 802.3af/at standard.

If V_{RTN} drops below 1.2V, and the 100ms inrush delay from UVLO begins is finished, the hot-swap current limit changes to 600mA, at the same time SY5601 releases the PG signal. The PG signal rises high if it is pulled up externally, so PG can be used to enable the DC/DC controller. If V_{VDD} drops below the falling UVLO, the hot-swap MOSFET is disabled.

If the output current overload occurs on the internal pass MOSFET, the current limit works, and V_{RTN}-V_{VSS} rises. If V_{RTN} rises above 10V for longer than 1.1ms, the current limit reverts to the inrush value, and PG will be pulled down at the same time.

Fig.2 shows the current limit, the PG work logic during start-up from the PSE power supply.

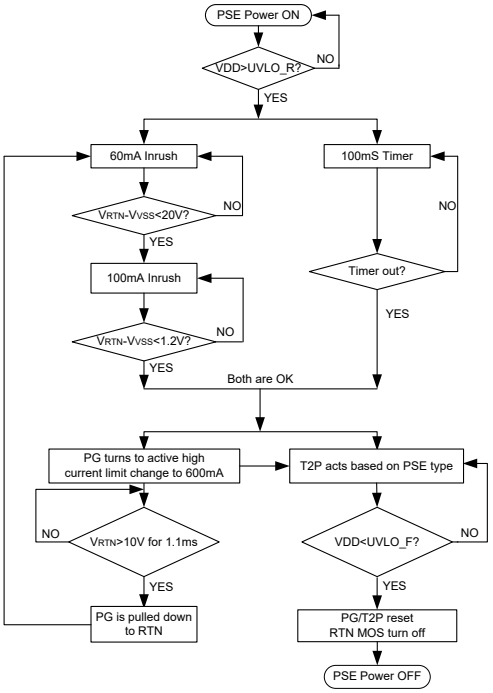


Fig.4 Typical Startup Sequence of PoE input

PG Control (PG)

When the input voltage is above UVLO, the SY5601 starts to inrush and a 100ms timer starts to count. PG will be pulled down to the RTN until the hot-swap switch turns on completely and the 100ms timer expires. It remains in a high impedance state at all other times. This pin is an open-drain output, and it may require a pull-up resistor or other interface to the downstream load. PG may be left open if it is not used.

Typical Application

Detection Resistor

The input diode bridge's incremental resistance can be hundreds of ohms at the low currents. The bridge resistance is in series with R_{DEN} and increases the total resistance seen by the PSE. This varies with the type of diode selected by the designer, and it is not usually specified on the diode data sheet. The value of R_{DEN} may be adjusted downwards to accommodate a particular diode type. Silergy recommends a resistor of 24.9 kΩ ± 1% for R_{DEN}.

Input Diodes or Diode Bridges

The IEEE 802.3af requires the PD to accept power on either set of input pairs in either polarity. This requirement is satisfied by using two full-wave input bridge rectifiers as shown in Figure 3. Silicon p-n diodes with a 1-A or 1.5-A rating and a minimum breakdown of 100 V are recommended, however Schottky diodes will yield a somewhat lower power loss. Diodes exhibit large dynamic resistance under low-current operating conditions such as in detection. The diodes should be tested for their behavior under this condition. The total forward drops must be less than 1.5 V at 500 µA and at the lowest operating temperature.

Input Capacitor

The IEEE 802.3af requires a PD input capacitance between 0.05 µF and 0.12 µF during detection. This capacitor should be located directly adjacent to the SY5601 as shown in Figure 3. A 100-V, 10%, X7R ceramic capacitor meets the specification over a wide temperature range.

Layout

The layout of the PoE front end must use good practices for power and EMI/ESD. A basic set of recommendations include:

1. The parts placement must be driven by the power flow in a point-to-point manner such as Ethernet Interface → diode bridges → TVS and 0.1-µF capacitor → SY5601 → output capacitor.

2. All leads should be as short as possible with wide power traces and paired signal and return.

3. The SY5601 should be over a local ground plane or fill area referenced to VSS.

Fig 4 and Fig 5 show the top and bottom layer and assemblies of the SY5601EVB as a reference for optimum parts placement.

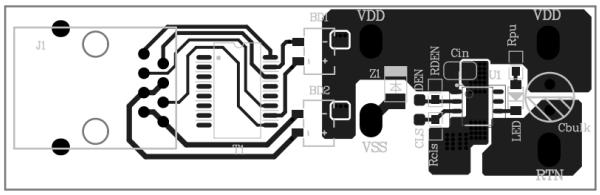


Fig.5 Top side

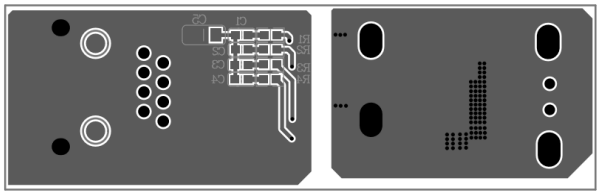


Fig.6 Bottom side

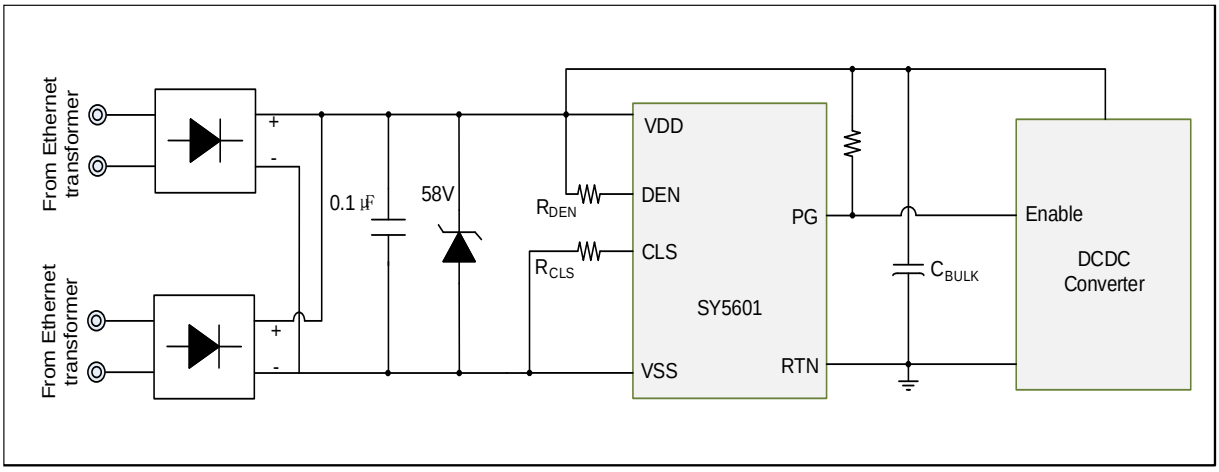
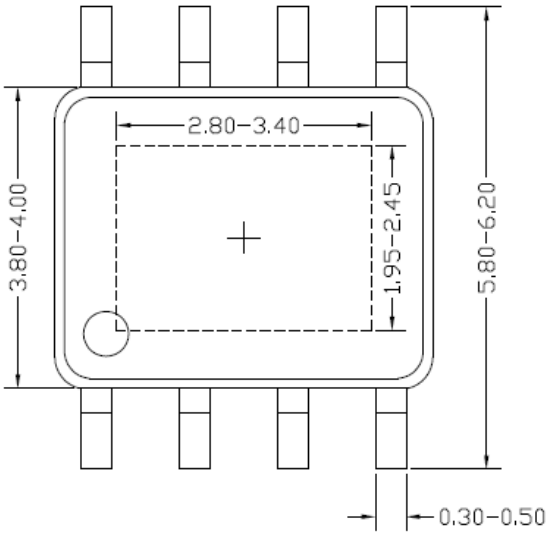
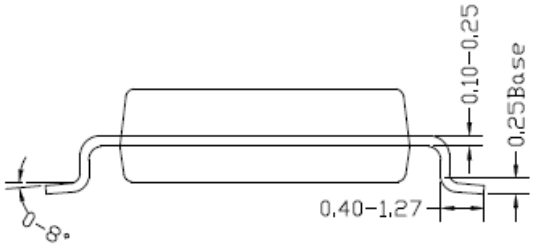


Fig.7 typical application circuit

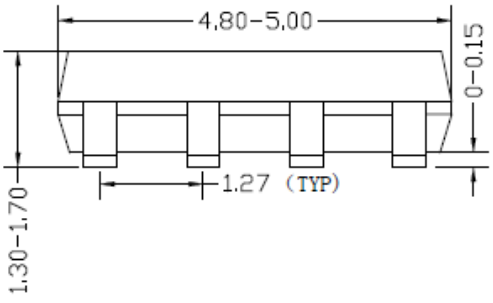
SO8E Package Outline & PCB layout



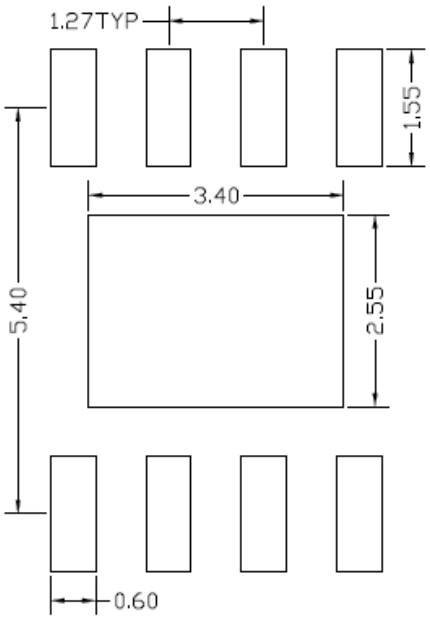
Top view



Side view



Front view



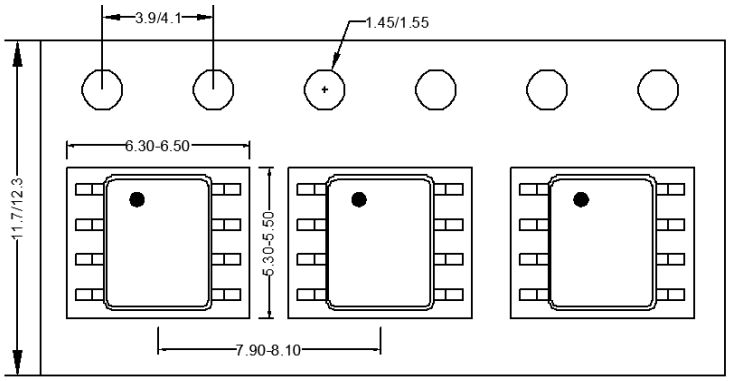
Recommended PCB Layout (Reference Only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

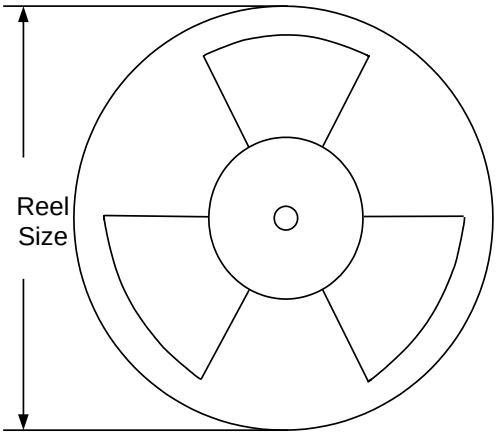
1. Taping orientation

SO8E



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
SO8E	12	8	13"	400	400	2500

Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
	Revision 0.9	Initial Release

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