SY6410

Cost-save Single Cell Li+ Battery Gauge IC

General Description

The SY6410 is a cost-save gauge IC for single cell lithium-ion (Li+) battery in handheld and portable equipments. The SY6410 senses battery terminal voltage and adopts the proprietary algorithm to calculate the corresponding state of charge (SOC).

Comparing with conventional voltage-based gauge which translates terminal voltage to SOC directly, the sophisticated algorithm in the SY6410 shows great advantage in SOC accuracy. The SY6410 can be classified as advanced voltage-based gauge which does not need current sensors and the SOC accuracy will not diverge with time. SOC and voltage information is accessed by the I²C interface. The SY6410 is available in DFN2×2-8.

Features

- ±7.5mV/Cell Voltage Measurement
- Provide Accurate State of Charge
- Temperature/Load Variation Compensation
- No Accumulated Errors
- Eliminate Current Sense Resistor
- I²C Interface
- Low SOC Alert Indicator
- Compact DFN2×2-8 Package

Applications

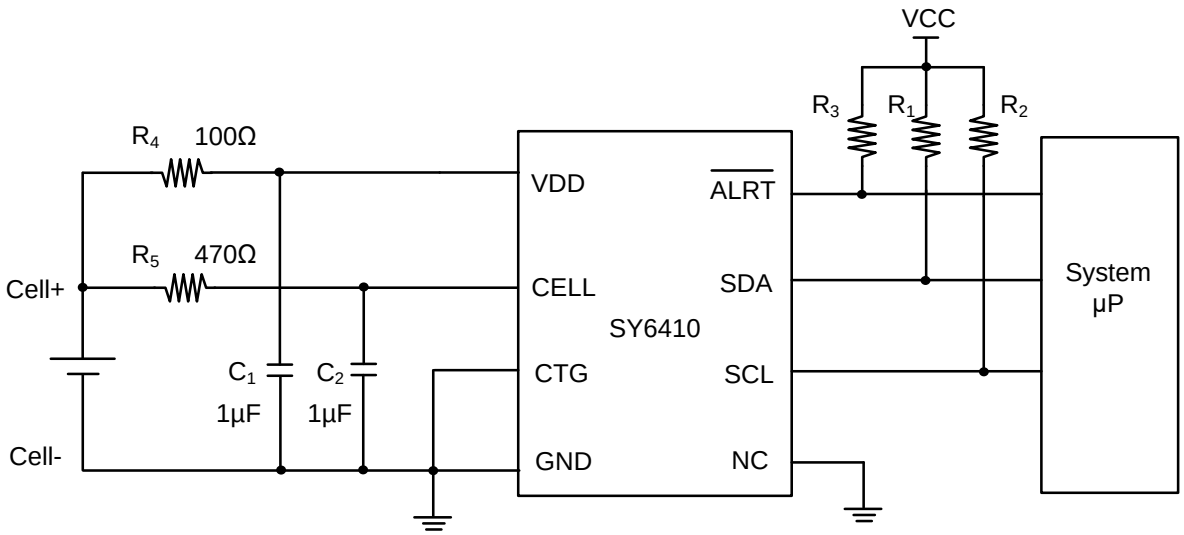
- Smart Phones/PDAs
- Portable Game Players
- Digital Still and Video Cameras
- Wireless Handsets

Ordering Information

SY6410 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY6410DFC	DFN2×2-8	

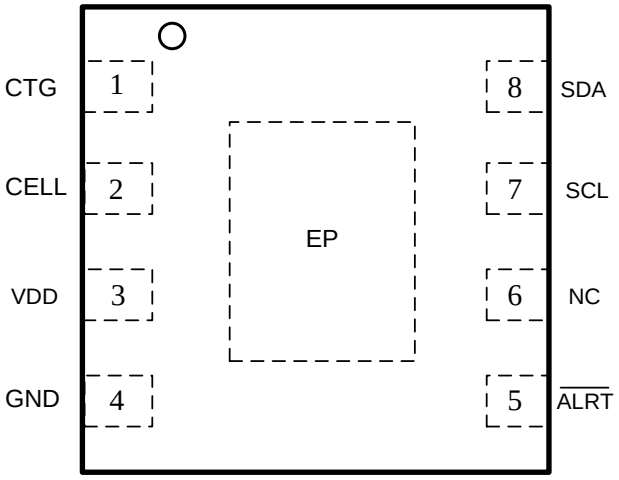
Typical Application



Note: CELL pin's resistance R_5 might not be more than 470 Ω, otherwise it will impact voltage sampling.

Fig.1 Typical Application Circuit

Pinout (top view)



Top View

(Pad Side Down)

Part Number	Package type	Top Mark①
SY6410DFC	DFN2×2-8	**Btxyz**

Note①： ***x=year code, y=week code, z= lot number code.***

Pin Name	Pin Number	Description
CTG	1	Connect to GND.
CELL	2	Battery voltage monitors I/O. Bypass with a 1μF capacitor to the GND. Connect to battery's positive terminal through R_5.
VDD	3	Power supply input. Bypass with a 1μF capacitor to GND. Connect to battery's positive terminal through R_4.
GND	4	Ground. Connect to battery's negative terminal.
$\overline{\text{ALRT}}$	5	Open-drain output. Low SOC alarm signal. When SOC is below the threshold, this pin will be pulled down.
NC	6	No connection. NC is recommended to connect to GND.
SCL	7	I^2C clock input. SCL has an internal pull-down resistance.
SDA	8	I^2C data input/output. SDA has an internal pull-down resistance.
EP	--	Exposed pad. Connected to GND.

Absolute Maximum Ratings (Note 1)

CELL, VDD, $\overline{ALRT}$, SCL, SDA to GND---------- -0.3V to 6.0V
Junction Temperature (T_J) ---------- 150°C
Storage Temperature ---------- -65°C to 150°C

Recommended Operating Conditions

VDD ---------- 2.7V to 4.5V
CELL ---------- 2.7V to 4.5V
SCL, SDA, $\overline{ALRT}$ ---------- -0.1V to 3.3V
CTG, NC ---------- Connect to GND
Operating Temperature Range ---------- -20°C to 60°C

Electrical Characteristics

(2.5V<V_{DD}<4.5V, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply						
Supply Voltage	V_{DD}		2.5		4.5	V
Under Voltage Lockout Threshold	V_{UVLO}	V_{IN} rising			2.5	V
		Hysteresis		0.3		
Input Operating Current	I_{IN}	Active mode		32	40	μA
Input Sleep Mode Current	$I_{IN(SLEEP)}$	Sleep mode		0.5	2	μA
Time Base Accuracy	t_{ERR}	V_{DD} =3.6V, T_A=25°C	-2		2	%
		-20°C<T_A<70°C(Note3)	-4		4	
ADC Sample Period		Active mode		250		ms
Voltage Error	V_{ERR}	V_{CELL}=3.75V, T_A=25°C	-7.5		7.5	mV
		-20°C<T_A<70°C(Note3)	-30		30	
Voltage Measurement Range		CELL pin	2.5		4.5	V
SDA, SCL Input Logic High	V_{IH}		1.4			V
SDA, SCL Input Logic Low	V_{IL}				0.5	V
SDA, $\overline{ALRT}$ Output Logic Low	V_{OL}	I_{OL}=4mA(Note3)			0.4	V
I^2C Interface(Note3)						
SCL Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between Stop/Start	t_{BUF}		1.3			μs
Start Condition(Repeated) Hold Time	$t_{HD, STA}$		600			ns
Repeat START Set Up Time	$t_{SU, STA}$		600			ns
Set Up Time for STOP	$t_{SU, STO}$		600			ns
Data Set Up Time	$t_{SU, DAT}$		100			ns
Data Hold Time	$t_{HD, DATI/O}$		0		900	ns
Data Output Fall Time	t_{Of}	(Note 2)	20+0.1C_B		300	ns

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: C_B is the total capacitance of one bus line in pF (C_B<=400pF).

Note 3: Guaranteed by design, not subject to test.

Timing Diagram

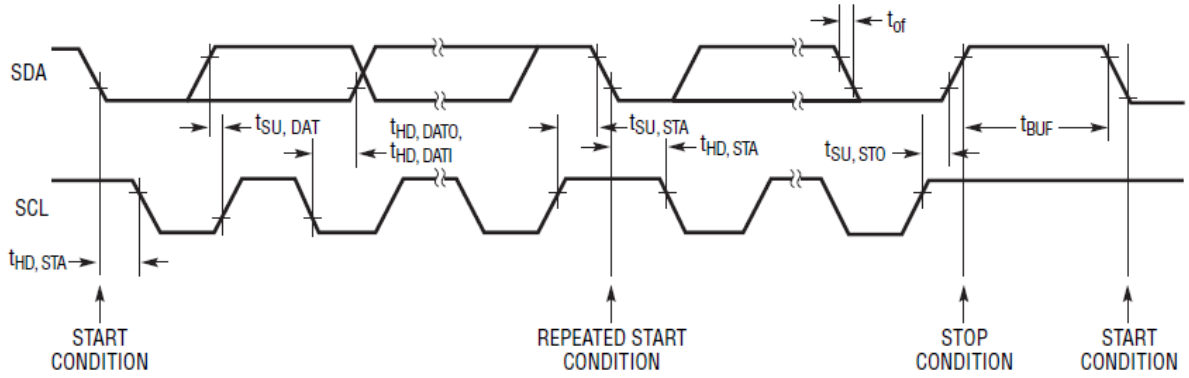


Fig.2 I²C Timing Diagram

Function Description

As the open circuit voltage (OCV) has a fixed relationship with SOC, SY6410 will calculate OCV to get the SOC. And the calculation of OCV will be based on the present and previous battery terminal voltages. To calculate OCV accurately, the battery parameters should be extracted beforehand. The extracted parameters are written into SY6410 by I²C interface. Temperature of the battery pack is measured by the host microcontroller and sent to SY6410 through the I²C interface. SY6410 can automatically compensate for battery temperature and load variation. SY6410 will take multi-samples at fixed interval and choose the maximum voltage as the OCV for the initial SOC indication at the battery insertion.

Temperature Compensation

The battery's performance is influenced by the battery's temperature. SY6410 changes parameters with the measured temperature, which can be written into SY6410 by I²C interface in order to maintain SOC accuracy.

Register Details

All the registers are read or written by I²C interface. The address of every register is shown as follow.

ADDRESS	NAME	16-BIT LSB	DESCRIPTION	READ/WRITE	DEFAULT
0x02	VBAT	(2.5/2^12)V	ADC sample value of battery.	R	—
0x04	SOC	(100/2^16)%	Battery state of charge.	R	—
0x06	MODE	—	Sleep mode enable.	W	0x0000
0x08	VERSION	—	The IC production version.	R	—
0x0C	CONFIG	—	Temperature, sleep mode, alert indicator and configuration.	R/W	0x3C1C
0x18	VRESET	—	Configure the IC reset threshold value, below which the IC will be reset.	R/W	0x0333
0x1A	STATUS	—	The indicator of charge or discharge.	R	—
0xFE	POR	—	Make SOC and STATUS registers reset.	R/W	0xFFFF

VBAT Register (0x02)

Battery voltage is measured at the CELL pin by an ADC. The battery voltage can be calculated by the following formula:

$Vcell(V) = Reg(VBAT)_{decimal} / 4096 \times 2.5V + 2.5V$

MSB (VBAT)—ADDRESS 0x02								LSB—ADDRESS 0x03							
x	x	x	x	VBAT 11	VBAT 10	VBAT 9	VBAT 8	VBAT 7	VBAT 6	VBAT 5	VBAT 4	VBAT 3	VBAT 2	VBAT 1	VBAT 0
Msb							Lsb	Msb							Lsb

Fig.3 VBAT Register Format

SOC Register (0x04)

The SOC register first updates within one second after power starts. The SOC value(%) can be calculated by the following formula:

$SOC(\%) = Reg(SOC)_{decimal} / 65535 \times 100(\%)$

MSB (SOC)—ADDRESS 0x04								LSB—ADDRESS 0x05							
SOC 15	SOC 14	SOC 13	SOC 12	SOC 11	SOC 10	SOC 9	SOC 8	SOC 7	SOC 6	SOC 5	SOC 4	SOC 3	SOC 2	SOC 1	SOC 0
Msb							Lsb	Msb							Lsb

Fig.4 SOC Register Format

MODE Register (0x06)

The system can configure the IC into sleep mode by sending command to MODE Register. The more information about sleep mode is described in **CONFIG Register**.

MSB—ADDRESS 0x06								LSB—ADDRESS 0x07							
x	x	Sleep Enable	x	x	x	x	x	x	x	x	x	x	x	x	x
Msb							Lsb	Msb							Lsb

Fig.5 MODE Register Format

VERSION Register (0x08)

This register's value is the version of the IC.

CONFIG Register (0x0C)

This register contains four parts: TEMP, SLEEP, ALERT and ALTHD.

1. Temperature configuration

TEMP is the value of battery's temperature, which can be written by I^2C interface. The temperature is used for battery's temperature compensation. In order to get enough accuracy at different temperature, it is necessary for the system to have the function to detect temperature. The default value of TEMP is 0x3C(20°C). The following formula shows how to calculate TEMP.

TEMP = INT{temperature (°C)+40}

Note: INT means to translate real number to integer by rejecting the fractional part. The operation temperature range is -20°C to 60°C.

2. Sleep mode configuration

SLEEP configures the IC in or out of sleep mode. The SLEEP bit default value is 0.

To enter sleep mode, write Sleep Enable = 1(MODE Register) and SLEEP = 1(CONFIG Register). If write or read anything through I^2C, it will get out of sleep mode and reset to work again.

3. ALERT configuration

The bit ALERT is the indicator of low SOC. This ALERT's default value is 0. ALTHD sets the SOC threshold. The value is (32-ALTHD)% (e.g. 00000b -> 32%, 11111b -> 1%).

When the SOC is lower than SOC threshold,

- The bit ALERT will be set high by the IC.
- The IC will make the pin ALRT low.

Then, write the bit ALERT= 0 to clear it,

- The bit ALERT will be set low by the IC.
- The pin ALRT will turn high again.

MSB —ADDRESS 0x0C								LSB—ADDRESS 0x0D			
TEMP 7	TEMP 6	TEMP 5	TEMP 4	TEMP 3	TEMP 2	TEMP 1	TEMP 0	SLEEP	x	ALERT	ALTHD4~ ALTHD0
Msb							Lsb	Msb			Lsb

Fig.6 CONFIG Register Format

VRESET Register (0x18)

This register defines the reset voltage. If the battery voltage (V_{CELL}) is lower than V_{RESET}, then the IC will be reset and the SOC value will be held at 0%. VRESET Register can be set by this formula:

$VRESET\_reg=(V_{RESET}(V)-2.5V)/2.5V\times4096$

MSB (VRESET)—ADDRESS 0x18								LSB—ADDRESS 0x19							
x	x	x	x	VRESET 11	VRESET 10	VRESET 9	VRESET 8	VRESET 7	VRESET 6	VRESET 5	VRESET 4	VRESET 3	VRESET 2	VRESET 1	VRESET 0
Msb							Lsb	Msb							Lsb

Fig.7 VRESET Register Format

STATUS Register (0x1A)

FLAG is the indicator of charge(FLAG=1) or discharge(FLAG=0).

MSB (STATUS)—ADDRESS 0x1A								LSB—ADDRESS 0x1B							
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	FLAG
Msb							Lsb	Msb							Lsb

Fig.8 STATUS Register Format

POR Register (0xFE)

Writing a value of 0x5400 to this register causes the IC's read only registers (e.g. SOC, STATUS register) to completely reset as if power had been removed. Then write a value of 0xFFFF to this register and the IC will work again.

Battery Parameters

All the battery parameters are read or written by I^2C interface and stored in MTP.
When program data into MTP, set VDD = 4~5.5V.
When SY6410 works normally to measure voltage and SOC, the MCU should not send command to write or read the MTP, otherwise the MCU will read SOC value by mistake. There are two ways to avoid this situation.
1. Shut down the power after writing and reading MTP. And then do not read or write the MTP any more when SY6410 is working normally.

2. After power on and then check the data in MTP, the IC will enter sleep mode by writing Sleep Enable = 1(MODE Register) and SLEEP =1(CONFIG Register) and then exit sleep mode by writing or reading anything through the I^2C. Using this method, it can exit the status of MTP's operation and then SY6410 can work normally.

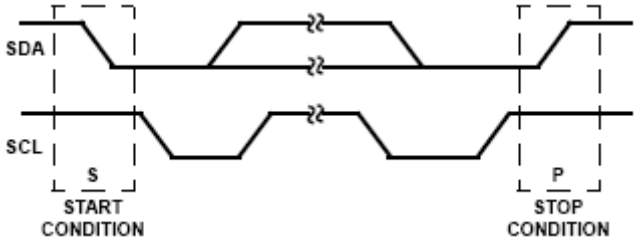
ADDRESS	16-BIT LSB	DESCRIPTION	READ/WRITE	DEFAULT
0x00 to 0x7F	—	Battery parameters	R/W	—

I²C Compatible Interface

The I²C interface supports clock at speed up to 400kHz and adopts the standard I²C commands. The SY6410 always operates as a slave device, receiving and transmitting data under the control of a master device. The master initiates all transactions on the bus and generates the SCL signal, as well as the START and STOP bits, which begin and end each transaction.

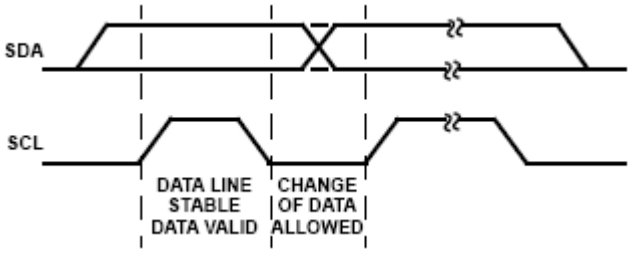
START and STOP Conditions

The SY6410 is controlled via a compatible I²C interface. The START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before the next START condition. The I²C master always generates the START and STOP conditions.



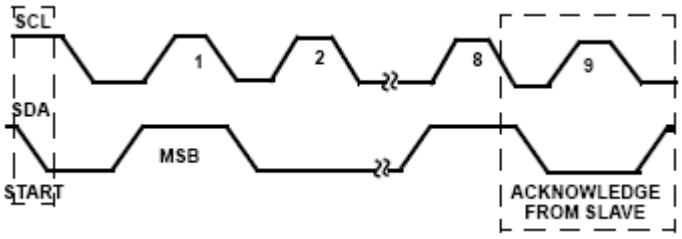
Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.



Acknowledge

Each address and data transmission uses 9-clock pulses. The ninth pulse is the acknowledge bit (ACK). After the START condition, the master sends 7-slave address bits and a $R/\overline{W}$ bit during the next 8-clock pulses. During the ninth clock pulse, the slave device which recognizes its own address holds the data line low to acknowledge. The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register address and data.

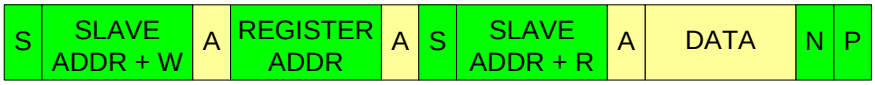


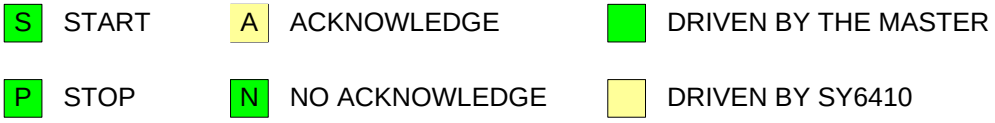
Data Transactions

All transactions start with a control byte sent from the I^2C master device. The control byte begins with a START condition, followed by 7-bits of a slave address (0110000 for the SY6410) and the read/write ($R / \overline{W}$) bit. $R / \overline{W}$ = 0 selects a write transaction with the following bytes being written by the master to the slave. $R / \overline{W}$ = 1 selects a read transaction with the following bytes being read from the slave by the master. If any slave devices on the I^2C BUS recognize their address, they will acknowledge by pulling the SDA line low for the last clock cycle in the control byte. If no slaves exist at that address or the slaves are not ready to communicate, the data line will be 1, indicating a Not Acknowledge condition. Once the control byte is sent, and the SY6410 acknowledges it, the 2nd byte sent by the master must be a register address byte. The register address byte tells the SY6410 which register to be written or read by the master. Once the SY6410 receives a register address byte it will respond with an ACKNOWLEDGE.

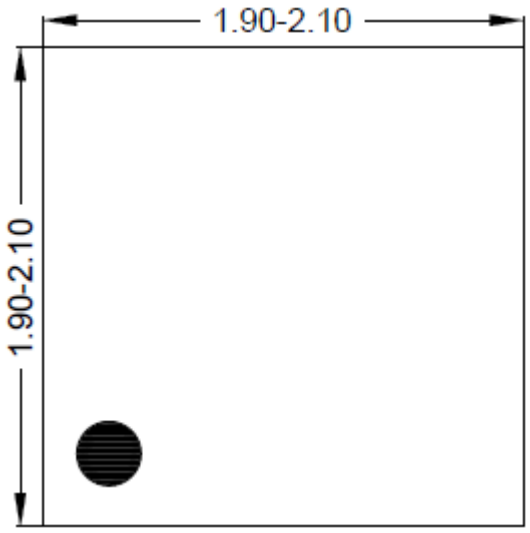
Write To A Register

Read From A Register

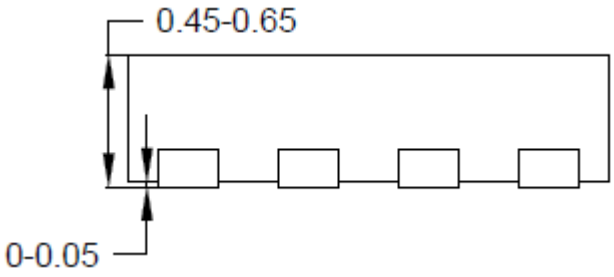




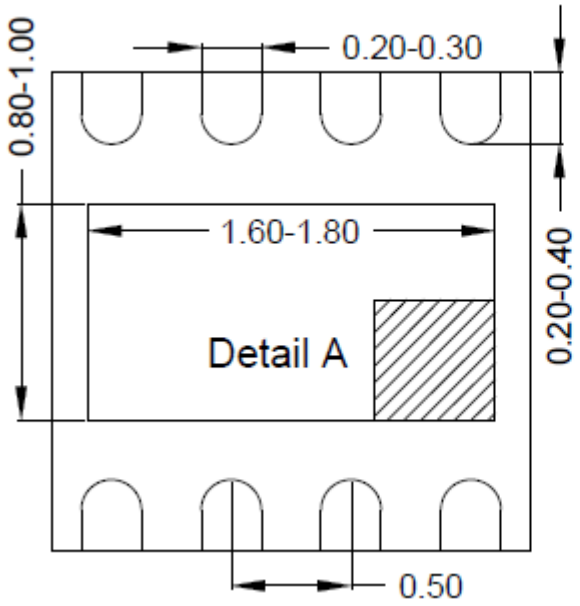
DFN2×2-8 Package Outline

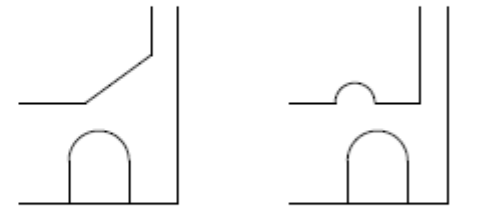


Top View



Side View

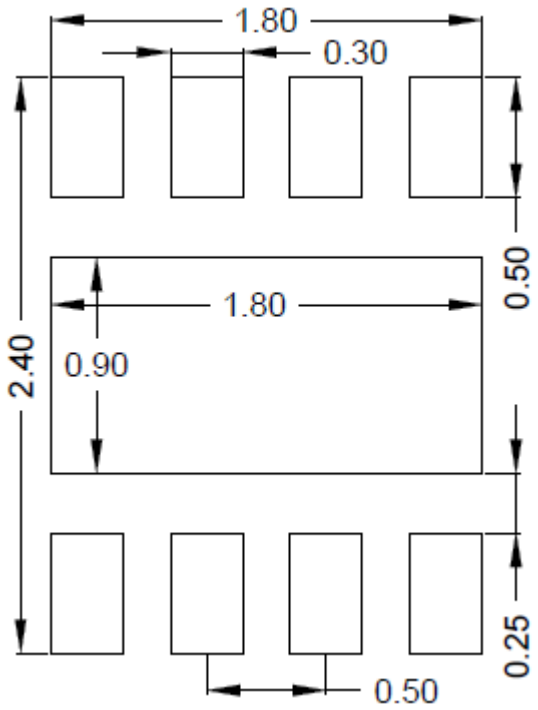




Detail A

Pin1 Identifier(Two options)

Bottom View

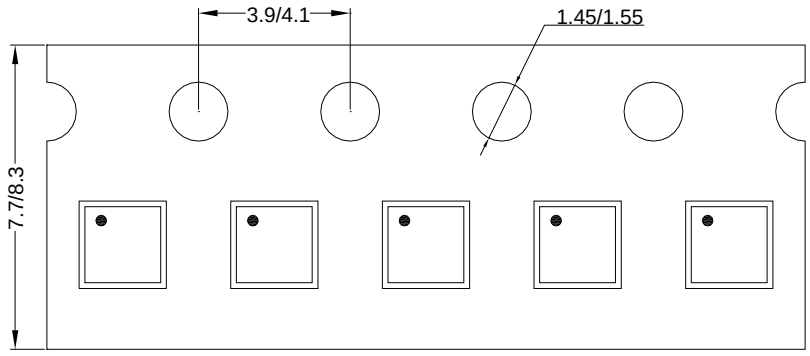


Recommended PCB Layout
(Reference Only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

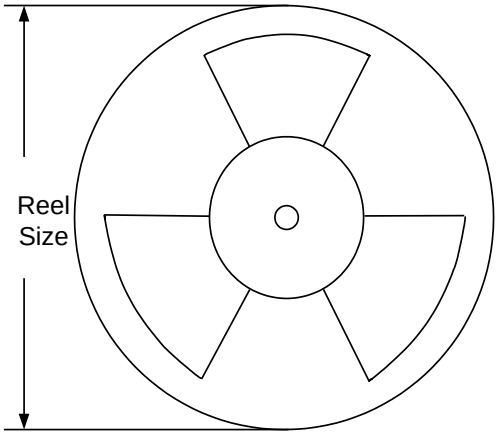
Taping & Reel Specification

1. DFN2×2-8 Taping orientation



Feeding direction

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
DFN2×2	8	4	7"	400	160	3000

3. Others: NA

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