SY20744

2A Switching Charger with Low Iq Power Path Management, OTG and LDO

General Description

The SY20744 is a fully-integrated switching battery charger with system power path management for single cell Li-Ion and Li-polymer battery in a wide range of TWS and other portable devices. Its low impedance power path optimizes switching conversion efficiency, reduces battery charging time and extends battery life during the discharging mode. The I^2C serial interface with charging and system settings makes the device a truly flexible solution.

The power path management regulates the system voltage slightly above battery voltage but does not drop below 3.5V minimum system voltage (programmable). With this feature, the switching converter keeps working to support the system load even when the battery is completely depleted or removed. When the input current limit or voltage limit is reached, the power path management reduces the charging current to zero firstly. If the system load continues to increase, the power path discharges the battery to provide the power required by system. This supplement mode operation prevents overloading the input source.

The device initiates and completes a charging cycle without software control. It automatically detects the battery voltage and charges the battery in three phases: preconditioning, constant current and constant voltage. At the end of the charging cycle, the charger automatically terminates when the charge current is below a preset limit in the constant voltage phase. When the full battery falls below the recharge threshold, the charger will automatically start another charging cycle. SY20744 can be compliant with JEITA spec for the 4.2V Li-Ion battery.

The SY20744 meets USB On-the-Go operation power rating specification by supplying 5.1V(programmable) on BUS with current limit up to 1.2A(programmable).

The device also integrates 2 channel independent switches to supply 5V(programmable) to portable device with current limit up to 200mA each in LDO mode and 350mA each in full on mode.

The device provides various safety features for battery charging and system operation, including negative thermistor monitoring, charging safety timer and over-voltage / over-current protections. The thermal regulation reduces charge current when the junction temperature exceeds 110°C (programmable).

The CHRG_STAT reports the charging status and fault conditions. The PG_STAT bit in SY20744 indicates if a good power source is present. The INT immediately notifies the host when a fault occurs.

The SY20744 is available in CSP 2.2×2.565-30 package.

Ordering Information

SY20744 □(□□□)

- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY20744VKS	CSP 2.2×2.565-30	

Features

- Extremely Low Battery Leakage Current and Support Shipping Mode
- High Efficiency 2A Buck Mode Charger
  - Support 3.8V-14V Input Voltage range
  - Programmable IDPM/VDPM to support the USB and adapter
  - 4.0V-4.5V Adjustable Charge Voltage
  - Support NVDC Power Path Management
  - JEITA Compliance
- Maximum 1.2A OTG Output Current
  - 4.5V-5.5V Adjustable Output Voltage
  - Selectable OTG Output Current Limit
- Maximum 350mA on BOOST1 and BOOST2 Channel
  - 1.6V-6.0V Adjustable Output Voltage
  - Maxmium 200mA Current Limit in LDO Mode
  - Maxmium 350mA Current Limit in Full On Mode

- Full BATFET Control to Support Shipping Mode, Wake Up, and System Reset
- Up to 8A Battery Discharge Current
- Safety
  - Battery Temperature Sensing for Charge and Boost Mode
  - Battery Charging Safety Timer
  - Thermal Regulation and Thermal Shutdown
  - Input/System Over-Voltage Protection
  - MOSFET Over-Current Protection

Applications

- Earphone Charging Case
- Wearable accessories
- Single Cell Li-Ion Portable Device

Typical Application

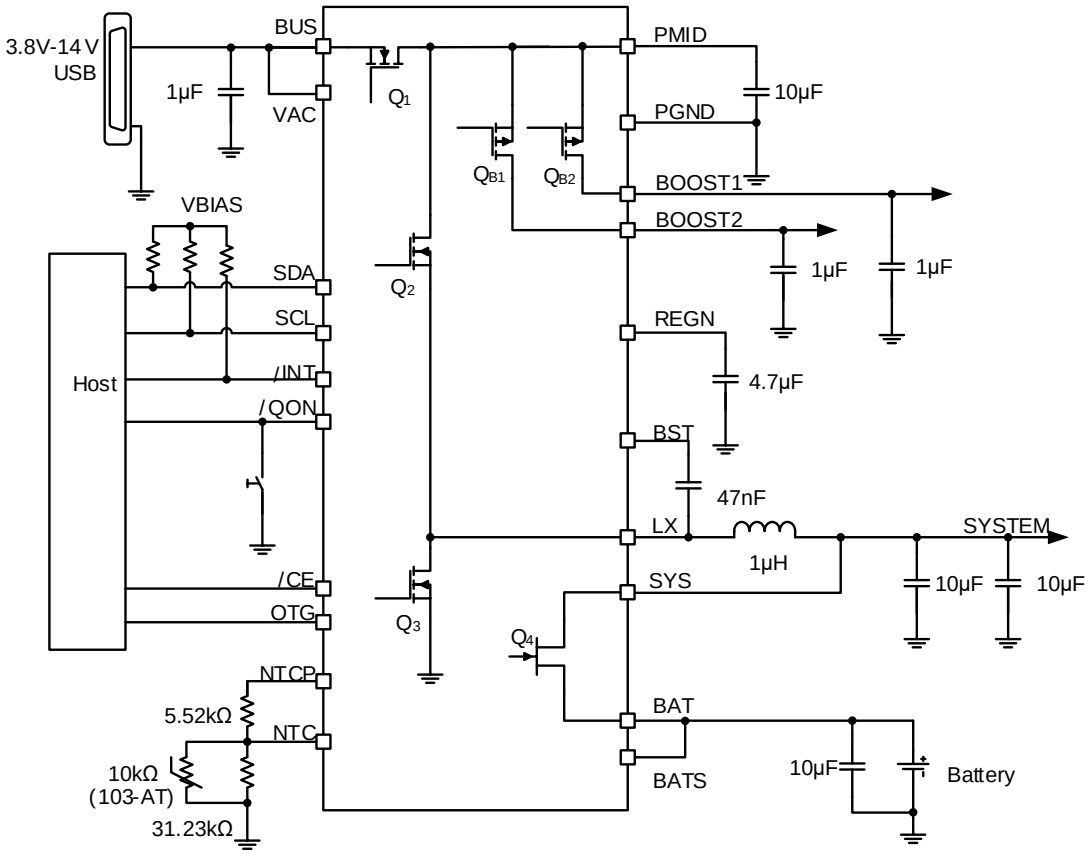
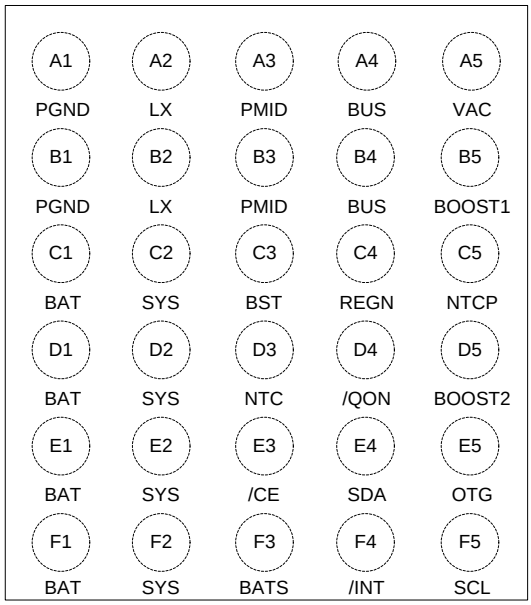


Figure 1. Schematic Diagram

Pinout (top view)



(CSP 2.2×2.565-30)

Top Mark: Y7*xyz*(device code: **Y7**, ***x=year code, y=week code, z= lot number code)***

Pin Name	Pin Number	Pin Description
PGND	A1,B1	Power ground connection for high-current power converter node. Internally, PGND is connected to the source of the n-channel LSFET. On PCB layout, connect directly to ground connection of input and output capacitors of the charger. A single point connection is recommended between power PGND and the analog GND near the IC PGND pin.
LX	A2,B2	Switching node connecting to output inductor. Internally LX is connected to the source of the n-channel HSFET and the drain of the n-channel LSFET. Connect the 0.047μF bootstrap capacitor from LX to BST.
PMID	A3,B3	Connected to the drain of the reverse blocking MOSFET and the drain of HSFET. Place at least a 10μF ceramic capacitor from PMID to PGND and place it as close as possible to IC.
BUS	A4,B4	Charge power input pin. The internal n-channel reverse block MOSFET (RBFET) is connected between BUS and PMID with BUS on source. Place a 1μF ceramic capacitor from BUS to PGND and place it as close as possible to IC.
VAC	A5	Charge input voltage sense. This pin must be connected close to BUS pin.
BOOST1	B5	Linear MOSFET (LNFET) output port 1.
BAT	C1,D1,E1,F1	Battery connection point to the positive terminal of the battery pack. The internal BATFET is connected between BAT and SYS. Connect a 10μF ceramic capacitor closely to the BAT pin.
SYS	C2,D2,E2,F2	System connection point. The internal BATFET is connected between BAT and SYS. When the battery falls below the minimum system voltage, switch mode converter keeps SYS above the minimum system voltage.

BST	C3	PWM high side driver positive supply. Internally, the BST is connected to the cathode of the bootstrap diode. Connect the 0.047μF bootstrap capacitor from LX to BST.
REGN	C4	PWM low side driver positive supply output. Internally, REGN is connected to the anode of the bootstrap diode. Connect a 4.7μF (10V rating) ceramic capacitor from REGN to analog GND. The capacitor should be placed close to the IC.
NTCP	C5	NTCP serves as bias rail of NTC pin.
NTC	D3	Temperature qualification voltage input. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from NTCP to NTC to PGND. Charge suspends when NTC pin is out of range. Recommend 103AT-2 thermistor. This thermal protection function can be disabled by BHOT bit.
/QON	D4	BATFET enable control in shipping mode and BATFET reset function. When BATFET is in shipping mode, logic high to low transition on this pin with minimum of T_{QON_LOW}(typical 50ms/2s, programmable) low level turns on BATFET to exit shipping mode. This pin is internally pulled up to default high logic. When the input source is not plugged in (or plugged in but in HIZ mode) and BATFET is in on state, a logic high to low of T_{QON_RST}(typical 4s to 20s, programmable) resets SYS (system power) by turn BATFET off with 30mA pull-down current for T_{BATFET_RST}(typical 2s/4s, programmable) and then re-enable BATFET. The device will enter default mode when SYS is reset by /QON.
BOOST2	D5	Linear MOSFET (LNFET) output port 2.
/CE	E3	Active low Charge Enable pin. Battery charging is enabled when REG01[4]=1 and /CE pin =Low. /CE pin must be pulled high or low.
SDA	E4	I^2C Interface data. Connect SDA to the logic rail through a 10k resistor.
OTG	E5	Active high enable pin during Boost mode. The Boost mode is activated when the OTG_CONFIG=1 or OTG pin is High. BLKFET can be controlled independently by Q1_EN bit when OTG_CONFIG=1.
BATS	F3	Battery voltage sensing pin for charge voltage regulation. BATSNS_STAT =0 indicates the charger regulates through BATS pin, BATSNS_STAT =1 indicates the charger regulates through BAT pin.
/INT	F4	Open-drain interrupt output. The /INT pin sends active low, 256us pulse to host to report charger device status and fault.
SCL	F5	I^2C Interface clock. Connect SCL to the logic rail through a 10k resistor.

Block Diagram

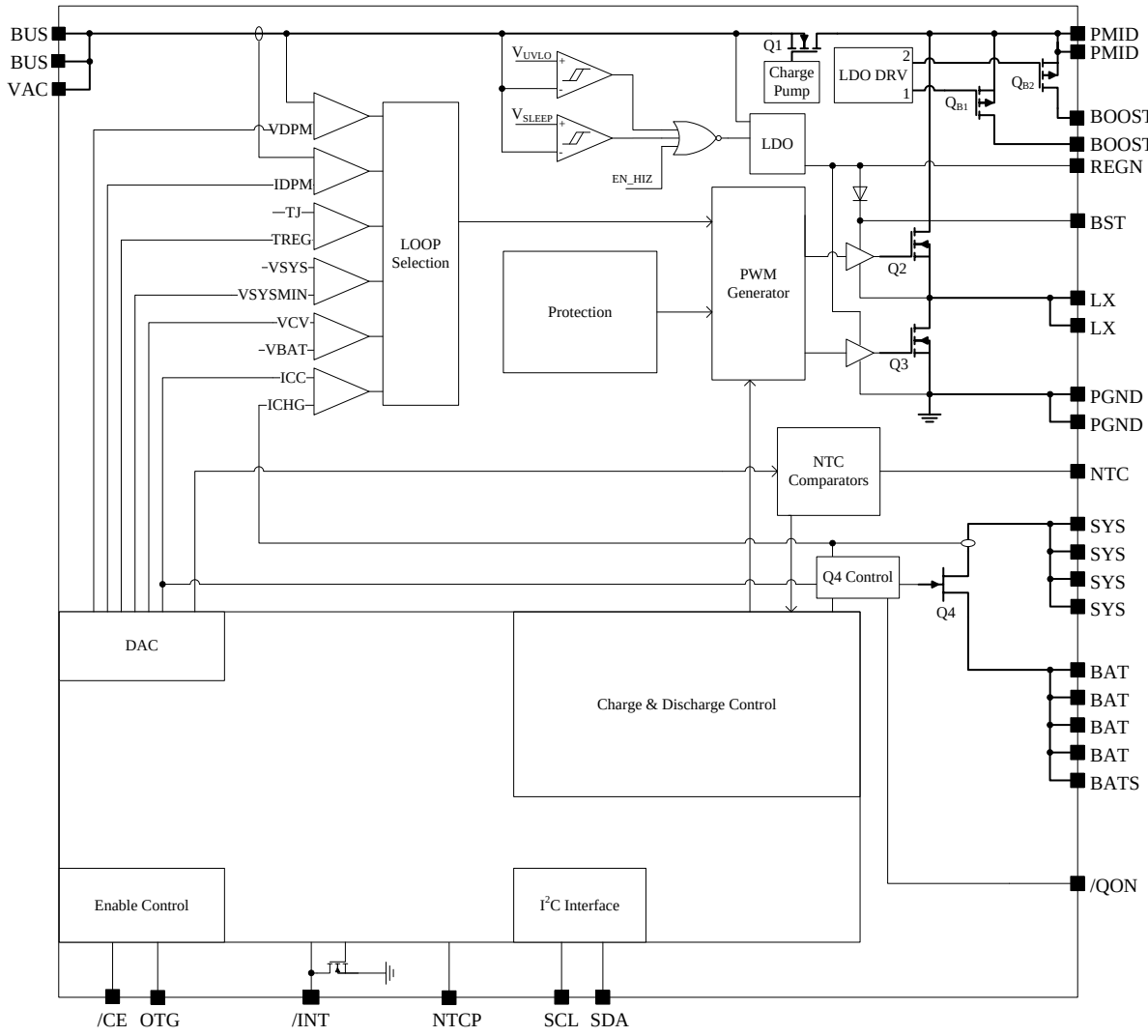


Figure 2. Block Diagram

Absolute Maximum Ratings (Note 1)

BUS, VAC, PMID, LX---------- -0.3V to +18V
BAT, BATS, SYS, NTC, BST-LX, REGN, NTCP, OTG, /QON, /CE, /INT, SDA, SCL, BOOST1, BOOST2 ---- -0.3V to +6.0V

Package Thermal Resistance (Notes 2)
CSP2.2×2.565-30 θ_{JA} ---------- 55°C/W
CSP2.2×2.565-30 θ_{JC} ---------- 1.6°C/W
Junction Temperature Range ---------- -40°C to +150°C
Storage Temperature ---------- -65°C to +150°C

ESD Susceptibility
HBM (Human Body Mode) ---------- 2kV
CDM (Charged Device Mode) ---------- 500V

Recommended Operating Conditions (Note 3)

BUS, VAC, PMID, LX---------- 0V to +16V
BAT, BATS, SYS, NTC, BST-LX, REGN, NTCP, OTG, /QON, /CE, /INT, SDA, SCL, BOOST1, BOOST2 ------- 0V to +5.5V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Note 1: Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective four layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(V_{BUS_UVLOZ}<V_{BUS}<V_{ACOV} and V_{BUS}>V_{BAT}+V_{SLEEPZ}, T_A=25℃ for typical values unless other noted.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
QUIESCENT CURRENTS						
Battery discharge current (BAT)	I_{BAT}	V_{BUS}<V_{BUS_UVLOZ}, V_{BAT}=4.5 V, leakage between BAT and BUS			1	μA
		V_{BAT}=4.5V,High-Z Mode, no BUS, BATFET disabled		3	5	μA
		V_{BAT}=4.5V,High-Z Mode, no BUS, BATFET enabled		10	15	μA
Input supply current in High-Z mode	I_{BUS_HIZ}	V_{BUS}=5V, battery monitor disabled, no battery, High-Z mode enabled		15	30	μA
		V_{BUS}=12V, battery monitor disabled, no battery, High-Z mode enabled		20	35	μA
Input supply current (BUS)	I_{BUS}	V_{BUS}>V_{BUS_UVLOZ}, V_{BUS}>V_{BAT}, converter not switching		1.5	3	mA
		V_{BUS}> V_{BUS_UVLOZ}, V_{BUS}>V_{BAT}, converter switching, V_{BAT}=3.2V, I_{SYS}=0A		1.6		mA
		V_{BUS}> V_{BUS_UVLOZ}, V_{BUS}>V_{BAT}, converter switching, charge disabled, V_{BAT}=3.8V, I_{SYS}=0A		1.6		mA
Battery discharge Current in Boost mode	$I_{OTGBOOST}$	V_{BAT}=4.2V, Boost mode, no load, converter switching, LNFET Q_{B1} and Q_{B2} on, Q1 off		37	60	μA
BUS/BAT POWER UP						
BUS operating range	V_{BUS_OP}		3.8		14	V
BUS for active IC and I²C, no battery	V_{BUS_UVLOZ}	Rising value to active I²C	3.0	3.2	3.4	V
		Falling hysteresis value		130		mV
Sleep mode falling threshold	V_{SLEEP}	V_{BUS} falling, V_{BUS}-V_{BAT}	50	100	150	mV
Sleep mode rising threshold	V_{SLEEPZ}	V_{BUS} rising, V_{BUS}-V_{BAT}	200	270	350	mV
BUS over-voltage rising threshold	V_{ACOV}	V_{BUS} rising, OVP(reg07[7:6]=00)	6.2	6.4	6.6	V
		V_{BUS} rising, OVP(reg07[7:6]=01)	8.5	8.7	8.9	V
		V_{BUS} rising, OVP(reg07[7:6]=10)	10.5	10.7	10.9	V
		V_{BUS} rising, OVP(reg07[7:6]=11)	13.8	14.1	14.4	V
BUS over-voltage recovery hysteresis	V_{ACOV_HYS}	V_{BUS} falling		100		mV
Battery for active I²C, no BUS	V_{BAT_UVLOZ}	V_{BAT} rising	2.3			V
Battery depletion threshold	V_{BAT_DPL}	V_{BAT} falling	2.3	2.4	2.5	V

Battery depletion recovery threshold	V_{BAT_DPLZ}	V_{BAT} rising hysteresis		300		mV
Bad adapter detection threshold	V_{BUSMIN}	V_{BUS} falling	3.4	3.5	3.6	V
Bad adapter detection hysteresis	V_{BUSMIN_HYST}	V_{BUS} rising		70		mV
Bad adapter detection current source	I_{BADSRC}			20		mA
Bad source detection duration	t_{BADSRC}			30		ms
POWER PATH MANAGEMENT						
System regulation voltage	V_{SYS_MAX}	I_{SYS} = 0A, V_{BAT}>V_{SYS_MIN}=3.5V, Q4 off, V_{BAT} up to 4.5V, V_{SYS}=V_{BAT}+50mV	4.54	4.57	4.6	V
System voltage output	V_{SYS_MIN}	I_{SYS}=0A, V_{BAT}<V_{SYS_MIN}=3.5V, Q4 off, V_{SYS}=V_{BAT}+150mV	3.6	3.65	3.7	V
Internal high-side reverse blocking MOSFET on-resistance	$R_{ON(RBFET)}$			30		mΩ
Internal high-side switching MOSFET on-resistance between PMID and LX	$R_{ON(HSFET)}$			45		mΩ
Internal low-side switching MOSFET on-resistance between LX and PGND	$R_{ON(LSFET)}$			50		mΩ
Internal LDO MOSFET on-resistance between PMID and BOOST1	$R_{ON(LNFET)}$			500		mΩ
Internal LDO MOSFET on-resistance between PMID and BOOST2	$R_{ON(LNFET)}$			500		mΩ
BATFET forward voltage in supplement mode	V_{FWD}	BAT discharge current 10mA		30		mV
BATTERY CHARGER						
Charge voltage regulation accuracy	$V_{BAT\_REG\_ACC}$	V_{BAT_REG} = 4.2V and 4.4V, T_A = 25°C	-0.3%		0.3%	
Fast charge current regulation accuracy	$I_{ICHG\_REG\_ACC}$	SYS_MIN=3.5V, V_{BAT} = 3.8V or V_{BAT} = 3.1V, I_{CHG} = 1.536A or 528mA	-5%		5%	
		SYS_MIN=3.5V, V_{BAT} = 3.8V or V_{BAT} = 3.1V, I_{CHG} = 512mA or 64mA	-8%		8%	
		SYS_MIN=3.5V, V_{BAT} = 3.8V or V_{BAT} = 3.1V, I_{CHG} = 16mA	-4		4	mA
Battery LOWV falling threshold	$V_{BATLOWV}$	Fast charge to precharge, V_{BAT} falling	2.7	2.8	2.9	V
Battery LOWV rising threshold	$V_{BATLOWV\_HYST}$	Precharge to fast charge, V_{BAT} rising	2.9	3.0	3.1	V

Precharge current regulation accuracy	I_{PRECHG_ACC}	V_{BAT}=2.5V, I_{PRECHG} = 512mA or 64mA	-15%		15%	
		V_{BAT}=2.5V, I_{PRECHG} = 40mA or 8mA	-6		6	mA
Termination current accuracy	I_{TERM_ACC}	I_{TERM} = 64mA or 256mA	-10%		10%	
		I_{TERM} = 8mA or 16mA	-5		5	mA
Battery Short Voltage	V_{SHORT}	V_{BAT} falling	1.9	2.0	2.1	V
Battery Short Voltage hysteresis	V_{SHORT_HYST}	V_{BAT} rising		200		mV
Battery short current	I_{SHORT_ACC}	I_{SHORT} = 80mA	-15%		15%	
		I_{SHORT} = 10mA	-7		7	mA
Recharge threshold below V_{BAT_REG}	V_{RECHG}	V_{BAT} falling, REG05[0] = 0	70	100	130	mV
		V_{BAT} falling, REG05[0] = 1	160	200	240	mV
SYS-BAT MOSFET on-resistance	R_{ON_BATFET}			15		mΩ
INPUT VOLTAGE/CURRENT REGULATION						
Absolute input voltage regulation accuracy	$V_{INDPM\_REG\_ACC}$	set Absolute VINDPM=4.8V	-1.5%		1.5%	
Relative input voltage regulation tracking VBAT accuracy	$V_{DPM\_BAT\_ACC}$	set VDPM=VBAT+250mV, V_{BAT}=4.2V	-2%		2%	
Input current limit range	I_{INDPM_RANGE}		100		2400	mA
USB Input current regulation limit, V_{BUS}=5V, current drawn from LX	I_{USB_DPM}	USB100	80	96	110	mA
		USB500	440	475	500	mA
Input current regulation accuracy	I_{ADPT_DPM}	I^2C Set input current limit above 500mA	-14%	-7%	0%	
BAT OVER-VOLTAGE PROTECTION						
Battery over-voltage threshold	V_{BATOVP}	V_{BAT} rising, as percentage of V_{BAT_REG}	103%	104%	105%	
Battery over-voltage hysteresis	V_{BATOVP_HYST}	V_{BAT} falling, as percentage of V_{BAT_REG}		2%		
BAT DISCHARGE OVER-CURRENT PROTECTION						
BATFET discharge over-current threshold	I_{BATFET_OCP}		8	10	11	A
THERMAL REGULATION AND THERMAL SHUTDOWN						
Junction temperature regulation accuracy	$T_{Junction\_REG}$	TREG bit=1		110		℃
Thermal shutdown rising temperature	T_{TSD}	Temperature increasing		160		℃
Thermal shutdown hysteresis	T_{TSD_HYS}			30		℃
JEITA THERMISTER COMPARATOR						
T1(0℃) threshold, charge suspended below this temp	V_{T1}	V_{NTC} rising, as percentage to V_{NTCP}, JEITA_ISET=0	72.5	73.25	74	%

Charge back to I_{CHG}/2 and V_{REG} above this temp	V_{T1_HYS}	Hysteresis, V_{NTC} falling, JEITA_ISET=0		1.25		%
T2(10℃) threshold, charge back to I_{CHG}/2 and V_{REG} below this temp	V_{T2}	V_{NTC} rising, as percentage to V_{NTCP}, JEITA_ISET=0	67.5	68.25	69	%
Charge back to I_{CHG} and V_{REG} above this temp	V_{T2_HYS}	Hysteresis, V_{NTC} falling, JEITA_ISET=0		1.25		%
T3(45℃) threshold, charge back to I_{CHG} and V_{REG}-100mV above this temp	V_{T3}	V_{NTC} falling, as percentage to V_{NTCP}, JEITA_VSET=0	44.25	44.75	45.25	%
Charge back to I_{CHG} and V_{REG} below this temp	V_{T3_HYS}	Hysteresis, V_{NTC} rising, JEITA_VSET=0		1.2		%
T5(60℃) threshold, charge suspended above this temp	V_{T5}	V_{NTC} falling, as percentage to V_{NTCP}, JEITA_VSET=0	33.875	34.375	34.875	%
Charge back to I_{CHG} and V_{REG}-100mV below this temp	V_{T5_HYS}	Hysteresis, V_{NTC} rising, JEITA_VSET=0		1.2		%
BOOST MODE THERMISTER COMPARATOR						
Cold Temperature Threshold 0, NTC pin Voltage Rising Threshold	V_{BCOLD0}	As Percentage to V_{NTCP} (Approx. -10℃ w/ 103AT)	76.25	77	77.75	%
Falling Hysteresis	V_{BCOLD0_HYS}	(Approx. 1℃ w/ 103AT)		1.25		%
Cold Temperature Threshold 1, NTC pin Voltage Rising Threshold	V_{BCOLD1}	As Percentage to V_{NTCP} (Approx. -20℃ w/ 103AT)	79.25	80	80.75	%
Falling Hysteresis	V_{BCOLD1_HYS}	(Approx. 1℃ w/ 103AT)		1.25		%
Hot Temperature Threshold 0, NTC pin Voltage Falling Threshold	V_{BHOT0}	As Percentage to V_{NTCP} (Approx. 55℃ w/ 103AT)	37.25	37.75	38.25	%
Rising Hysteresis	V_{BHOT0_HYS}	(Approx. 3℃ w/ 103AT)		3		%
Hot Temperature Threshold 1, NTC pin Voltage Falling Threshold	V_{BHOT1}	As Percentage to V_{NTCP} (Approx. 60℃ w/ 103AT)	33.875	34.375	34.875	%
Rising Hysteresis	V_{BHOT1_HYS}	(Approx. 3℃ w/ 103AT)		3		%
Hot Temperature Threshold 2, NTC pin Voltage Falling Threshold	V_{BHOT2}	As Percentage to V_{NTCP} (Approx. 65℃ w/ 103AT)	30.75	31.25	31.75	%
Rising Hysteresis	V_{BHOT2_HYS}	(Approx. 3℃ w/ 103AT)		3		%
BUCK MODE OPERATIONS						
HSFET cycle-by-cycle current limit	I_{HSFET_OCP}			6		A
PWM Switching frequency	F_{SW}			1500		kHz
BOOST MODE OPERATIONS						
PWM Switching frequency	F_{SW_BOOST}	V_{BAT}=3.2V, V_{BUS}=5V, I_{BUS}=1A		1500		kHz
OTG PMID output voltage range	V_{OTG_REG}		4.5		5.5	V
OTG PMID output voltage	$V_{OTG\_REG\_ACC}$	I_{BUS}=0A	-1.2%		1.2%	

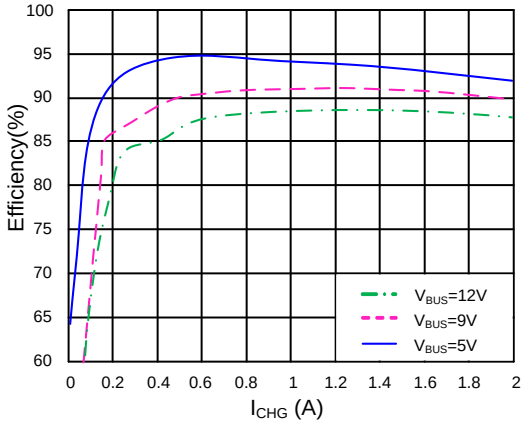
accuracy						
Battery voltage exiting Boost mode	V_{OTG_BAT}	REG01[0]) = 0, V_{BAT} falling	2.7	2.8	2.9	V
Battery voltage entering Boost mode	$V_{OTG\_BAT\_HYST}$	REG01[0]) = 0, V_{BAT} rising		3.0		V
Battery voltage exiting Boost mode	V_{OTG_BAT}	REG01[0]) = 1, V_{BAT} falling	2.5	2.6	2.7	V
Battery voltage entering Boost mode	$V_{OTG\_BAT\_HYST}$	REG01[0]) = 1, V_{BAT} rising		2.8		V
Boost mode output over-current Limit in OCP mode	I_{OTG_OCP}	BOOST_LIM=0.5A or 1.2A	120%	135%	155%	I_{OTG}
HSFET cycle-by-cycle valley current limit in Boost mode	I_{OTG_ILIM}			7		A
OTG over-voltage threshold	V_{OTG_OVP}	V_{BUS} rising edge	5.7	5.85	6.0	V
OTG over-voltage threshold Hysteresis	$V_{OTG\_OVP\_HYS}$	V_{BUS} falling edge		120		mV
LNFETs LDO						
LDO output voltage range	V_{LDO_REG}		1.6		6.0	V
LDO output voltage accuracy	$V_{LDO\_REG\_ACC}$	V_{LDO}=5.0V	-0.5%		0.5%	
LDO output CC- current limit	I_{LDO_REG}	I_{LDO}=200mA or 100mA, V_{LDO}=5V, LDO_MODE=1	100%		120%	
LDO output OCP threshold in full on mode	I_{LDO_OCP}	LDO_MODE=0	350	400	440	mA
LDO output short protection threshold	V_{LDO_SC}	V_{LDO} Falling edge	0.6	0.8	1	V
		V_{LDO} Rising edge		200		mV
REGN LDO						
REGN LDO output voltage	V_{REGN}	V_{BUS} = 10V, I_{REGN} = 40mA		5		V
		V_{BUS} = 5V, I_{REGN} = 20mA		4.8		V
REGN LDO current limit	I_{REGN}	V_{BUS} = 5V, V_{REGN} = 3.8V	50	70		mA
/QON TIMING						
/QON low time to turn on BATFET and exit ship mode	T_{QON_LOW}	T_{QON_LOW}= 2s	1.5	2	2.35	s
/QON low time accuracy to reset BATFET	$T_{QON\_RST\_ACC}$	T_{QON_RST}= 4s	2.6	3.4	4	s
		T_{QON_RST}= 20s	14	18	21	s
Reset duration(BATFET off time)	T_{BATFET_RST}	T_{BATFET_RST}= 2s	1.2	1.7	2.2	s
		T_{BATFET_RST}= 4s	2.6	3.5	4.3	
Enter ship mode delay	T_{SM_DLY}	BATFET_DIS set at BATFET_DLY=1 and TSM_DLY=11, 10s	6.5	9	11	s
LOGIC I/O PIN CHARACTERISTICS (/CE, /QON, DSEL)						
Input low threshold	V_{ILOW}				0.4	V
Input high threshold	V_{IHGH}		1.3			V

Output low saturation voltage	V_{OUT_LOW}	Sink current = 5mA			0.4	V
High level leakage current (OTG, /CE, /INT)	I_{BIASLK}	Pull up rail 1.8V or 3.3V			1	μA
Internal /QON pull up	R_{QON}		90	150	200	kΩ
I²C INTERFACE (SDA, SCL, /INT)						
Input high threshold level	V_{IH}	$V_{PULL-UP}$ = 1.8V, SDA and SCL	1.3			V
Input low threshold level	V_{IL}	$V_{PULL-UP}$ = 1.8V, SDA and SCL			0.4	V
Output low threshold level	V_{OL}	Sink current = 5mA			0.4	V
SCL clock frequency	f_{SCL}				400	kHz
DIGITAL CLOCK AND WATCHDOG TIMER						
WATCHDOG=11	t_{WDT}	REGN LDO disabled	110	160	180	s
		REGN LDO enabled	140	160	180	s

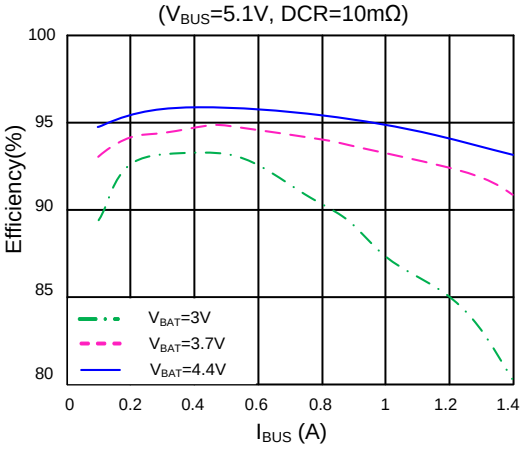
Typical Performance Characteristics

T_A=25°C, V_{BUS}=5V, 1cell battery, unless otherwise specified.

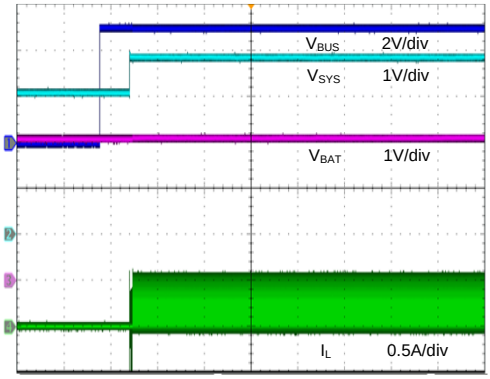
Efficiency vs. Charge Current (CC Mode)
(V_{BAT}=3.8V,DCR=10mΩ)



Efficiency vs. I_{BUS} (Boost Mode)
(V_{BUS}=5.1V, DCR=10mΩ)

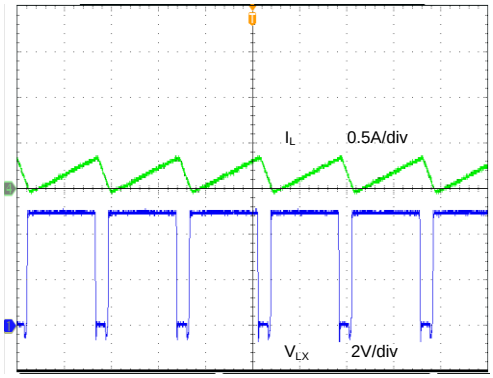


Adapter Plug-in in Default Mode
(V_{BAT}=3.1V)



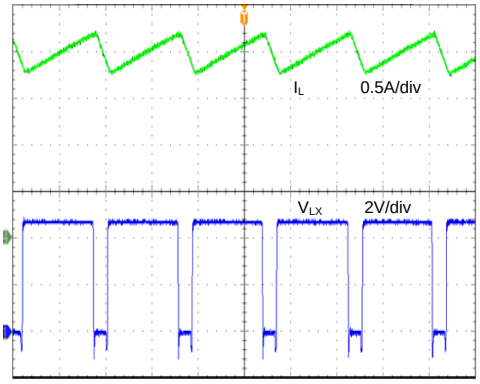
Time (400ms/div)

CV Mode Steady State
(V_{BAT}=4.2V)



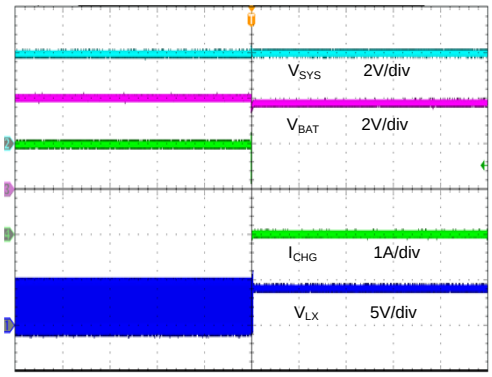
Time (400ns/div)

CC Mode Steady State
(V_{BAT}=3.7V)



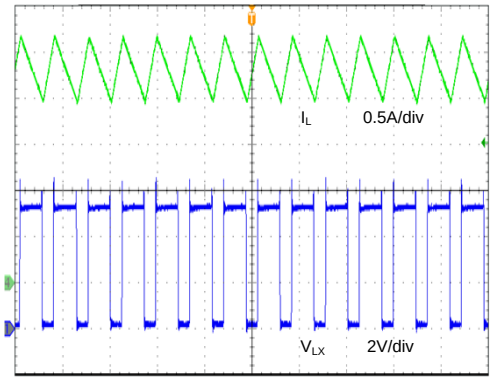
Time (400ns/div)

Charge Enable to Disable



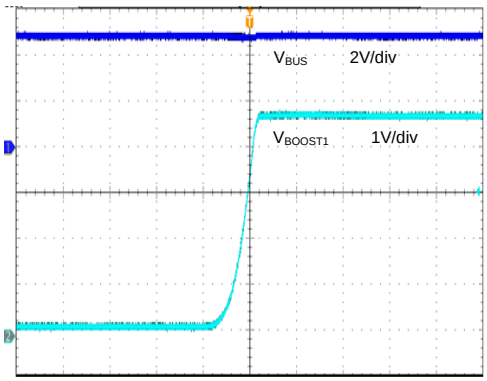
Time (2ms/div)

Boost Mode Steady State
(I_{BUS}=1.5A)



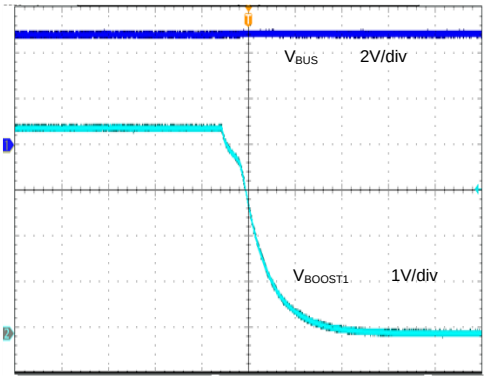
Time (1μs/div)

BOOST1 Turn On in Buck Mode



Time (40μs/div)

BOOST1 Turn Off in Buck Mode



Time (40μs/div)

I²C Registers

Address: 6BH

REG00

BIT	Name	POR	Reset by REG_RST	Reset by Watchdog	DESCRIPTION
7	EN_HIZ	0	Y	N	**Enable HIZ Mode:** 0–Disable, 1–Enable
6	LDO_MODE1	1	Y	N	**LNFET Mode Select for Q_{B1}:** 0 – Full on mode with OCP 1 – LDO mode with CC current limit(Default)
5	LDO_MODE2	1	Y	N	**LNFET Mode Select for Q_{B2}:** 0 – Full on mode with OCP 1 – LDO mode with CC current limit(Default)
4:0	IINLIM[4:0]	00100	Y	N	**Input current limit:** Actual input current limit is always limited by the IINLIM register (and AICL adjustment when AICL_EN bit is set). IINLIM=100mA+100mA*[IINLIM] Range:100mA(00000)-2.4A(10111~11111) 00000=100mA 00001=200mA … 00100=500mA(Default) … 10111=2400mA 10111~11111=2.4A

REG01

BIT	Name	POR	Reset by REG_RST	Reset by Watchdog	DESCRIPTION
7	PFM _DIS	0	Y	N	**PFM mode Disable**: 0- Enable PFM 1- Disable PFM
6	WD_RST	0	Y	Y	**I²C Watchdog Timer Reset:** 0-Normal 1-Reset Back to 0 after watchdog timer reset.

5	OTG_CONFIG	0	Y	Y	**Boost (OTG) Mode Configuration:** 0-OTG Disable 1-OTG Enable Note: OTG_CONFIG would over-ride Charge Enable Function in CHG-CONFIG
4	CHG_CONFIG	1	Y	Y	**Charge Enable Configuration:** 0-Charge Disable 1-Charge Enable
3:1	SYS_MIN[2:0]	110	Y	N	**Minimum System Voltage Limit:** Range:3.1V-3.8V 000=3.1V 001=3.2V 010=3.3V 011=3.4V 100=3.5V 101=3.6V 110=3.7V(Default) 111=3.8V
0	OTG_BAT	0	Y	N	0 – 2.8 V BAT falling(Default) 1 – 2.5 V BAT falling

REG02

BIT	Name	POR	Reset by REG_RST	Reset by Watchdog	DESCRIPTION
7	BATSNS_DIS	0	Y	N	**Select either BATS pin or BAT pin to regulate battery voltage:** 0 – Enable BATSNS in battery CV regulation. (default) 1 – Disable BATSNS. Use BAT pin in battery CV regulation. Note: If the device fails BATSNS open/short detection or in SYSMIN regulation (BATSNS_STAT= 1), battery voltage is regulated through BAT pin, and BATSNS_DIS will be set to 1 automatically.
6:0	ICHG[6:0]	0001001	Y	Y	**Fast Charge Current Limit:** ICHG=16mA+[ICHG]*16mA Range:16mA(0000000)-2048mA(1111111) 0000000=16mA 0000001=32mA … 0001001=160mA(Default) … 1111111=2048mA

REG03

BIT	Name	POR	Reset by REG_RST	Reset by Watchdog	DESCRIPTION
7	VINDPM_INT _ MASK	0	Y	N	**Mask INT when VINDPM:** 0 – Allow VINDPM INT pulse 1 – Mask VINDPM INT pulse
6	IINDPM_INT_ MASK	0	Y	N	**Mask INT when IINDPM:** 0 – Allow IINDPM INT pulse 1 – Mask IINDPM INT pulse
5:0	IPRECHG [5:0]	000000	Y	Y	**Charge Current Limit in Pre-charge mode:** IPRECHG =8mA+[IPRECHG]*8mA Range:8mA-512mA 000000=8mA(Default) … 010011=160mA … 011101=240mA … 111111=512mA

REG04

BIT	Name	POR	Reset by REG_RST	Reset by Watchdog	DESCRIPTION
7:6	ISHORT [1:0]	00	Y	Y	**Charge Current Limit in Battery Short mode:** Range:10mA-80mA 00=10mA(Default) 01=20mA 10=40mA 11=80mA
5	Reserved	0	Y	Y	Reserved
4:0	ITERM [4:0]	00000	Y	Y	**Termination Current Limit:** ITERM=8mA+[ITERM]*8mA Range:8mA-256mA 00000=8mA(Default) … 10011=160mA … 11101=240mA … 11111=256mA

REG05

BIT	Name	POR	Reset by REG_RST	Reset by Watchdog	DESCRIPTION
7:2	VREG[5:0]	010100	Y	Y	**Charge Voltage Limit:** VREG=4.000V+[VREG]*10mV Range: 4.000V(000000)-4.5V(111111) 000000=4.000V 000001=4.010V … 010100=4.200V(Default) … 100011=4.350V … 110010~111111=4.5V
1	EN_TERM	1	Y	Y	**Charging Termination Enable:** 0-Disable 1-Enable(Default)
0	VRECHG	0	Y	Y	**Battery Recharge Threshold Offset:** 0-100mV(Default) 1-200mV

REG06

BIT	Name	POR	Reset by REG_RST	Reset by Watchdog	DESCRIPTION
7:6	WATCHDOG[1:0]	11	Y	Y	**I²C Watchdog Timer Setting:** 00-Disable timer 01-40s 10-80s 11-160s(Default)
5	EN_TIMER	1	Y	Y	**Charging Safety Timer Enable:** 0-Disable 1-Enable(Default)
4	CHG_TIMER	1	Y	Y	**Fast Charge Timer Setting:** 0-5 hrs 1-10 hrs(Default)

3	TMR2X_EN	1	Y	Y	**Safety Timer Setting during Input DPM and Thermal Regulation and JEITA cool:** 0-Safety timer not slowed by 2X during input DPM or thermal regulation or JEITA cool. 1-Safety timer slowed by 2X during input DPM or thermal regulation or JEITA cool.
2	TREG	1	Y	Y	**Thermal Regulation Threshold:** 0-90°C 1-110°C(Default)
1	JEITA_VSET (45℃-60℃)	0	Y	Y	**JEITA High Temperature Voltage Setting:** 0-Max. 4.1V(Default) 1-VREG
0	JEITA_ISET (0℃-10℃)	1	Y	Y	**JEITA Low Temperature Current Setting:** Percentage with respect to ICHG register REG02[6:0] 0-50% 1-20%

REG07

BIT	Name	POR	Reset by REG_RST	Reset by Watchdog	DESCRIPTION
7:6	OVP[1:0]	00	Y	N	**ACOV threshold:** 00 – 6.4 V (Default) 01 – 8.7 V (7-V input) 10 – 10.7 V (9-V input) 11 – 14.1 V (12-V input)
5	NTC_JEITA	0	Y	N	**JEITA Compliance:** 0 – Cold/Hot (Default) 1 – JEITA
4	Q1_EN	0	Y	N	**BLKFET Turn On Control in Boost Mode:** 0 – Disable (Default) 1 – Enable
3:0	VINDPM[3:0]	0111	Y	N	**Absolute VINDPM Threshold:** VINDPM=3.8V+[VINDPM]*100mV Range:3.8V(0000)-5.3V(1111) 0000=3.8V 0001=3.9V … 0111=4.5V(Default) … 1111=5.3V

REG08

BIT	Name	POR	Reset by REG_RST	Reset by Watchdog	DESCRIPTION
7:6	BHOT[1:0]	00	Y	Y	**Boost mode Hot Temperature Monitor Threshold:** 00-VBHOT0 Threshold (Typ. 37.75%) 01-VBHOT1 Threshold (Typ. 34.37%) 10-VBHOT2 Threshold (Typ. 31.25%) 11-Disable battery thermal protection
5	BCOLD	0	Y	Y	**Boost mode Cold Temperature Monitor Threshold**: 0-VBCOLD0 Threshold (Typ. 77%) 1-VBCOLD1 Threshold (Typ. 80%)
4	BATFET_DIS	0	Y	N	**Force BATFET Off:** 0-Allow Q4 turn on 1-Turn off Q4 with T_{SM_DLY} delay time or immediately (REG08(3)) In OTG mode, OTG_CONFIG will be cleared once BATFET is turned off (with T_{SM_DLY} or not).
3	BATFET_DLY	1	Y	N	**BATFET turn off delay control:** 0-Turn off BATFET immediately when BATFET_DIS is set. 1-Turn off BATFET with the delay T_{SM_DLY} when BATFET_DIS is set.
2	BATFET_RST_EN	1	Y	N	**BATFET Reset Enable by /QON:** 0-Disable BATFET reset function 1-Enable BATFET reset function
1:0	VDPM_BAT_TRACK[1:0]	00	Y	N	**Limit VINDPM to above BAT voltage.** 00 – Disable function (VINDPM set only by REG07[3:0]) 01 – VBAT + 200mV 10 – VBAT + 250mV 11 – VBAT + 300mV When this bit enabled, Actual VINDPM is higher of VINDPM register value and VBAT + VDPM_BAT_TRACK

REG09

BIT	Name	POR	Reset by REG_RST	Reset by Watchdog	DESCRIPTION
7:6	TSR_FAULT [1:0]	00	Y	N	**System Reset Time when Exit host mode:** Range:1s-4s 00=1s(Default) 01=2s 10=3s 11=4s
5:4	TSM_DLY [1:0]	11	Y	N	**BATFET Turn Off Delay Time:** Range:2s-10s 00=2s 01=5s 10=7s 11=10s(Default)
3:1	TQON_RST[2:0]	110	Y	N	**/QON Low Duration Time to Reset BATFET:** TQON_RST =4s+[TQON_RST]*2s Range:4s-20s 000 – 4s 001 – 6s … 110 – 16s (Default) 111 – 20s
0	TBATFET_RST	0	Y	N	**BATFET Turn Off Time during /QON Reset:** 0 – 2s (Default) 1 – 4s

REG0A

BIT	Name	POR	Reset by REG_RST	Reset by Watchdog	DESCRIPTION
7:6	NTC_TOFF[1:0]	11	Y	N	**NTC Detection Turn Off Time during one Period:** 00 = 0s 01 = 500ms 10 = 1s 11 = 2s(Default)
5	BOOST_LIM	1	Y	Y	**Boost Mode BLKFET Over Current minimum Limit:** 0 = 0.5 A 1 = 1.2 A
4:0	IDPM_LIM[4:0]	NA	NA	NA	Current Input Current Limit setting (Read only):

					IDPM_LIM=100mA+[IDPM_LIM] *100mA Range:100mA (00000)-2.4A (10111~11111) 00000=100mA (Default) 00001=200mA … 10111=2400mA 10111~11111=2.4A

REG0B

BIT	Name	POR	Reset by REG_RST	Reset by Watchdog	DESCRIPTION
7	LDO_HIZ_EN	0	Y	N	**Enable LDO1 in HIZ mode when ILDO not 00:** 0 – Disable (Default) 1 – Enable
6	Reserved	0	Y	Y	Reserved
5	SYSR_NTC	0	Y	N	**Enable SYS Shutdown and latch-off when NTC fault:** 0 – Disable (Default) 1 – Enable
4	SYSR_TIMER	0	Y	N	**Enable SYS Reset When Exit Host Mode:** 0 – Disable (Default) 1 – Enable System reset time is controlled by REG09[7:6] TSR_FAULT bits.
3:0	BOOSTV[3:0]	0110	Y	N	**Boost Regulation PMID Voltage:** BOOSTV =4.5V+ [BOOSTV] * 0.1V Range: 4.5V-5.5V 0000=4.5V 0001=4.6V … 0110=5.1V (Default) … 1010~1111=5.5V

REG0C

BIT	Name	POR	Reset by REG_RST	Reset by Watchdog	DESCRIPTION
7:6	ILDO1[1:0]	00	Y	N	**LDO Output Port1 CC Current Limit when LDO_MODE1=0** 00 – 0mA (Default)) 01 – 50mA

					10 – 100mA 11 – 200mA Note: None-zero CC current limit is only for LDO mode, fully–on mode is OCP 350mA current limit.
5:0	VLDO1[5:0]	100010	Y	N	**LDO1 Output Port1 Regulation Voltage:** VLDO1=1.6V+ [VLDO1] * 0.1V Range:1.6V-6.0V 000000 – 1.6V 000001 – 1.7V … 100010 – 5.0V (Default) … 101100 ~111111 – 6.0V

REG0D

BIT	Name	POR	Reset by REG_RST	Reset by Watchdog	DESCRIPTION
7:6	ILDO2[1:0]	00	Y	N	**LDO Output Port2 CC Current limit when LDO_MODE2=0:** 00 – 0mA (Default) 01 – 50mA 10 – 100mA 11 – 200mA Note: None-zero CC current limit is only for LDO mode, fully–on mode is OCP 350mA current limit.
5:0	VLDO2[5:0]	100010	Y	N	**LDO2 Output Port1 Regulation Voltage:** VLDO2=1.6V+ [VLDO2] *0.1V Range:1.6V-6.0V 000000 – 1.6V 000001 – 1.7V … 100010 – 5.0V (Default) … 101100 ~111111 – 6.0V

REG0E

BIT	Name	POR	Reset by REG_RST	Reset by Watchdog	DESCRIPTION
7	TQON_LOW	0	Y	N	**BATFET Turn On Time when Exit Shipping Mode:** 0 – 2s (Default) 1 – 50ms
6	AICL_EN	1	Y	N	**Adaptive Input Current Limit Enable:** 0 – Disable 1 – Enable (Default)
5	FORCE_AICL	0	Y	Y	**Force Start Adaptive Input Current Limit:** 0 – Do not force 1 – Force
4	Q1_FULLON	0	Y	N	**RBFET full on for better efficiency in Buck mode:** 0 – Use higher Q1 RDSON when programmed IINDPM ≤ 500mA (better accuracy, 1/4 on RBFET) 1 – Use lower Q1 RDSON always (better efficiency)
3:0	TOPOFF_TIMER[3:0]	0000	Y	Y	**The extended charging time after termination enabled and satisfied:** ITOPOFF= [ITOPOFF_TIMER]*5min 0000 – Disabled (Default) 0001 – 5 minutes 0010 – 10 minutes … 1100~1111– 60 minutes When disabled, charging terminated when termination conditions satisfied.

REG0F(Read only)

BIT	Name	POR	Reset by REG_RST	Reset by Watchdog	DESCRIPTION
7:5	BUS_STAT [2:0]	NA	NA	NA	**BUS Status register:** 000:No input 011:Adapter(0.5A) 111:OTG Note: Software current limit is reported in IDPM_LIM register.

4:3	CHRG_STAT [1:0]	NA	NA	NA	**Charging status:** 00-Not Charging 01-Pre-charge (<$V_{BATLOWV}$) 10-Fast Charging 11-Charge Termination Done
2	PG_STAT	NA	NA	NA	**Power Good Status:** 0-Not Power Good 1-Power Good
1	THERM_STAT	NA	NA	NA	**Thermal Regulation Status:** 0-Not in thermal regulation 1- In thermal regulation
0	VSYS_STAT	NA	NA	NA	**VSYS Regulation Status:** 0-Not in VSYSMIN regulation (V_{BAT}>V_{SYS_MIN}) 1-In VSYSMIN regulation (V_{BAT}<V_{SYS_MIN})

REG10 (Read only)

BIT	Name	POR	Reset by REG_RST	Reset by Watchdog	DESCRIPTION
7	WATCHDOG_ FAULT	NA	NA	NA	**Watchdog Fault status:** 0-Normal 1-Watchdog timer expiration
6	BOOST_FAUL T	NA	NA	NA	**Boost Mode Fault Status:** 0-Normal 1-BUS overloaded or BUS shorted in OTG, or BUS OVP, or battery is too low (any conditions that we cannot start Boost function)
5:4	CHRG_FAULT [1:0]	NA	NA	NA	**Charge Mode Fault Status:** 00-Normal 01-Input fault (BUS OVP or V_{BAT}<V_{BUS}<3.8V) 10-Thermal shutdown 11-Charge Safety Timer Expiration
3	BAT_FAULT	NA	NA	NA	**Battery Fault Status:** 0-Normal 1-BATOVP (104%*CV in charging mode)
2	ACOV_STAT	NA	NA	NA	**BUSOVP Status In Buck Mode:** 0-Normal 1-ACOV
1	LDO1_FAULT	NA	NA	NA	**LDO1 Status in all Modes:** 0-Normal 1- LDO1 OCP or short

0	LDO2_FAULT	NA	NA	NA	**LDO2 Status in all Modes:** 0-Normal 1- LDO2 OCP or short

REG11(Read only)

BIT	Name	POR	Reset by REG_RST	Reset by Watchdog	DESCRIPTION
7	VDPM_STAT	NA	NA	NA	**VINDPM Status:** 0-Not in VINDPM 1-In VINDPM
6	IDPM_STAT	NA	NA	NA	**IINDPM Status:** 0-Not in IINDPM 1-In IINDPM
5	BATSNS_STAT	NA	NA	NA	**BATSNS Status:** 0–Regulation battery voltage through BATS pin. 1–Regulate battery voltage through BAT pin.
4	TOPOFF_ACTIVE	NA	NA	NA	**Top-off Timer Status:** 0 – Top off timer not counting. 1 – Top off timer counting
3	AICL_OPTIMIZED	NA	NA	NA	**Adaptive Input Current Limit Status:** 0 – Detection in process 1 – Maximum input current detected When AICL does not start, this bit is 0. When FORCE_AICL is set, but the VDPM condition is not detected, keep this bit 0. IDPM_LIM register updates according to the actual input current.
2:0	NTC_FAULT[2:0]	NA	NA	NA	**NTC Fault Status:** Buck Mode 000-Normal 010-NTC Warm 011-NTC Cool 101-NTC Cold 110-NTC Hot Boost Mode 000-NTC Normal 101-NTC Cold 110-NTC Hot

REG12

BIT	Name	POR	Reset by REG_RST	Reset by Watchdog	DESCRIPTION
7	REG_RST	0	NA	NA	**Register Reset:** 0-Keep current register setting(Default) 1-Reset to default register value and reset safety timer Reset to 0 after register reset is completed.
6	BYPASS_EN	0	Y	Y	**Force HSFET Enable in Bypass Mode:** 0-Keep current switching status(Default) 1-Force HSFET to fully turn on. This bit can be set only when Boost mode is enabled.
5:2	PN[3:0]	NA	NA	NA	**Device Configuration:** 1001
1:0	DEV_REV[1:0]	NA	NA	NA	00

Operation Principle

The SY20744 is a fully-integrated switching battery charger with system power path management for single cell Li-Ion and Li-polymer battery in a wide range of TWS and other portable devices. It integrates the input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), BATFET (Q4) between system and battery, and two LNFETs (Q_{B1}, Q_{B2}) to supply 5V(programmable) to portable devices. The extremely low R_{DSON} achieves very high conversion efficiency up to 2A charging current. The device also integrates the bootstrap diode for the high-side gate drive.

Power-On-Reset (POR)

The internal bias circuits are powered from the higher voltage between BUS and BAT. When BUS or BAT voltage rises above UVLOZ, the sleep comparator, battery depletion comparator and BATFET driver are active. I^2C interface is ready for communication and all the registers are reset to default value. The host can access all the registers after POR.

Power Up from Battery without DC Source

If only battery is present and the voltage is above depletion threshold (V_{BAT_DPLZ}), the BATFET will turn on and provide power to system. The device is in HIZ mode and the REGN LDO stays off to minimize the quiescent current. The low R_{DSON} of BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time. The device always monitors the discharge current through BATFET. When the system is overloaded or shorted, the device will immediately turn off BATFET and latch off and set BATFET_DIS bit to indicate BATFET is disabled, until the input source plugs in again or one of the methods describe in section "BATFET Enable Mode" to re-enable BATFET.

Power Up from DC Source

When the DC source plugs in, the SY20744 checks the input source voltage to turn on REGN LDO and all the bias circuits. The power up sequence from DC source is as below:

1. Power up REGN LDO
2. Poor source qualification
3. Input voltage limit threshold setting (VINDPM threshold)
4. Converter Power-up

REGN LDO

The REGN LDO supplies internal bias circuits as well as the HSFET and LSFET gate drive.

When the device is in high impedance mode (HIZ) with REGN LDO off, the device draws less than I_{BUS_HIZ} from BUS. The battery powers up the system when the device is in HIZ mode.

Blocking FET (Q1)

After REGN LDO powers up, the SY20744 turns on the blocking FET to reduce the power loss.

Input Source Qualification

After REGN LDO powers up, the SY20744 will check the current capability of the input source. The input source capability is qualified by the internal active detection circuit.

Once a good input source is present, the status register PG_STAT bit will go high. An INT is asserted to the host.

Input Current Limit Setting

After input source qualification, the charger will set the input current limit automatically (0.5A when AICL_EN=1, 0.1A when AICL_EN=0). The host can over-write IINLIM register to change the input current limit if necessary.

Input voltage limit setting

The device supports wide range of input voltage (3.8V-14V) source and provides two methods to set input voltage limit (VINDPM) threshold to facilitate autonomous detection.

1. VINDPM based on VINDPM [3:0] register bits. (Register VDPM_BAT_TRACK=00)
2. VINDPM based on the higher of the VINDPM register bits and VDPM_BAT_TRACK register bits. (Register VDPM_BAT_TRACK not 00)

Converter Power-Up

After the input current and voltage are set, the converter is enabled and the HSFET and LSFET start switching. If battery charging is disabled or done, BATFET will turn off. Otherwise, BATFET stays on to charge the battery.

The SY20744 provides soft-start when ramps up the system rail. When the system rail is below 2.2V, the input current limit is 100mA.

As a battery charger, the SY20744 deploys a 1.5MHz step-down switching regulator. Internal compensation

network allows minimizing the peripheral circuit design.

In order to improve light-load efficiency, the device switches to PFM control at light load.

Adaptive Input Current Limit (AICL)

The SY20744 uses adaptive input current limit (AICL) to identify maximum power point of input source. The algorithm automatically identifies maximum input current limit of power source to avoid source overload.

Boost Mode Operation from Battery

The SY20744 deploys a 1.5MHz Boost converter to deliver power from the battery to other portable devices, both for BUS port and BOOST1, BOOST2 port.

The Boost operation can be enabled by setting OTG_CONFIG bit to 1, or pulling OTG pin high. In Boost mode, PMID is regulated to default 5.1V (programmable by REG0B [3:0] BOOSTV bits), and the status register BUS_STAT is set to 111.

In Boost mode with OTG_CONFIG bit=1, the blocking FET Q1 can be turned on by setting Q1_EN bit to 1, to supply power from PMID to BUS with output current limit up to 1.2A (programmable by REG0A[5] BOOST_LIM bit).

The BOOST1 and BOOST2 voltage can be regulated to the respective preset value of VLDO1 and VLDO2 bits (programmable, 1.6V-6.0V), by setting ILDO1 and ILDO2 bits to none 00 when not in HIZ mode. In HIZ mode, LDO_HIZ_EN bit also need to be set to enable BOOST1 and BOOST2 output.

Each LNFET (Q_{B1}, Q_{B2}) has a programmable current limit, with current limit up to 200mA (programmable by REG0C[7:6] and REG0D[7:6] ILDO bits) each in LDO mode (REG00 LDO_MODE=1) and 350mA (fixed) each in full on mode (REG00 LDO_MODE=0).

Similar to Buck operation, the device switches from PWM operation to PFM operation at light load to improve the efficiency. The PFM_DIS bit can be used to prevent PFM operation.

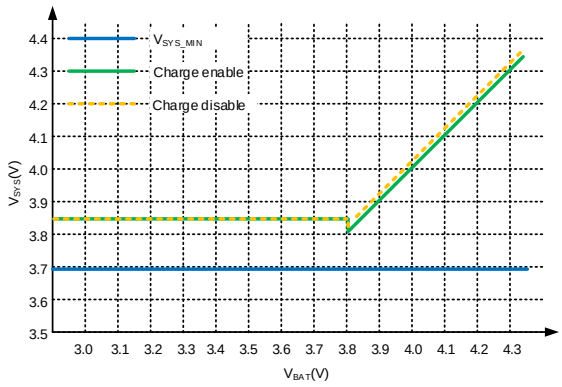
Any fault during Boost operation, including BUS over-voltage, BUS OCP or BUS short, or battery too low (V_{BAT}<V_{OTG_BAT}), sets the BOOST_FAULT register to 1 and an INT is asserted.

Power Path Management

The SY20744 accommodates a wide range of input sources from USB, wall adapter, or car battery. The device provides automatic power path selection to supply the system (SYS) from input source (BUS), battery (BAT), or both.

Narrow VDC Architecture

The device deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. When BUS source is present, the minimum system voltage is set by SYS_MIN bits, even with a fully depleted battery the system is regulated above the minimum system voltage (default 3.7V). The status register VSYS_STAT bit goes high when the system is in minimum system voltage regulation.



Dynamic Power Management

The SY20744 can manage the input power limit very well. It has input VINDPM and IINDPM function to protect the input source from over-loading.

When input source is over-loaded, either the current will exceed the input current limit (IINLIM) or the voltage will fall below the input voltage limit (VINDPM). The device will reduce the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero but the input source is still over-loading, the system voltage will start to drop. Once the system voltage falls below the battery voltage, the device will automatically enter the supplement mode where the BATFET turns on and battery starts discharging so that the system is supported from both the input source and battery.

During DPM mode, the status register VDPM_STAT or IDPM_STAT will go high.

Battery Charging Management

The SY20744 charges 1-cell Li-Ion battery with up to 2.0A charge current for high capacity battery. The 15mΩ BATFET improves charging efficiency and minimizes the voltage drop during discharging.

Autonomous Charging Cycle

With battery charging enabled at POR (CHG_CONFIG bit =1 and /CE pin is low), the SY20744 can complete a charging cycle without host involvement. The device default charging parameters are listed below.

Charging Parameter Default Setting	
Charging Voltage	4.2 V
Charging Current	160 mA
Pre-charge Current	8 mA
Termination Current	8 mA
Temperature Profile	Cold/Hot
Safety Timer	10 hours

The charger device automatically terminates the charging cycle when the charging current is below termination threshold and in constant voltage charge phase. When a full battery voltage is discharged below recharge threshold (Programmable by REG05[0]), the SY20744 automatically starts another charging cycle.

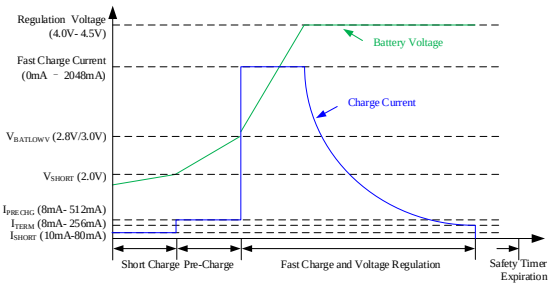
The status register CHRG_STAT indicates the different charging phases: 00-Not Charging, 01-Pre-charge, 10-Fast Charging (constant current and constant voltage mode), 11-Charge Termination Done. Once a charging cycle is complete, an INT is asserted to notify the host.

The host can always control the charging operation and optimize the charging parameters by writing to the registers through I^2C.

Battery Charging Profile

The device charges the battery in three phases: pre-charge, constant current charge, and constant voltage charge. At the beginning of a charging cycle, the device checks the battery voltage and applies current.

If the charger device is in DPM regulation or thermal regulation during charging, the actual charging current will be less than the programmed value. In this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate.



Charging Termination

The SY20744 will terminate a charge cycle when in constant voltage charge, and the current is below termination current. After the charging cycle is complete, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn back on to engage supplement mode.

When termination occurs, the CHRG_STAT is 11, and an INT is asserted to the host. Termination function can be disabled by writing 0 to EN_TREM.

A programmable top-off timer can be applied after termination is detected. The host can read CHRG_STAT and TOPOFF_ACTIVE to find out the termination status.

The top-off timer settings are read in once termination is detected by the charger. Programming a top-off timer value after termination will have no effect unless a recharge cycle is initiated. An INT will be asserted to the host when entering top-off timer segment (due to termination) as well as when top-off timer expires.

Charging Safety Timer

The SY20744 has safety timer to prevent extended charging cycle due to abnormal battery conditions.

The device keeps charging the battery until the fast charging safety timer expired. The duration of safety timer can be set by the CHG_TIMER bit (default = 10 hours). At the end of safety timer, the fault register CHRG_FAULT bits are set to 11 and an INT is asserted to the host. The safety timer feature can be disabled by setting EN_TIMER bit.

The safety timer is 2 hours when the battery is below $V_{BATLOWV}$ threshold.

During input voltage, input current regulation or thermal regulation or JEITA cool, the safety timer counts at half clock rate since the actual charge current is likely to be below the register setting. For example, if the charger is in input current regulation (IINDPM) throughout the whole charging cycle, and the safety time is set to 5 hours, the safety timer will

expire in 10 hours. This feature can be disabled by writing 0 to REG06[3] (bit TMR2X_EN).

Host Mode and Default Mode

The SY20744 can operate with or without host. In default mode, the SY20744 can be used as an autonomous charger with no host or with host in sleep.

When the charger is in default mode, WATCHDOG_FAULT bit is high. When the charger is in host mode, WATCHDOG_FAULT is low.

After power-on-reset, the device starts operation in default mode. The registers are in the default settings.

Any host writing command to I^2C transitions the device from default mode to host mode. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WD_RST bit before the watchdog timer expires or disable watchdog timer by setting WATCHDOG bits to 00.

When the watchdog timer is expired, the device gets back to the default mode.

Status Outputs (PG_STAT and /INT)

Power Good Indicator (PG_STAT)

In the SY20744, PG_STAT is set to indicate a good input source.

Interrupt to Host (INT)

In some applications, the host does not always monitor the charger operation. The INT notifies the system on the device operation.

When a fault occurs, the charger device sends out INT and latches the fault state in REG10 until the host reads the fault register. Before the host reads REG10 and all the faults (not including watchdog timer fault) are cleared, the charger device would not send any INT upon new faults.

In order to read the current fault status, the host has to read REG10 two times consecutively. The 1st reads fault register status from the last INT and the 2nd reads the current fault register status. The only exception is NTC_FAULT which always reports the actual condition on the NTC pin.

BATFET (Q4) Control

BATFET Disable Mode (Shipping mode)

To extend battery life and minimize power when system is powered off during system idle, shipping, or storage, the device can turn off BATFET so that the system voltage is zero to minimize the battery leakage current.

When the host set BATFET_DIS bit, the charger can turn off BATFET immediately or delay by T_{SM_DLY} as configured by BATFET_DLY bit.

BATFET Enable Mode (Exit Shipping mode)

When the BATFET is disabled (in shipping mode) and indicated by setting BATFET_DIS, plugging in adapter or a logic high to low transition on /QON pin with T_{QON_LOW} can enable BATFET to restore system power.

BATFET System Reset

When the input source is not plugged in (or plugged in but in HIZ mode) and BATFET is in on state, a logic high to low of T_{QON_RST} (typical 4s to 20s, programmable) resets SYS (system power) by turn BATFET off with 30mA pull-down current for T_{BATFET_RST} (typical 2s/4s, programmable) and then re-enable BATFET. The device will enter default mode when SYS is reset by /QON.

The function can be disabled by setting BATFET_RST_EN bit to 0.

Q_{B1} and Q_{B2} Control

Each LNFET (Q_{B1}, Q_{B2}) has a programmable current limit, with current limit up to 200mA (programmable by REG0C [7:6] and REG0D [7:6] ILDO bits) each in LDO mode (REG00 LDO_MODE=1) and 350mA (fixed) each in full on mode (REG00 LDO_MODE=0).

The BOOST1 and BOOST2 voltage can be regulated to the respective preset value of VLDO1 and VLDO2 bits (programmable, 1.6V-6.0V), by setting ILDO1 or ILDO2 bits to none 00 when not in HIZ mode. In HIZ mode, LDO_HIZ_EN bit also need to be set to enable BOOST1 and BOOST2 output.

Protections

Thermal Regulation and Thermal Shutdown

Buck Mode

The SY20744 monitors the internal junction temperature T_J to avoid overheat the chip and limits the IC surface temperature. When the internal junction temperature exceeds the preset limit (TREG bit), the device reduces the charge current. The wide thermal regulation range from 90°C to 110°C allows the user to optimize the system thermal performance.

During thermal regulation, the actual charging current is usually below the programmed battery charging current. Therefore, termination is disabled, the safety timer runs at half the clock rate, and the status register THERM_STAT goes high.

Additionally, the device has thermal shutdown to turn off the converter and BATFET. The fault register CHRG_FAULT is 10 and an INT is asserted to the host. The BATFET and converter are enabled to recover when IC temperature is below T_{TSD}-T_{TSD_HYS}.

Boost Mode

The device monitors the internal junction temperature to provide thermal shutdown during Boost mode. When IC junction temperature exceeds T_{TSD}, the Boost mode is disabled, OTG_CONFIG is cleared and BATFET is turned off. When IC junction temperature is below T_{TSD}-T_{TSD_HYS}, the BATFET is enabled automatically to allow system to restore.

Voltage and Current Monitoring in Buck Mode

The SY20744 closely monitors the input and system voltage, as well as HSFET and LSFET current for safe Buck mode operation.

Input Over-Voltage (ACOV)

The maximum input voltage for Buck mode operation is V_{BUS_OP}. If BUS voltage exceeds V_{ACOV}, the device stops switching immediately. During input over voltage (ACOV), the fault register ACOV_STAT will be set to 1, and CHRG_FAULT will be set to 01. An INT is asserted to the host.

System Over-Voltage Protection (SYSOVP)

The charger device monitors the voltage at SYS. When system over-voltage is detected, the converter is stopped to protect components connected to SYS from high voltage damage.

The charger maintains 30mA discharge current to bring down the system voltage once SYS stays in SYSOVP (only in charging mode).

Voltage and Current Monitoring in Boost Mode

The SY20744 closely monitors the BUS and BAT voltage, as well as RBFET, HSFET and LSFET current to ensure safe Boost mode operation.

Over-Current Protection

When BUS output current exceeds I_{OTG_OCP}, the device will retry 7 times in hiccup mode for protection. When over-current condition continues to exist after 7 times retry, Q1 is turned off (Q1_EN is cleared to 0). The fault register BOOST_FAULT is set high to indicate fault in Boost operation. An INT is asserted to the host.

Over-Voltage Protection

Once the BUS voltage exceeds V_{OTG_OVP}, the SY20744 stops switching and clears OTG_CONFIG bit and exits Boost mode. The fault register BOOST_FAULT is set high to indicate fault in Boost operation. An INT is asserted to the host.

Battery Protection

Battery Over-Voltage Protection (BATOVP)

The battery over-voltage limit is clamped at 4% above the battery regulation voltage. When battery over voltage occurs, the charger device immediately disables charge. The fault register BAT_FAULT goes high and an INT is asserted to the host.

Battery Over Discharge Protection

When battery voltage is discharged below V_{BAT_DPL}, the BATFET is turned off to protect battery from over discharge. To recover from over-discharge, an input source is required at BUS. When an input source is re-plugged in, the BATFET turns on again.

If the battery voltage falls below V_{SHORT}, the charge current is reduced to ISHORT for battery safety.

System Over-Current Protection

If the system is shorted or BATFET OCP occurs, the BATFET will be latched off. Section “BATFET Enable Mode” can reset the latch off condition and turn on BATFET.

Thermistor Temperature Window

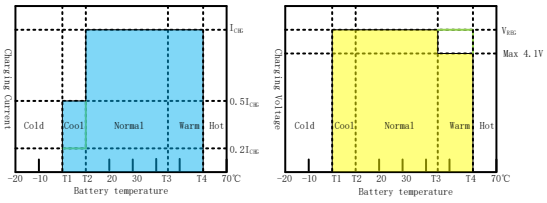
The SY20744 continuously monitors battery temperature by measuring the voltage between the NTC pin and ground, typically determined by a negative temperature coefficient thermistor and an external voltage divider.

Charging JEITA Guideline Compliance

JEITA recommends suspending the battery charging process when NTC pin voltage is out of the VT1 to VT4 range, and recovering charging process once the NTC voltage is within the range. JEITA also recommends that the charge current to be reduced to at least half of the charge current or lower at cool temperature(T1-T2), and the charge voltage to be reduced less than nominal charge voltage at warm temperature(T3-T4).

The SY20744 provides flexibility charge voltage/current settings beyond the JEITA requirement. REG06[1] is used for setting the charge voltage to be VREG or max 4.1V at warm temperature (T3-T4). REG06[0] is used for setting the current setting to be 20% or 50% of fast charge current at cool temperature (T1-T2).

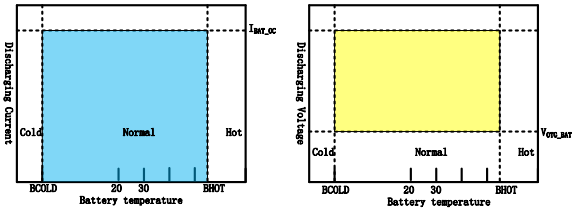
When the NTC fault occurs, the fault register NTC_FAULT will indicate the actual condition on NTC pin and an INT will be asserted to the host.



Discharging Cold/Hot Temperature Window

The device will terminate the battery discharging process when NTC pin voltage is out of the V_{BCOLD} to V_{BHOT} range. To allow the discharge, the battery temperature must be within this range. The threshold of V_{BCOLD} and V_{BHOT} is selectable by setting REG08.

When the NTC fault occurs, the fault register NTC_FAULT will indicate the actual condition on NTC pin and an INT will be asserted to the host.



Serial Interface

The SY20744 uses I²C compatible interface for flexible charging parameter programming and instantaneous device status reporting. Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address 6BH, receiving control inputs from the master device like micro controller or a digital signal processor. The I²C interface supports both standard mode (up to 100k bits), and fast mode (up to 400k bits).

Both SDA and SCL are bi-directional lines, connecting to the positive supply voltage via a current source or pull- up resistor. When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain.

Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

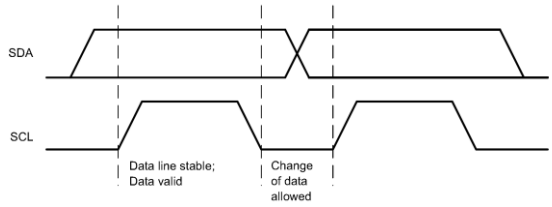


Figure 3. Bit Transfer on the I²C Bus

START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

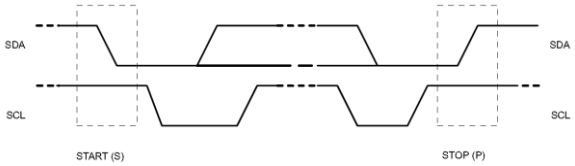


Figure 4. START and STOP conditions

Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

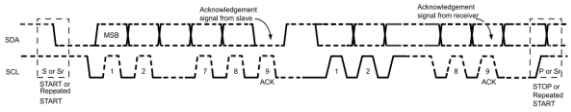


Figure 5. Data Transfer on the I²C Bus

Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses,

including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains high during the 9th clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated start to start a new transfer.

Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

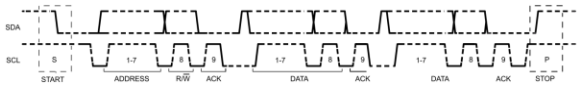


Figure 6. Complete Data Transfer

Single Read and Write

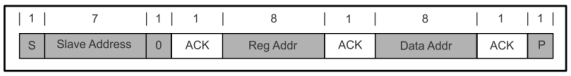


Figure 7. Single Write

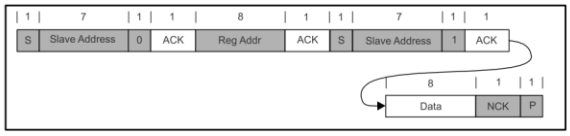


Figure 8. Single Read

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

Multi-Read and Multi-Write

The charger device supports multi-read and multi-write.

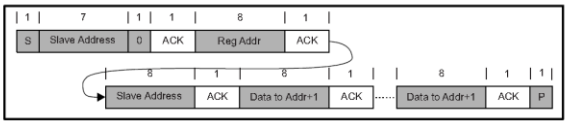


Figure 9. Multi-Write

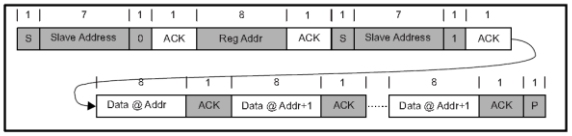


Figure 10. Multi-Read

The fault register REG10 locks the previous fault and only clears it after the register is read. For example, if Charge Safety Timer Expiration fault occurs but recovers later, the fault register REG10 reports the fault when it is read the first time, but returns to normal when it is read the second time. To verify real time fault, the fault register REG10 should be read twice to get the real condition. In addition, the fault register REG10 does not support multi-read or multi-write.

Applications Information

The following battery charger design refers to the "Application Schematic". This section describes how to select the external components including the inductor, the input and output capacitors.

Inductor Selection

Higher switching frequency allows the using of the smaller inductor and the capacitor values. The inductor saturation current should be higher than the load current (I_{LOAD}) plus half of the ripple current (I_{Ripple}):

$$I_{SAT} \geq I_{LOAD} + \frac{1}{2} \times I_{Ripple}$$

The inductor ripple current depends on the input voltage (V_{IN}), the duty cycle ($D = V_{OUT}/V_{IN}$), the switching frequency (F_{SW}) and the inductance (L):

$$I_{Ripple} = \frac{V_{IN} \times D \times (1 - D)}{F_{SW} \times L}$$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. Usually the inductor ripple is designed in the range of (20-40%) maximum charging current as a trade-off between the inductor size and efficiency for a practical design.

Output Capacitor Selection

The output capacitor in parallel with the battery is used for absorbing the high frequency switching ripple current and smoothing the output voltage. The RMS value of the output ripple current I_{RMS} is calculated as follow:

$$I_{RMS} = \frac{V_{IN} \times D \times (1 - D)}{\sqrt{12}L \times F_{SW}}$$

Where the duty cycle D is the ratio of the output voltage (battery voltage) over the input voltage for CCM mode which is the typical operation for the battery charger. During the battery charge period, the battery voltage varies from its initial battery voltage to the rated voltage. A typical 10μF ceramic capacitor is a good choice to absorb this current and also has a very small size.

Input Capacitor Selection

The input capacitor absorbs input ripple current from the Buck converter, which is given by the below equation:

$$I_{RMS} = \frac{I_{LOAD} \times \sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

This RMS ripple current must be smaller than the rated RMS current in the capacitor datasheet. At the same time, the input capacitor is also as the output capacitor when Boost works. At this condition, the input capacitor can be calculated as below:

Usually V_{RIPPLE} is designed less than 0.5% of the Boost output voltage. A typical 10μF ceramic capacitor is a good choice to absorb this current and also has a very small size. For best performance, BUS should be decoupled to PGND with 1μF capacitance. The remaining input capacitor should be place on PMID.

$$C_{IN} = \frac{I_{IN} \times (V_{IN} - V_{OUT})}{F_{SW} \times V_{IN} \times V_{Ripple}}$$

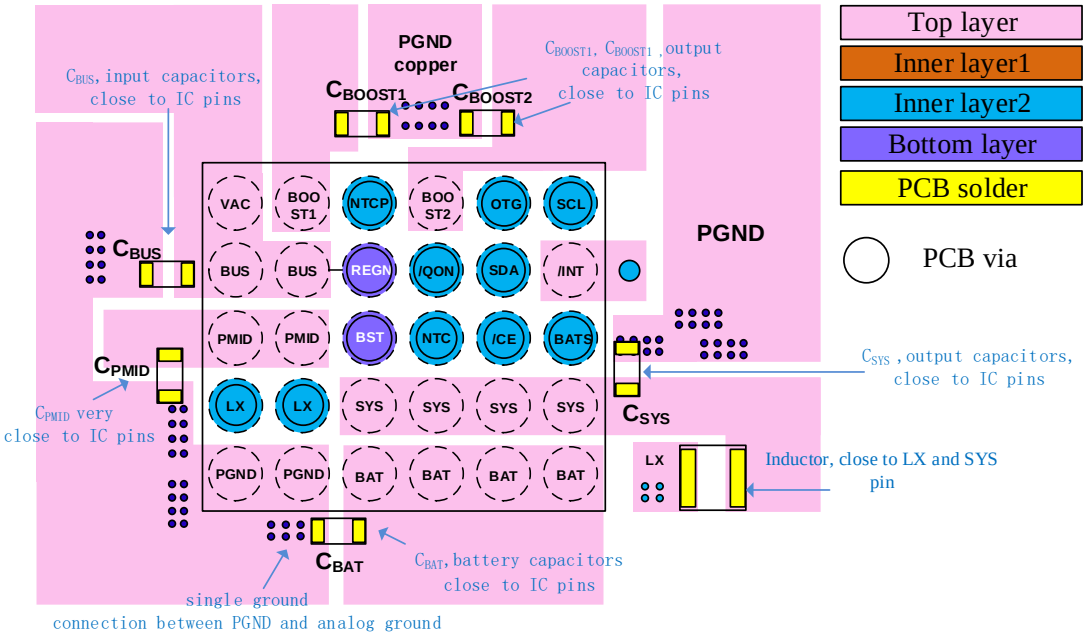
Layout Design

The layout design of the SY20744 regulator is relatively simple. For the best efficiency and to minimize noise problems, we should place the following components close to the IC: C_{PMID}, C_{REGN}, C_{BST}, C_{SYS}, C_{BOOST1}, C_{BOOST2} and C_{BAT}.

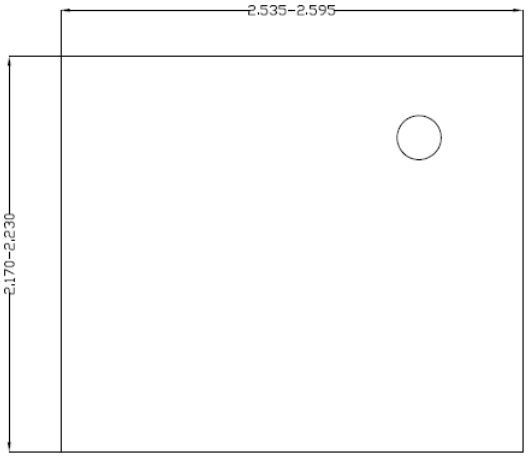
1) It is desirable to maximize the PCB copper area adjacent to PGND pin to achieve the best thermal and noise performance. If the board space allows, a ground plane is highly desirable.

2) C_{PMID}, C_{REGN}, C_{BST}, C_{SYS}, C_{BOOST1}, C_{BOOST2} and C_{BAT} must be close to the IC.

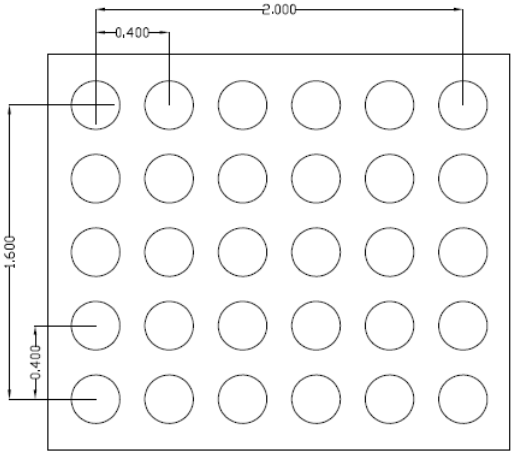
3) The loop area formed by C_{PMID} and PGND must be minimized. The PCB copper area adjacent to LX pin must be minimized to avoid the potential noise problem. The following picture is the recommended layout design of LX, C_{PMID}, C_{REGN}, C_{BST}, C_{SYS}, C_{BOOST1}, C_{BOOST2} and C_{BAT}.



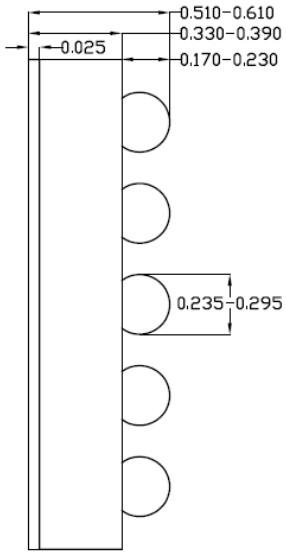
CSP2.2×2.565-30 Package Outline Drawing



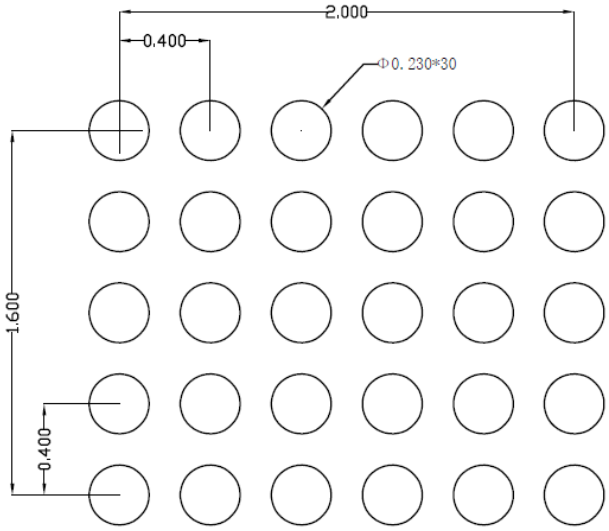
Top view



Bottom view



Side view



Recommend PCB Layout

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

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