# SY2A54024

## High Common-Mode Rejection Line Receiver

## General Description

The SY2A54024 is a differential amplifier designed for car radio applications. It is especially useful in applications with long connections between signal sources and amplifiers where ground noise elimination is crucial. The device utilizes an instrumentation amplifier topology with 0dB gain, ensuring high input impedance and a high common-mode rejection ratio (CMRR). The SY2A54024 achieves a typical common-mode rejection of 106dB, maintaining its effectiveness even with mismatched source impedances.

The SY2A54024 device is designed to operate at a high level of performance in audio line-receiver applications with minimal external components. Figure 1 illustrates the use of SY2A54024 in professional audio applications. In these applications, the line receiver recovers a differential audio signal that may have been affected by considerable common-mode noise.

The SY2A54024 is available in a compact TSSOP14 package.

## Features

- Wide Input Voltage Range: 4.5V to 18V
- High Common-Mode Rejection: 106dB typ.
- 1MΩ Differential High Input Impedance
- Common-Mode Suppression Independent of Source Resistance
- Ultra-Low Total Harmonic Distortion and Noise: <0.001%
- Low Quiescent Current: 4.1mA typ.
- Few External Components
- Short-Circuit Protection
- Integrated EMI Filters
- AEC-Q100 Grade 1 Qualified
- -40°C to 125°C Ambient Temperature Range

## Applications

- Differential Audio Interfaces
- Audio Input Circuitry
- Line Drivers
- Audio Power Amplifiers
- Audio Analyzers
- High-End Audio and Video (A/V) Receivers

## Typical Application

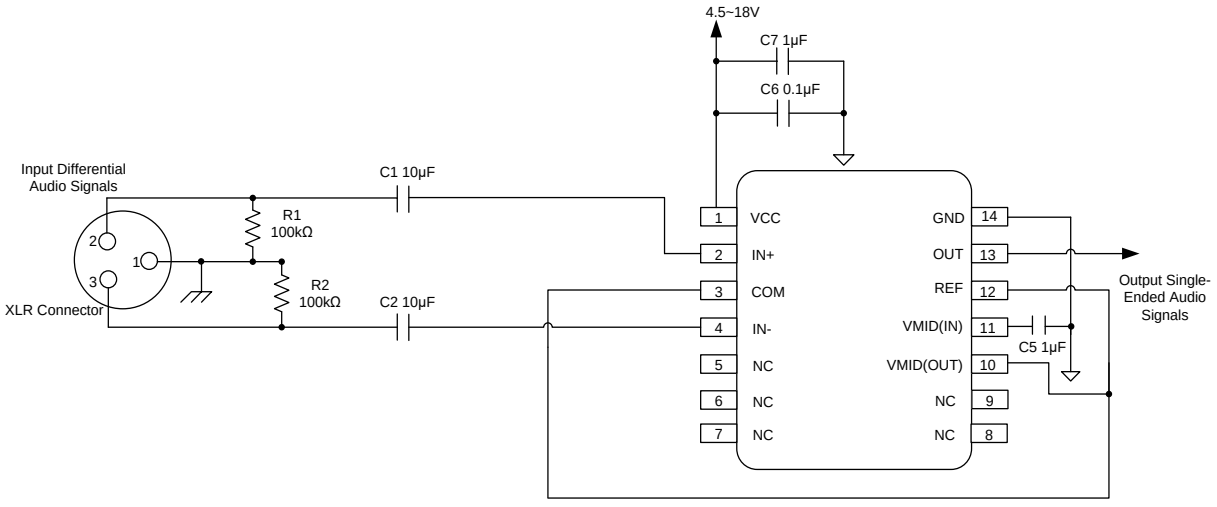


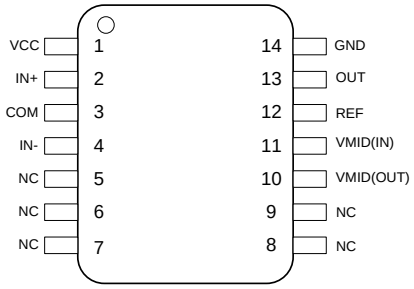

*Figure 1. Typical Application*

## Ordering Information

| Ordering Part Number | Package Type | Top Mark |
|---|---|---|
| SY2A54024HDA | TSSOP14<br>RoHS Compliant and Halogen Free | **BYY*xyz*** |

***x=year code, y=week code, z= lot number code***

## Pinout (Top View)




| Pin Name | Pin No. | Type(1) | Pin Description |
|---|---|---|---|
| VCC | 1 | P | Power supply. |
| IN+ | 2 | AI | Non-inverting input. |
| COM | 3 | AI | Input common. |
| IN- | 4 | AI | Inverting input. |
| NC | 5,6,7,8,9 | | No connection. |
| VMID(OUT) | 10 | AO | Buffered output of internal supply divider. |
| VMID(IN) | 11 | AI | Input node of internal supply divider. Connect a capacitor to this pin to reduce noise from the supply divider circuit. |
| REF | 12 | AI | Reference input, this pin must be driven from a low impedance. |
| OUT | 13 | AO | Output. |
| GND | 14 | P | Ground pin. |

**Note:** Type: A =analog; D =digital; P =power/ground/decoupling; I =input; O =output; IO=inout

## Block Diagram

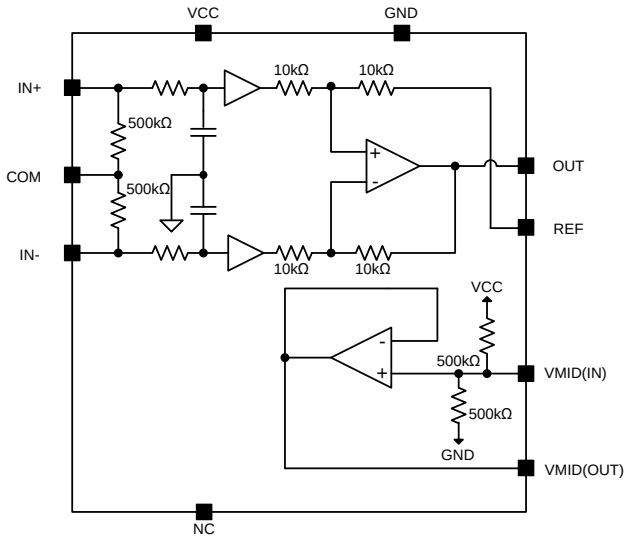



*Figure 2. Block Diagram*

| **Absolute Maximum Ratings** (1) | **Min** | **Max** | **Unit** |
|---|---|---|---|
| $V_{CC}$, Supply Voltage | -0.3 | 30 | V |
| Input Pins Voltage | -0.3 | $V_{CC}$+0.3 | |
| Input Pins Current | -10 | 10 | mA |
| $T_J$, Operating Junction Temperature | -40 | 150 | °C |
| $T_{stg}$, Operating Storage Temperature | -65 | 150 | |

| **Thermal Information** (2) | **Value** | **Unit** |
|---|---|---|
| $\theta_{JA}$ | 95 | °C/W |
| $\theta_{JC}$ (Top) | 15 | |
| $\theta_{JB}$ | 47 | |
| $\Psi_{JT}$ | 0.84 | |

| **Recommended Operating Conditions** | **Min** | **Max** | **Unit** |
|---|---|---|---|
| $V_{CC}$, Supply Voltage Range | 4.5 | 18 | V |
| Input Pins Voltage Range- | 0 | $V_{CC}$ | |
| $T_A$, Ambient Temperature Range | -40 | 125 | °C |

**Electrical Characteristics** $T_A$ = -40°C to 125°C, $V_{CC}$ = 4.5V to 18V, $V_{CM}$ = $V_{OUT}$ = midsupply, and $R_L$ = 2kΩ, unless otherwise specified.

| Parameter | | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Audio Performance (4) | Total Harmonic Distortion + Noise | THD+N | $V_O$=3VRMS, f=1kHz, $V_{CC}$=18V, 90kHz measurement bandwidth | | | 0.0007 % | | |
| | Intermodulation Distortion | IMD | SMPTE and DIN two-tone, 4:1 (60Hz and 7kHz),$V_O$ =3VRMS, 90kHz measurement bandwidth | | | 0.0011 % | | |
| | | | CCIF twin-tone (19kHz and 20kHz), $V_O$ =3VRMS, 90kHz Measurement bandwidth | | | 0.0002 7% | | |
| AC Performance (4) | Small Signal Bandwidth | BW | $V_{OUT}$ =0.1$V_P$ | | | 3.5 | | MHz |
| | Slew Rate | SR | | | | 3 | | V/μs |
| | Full-Power Bandwidth (3) | | $V_{OUT}$ =1$V_P$ | | | 0.47 | | MHz |
| | Phase Margin | PM | $C_L$ = 20 pF | | | 80.5 | | ° |
| | | | $C_L$ = 200 pF | | | 76.5 | | ° |
| | Settling Time | $t_s$ | To 0.01%, $V_{CC}$=18V, 10V step | | | 2.2 | | μs |
| | Overload Recovery Time | | | | | | 330 | ns |
| | EMI/RFI Filter Corner Frequency (5) | | | | | 80 | | MHz |
| Noise (4) | Output Voltage Noise | | f = 20Hz to 20kHz, no weighting | | | 6 | | μVRMS |
| | | | | | | –104.7 | | dBu |
| | Output Voltage Noise Density (5) | $e_n$ | f = 100Hz | | | 90 | | nV/√Hz |
| | | | f = 1kHz | | | 45 | | |
| Offset Voltage | Output Offset Voltage | $V_{OS}$ | | | | ±1 | ±4 | mV |
| | Output Offset Voltage Drift (5) | $dV_{OS}/dT$ | | | | 3 | | μV/°C |
| | Power-Supply Rejection Ratio (4) | PSRR | | | | 2 | | μV/V |
| Gain (4) | Gain | | | | | 1 | | V/V |
| | Gain Error | | | | | 0.08% | | |
| | Gain Nonlinearity(5) | | | | | 1 | 5 | ppm |
| Input Voltage Range | Common-Mode Voltage Range | $V_{CM}$ | | | 0.25 | | $V_{CC}$ – 2 | V |
| | Common-Mode Rejection Ratio | CMRR | 0.25V ≤ $V_{CM}$ ≤ $V_{CC}$-2V, REF and COM pins connected to $V_{MID(OUT)}$, $V_{CC}$=18V | | 90 | 106 | | dB |
| Input Impedance | Differential | | | | 850 | 1000 | 1150 | kΩ |
| | Common-Mode | | | | 212.5 | 250 | 287.5 | kΩ |
| | Input Resistance Mismatch | | | | | 0.01% | 0.25% | |
| Supply Divider Circuit (4) | Nominal Output Voltage | | | | | $V_{CC}$/ 2 | | V |
| | Output Voltage Offset | | $V_{MID(IN)}$ = $V_{CC}$/2 | | | 1 | 4 | mV |
| | Input Impedance | | VMID(IN) pin, f=1kHz | | | 240 | | kΩ |
| | Output Resistance | | VMID(OUT) pin | | | 0.96 | | Ω |
| | Output Voltage Noise | | 20Hz to 20kHz, $C_{MID}$=1μF | | | 2.7 | | μVRMS |
| | Output Capacitive Load Limit | | Phase Margin > 45°, $R_{ISO}$=0Ω | | | 150 | | pF |
| Output | Voltage Output Swing from Rail | $V_O$ | Positive rail | $R_L$ = 2kΩ | 160 | 280 | 400 | mV |
| | | | | $R_L$ = 600Ω | 650 | 850 | 1200 | |
| | | | Negative rail | $R_L$ = 2kΩ | 100 | 180 | 250 | |
| | | | | $R_L$ = 600Ω | 330 | 550 | 800 | |
| | Output Impedance (4) | $Z_{OUT}$ | $T_A$=25°C,f ≤ 100kHz, $I_{OUT}$ = 0A | | | 0.96 | | Ω |
| | Short-Circuit Current | $I_{SC}$ | $V_{CC}$=18V | | | ±70 | ±83 | mA |
| Power Supply | Quiescent Current | $I_Q$ | $I_{OUT}$ = 0 A | | | 4.1 | 5.1 | mA |

**Note 1:** Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the

operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain a possibility to affect device reliability.

**Note 2:** $\theta_{JA}$ is measured in the natural convection at $T_A$ = 25°C on a highly effective four-layer thermal conductivity test board as defined in JEDEC 51-7.

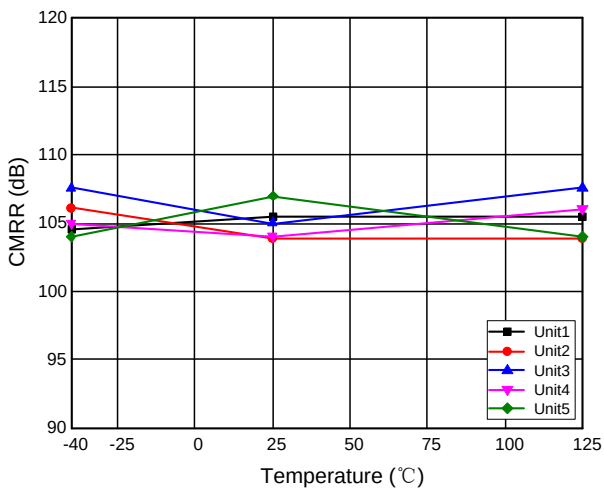
**Note 3:** Full-power bandwidth = SR / ($2\pi \times V_P$), where SR = slew rate.

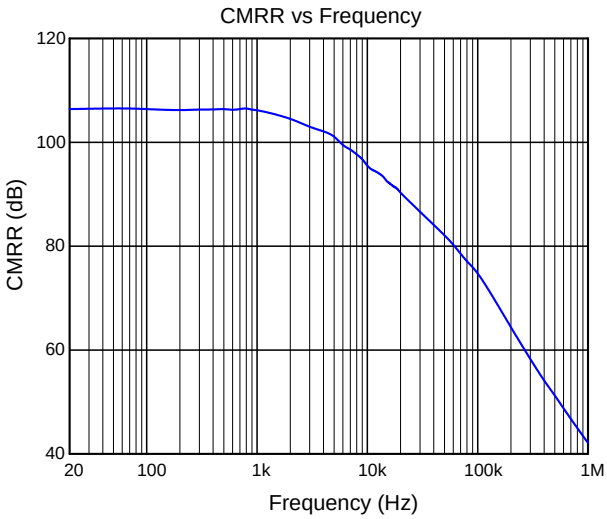
**Note 4:** Typical value tested on the demonstration board is guaranteed by design.

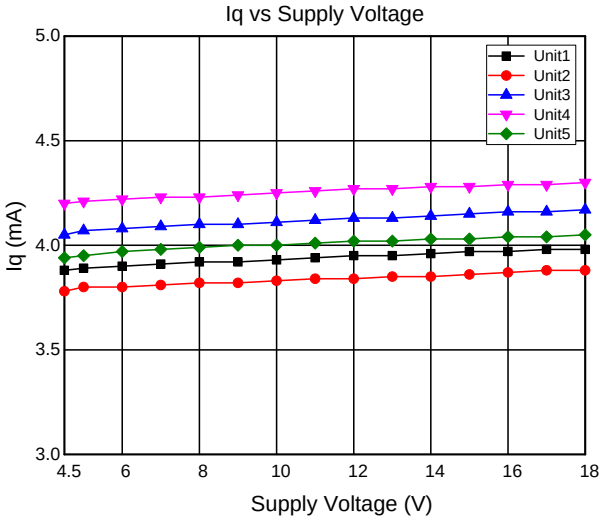
**Note 5:** Specified by design and characterization.

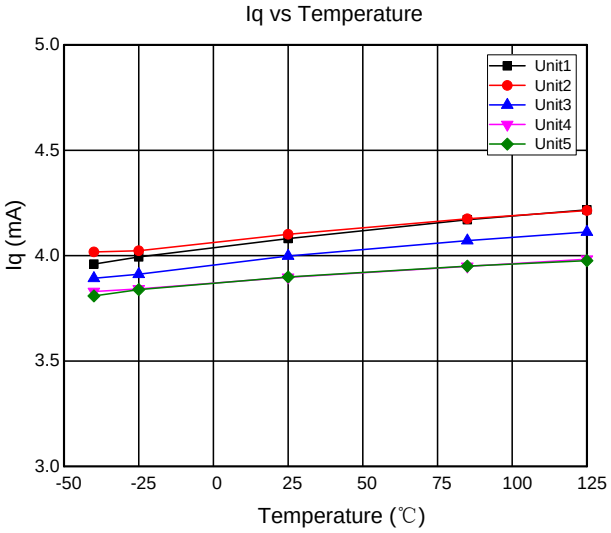
## Typical Performance Characteristics

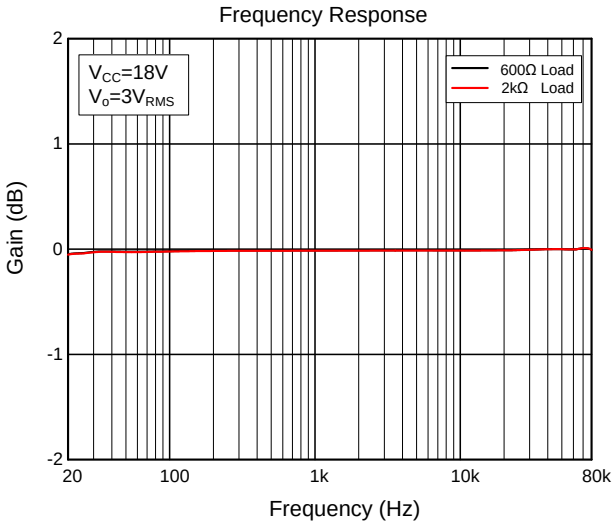
($T_A$=25℃, $V_{CC}$=18V, $V_{CM}$ = $V_{OUT}$ = midsupply, and $R_L$ = 2 kΩ unless otherwise specified)

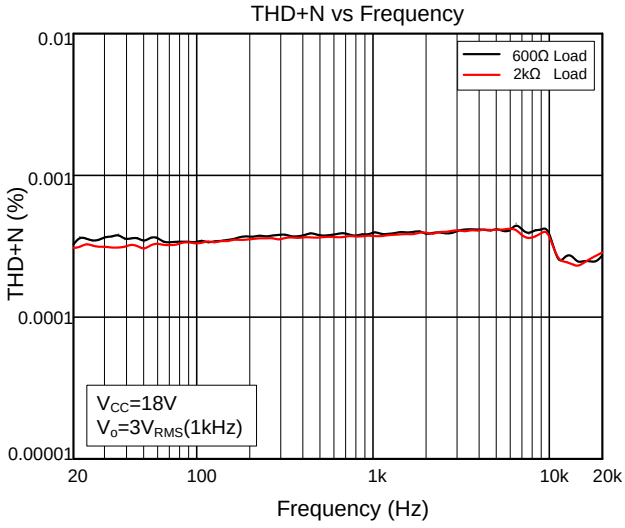


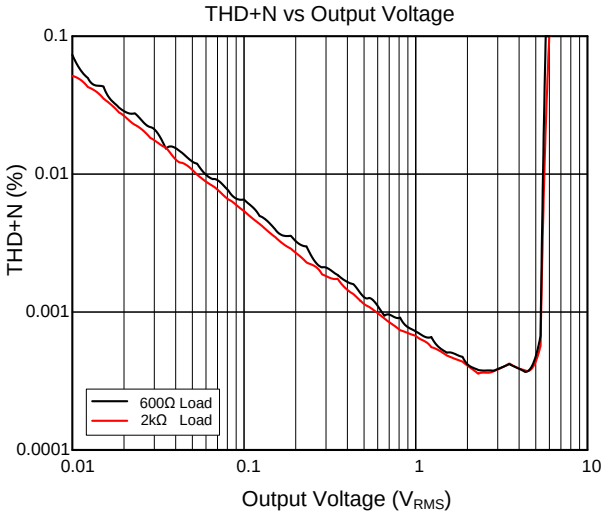



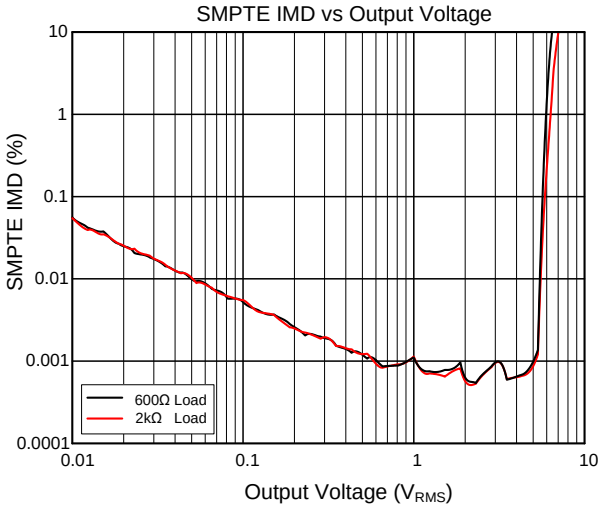



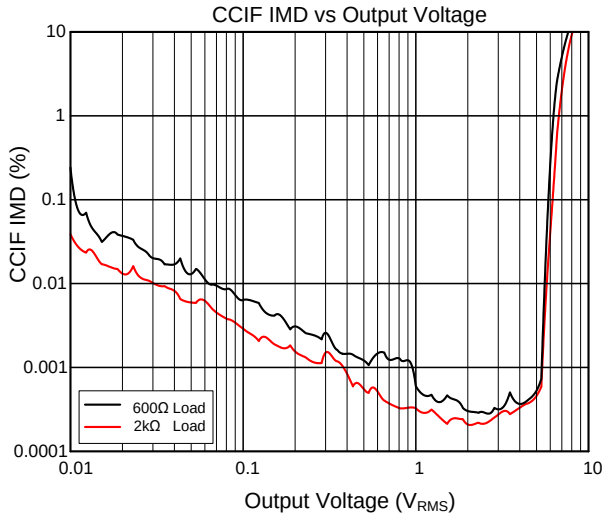





# Function Description

## Audio Signal Path

The basic components in the SY2A54024 audio signal path are shown in Figure 3. The main components include an input bias resistor, electromagnetic interference (EMI) filter, input buffer, and differential amplifier.

The primary role of the audio line receiver is to convert the differential input signal into a single-ended output signal while suppressing the common-mode noise present at the inputs. The device uses a differential amplifier (consisting of an operational amplifier and four matching 10kΩ resistors) to provide this function. The transfer function of the circuit is shown in equation 1:

$$V_{OUT} = (V_{IN+} - V_{IN-}) + V_{REF} \quad (1)$$

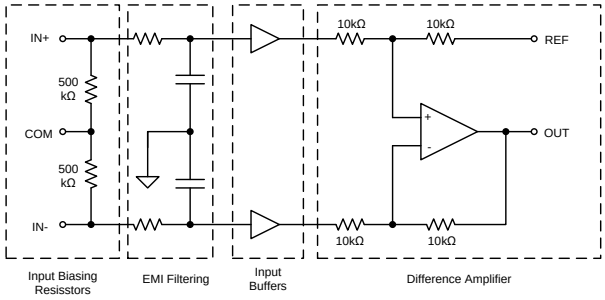



*Figure 3. Audio Signal Path*

The input buffer prevents external resistances (such as those from PCBs, connectors, or cables) from affecting the precise matching of internal 10kΩ resistors, thereby reducing the differential amplifier's high common-mode suppression.

Typical of many amplifiers, a small bias current flows into or out of the buffer amplifier inputs. This current must flow to a common potential for the buffer to work properly. The input bias resistance provides an internal path for this current to reach the COM pin. The COM pin is connected to the output of the internal power divider (VMID(OUT)). In addition, EMI filtering is added to the input buffer to prevent high-frequency interference signals from propagating through the audio signal path.

## Supply Divider

The SY2A54024 incorporates a supply divider circuit that allows the input common-mode voltage and output reference voltage to be biased to the midpoint between the added power supply voltages. The nominal output voltage of the power supply voltage divider circuit is shown in Formula 2:

$$V_{MID(OUT)} = \frac{V_{CC}}{2} \quad (2)$$

Figure 4 illustrates the internal topology of the supply-divider circuit. The supply divider consists of two 500kΩ resistors connected between the VCC and GND pins of the SY2A54024. The non-inverting input of the buffer amplifier is connected to the midpoint of the voltage divider that is formed by the 500kΩ resistors. The buffer amplifier provides a low-impedance output that is required to bias the REF pin without lowering the CMRR.

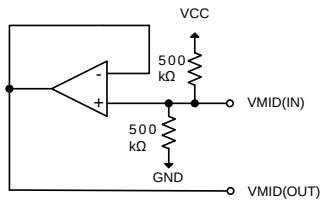



*Figure 4. Internal Supply Divider Circuit*

## Thermal Shutdown

If the junction temperature of the SY2A54024 exceeds approximately 170ºC, the thermal shutdown circuit will disable the amplifier to protect the device from damage. The amplifier will automatically re-enable when the junction temperature is below the shutdown threshold temperature. If the conditions leading to excessive power consumption are not eliminated, the amplifier will oscillate between the shutdown and enabled states until the output fault is corrected.

## Single-Supply Operation

The SY2A54024 is suitable for single power supplies ranging from 4.5V to 18V. Use the COM and REF pins to provide the output reference voltage level and ensure operation in the linear region. Ideally, connecting the REF and COM pins to the medium power potential (such as the VMID (OUT) pin) can avoid the output saturation of the internal amplifier.

## Typical Application Schematic

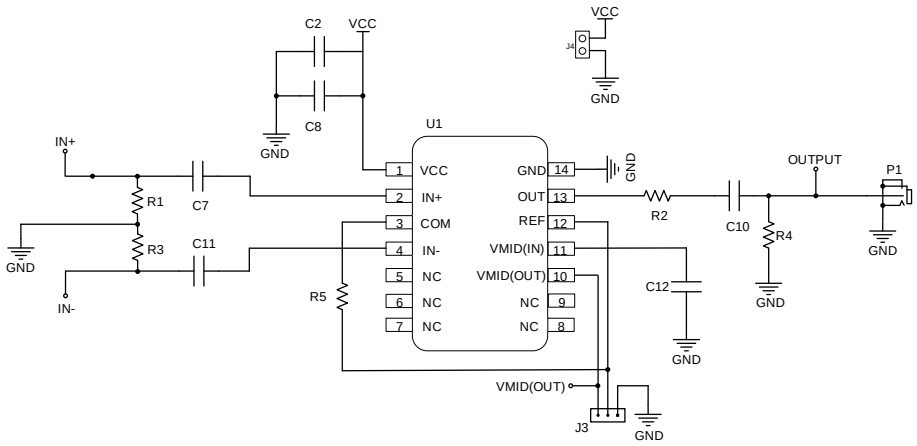



*Figure 5. SY2A54024 EVM Schematic*

## BOM List

| Designator | Description | Part Number | Manufacturer |
|---|---|---|---|
| U1 | High Common-Mode Rejection Line Receiver, SSOP-14 | SY2A54024HDA | Silergy |
| C12 | 1uF/50V, ±10%, X7R, 1206 | | |
| C2, C7, C10, C11 | 10uF/50V, ±10%, X7R, 1206 | | |
| C8 | 100nF/50V, ±10%, X7R, 1206 | | |
| R1, R3, R4 | 100k, 1%, 1206 | | |
| R2 | 49.9, 1%, 1206 | | |
| R5 | 0, 5%, 1206 | | |
| P1 | RCA Jack, 1Pos, Tin, White, R/A, TH | | CUI Inc. |
| J3 | JUMPER3P | | |
| J4 | B2PS-VH | | |

## PCB Layout Guideline

For best performance of the SY2A54024, the following guidelines must be followed:

1. Provide a separate short and thick power line to the SY2A54024 to decrease voltage drop.
2. The high-frequency VCC decoupling capacitors should be placed as close to the VCC pin as possible. These caps can be connected to the ground plane directly. It is recommended to select low ESR ceramic capacitors.
3. The input capacitors should be placed close to the IN+ and IN- input pins. The input lines should be arranged in parallel to suppress common-mode noise coupling effectively.

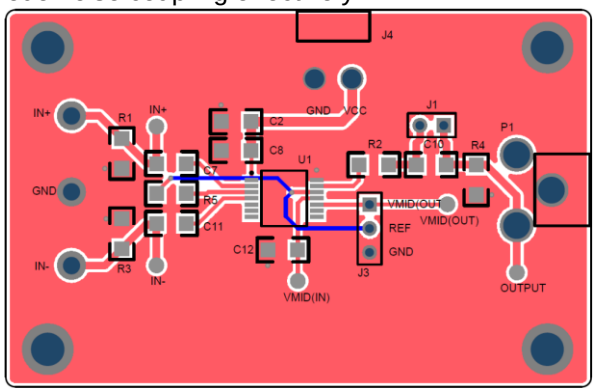
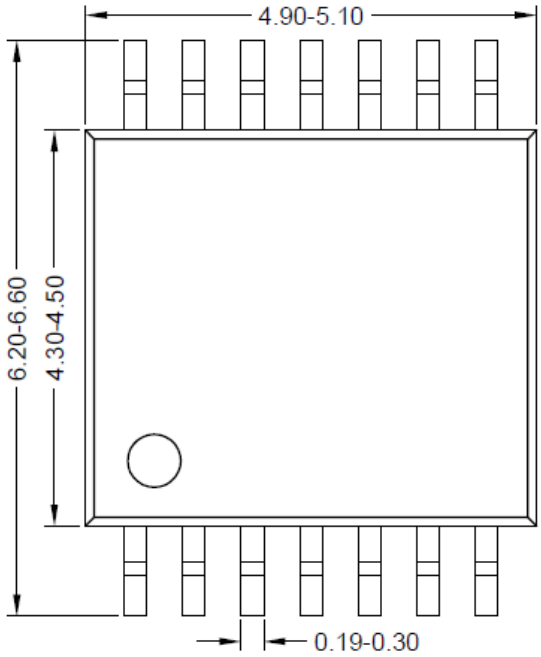
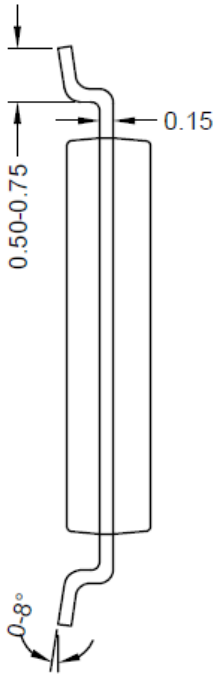



*Figure 6. PCB Layout Suggestion*

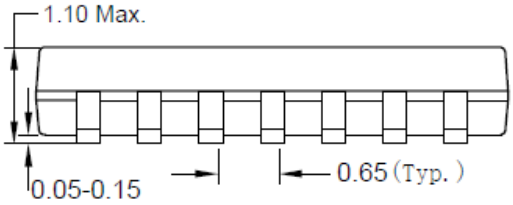
## TSSOP14 Package Outline Drawing



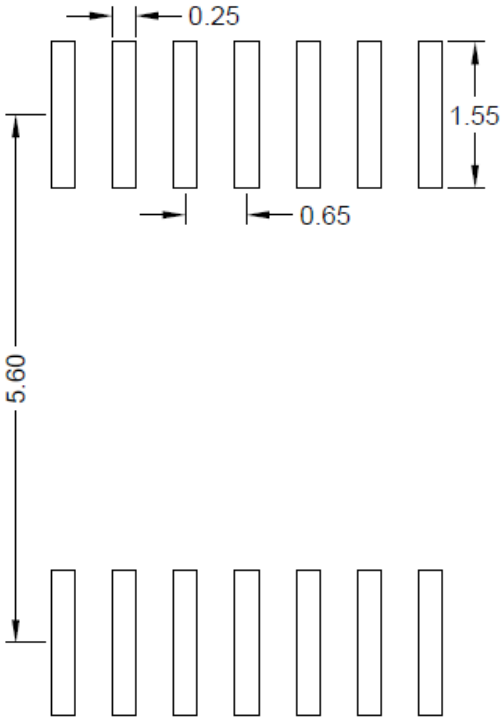

Top View




Side View




Front View

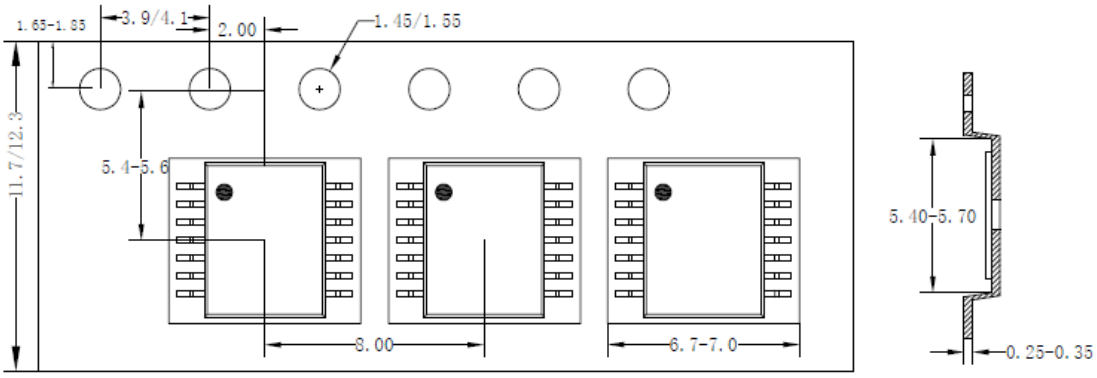



Recommended PCB Layout
(Reference only)

*Note: All dimensions are in millimeters and exclude mold flash and metal burr.*

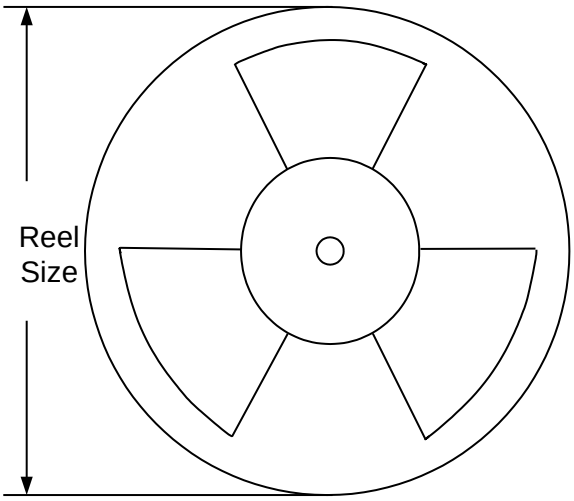
# Taping & Reel Specification

## TSSOP14 Taping Orientation




Feeding direction ⟶

## Carrier Tape & Reel Specification for Packages




| Package Types | Tape Width (mm) | Pocket Pitch (mm) | Reel Size (Inch) | Trailer Length (mm) | Leader Length (mm) | Qty per Reel |
|---|---|---|---|---|---|---|
| TSSOP14 | 12 | 8 | 13" | 400 | 400 | 2500 |

## Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

| Revision Number | Revision Date | Description | Pages changed |
|---|---|---|---|
| 0.9 | 12/10/2020 | Initial Release | |
| 1.0 | 12/10/2021 | Production Release | |

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