SY21618

High Efficiency, 28V Input Single Inductor Synchronous Step Up/Down Regulator

General Description

The SY21618 is a high voltage Buck-boost converter for USB power delivery applications. With user-selectable source mode and sink mode, it features bidirectional power delivery. In source mode, the output voltage V_{VBUS} can be controlled in 0.1V per step from 3.6V to 21V. In sink mode, the output voltage V_{BAT} is adjustable with an external resistor divider. The four integrated low $R_{DS(ON)}$ switches minimize the conduction loss.

The SY21618 integrates an I²C compatible interface for mode selecting, output voltage setting, frequency setting, protection setting, and etc.

The device is available in compact QFN5×5-32 package.

Ordering Information

SY21618 □(□,□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY21618QEC	QFN5×5-32	

Features

- Bidirectional Power Delivery: Source Mode and Sink Mode
- 4V to 28V Input Voltage Range
- Low $R_{DS(ON)}$ for Internal Switches: 19mΩ
- Internal soft-start
- Support Interrupt for Status Feedback
- Optional External P-channel FET Driver
- Cable Impedance Compensation
- 8-bit ADC for Output Voltage, Input Voltage and Output Current Detection
- Fully Protected for Output Over Current, Short-circuit and Over-temperature
- I²C Compatible Interface
  - Support Interrupt for Status Feedback
  - Selectable Switching Frequency: 250kHz, 500kHz, 750kHz, 1MHz
  - VBUS Output Voltage can be Configured in 0.1V per Step from 3.6V to 21V
  - Selectable Inductor Current Limit and Output Current Limit
- Compact Package: QFN5×5-32
- UL Certificate Number E491480
- IEC 62368-1 Certified

Applications

- Docking Station
- Laptop
- Power Bank
- Monitor
- USB PD

Typical Application

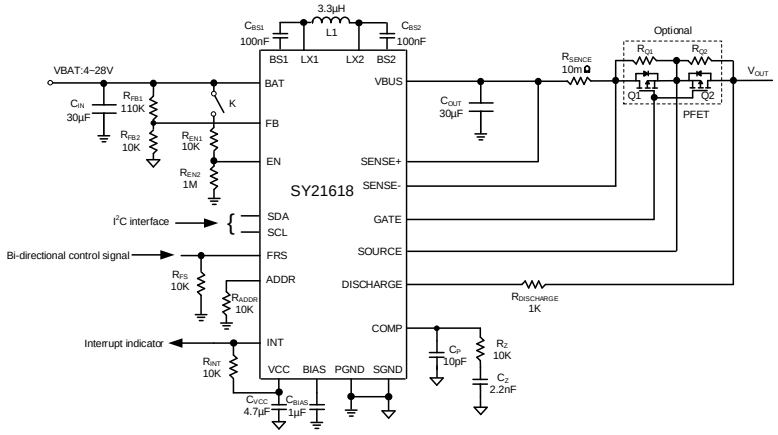
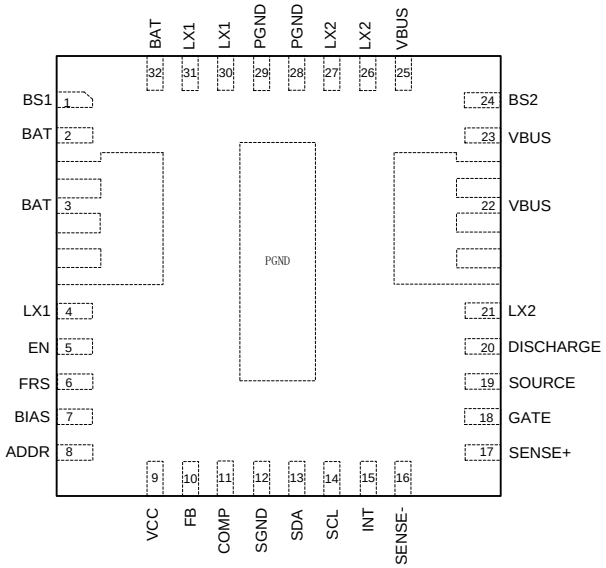


Figure1. Typical Schematic Diagram

Pinout (Top View)



(QFN5×5-32)

Top Mark: BQR*xyz* **(**Device code: BQR, ***x=year code, y=week code, z= lot number code*****)**

Pin Name	Pin Number	Description
BS1	1	Boot-strap pin. Supply high side gate driver. Recommend to connect a 0.1μF ceramic capacitor between this pin and the LX1 pin. Do not connect a resistor in series with the capacitor.
BAT	2,3,32	Power input/output pin, decouple this pin to PGND with at least a 22μF ceramic capacitor. This pin is power input in source mode and power output in sink mode. This pin is also one of the three LDO inputs.
LX1	4 ,30,31	Inductor connection 1.
EN	5	IC Enable control pin, logic high enable. This pin is internally pulled high by 200nA pull-up current.
FRS	6	Fast role swap pin. Once the rising edge is detected, the 'Bidirectional Mode' bit (0x01[4]) is automatically inverted and the 'VBUS Output Voltage Setting' register (0x02) is automatically reset to '0x32'. While the FRS pin is logic high, the 'Bidirectional Mode' bit and 'VBUS Output Voltage Setting' register cannot be changed via the I^2C interface. After the FRS pin is logic low, the I^2C interface resumes normal operation. In bidirectional mode, an external 10kΩ pull-low resistor is recommended. Connect this pin to ground directly if working in source mode only. Do not leave it floating.
BIAS	7	One of the internal VCC LDO's input. BIAS pin is used as the VCC LDO's input when voltage on this pin is within 4V to 6V, otherwise the BAT pin or the SOURCE pin, whichever voltage is higher, is selected as the LDO's input. Decouple this pin to PGND with a minimum of 1μF ceramic capacitor. Leave this pin floating if it is not used.
ADDR	8	The device address set pin. Ground this pin to select 0x70, connect this pin to GND with an external resistor to select 0x71(R_{ADDR}=91kΩ) or 0x72(R_{ADDR}=470kΩ), and float this pin or connect this pin to VCC to select 0x73.

Pin Name	Pin Number	Description
VCC	9	3.3V LDO output, power supply for internal driver and control circuits. Decouple this pin to SGND with a minimum of 1μF ceramic capacitor.
FB	10	V_{BAT} feedback pin. Connect this pin to the center point of the output resistor divider to adjust the BAT voltage in sink mode. $V_{BAT}=1V\times(1+R_{TOP}/R_{BOT})$ Connect this pin to VCC directly if working in source mode only.
COMP	11	Compensation pin. Connect RC network between this pin and SGND.
SGND	12	Signal ground.
SDA	13	I^2C Interface serial data pin. Logic level input/output.
SCL	14	I^2C Interface serial clock pin. Logic level input.
INT	15	The INT pin is an open-drain output. When an interrupt event happens, the INT pin is internally pulled low to inform the host. After the host reads the interrupt register, the INT pin is externally pulled high. A 10kΩ pull-up resistor is recommended.
SENSE-	16	Output current sense “-” input. The regulator also uses this for sensing output voltage.
SENSE+	17	Output current sense “+” input. Recommend to connect a 10mΩ resistor R_{SENSE} between SENSE+ and SENSE- to detect output current.
GATE	18	Gate driver of the external P-channel FET. The use of external PFET is optional, if not used, leave GATE pin floating. The GATE must be activated via the I^2C interface where it can turn on or turn off the PFET. The default state is to have the PFET turned off.
SOURCE	19	The source of external PFET. This pin is also one of the three LDO inputs. If the external PFET is not used, connect this pin to SENSE- directly.
DISCHARGE	20	Output discharge pin. Connect a resistor between this pin and the power output to program the discharge current. The maximum discharge current should be little than 150mA.
LX2	21,26,27	Inductor connection 2.
VBUS	22,23,25	Power input/output pin, decouple this pin to PGND with at least a 22μF ceramic capacitor. This pin is power output in source mode and power input in sink mode.
BS2	24	Boot-strap pin. High side gate driver supply. Recommend to connect a 0.1μF ceramic capacitor between this pin and the LX2 pin. Do not connect a resistor in series with the capacitor.
PGND	28,29 Exposed Pad	Power ground.

Block Diagram:

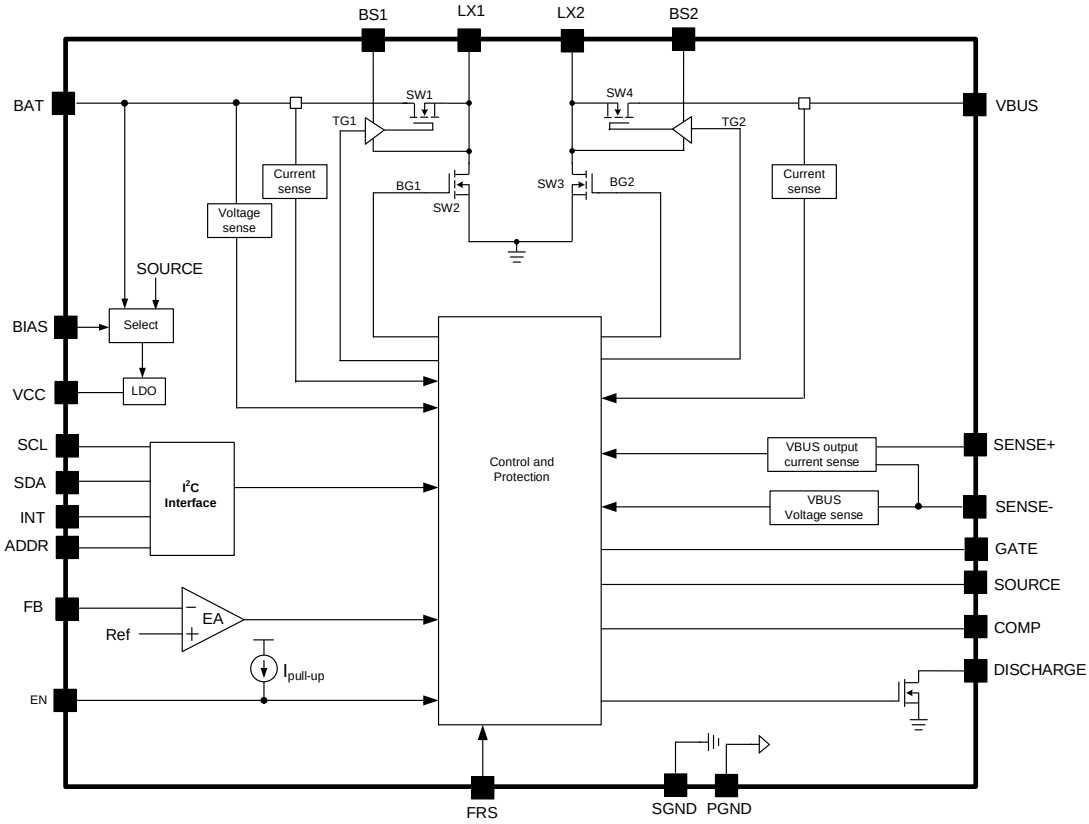


Figure2. Block Diagram

Absolute Maximum Ratings (Note 1)

BAT, LX1, LX2, VBUS, SENSE+, SENSE-, FB, EN, SDA, SCL , DISCHARGE, GATE, SOURCE, FRS, COMP ---------- -0.3V to 30V
BS-LX, ADDR, VCC, INT ---------- -0.3V to 4V
BIAS ---------- -0.3V to 7V
Power Dissipation, P_D @ T_A = 25°C QFN5×5-32 ---------- 3.8W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 26°C/W
θ_{JC} ---------- 2.8°C/W
Junction Temperature Range ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

BAT Voltage ---------- 4V to 28V
VBUS Voltage ---------- 4V to 28V
BIAS Voltage ---------- 4V to 6V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{BAT} = 12V, V_{VBUS}=12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
BAT Voltage Range	V_{BAT}		4		28	V
VBUS Voltage Range	V_{BUS}		4		28	V
VBUS Step Voltage	V_{BUS_STEP}	Source mode		100		mV
BIAS Voltage Range	V_{BIAS}		4		6	V
LDO Voltage	VCC	I_{LDO}=50mA	3.12	3.3	3.46	V
LDO Current Limit	I_{LMT_LDO}	V_{BIAS}=0V	50	85	120	mA
		V_{BIAS}=5V	100	170	240	mA
Quiescent Current	I_Q	No switching		450	650	μA
Shutdown Current	I_{SD}	IC is disabled		5	10	μA
Feedback Reference Voltage	V_{REF}	Sink mode	0.985	1	1.015	V
FB Input Current	I_{FB}		-50		50	nA
VBUS Voltage Set-point	$V_{BUS,SET}$	Source mode, VBUS voltage set 12V, 0x02[7:0]='78'	11.82	12	12.18	V
Output OVP Threshold	$V_{OUT,OVP}$	0x03[4:3]='10'		120		$\%V_{OUT,SET}$
Internal Power MOSFET $R_{DS(ON)}$	$R_{DS(ON)}$			19		mΩ
Inductor Average Current Limit	I_{AVG}	0x04[7:6]='00'		6		A
Inductor Peak Current Limit	I_{PK}	0x04[7:6]='00'	6.8	8.8	11.1	A
VBUS/BAT Input UVLO Threshold	V_{UVLO}		3.3	3.5	3.7	V
UVLO Hysteresis	V_{HYS}			0.2		V
EN Logic High Threshold	V_{ENH}	Rising	1.5			V
EN Logic Low Threshold	V_{ENL}	Falling			0.5	V
Output Current Limit	$V_{OUT.ILIM}$	0x03[7:5]='000'	1	5	9.5	mV
		0x03[7:5]='001'	5	10	14.5	mV
		0x03[7:5]='010'	10	15	19.5	mV
		0x03[7:5]='011'	15	20	24.5	mV
		0x03[7:5]='100'	25	30	34.5	mV
		0x03[7:5]='101'	36	40	44	mV
		0x03[7:5]='110'	46	50	54	mV
		0x03[7:5]='111'	56	60	64	mV
Oscillator Frequency	f_{OSC}	0x01[6:5]='01'	425	500	575	kHz
Min ON Time	t_{ON_MIN}			150		ns
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C
Soft-start Time	t_{SS}	Source mode, V_{VBUS}=5V		1.5		ms
Slew Rate		Source mode, slew rate set 2mV/us		2		mV/μs
Discharge Turn-on Resistance	R_{DISC}			10		Ω
Gate Driver						
GATE Low Clamp		V_{SOURCE}-V_{GATE}		7		V
GATE Sink Current				30		μA
GATE Pull Up Resistance				100		Ω
ADC Control						

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
ADC Resolution				8		Bits
ADC Voltage Sense Accuracy		V_{BAT}=23V	-5		5	%
ADC Current Sense Accuracy		V_{RSENSE}=50mV	-8		8	%
V_{BAT} Full Scale Range			0		25	V
V_{BUS} Full Scale Range			0		25	V
Sense Current Full Scale Range			0		60	mV
I²C Compatible Interface						
Maximum Operating Frequency				400		kHz
SDA and SCL Input Logic Threshold	Logic_L				0.8	V
	Logic_H		2			V
SDA Output Low Voltage		3mA sink current			0.4	V

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a four-layer Silergy evaluation board.

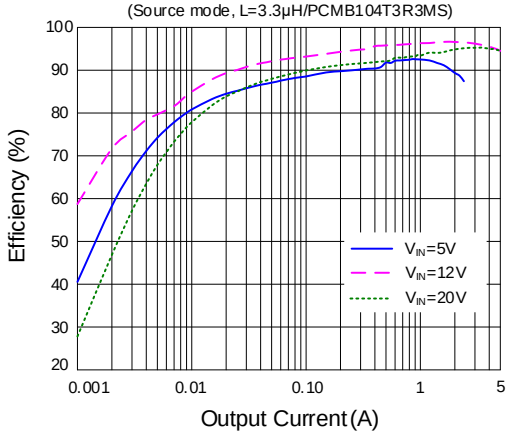
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

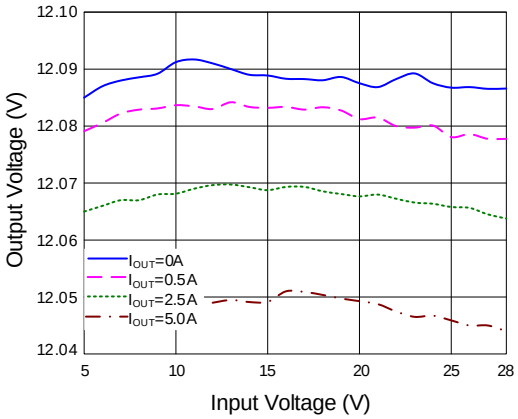
(fsw=500kHz， TA=25°C)

Efficiency vs. Output Current

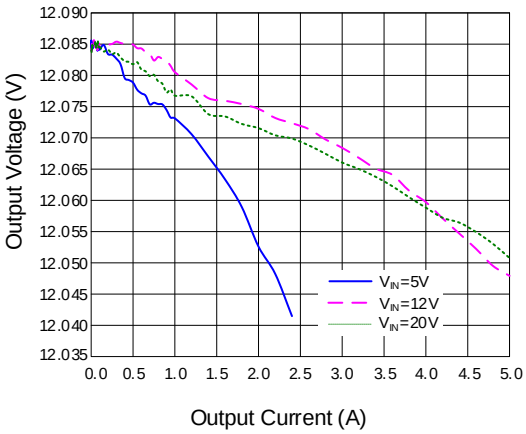
(Source mode, L=3.3μH/PCMB104T3R3MS)



Output Voltage vs. Input Voltage

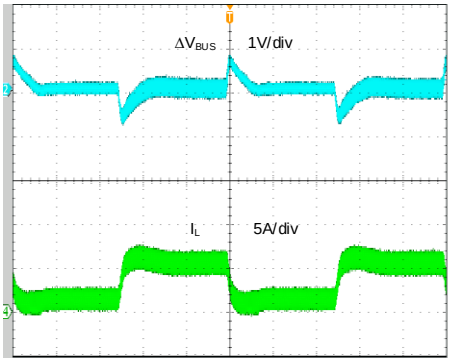


Output Voltage vs. Output Current



Load Transient

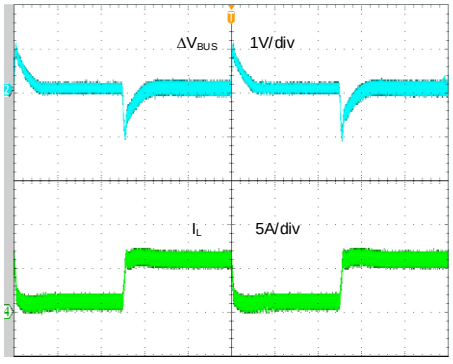
(V_{IN}=5V, V_{OUT}=12V, I_{OUT}=0.5A~2.5A)



Time (200μs/div)

Load Transient

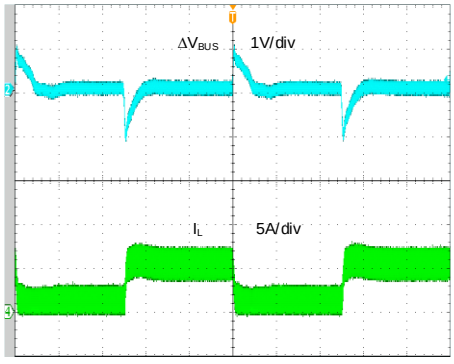
(V_{IN}=12V, V_{OUT}=12V, I_{OUT}=0.5A~5A)



Time (200μs/div)

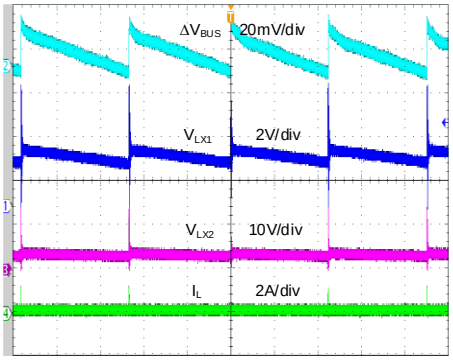
Load Transient

(V_{IN}=20V, V_{OUT}=12V, I_{OUT}=0.5A~5A)



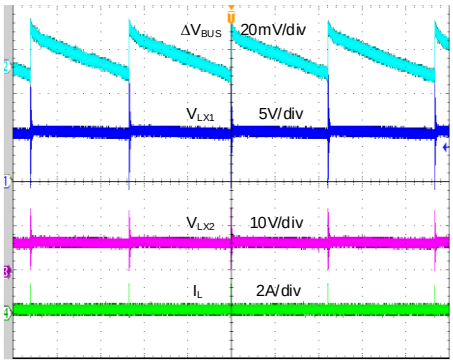
Time (200μs/div)

Output Ripple
(V_{IN}=5V, V_{OUT}=12V, I_{OUT}=0A)



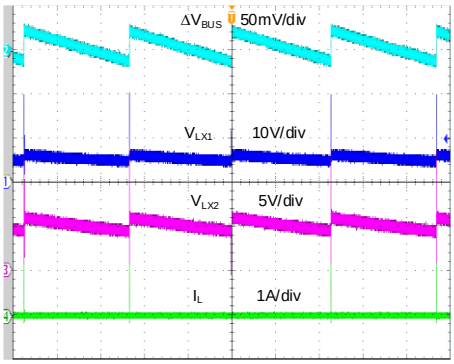
Time (200μs/div)

Output Ripple
(V_{IN}=12V, V_{OUT}=12V, I_{OUT}=0A)



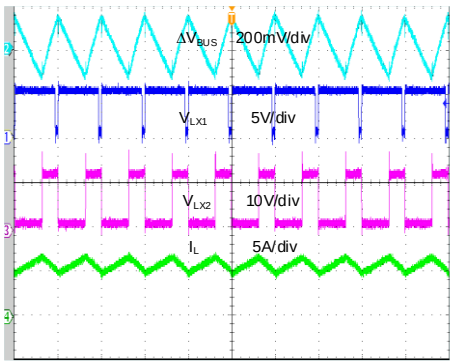
Time (200μs/div)

Output Ripple
(V_{IN}=20V, V_{OUT}=12V, I_{OUT}=0A)



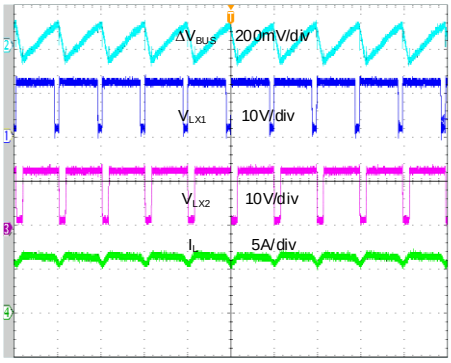
Time (800μs/div)

Output Ripple
(V_{IN}=5V, V_{OUT}=12V, I_{OUT}=2.5A)



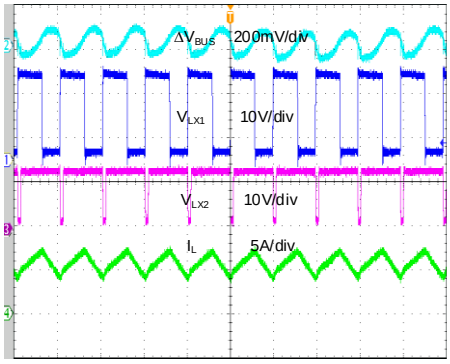
Time (2μs/div)

Output Ripple
(V_{IN}=12V, V_{OUT}=12V, I_{OUT}= 5A)



Time (2μs/div)

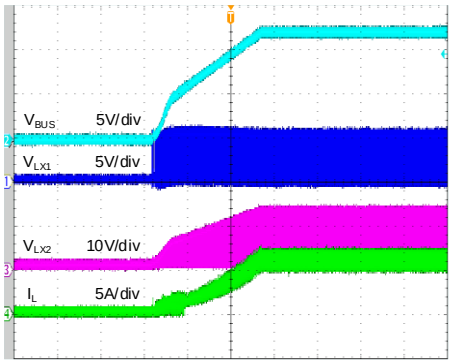
Output Ripple
(V_{IN}=20V, V_{OUT}=12V, I_{OUT}= 5A)



Time (2μs/div)

Start up from Enable

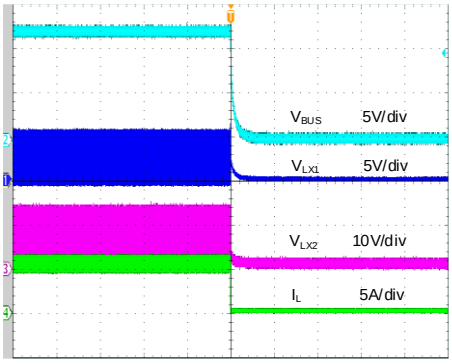
(V_{IN}= 5V, V_{OUT}=12V, I_{OUT}= 2.5A)



Time (2ms/div)

Shutdown from Enable

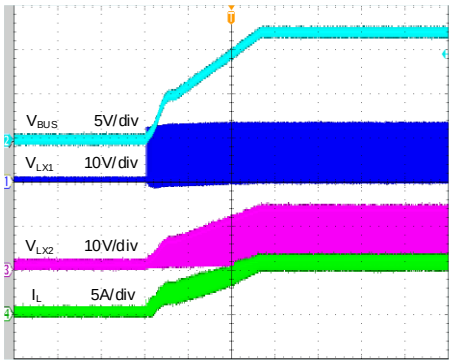
(V_{IN}= 5V, V_{OUT}=12V, I_{OUT}= 2.5A)



Time (2ms/div)

Start up from Enable

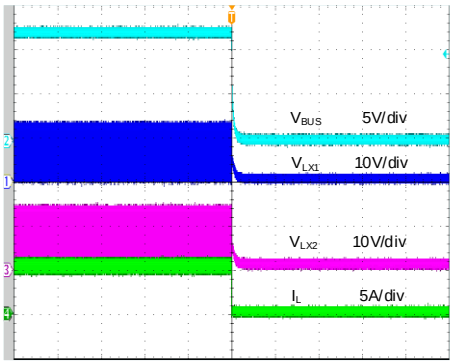
(V_{IN}=12V, V_{OUT}=12V, I_{OUT}= 5A)



Time (2ms/div)

Shutdown from Enable

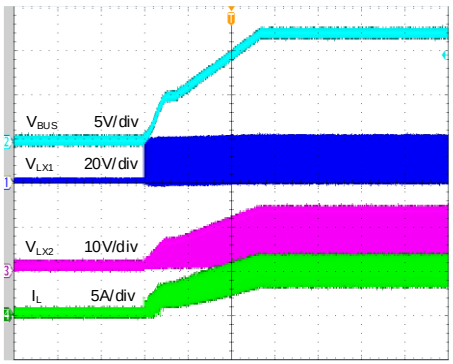
(V_{IN}=12V, V_{OUT}=12V, I_{OUT}= 5A)



Time (2ms/div)

Start up from Enable

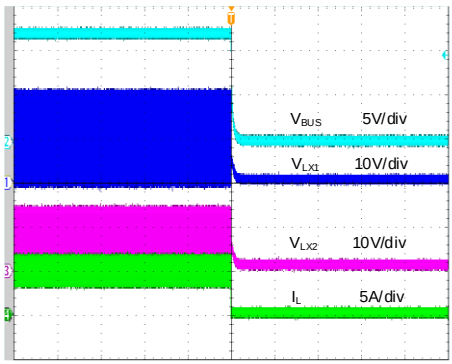
(V_{IN}=20V, V_{OUT}=12V, I_{OUT}= 5A)



Time (2ms/div)

Shutdown from Enable

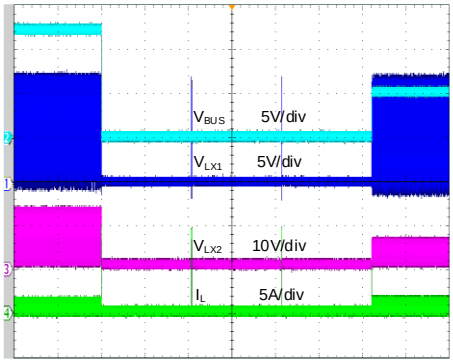
(V_{IN}=20V, V_{OUT}=12V, I_{OUT}= 5A)



Time (2ms/div)

Short Circuit Protection

(V_{IN}=12V, V_{OUT}=12V, I_{OUT}= 0A)



Time (2s/div)

Typical Function Description

I²C Compatible Interface

The SY21618 integrates an I²C compatible interface. To ensure compatibility with a wide range of system processors, the I²C interface supports clock speeds of up to 400 kHz (“Fast-Mode”) and uses standard I²C commands. The SY21618 always operates as a slave device, and is addressed using a 7-bit slave address followed by an 8th bit, which indicates whether the transaction is a read-operation or a write-operation.

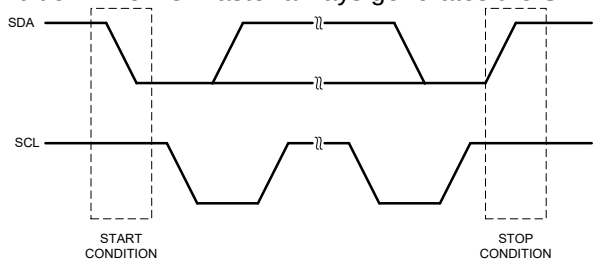
I²C Device Address:

When communicating with multiple devices using the I²C interface, each device must have its own unique address so the host can distinguish between the devices. The most significant 4-bits of the device address is '1110'. The 5th, 6th and 7th-bit device address is selected by ADDR pin.

ADDR	Device Address
ADDR short to GND	1110000
R_{ADDR}=91k	1110001
R_{ADDR}=470k	1110010
ADDR floating or connect to VCC	1110011

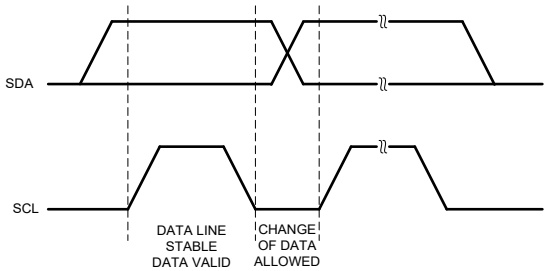
START and STOP Conditions:

The START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition. The I²C master always generates the START and STOP conditions.



Data Validity:

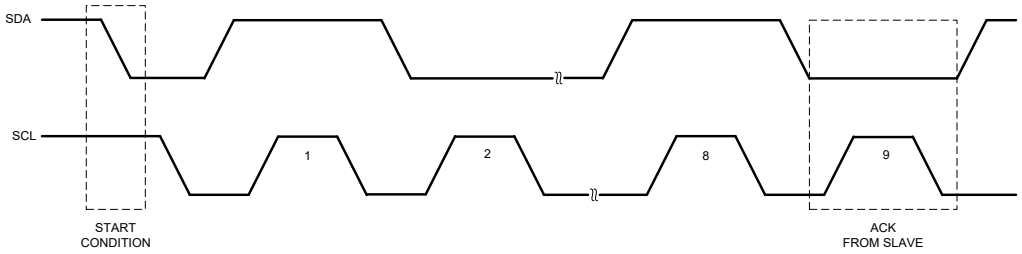
The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.



Acknowledge:

Each address and data transmission uses 9-clock pulses. The ninth pulse is the acknowledge bit (ACK).

After the START condition, the master sends 7-slave address bits and an R/$\overline{W}$ bit during the next 8-clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge. The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data.

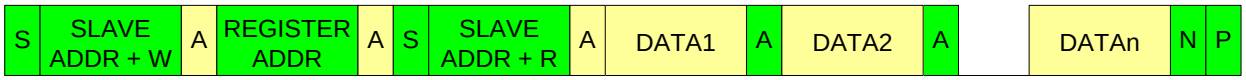


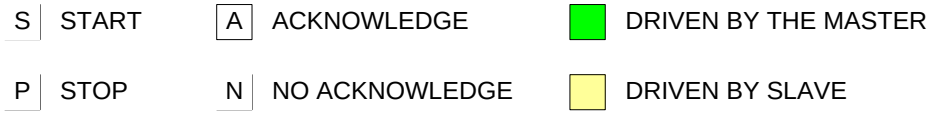
Data Transactions:

All transactions start with a control byte sent from the I²C master device. The control byte begins with a START condition, followed by 7-bits of slave address followed by the R/W bit. The R/W bit is 0 for a write or 1 for a read. If any slave devices on the I²C bus recognize their address, they will acknowledge by pulling the SDA line low for the last clock cycle in the control byte. If no slaves exist at that address or are not ready to communicate, the data line will be 1, indicating a Not Acknowledge condition. Once the control byte is sent, and the slave acknowledges it, the 2nd byte sent by the master must be a register address byte. The register address byte tells the slave which register the master will write or read. Once the slave receives a register address byte it responds with an acknowledge. If a STOP condition is detected after the register address byte is received, the SY21618 takes no further action but storing the register address byte. The register address byte auto increase when multiple date bytes are transited.

Write

Random Read





Register Map:

Address	Data	Note
0x00	Function setting 1	R/W
0x01	Function setting 2	R/W
0x02	VBUS Output Voltage Setting	R/W
0x03	Protection Setting 1	R/W
0x04	Protection Setting 2	R/W
0x05	State Register	R
0x06	INT Register	Read then Clear
0x07	BAT Voltage ADC	R
0x08	VBUS Voltage ADC	R
0x09	Output Current Sense Voltage ADC	R
0x0A	Vender ID	R
0x0B	Version ID	R

Function setting1 (0x00)

Name	# of Bits	Access	Default	Description
Regulator Enable	7	R/W	0	0: Disable 1: Enable
Switching Frequency	6	R/W	0	00: 250KHz 01: 500KHz 10: 750KHz 11: 1MHz
	5	R/W	1	
ADC ON/OFF	4	R/W	0	0:Inactive 1:Active
ADC Detect Mode	3	R/W	0	0: Single detect mode 1:Auto detect mode
Output Discharge ON/OFF	2	R/W	0	0: Active discharge when regulator is disabled 1: Inactive discharge when regulator is disabled
GATE ON/OFF	1	R/W	0	0: Turn off external PMOS 1: Turn on external PMOS
Reserved	0	R/2	0	

Function setting2 (0x01)

Name	# of Bits	Access	Default	Description
Cable Impedance Compensation (source mode)	7	R/W	0	000: R_{CMP} =0mΩ 001: R_{CMP} =50mΩ 010: R_{CMP} =100mΩ 011: R_{CMP} =150mΩ 100: R_{CMP} =200mΩ 101 R_{CMP} =250mΩ 110: R_{CMP} =350mΩ 111 R_{CMP} =500mΩ $V_{CMP} = \frac{R_{SENSE}(m\Omega)}{10m\Omega} \times I_{OUT} \times R_{CMP}$
	6	R/W	0	
	5	R/W	0	
Bidirectional Mode	4	R/W	0	0: Source mode 1: Sink mode If 0x00[7]='0', this bit is reset to '0' and cannot be overwritten
Reserved	3	R/W	0	
Reserved	2:0	R/W	0	

VBUS Output Voltage Setting (0x02)

Name	# of Bits	Access	Default	Description
VBUS Output Voltage Setting (source mode)	7:0	R/W	0x32 (5.0V)	0x00~0x24: 3.6V 0x25: 3.7V 0x26: 3.8V 0x27: 3.9V 0x28: 4.0V 0x29: 4.1V 0x2A: 4.2V 0x2B: 4.3V 0x2C: 4.4V … 0xD2~0xFF:21.0V 0.1V per step, up to 21.0V If 0x00[7]='0',or 0x01[4]='1', this register is reset to '0x32' and cannot be overwritten

Protection setting 1 (0x03)

Name	# of Bits	Access	Default	Description
Output Current Limit	7	R/W	1	000: 5mV 001: 10mV 010: 15mV 011: 20mV 100: 30mV 101: 40mV 110: 50mV 111: 60mV
	6	R/W	1	
	5	R/W	1	
OVP Threshold	4	R/W	1	00:110% 01:115% 10:120% 11:125%
	3	R/W	0	
Slew Rate Selection	2	R/W	1	00: 0.5mV/us 01: 1mV/us 10: 2mV/us 11: 4mV/us
	1	R/W	0	
Reserved	0	R/W	0	

Protection setting 2 (0x04)

Name	# of Bits	Access	Default	Description
Inductor Average Current Limit Setting	7	R/W	0	00: 6A 01: 6A 10: 8A 11: 10A
	6	R/W	0	
UVP Threshold	5	R/W	1	00:50% 01:60% 10:70% 11:80%
	4	R/W	0	

Inductor Average Current Limit Protection Mode	3	R/W	0	0: Latch off: 0x00[7] is reset to '0' 1: Auto recover: 0x02 is reset to '0x32'.
Under Voltage Protection Mode	2	R/W	0	0: Latch off: 0x00[7] is reset to '0' 1: Auto recover: 0x02 is reset to '0x32'.
Over Temperature Protection Mode	1	R/W	0	0: Latch off: 0x00[7] is reset to '0' 1: Auto recover: 0x02 is reset to '0x32'.
Over Voltage Protection Mode	0	R/W	0	0: Latch off: 0x00[7] is reset to '0' 1: Auto recover

State Register (0x05)

Name	# of Bits	Access	Description
Power Good State	7	R	0: Power is not in good range 1: Power good (feedback is 90%~110%Vref)
BAT/VBUS Voltage Relation	6	R	0:BAT voltage > VBUS voltage 1: BAT voltage < VBUS voltage
Reserved	5:0	R	

Interrupt Register (0x06)

Name	# of Bits	Access	Description
ADC Data Ready	7	R	0: None 1: Data ready
Output Over Current Limit	6	R	0: Normal 1:Output current OCP
Average Inductor Current Protection	5	R	0: Normal 1: Inductor OCP
Under Voltage Protection	4	R	0: Normal 1:UVP
Over Temperature Protection	3	R	0: Normal 1: OTP
Over Voltage Protection	2	R	0:Normal 1:OVP
Reserved	1	R	
Reserved	0	R	

BAT Voltage ADC (0x07)

Name	# of Bits	Access	Description
BAT Voltage Value	7:0	R	00000000: 0V …… 11111111: 25V

VBUS Voltage ADC (0x08)

Name	# of Bits	Access	Description
VBUS Voltage Value	7:0	R	00000000: 0V …… 11111111: 25V

Output Current Sense Voltage ADC (0x09)

Name	# of Bits	Access	Description
Output Current Sense Voltage	7:0	R	00000000: 0mV …… 11111111: 60mV

Vender ID (0x0A)

Name	# of Bits	Access	Default	Description
Product	7:4	R	1000	Product code
Vender	3:0	R	0010	Vender code

Version ID (0x0B)

Name	# of Bits	Access	Default	Description
Customer code	7:4	R	0000	0000: special customer 0 0001: special customer 1 0010: special customer 2 …
Revision	3:0	R	0000	0000: ES1 0001: ES2 … 1000: MP

Application Information

Bidirectional Buck-Boost Regulator Operation Mode

The SY21618 is a bidirectional device which can be operated under both source mode and sink mode. 0x01[4]='0' selects source mode while 0x01[4]='1' selects sink mode.

Under source mode, which is also the default mode, the BAT pin is connected to the power input and the VBUS pin is the power output. The output voltage V_{VBUS} is configured by 'VBUS Output Voltage Setting' register (0x02). Once the 'Regulator Enable' bit is cleared (0x00[7]='0'), operation mode will be reset to source mode(0x01[4] is reset to '0' and cannot be overwritten).

Under sink mode, the VBUS pin is connected to the power input, the BAT pin is the power output and the FB pin is the feedback input. The output voltage V_{BAT} is programmed by external voltage divider (see Figure. 3) with the 1V internal voltage reference as given in equation (1)

$$V_{BAT} = 1V \times \frac{R_{TOP} + R_{BOT}}{R_{BOT}} \quad (1)$$

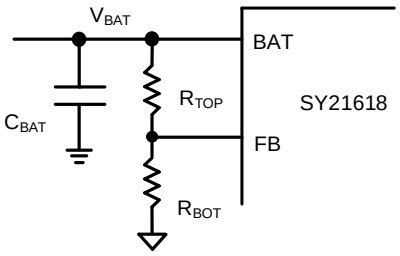


Figure3. Schematic of V_{BAT} under Sink Mode

Fast Role Swap

The SY21618 support fast power role swap to change power path direction by detecting the FRS pin. Once the rising edge is detected, the 'Bidirectional Mode' bit (0x01[4]) is automatically inverted and the 'VBUS Output Voltage Setting' register (0x02) is automatically reset to '0x32'. While the FRS pin is logic high, the 'Bidirectional Mode' bit and 'VBUS Output Voltage Setting' register cannot be changed via the I²C interface. After the FRS pin is logic low, the I²C interface resumes normal operation. In bidirectional mode, an external 10kΩ pull-low resistor is recommended. Connect this pin to ground directly if working in source mode only. Do not leave it floating.

Cable Impedance Compensation

In some applications where cable impedance cannot be ignored, the voltage drop become prominent as the output current increases so that the actual output voltage is smaller than target value. To compensate cable voltage drop, the device incorporates cable impedance compensation function. The regulated output voltage will increase as the output current increases and the relationship is given in equation (2)

$$V_{VBUS} = V_{VBUS\_SET} + \frac{R_{SENSE}(m\Omega)}{10m\Omega} \times I_{OUT} \times R_{CMP} \quad (2)$$

Where R_{CMP} is configured by register 0x01[7:5].

Note: The cable impedance compensation only functions under source mode.

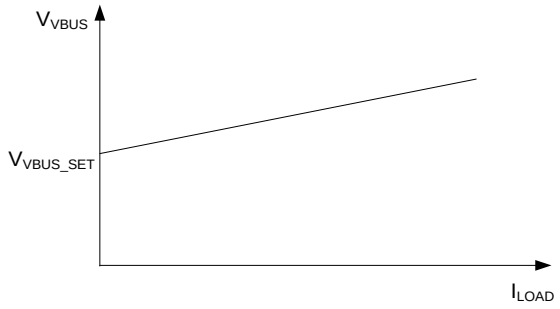


Figure4. Description of Cable Impedance Compensation

Interrupt

When an interrupt event happens, the open drain /INT pin is pulled low to inform the host. After the host reads the interrupt register, the /INT pin will be pulled high by external pull-up resistor.

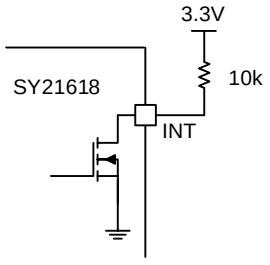


Figure5. Description of Interrupt Function

Under Voltage Protection

The SY21618 activates UVP (under voltage protection) function when output short occurs. There are two UVP protection modes. One is latch

off operation by setting 0x04[2]='0', the other is auto recover operation with 0x04[2]='1'.

1) Latch off operation: Once the output voltage is lower than UVP threshold for 1ms, the regulator will be disabled (0x00[7]='0').

2) Auto recover operation (hiccup mode): When output voltage is lower than UVP threshold for 1ms, then the device will shut down for approximately 4s, and the 'hiccup' on time is about 4ms. If the short circuit condition remains another 'hiccup' cycle of shutdown and restart will continue indefinitely.

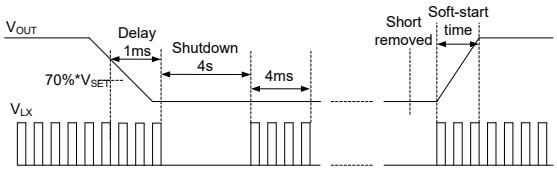


Figure6. Description of UVP Auto Recover Function

Average Inductor current limit

When average inductor current is greater than the current limit threshold, the internal control loop will regulate the average inductor current by decreasing duty cycle. Both latch off operation and auto recover operation are provided by the device: 0x04[3]='0' enters latch off operation, and 0x04[3]='1' enters auto recover operation.

1) Latch off operation: When average inductor current exceeds a certain threshold for 1ms, the regulator is disabled (0x00[7]='0').

2) Auto recover operation: The device will regulate the average inductor current to the setting value. IC resumes normal operation when the fault condition is removed.

Output Current Limit

The SY21618 provides a function for output current limit by sensing the voltage drop between SENSE+ and SENSE- (as shown in figure1). Once the voltage difference (V_{SENSE+}-V_{SENSE-}) exceeds the voltage threshold, which can be configured by register 0x03[7:5], the internal control loop will regulate the output current by decreasing duty cycle until UVP or OTP is triggered.

Note: The output current limit only functions until soft-start time is finished.

Over Temperature Protection

The device provides two protection modes for OTP (over temperature protection). If 0x04[1]='0', it selects latch off operation , and if 0x04[1]='1' , it is auto recover operation.

1) Latch off operation: The regulator is disabled (0x00[7]='0') when the junction temperature exceeds 150℃.

2) Auto recover operation: The regulator stops switching when the junction temperature exceeds 150 ℃ . Once the junction temperature falls below 135℃, the device will resume normal operation.

Output Over-voltage Protection

The device includes output over voltage protection (OVP). If 0x04[0]='0', it selects latch off operation , and if 0x04[0]='1' , it is auto recover operation.

1) Latch off operation: The regulator is disabled (0x00[7]='0') when the output voltage exceeds OVP threshold for 30μs.

2) Auto recover operation: When the output voltage exceeds OVP threshold, the regulator stops switching and turns on the discharge FET until the output voltage drop below OVP threshold.

Device Enable

The internal LDO can be enabled when BAT voltage is above 3.5V and EN voltage is greater than 1.5V, or SOURCE voltage exceeds 3.5V (see Figure7).When the LDO is turned on, then the device can be enabled through I²C interface. To disable the device, it is better to disable the regulator through I²C first, and then the device will automatically turn on discharge FET. After SOURCE voltage falls below 3.5V, and BAT voltage is under 3.5V or EN voltage is lower than 0.5V, the LDO will be turned off to totally disable the device.

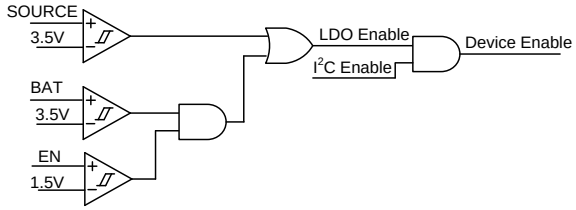
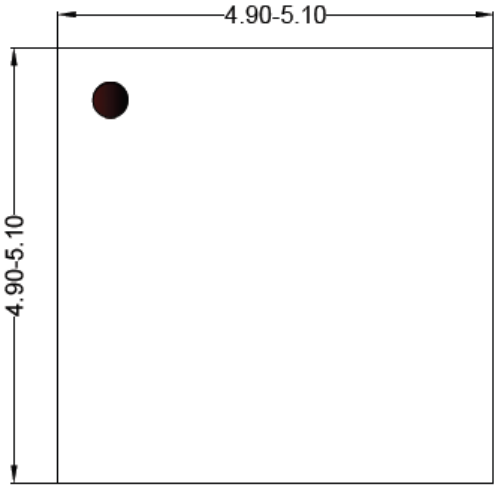
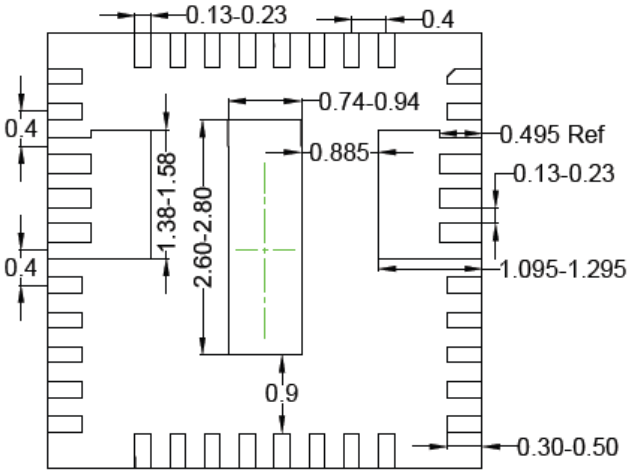


Figure7. Description of IC Enable Function

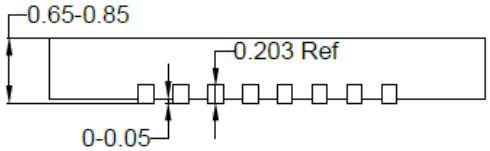
QFN5×5-32 Package Outline & PCB Layout



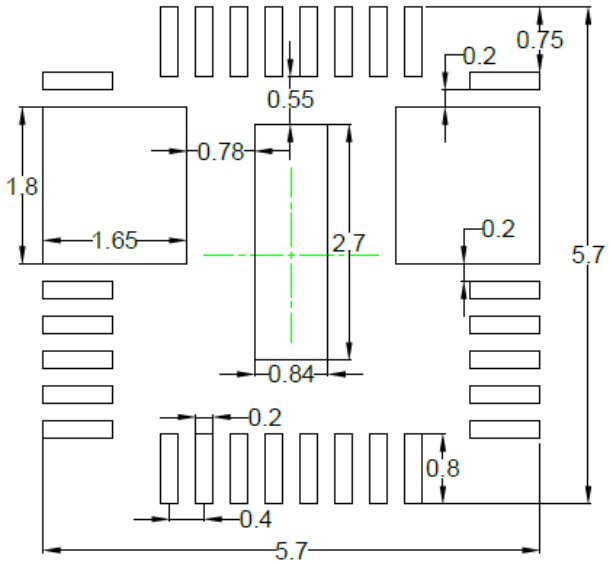
Top View



Bottom View



Side View



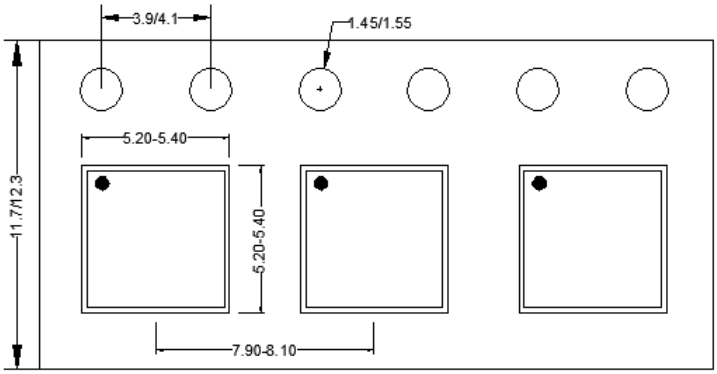
PCB Layout (Recommended)

Notes: 1. All dimension in millimeter and exclude mold flash & metal burr.
2. The center on PCB refers the chip center.

Taping & Reel Specification

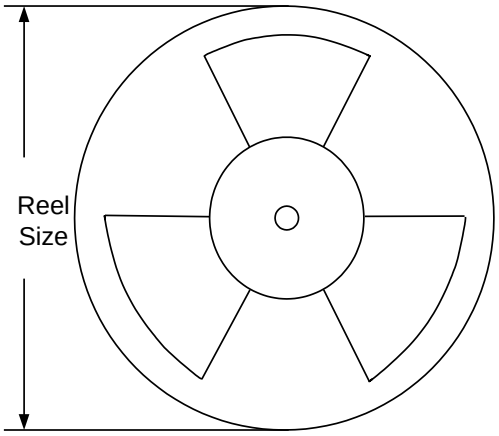
1. Taping Orientation

QFN5×5



Feeding direction ⟶

2. Carrier Tape & Reel Specification for Packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
QFN5×5	12	8	13	400	400	5000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
June 13, 2025	Revision 1.0A	Add the following description to the BS1 pin description and the BS2 pin description (Page2): ---- Do not connect a resistor in series with the capacitor.
Feb.19, 2024	Revision 1.0	Correct clerical errors
Aug.08, 2022	Revision 0.9	Initial Release

IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.

2. Applications. Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.

3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.

4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of a Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

5. **Terms and conditions of commercial sale**. Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at http://www.silergy.com/stdterms, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.

6. **No offer to sell or license**. Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com