SY21525A

20A Quad-Phase Buck Converter

General Description

The SY21525A is a single output, synchronous quad-phase Buck converter. The SY21525A features four integrated power stages and each phase has the capability to deliver up to 5A continuous output current. This flexibility allows the device to work for a wide range of applications where high power is needed.

The SY21525A operates over a wide input voltage range from 2.5V to 5.5V. This device adopts instant PWM control scheme to achieve fast transient response and loop stabilization. And seamless DCM/CCM transitions maximizes efficiency at either heavy load or light load. During start-up and voltage change, the device controls the output slew rate to minimize output voltage overshoot and inrush current.

The SY21525A supplies under voltage lockout, over voltage, over current and over temperature protection to ensure reliable operation of the system.

In addition to the standard interrupt, chip enable, and watchdog reset functions, the SY21525A also supports I^2C communication protocol.

The part is available in a WLCSP 2.66x3.89-54 package. See Family Parts for more detailed information.

Features

- 2.5V to 5.5V Wide Input Voltage Range
- Single Output 4-Phase
- 5A per Phase, 4-Phase total 20A Output Current Capability
- Supports Phase Shedding
- I^2C Programmable Output Voltages from 0.3V to 1.85V
- COT Control Achieves Fast Transient Performance
- ±0.7% Accuracy with Remote Sensing
- Light Load Mode Available
- Support Start-up with Pre-bias Voltage
- Status Feedback with Interrupt Pin
- Reliable OTP/SCP/UVP/OVP Protection
- Compact Package: WLCSP 2.66x3.89-54

Applications

- Smart Phones, Tablets
- FPGA and ASIC Power
- Industrial MPU Power

Ordering Information

SY21525□(□□□)

- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY21525AVCS	WLCSP 2.66x3.89-54	--

Typical Application

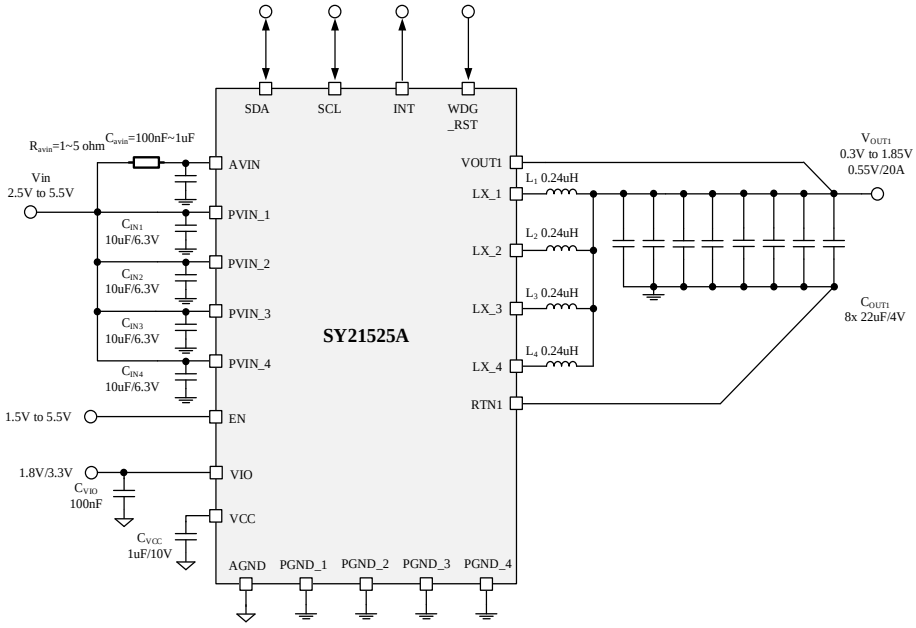


Fig.1 SY21525A: 4-phase single output

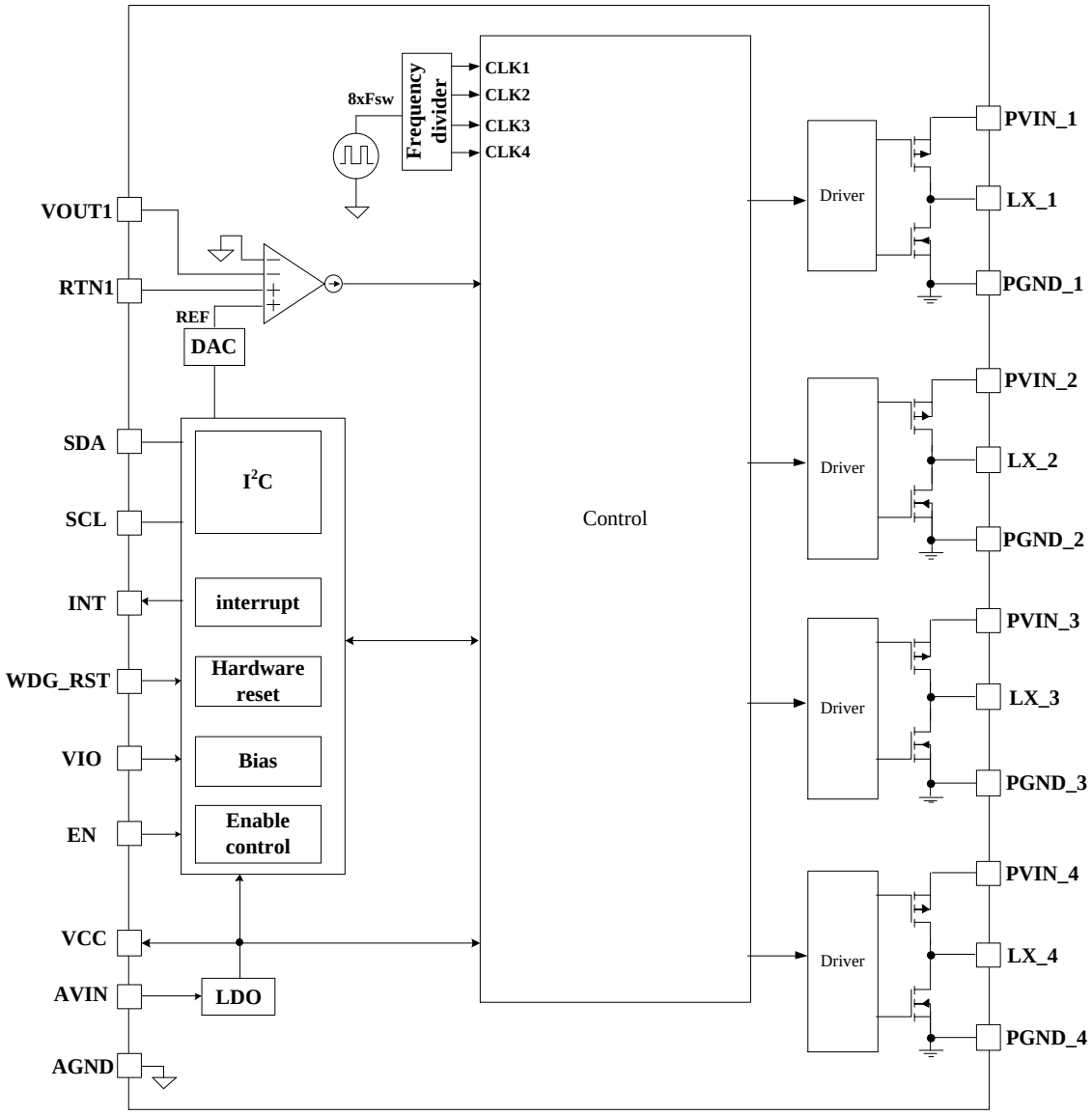
Capacitor Selection

	Part Number	Size	Value / μF	Voltage Rating / V
PVIN Capacitors	GRM188D70J106MA73	0603	10	6.3
VCC Capacitors	GRM155C81A105KA12	0402	1	10
VIO Capacitors	GRM155R71A104MA01	0402	0.1	10
VOUT Capacitors	GRM188C80G226ME15	0603	22	4

Inductor Selection

Part Number	Size	Value / nH	DCR/mΩ	ISAT / A
DFE201610E-R24M	2.0mm*1.6mm*1.2mm	240	16	6.8

Block Diagram



Pin Description

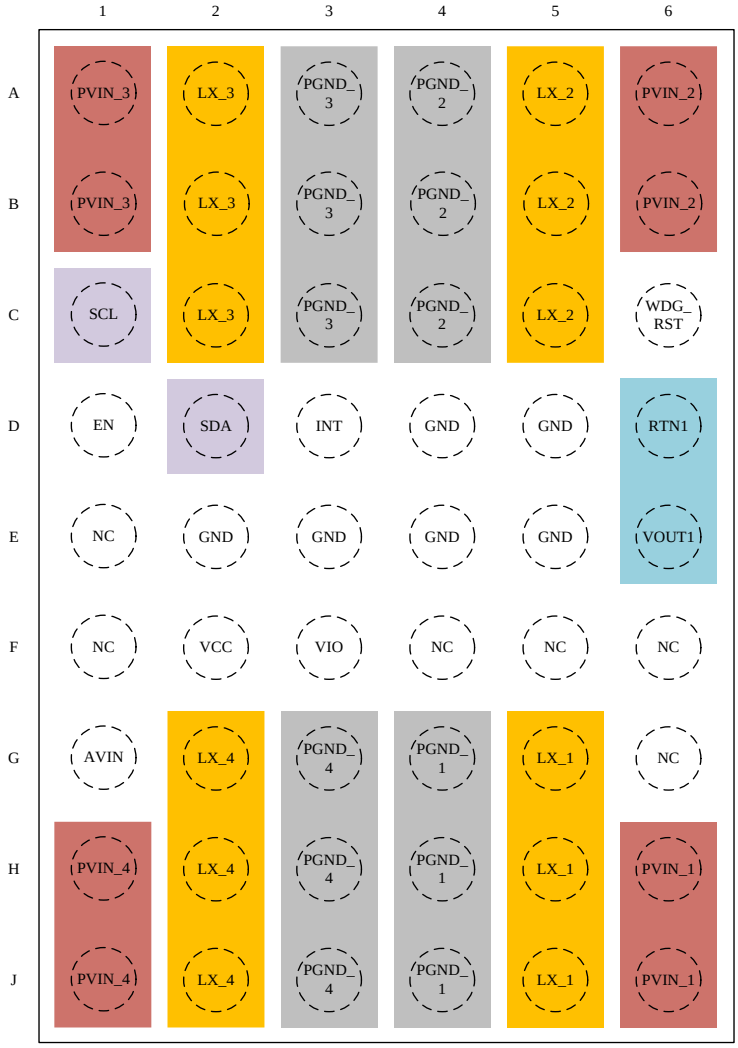


Fig.2 Pin out (Top view)

Top Mark: EAH *xyz* (device code: EAH, ***x=year code, y=week code, z= lot number code)***

Pin Name	Pin Number	Type (Note 1)	Description
PVIN_3	A1, B1	PS	Power supply for Power Stage 3.
LX_3	A2, B2, C2	A/O	Switching node for Power Stage 3.
PGND_3	A3, B3, C3	G	Ground connection for Power Stage 3.
PGND_2	A4, B4, C4	G	Ground connection for Power Stage 2.
LX_2	A5, B5, C5	A/O	Switching node for Power Stage 2.
PVIN_2	A6, B6	PS	Power supply for Power Stage 2.
SCL	C1	D/I	I^2C clock.
WDG_RST	C6	D/I	Digital input, resets the bucks to default output voltage.
EN	D1	D/I	Master chip enable input, NMOS logic threshold.

SDA	D2	D/I/O	I^2C data.
INT	D3	D/O	Interrupt line.
GND	D4, D5, E2 E3, E4, E5	-	Analog chip ground. Ensure that pin D5 has a low impedance connection to the internal ground layer.
NC	E1, F1, F4, F5, F6, G6	-	Not connected.
RTN1	D6	A/I	Remote ground voltage sense for output 1.
VOUT1	E6	A/I	Remote output voltage sense for output 1.
VCC	F2	A/O	Internal 2.7V LDO output, power supply for the internal analog and digital control circuits. Decouple this pin to AGND pin with at least 1μF ceramic capacitor.
VIO	F3	PS	IO supply voltage for digital communications. SDA/SCL should be pull up to VIO voltage with pull up resister. Normally connected to 1.8V/3.3V supply. Decouple this pin to AGND pin with at least 100nF ceramic capacitor, if VIO connect to PVIN, it is better to add RC filter to decrease input ripple voltage.
AVIN	G1	PS	Analog supply voltage, 2.5V to 5.5V. Decouple this pin to AGND pin with at least 100nF ceramic capacitor, if AVIN connect to PVIN, it is better to add RC filter to decrease input ripple voltage.
LX_4	G2, H2, J2	A/O	Switching node for Power Stage 4.
PGND_4	G3, H3, J3	G	Ground connection for Power Stage 4.
PGND_1	G4, H4, J4	G	Ground connection for Power Stage 1.
LX_1	G5, H5, J5	A/O	Switching node for Power Stage 1.
PVIN_4	H1, J1	PS	Power supply connection for Power Stage 4.
PVIN_1	H6, J6	PS	Power supply connection for Power Stage 1.

Note 1: A: Analog Pin, D: Digital Pin, G: Ground Pin, PS: Power Supply Pin, I: Input Pin, O: Output Pin

Absolute Maximum Ratings (Note 1)

PVIN, AVIN---------- -0.3 to 6V
LX---------- -0.3V to PVIN+0.3V
VIO, EN, SCL, SDA---------- -0.3 to AVIN+0.3V
OUT---------- -0.3 to 3V
RTN, GND---------- -0.3 to 0.3V
Other PINs---------- -0.3 to 6V
Junction Temperature ---------- 150°C
Ambient Temperature ---------- -40°C to 105°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature ---------- -65°C to +150°C
Power Dissipation,
PD @ T_A = 25°C WLCSP 2.66x3.89-54---------- 5W
Package Thermal Resistance (Note 2)
θ_{JA}---------- 21°C/W
θ_{JC_TOP} ---------- 2°C/W
Dynamic VDS for HS and LS MOSFET Tested ---------- Down to -2V<40ns
Dynamic VDS for HS and LS MOSFET Tested ---------- Down to -3V <10ns
Dynamic VDS for HS and LS MOSFET Tested ---------- Up to +7V<15ns
Dynamic VDS for HS and LS MOSFET Tested ---------- Up to +8V<5ns
ESD Rating
HBM (Human Body Model) ----------2kV
CDM (Charged Device Model) ---------- 750V
Latch-up ----------200mA

Recommended Operating Conditions (Note 3)

PVIN, AVIN---------- 2.5V to 5.5V
VIO---------- 1.7V to AVIN
Junction Temperature Range ---------- -40°C to 150°C
Ambient Temperature Range ---------- -40°C to 105°C

Electrical Characteristics

(T_A = -40℃~125℃, AVIN/PVIN=3.7V, V_{OUT}=1V, unless otherwise specified)

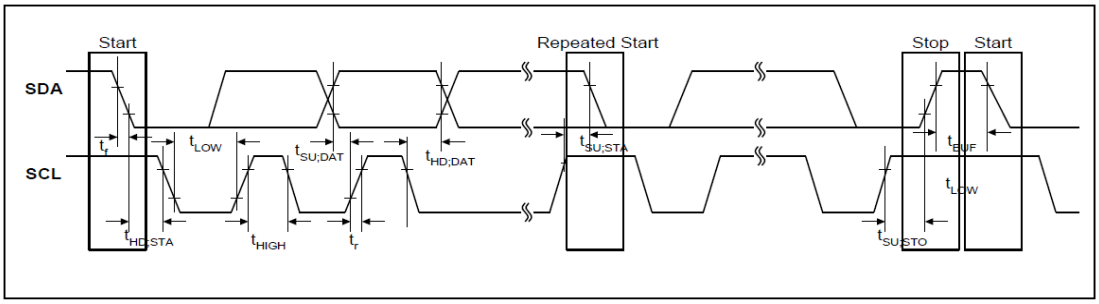
General Characteristics						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
Input Supply						
Supply Voltage	AVIN		2.5		5.5	V
Supply Voltage	PVIN		2.5		5.5	V
AVIN Supply Current	I_Q	EN=0		1.5	2	μA
AVIN + PVIN Supply Current		EN=0		3	6	μA
AVIN + PVIN Supply Current EN=3.3V		All BUCK off (EN bit=0)		42		μA
		No switching, DCM mode		180		μA
UVLO Rising Threshold	V_{UVLOR}	Rising	2.52	2.60	2.67	V
UVLO Falling Threshold	V_{UVLOF}	Falling	2.28	2.34	2.40	V
Input OVP Rising Threshold	V_{OVPR}	Rising	5.684	5.8	5.916	V
Input OVP Falling Threshold	V_{OVPF}	Falling	5.567	5.68	5.794	V
Power Stage						
VOUT Voltage Range	V_{OUT}		0.3		1.85	V
VOUT Step Size	V_{step}	V_{OUT}≤1.3V		5		mV
		V_{OUT}>1.3V		10		mV
VOUT Accuracy	V_{ACC}	CCM, V_{OUT}>0.6V T_A=+25℃	-0.5		0.5	%
		CCM, V_{OUT}>0.6V T_A=-10℃ to +85℃	-0.7		0.7	%
		CCM, V_{OUT}>0.6V T_A=-40℃ to +125℃	-1		1	%
		CCM,V_{OUT}<0.6V T_A=+25℃	-4		+4	mV
		CCM,V_{OUT}<0.6V T_A=-10℃ to +85℃	-5.5		+5.5	mV
		CCM,V_{OUT}<0.6V T_A=-40℃ to +125℃	-8		+8	mV
Current Sharing	I_{match}	4 phase, I_{OUT}=10A,2.5A per phase.			0.5	A
		4 phase, I_{OUT}=15A,3.75A per phase.			0.5	A
		4 phase, I_{OUT}=20A,5A per phase.			0.5	A
DVS Slew Rate Accuracy	V_{DVS}	Default DVS Up=16mV/us Default DVS Down=4mV/us	-15		15	%
Soft Start Slew Rate Accuracy	T_{SS}	Slew Rate=10mV/us	-15		15	%
Switching Frequency	f_{sw}	T_A=25℃	1.8	2	2.2	MHz
		T_A=-40℃ to 125℃	1.7	2	2.3	MHz
Maximum Output Current (Each Phase)	I_{OUT}		5			A
Top FET Ron	$R_{ds(on)\_T}$	PVIN=3.7V		26		mΩ

Bottom FET Ron	$R_{ds(on)\_B}$	PVIN=3.7V		9		mΩ
Output Discharge Resistance	R_{DIS}	Output disabled		125		Ω
Min off time	T_{MIN_OFF}			100		ns
I^2C Turn on Command to output response delay time	T_{I2C_OUT}				100	μs
Protection Characteristics						
High Side Switch Current Limit	I_{PLMT}	T_A=25℃	7.7		9.3	A
		T_A=-40℃ to +125℃	6.8		10.2	A
Low Side Switch Current Limit	I_{VLMT}	T_A=25℃	5.8		7	A
		T_A=-40℃ to +125℃	4.8		8	A
Low Side Switch Negative Current Limit	I_{NLMT}	T_A=25℃	-4.8		-2.4	A
		T_A=-40℃ to +125℃	-5.4		-1.8	A
Thermal Warning Threshold	T_{WN}	Typical=+109℃	-10		10	%
Thermal Warning Hysteresis	T_{WNHYS}	Typical=+15℃	-10		10	%
Thermal Shutdown Temperature	T_{SD}	Typical=+155℃	-10		10	%
Thermal Shutdown Hysteresis	T_{SDHYS}	Typical=+15℃	-10		10	%
Output OVP Threshold	V_{TH_OVP}		116	126	136	$\%V_{SET}$
Output UVP Threshold	V_{TH_UVP}		30	40	50	$\%V_{SET}$
Output OCP Threshold	V_{TH_OCP}		70	80	90	$\%V_{SET}$
IO PINs						
EN						
Low-Level Input Voltage	V_{ENIL}				0.4	V
High-Level Input Voltage	V_{ENIH}		1.2			V
VIO PIN						
Power Supply Voltage			1.7	1.8/3.3	AVIN	V
Supply Current					1	μA
WDG_RST						
Low-Level Input Voltage	V_{RSTIL}				0.3* VIO	V
High-Level Input Voltage	V_{RSTIH}		0.7* VIO			V
SCL, SDA						
Low-Level Input Voltage	V_{I2CIL}				0.3* VIO	V
High-Level Input Voltage	V_{I2CIH}		0.7* VIO			V
Serial Interfaces						
I^2C Frequency Capability	f_{I2C}				3.4	MHz

I^2C Timing Spec table.

Characteristics	Symbol	Units	Standard Mode		Fast Mode		High-Speed Mode	
			Min	Max	Min	Max	Min	Max
Pull-up Voltage	V_{PU}	V	1.7V to VIO					

SCL clock frequency	f_{SCL}	kHz	0 to 100kHz		0 to 400kHz		0 to 3.4MHz	
Hold time (repeated) START condition. After this period,	$t_{HD;STA}$	ms	4		0.6		0.16	
LOW period of the SCL clock	t_{LOW}	ms	4.7		1.3		0.16	
HIGH period of the SCL clock	t_{HIGH}	ms	4		0.6		0.06	
Set-up time for a repeated START condition	$t_{SU;STA}$	ms	4.7		0.6		0.16	
DATA in Hold time	$t_{HD;DI}$	ns	0	900	0	900	0	70
DATA out Hold time	$t_{HD;DO}$	ns	12	900	12	900	12	70
Data set-up time	$t_{SU;DAT}$	ns	250		100		10	
Rise time of both SDA and SCL signals	t_r	ns		1000	5	300	5	40
Fall time of both SDA and SCL signals	t_f	ns		300	5	300	5	40
Set-up time for STOP condition	$t_{SU;STO}$	ms	4		0.6		0.16	
Bus free time between STOP and START conditions	t_{BUF}	ms	4.7		1.3			
Capacitive load for each bus line	C_b	pF		400		400		100



Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C according to JESD51-2 and PCB is built as Silergy EVB. θ_{JC_TOP} is measured according to JESD51-14.

Note 3: The device is not guaranteed to function outside its operating condition.

Description

1 Output Voltage Setting and Dynamic Voltage Scaling (DVS)

1.1 Output Voltage Setting

The output voltage can be programmed by writing an 8-bit register BUCK1_DVS0CFG1. The corresponding output voltage of the DAC code is shown below. For more details, see Register "BUCK1_DVS0CFG1".

Table. 1 DAC code vs. setting Vout

DAC code	Vo/V	DAC code	Vo/V	DAC code	Vo/V	DAC code	Vo/V
0000 0000	0.300	0100 0001	0.625	1000 0010	0.950	1100 0011	1.275
0000 0001	0.305	0100 0010	0.630	1000 0011	0.955	1100 0100	1.280
0000 0010	0.310	0100 0011	0.635	1000 0100	0.960	1100 0101	1.285
0000 0011	0.315	0100 0100	0.640	1000 0101	0.965	1100 0110	1.290
0000 0100	0.320	0100 0101	0.645	1000 0110	0.970	1100 0111	1.295
0000 0101	0.325	0100 0110	0.650	1000 0111	0.975	1100 1000	1.300
0000 0110	0.330	0100 0111	0.655	1000 1000	0.980	1100 1001	1.310
0000 0111	0.335	0100 1000	0.660	1000 1001	0.985	1100 1010	1.320
0000 1000	0.340	0100 1001	0.665	1000 1010	0.990	1100 1011	1.330
0000 1001	0.345	0100 1010	0.670	1000 1011	0.995	1100 1100	1.340
0000 1010	0.350	0100 1011	0.675	1000 1100	1.000	1100 1101	1.350
0000 1011	0.355	0100 1100	0.680	1000 1101	1.005	1100 1110	1.360
0000 1100	0.360	0100 1101	0.685	1000 1110	1.010	1100 1111	1.370
0000 1101	0.365	0100 1110	0.690	1000 1111	1.015	1101 0000	1.380
0000 1110	0.370	0100 1111	0.695	1001 0000	1.020	1101 0001	1.390
0000 1111	0.375	0101 0000	0.700	1001 0001	1.025	1101 0010	1.400
0001 0000	0.380	0101 0001	0.705	1001 0010	1.030	1101 0011	1.410
0001 0001	0.385	0101 0010	0.710	1001 0011	1.035	1101 0100	1.420
0001 0010	0.390	0101 0011	0.715	1001 0100	1.040	1101 0101	1.430
0001 0011	0.395	0101 0100	0.720	1001 0101	1.045	1101 0110	1.440
0001 0100	0.400	0101 0101	0.725	1001 0110	1.050	1101 0111	1.450
0001 0101	0.405	0101 0110	0.730	1001 0111	1.055	1101 1000	1.460
0001 0110	0.410	0101 0111	0.735	1001 1000	1.060	1101 1001	1.470
0001 0111	0.415	0101 1000	0.740	1001 1001	1.065	1101 1010	1.480
0001 1000	0.420	0101 1001	0.745	1001 1010	1.070	1101 1011	1.490
0001 1001	0.425	0101 1010	0.750	1001 1011	1.075	1101 1100	1.500
0001 1010	0.430	0101 1011	0.755	1001 1100	1.080	1101 1101	1.510
0001 1011	0.435	0101 1100	0.760	1001 1101	1.085	1101 1110	1.520
0001 1100	0.440	0101 1101	0.765	1001 1110	1.090	1101 1111	1.530
0001 1101	0.445	0101 1110	0.770	1001 1111	1.095	1110 0000	1.540
0001 1110	0.450	0101 1111	0.775	1010 0000	1.100	1110 0001	1.550
0001 1111	0.455	0110 0000	0.780	1010 0001	1.105	1110 0010	1.560
0010 0000	0.460	0110 0001	0.785	1010 0010	1.110	1110 0011	1.570
0010 0001	0.465	0110 0010	0.790	1010 0011	1.115	1110 0100	1.580
0010 0010	0.470	0110 0011	0.795	1010 0100	1.120	1110 0101	1.590
0010 0011	0.475	0110 0100	0.800	1010 0101	1.125	1110 0110	1.600
0010 0100	0.480	0110 0101	0.805	1010 0110	1.130	1110 0111	1.610
0010 0101	0.485	0110 0110	0.810	1010 0111	1.135	1110 1000	1.620
0010 0110	0.490	0110 0111	0.815	1010 1000	1.140	1110 1001	1.630
0010 0111	0.495	0110 1000	0.820	1010 1001	1.145	1110 1010	1.640
0010 1000	0.500	0110 1001	0.825	1010 1010	1.150	1110 1011	1.650

0010 1001	0.505	0110 1010	0.830	1010 1011	1.155	1110 1100	1.660
0010 1010	0.510	0110 1011	0.835	1010 1100	1.160	1110 1101	1.670
0010 1011	0.515	0110 1100	0.840	1010 1101	1.165	1110 1110	1.680
0010 1100	0.520	0110 1101	0.845	1010 1110	1.170	1110 1111	1.690
0010 1101	0.525	0110 1110	0.850	1010 1111	1.175	1111 0000	1.700
0010 1110	0.530	0110 1111	0.855	1011 0000	1.180	1111 0001	1.710
0010 1111	0.535	0111 0000	0.860	1011 0001	1.185	1111 0010	1.720
0011 0000	0.540	0111 0001	0.865	1011 0010	1.190	1111 0011	1.730
0011 0001	0.545	0111 0010	0.870	1011 0011	1.195	1111 0100	1.740
0011 0010	0.550	0111 0011	0.875	1011 0100	1.200	1111 0101	1.750
0011 0011	0.555	0111 0100	0.880	1011 0101	1.205	1111 0110	1.760
0011 0100	0.560	0111 0101	0.885	1011 0110	1.210	1111 0111	1.770
0011 0101	0.565	0111 0110	0.890	1011 0111	1.215	1111 1000	1.780
0011 0110	0.570	0111 0111	0.895	1011 1000	1.220	1111 1001	1.790
0011 0111	0.575	0111 1000	0.900	1011 1001	1.225	1111 1010	1.800
0011 1000	0.580	0111 1001	0.905	1011 1010	1.230	1111 1011	1.810
0011 1001	0.585	0111 1010	0.910	1011 1011	1.235	1111 1100	1.820
0011 1010	0.590	0111 1011	0.915	1011 1100	1.240	1111 1101	1.830
0011 1011	0.595	0111 1100	0.920	1011 1101	1.245	1111 1110	1.840
0011 1100	0.600	0111 1101	0.925	1011 1110	1.250	1111 1111	1.850
0011 1101	0.605	0111 1110	0.930	1011 1111	1.255		
0011 1110	0.610	0111 1111	0.935	1100 0000	1.260		
0011 1111	0.615	1000 0000	0.940	1100 0001	1.265		
0100 0000	0.620	1000 0001	0.945	1100 0010	1.270		

1.2 DVS

The ramp up slew rate BUCK1_RSPUP[2:0] bits and the ramp down slew rate BUCK1_RSPDN[2:0] bits in the BUCK1_RSPCFG1 register set the slew rates (DVS speed) in BUCK1 during normal DVS transition. For more details, see Register "BUCK1_RSPCFG".

During DVS process, the device has the option to choose full phase mode and auto phase mode. When select full phase operation, all phases will be activated during DVS transition. When select auto phase operation, the converter will follow auto-phase adjustment logic.

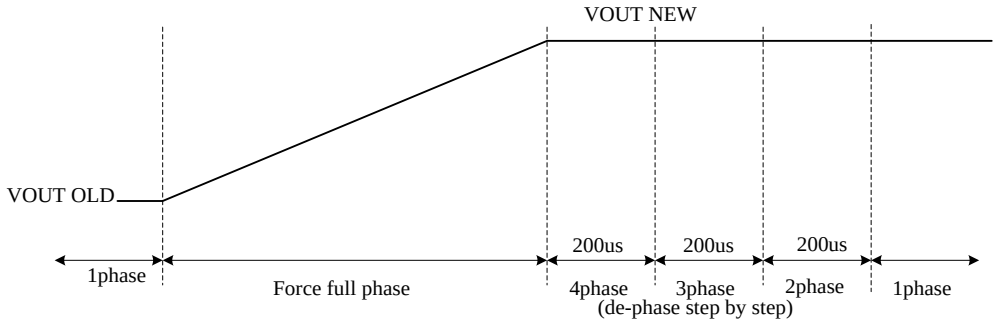


Fig.3 DVS full phase mode

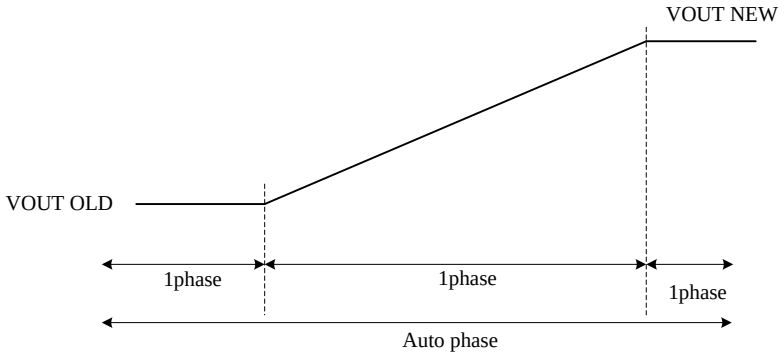


Fig.4 DVS auto phase mode

2 Power Sequencing

2.1 Enable Logic

There are two levels of enabling logic in SY21525A, which go down step by step:

- Global EN pin
- Software EN bit [BUCKx_EN_DVS0] in "BUCK1_DVS0CFG0" Register.

When PVIN rise above UVLO, the Enable Logic happens as the following:

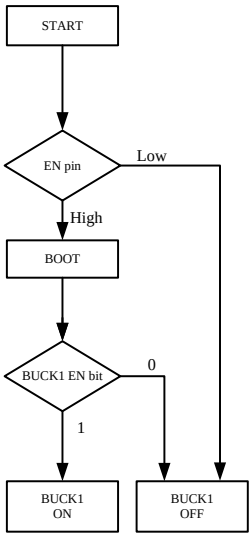


Fig.5 Enable logic

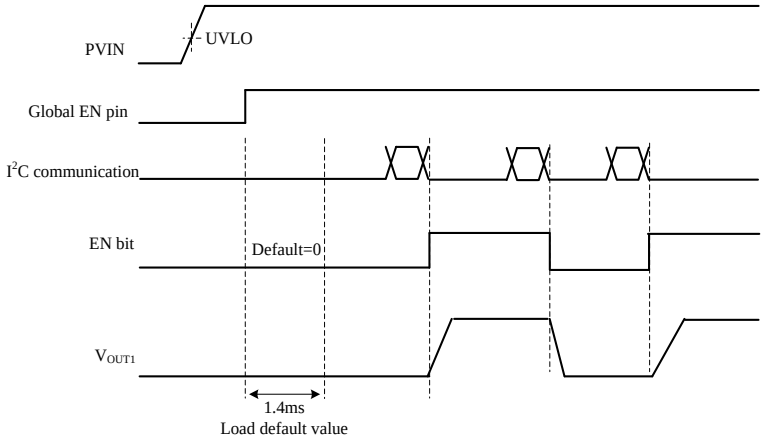


Fig.6 Power up sequencing

2.2 Power-Up Operation

When the global chip Enable (EN) pin is brought above the threshold, the device will power up its key biasing circuits, load the One-Time-Programmable (OTP) configuration registers. And when the turn-on signal is detected, the buck will enter forced CCM mode and all phases will be activated, then it will start a power-up sequence at a specified slew rate. When the output voltage reaches 0.25V, the Phase-Lock-Loop (PLL) begins to work. After the output voltage reaches default value, the auto-phase adjustment logic will be activated, and finally it will work in a specific phase mode, which is determined by the output current level.

The slew rate of each buck during its soft-start can be configured in Register "BUCK1_SLEWCTRL".

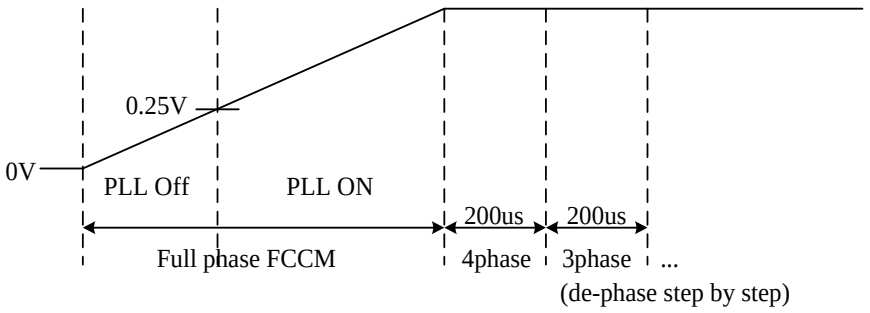


Fig.7 Power-up operation

2.3 Shutdown Operation

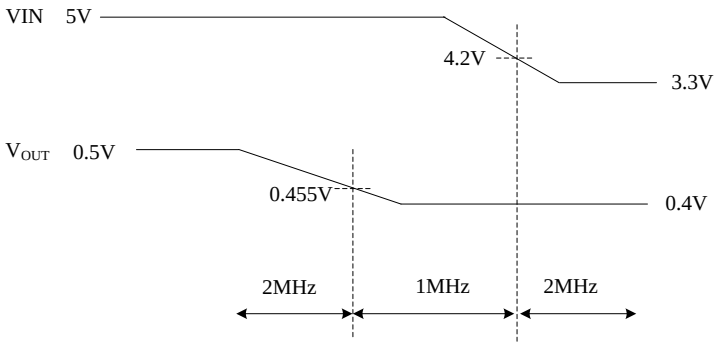
When the turn-off signal is detected, the buck will turn off the high-side switch and turn on the low side switch until the inductor current reach zero.. A discharge resistor can be used to pull down the output and it can be disabled by [VOUT_DISCHARGE_EN] bit in Register "BUCK1_CFG0".

3 PFM/PWM Operation

The converter can be either operated at forced PWM mode or automatic PFM/PWM mode through register "BUCKx_DVS0CFG0". In forced PWM mode, the converter always operates in forced continuous conduction mode even at light load. The advantage is that the converter operates with a fixed frequency that allows simple filtering of the switching frequency for noise-sensitive applications. In this mode, the efficiency is lower than the PFM during light loads. In automatic PFM/PWM mode, the converter operates in regulated frequency PWM mode

at moderate to heavy loads and in the PFM mode during light loads, which maintains high efficiency over a wide load current range.

In order to prevent the interleaving from being out of control due to the minimum on time, the device will decrease frequency from 2MHz to 1MHz when V_{OUT}<0.455V and V_{IN}>4.2V. This is called frequency foldback. Note that the default frequency can be changed by MTP. When the default frequency is 1MHz, the frequency foldback function will be disabled.



4 Watchdog Debounce Time (WDG_RST Pin)

The SY21525A implements a watchdog function which allows the output voltages to return to a safe default value when communication to the processor host is lost. This is determined by monitoring the state of the WDOG_RST pin. If the falling edge is detected, and the low state for a duration is greater than the debounce time (0ms typically), the output voltage setting register (BUCK1_DVS0CFG1 and BUCK1_DVS1CFG1) and the EN bit (BUCK1_EN_DVS0 and BUCK1_EN_DVS1) will be reset to default code. The watchdog reset function can be disabled and the debounce time is also programmable by register "IO_RSTDVS".

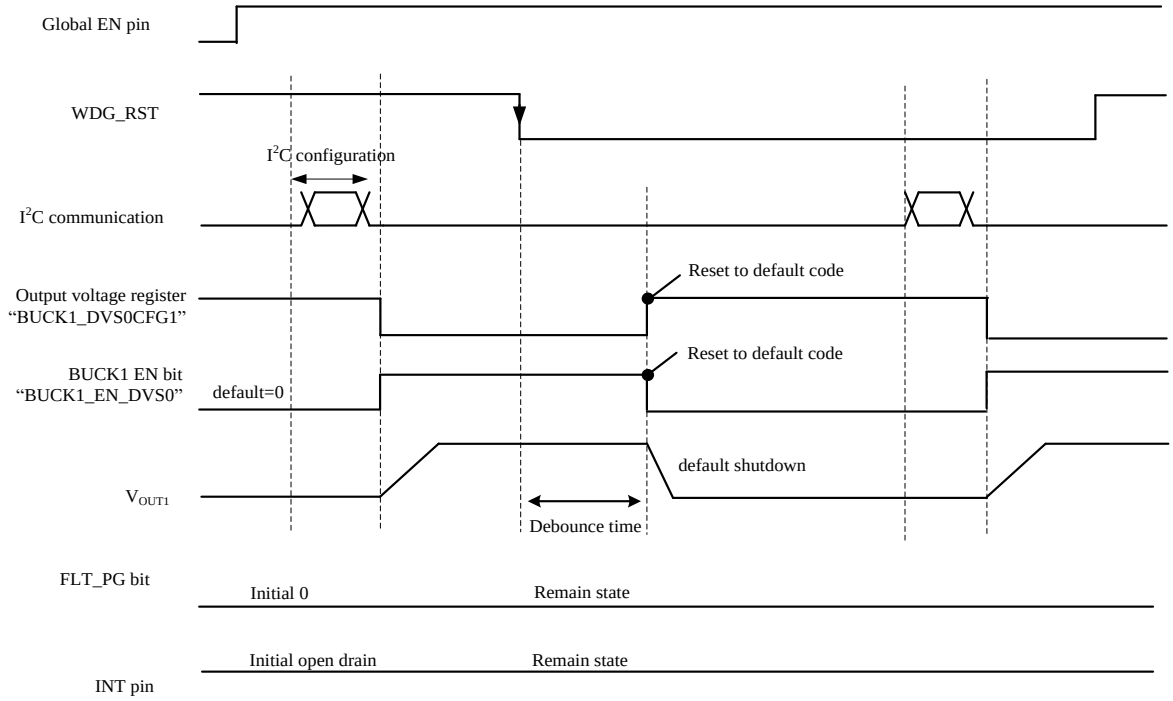


Fig.8 Watch-dog reset function

5 Protection Features

The SY21525A has integrated overcurrent (OC), overvoltage (OV), undervoltage (UV), and over-Temperature (OT) protection features.

Table. 2 protection features

Protection	Threshold	Deglitch time	Operation
Thermal shutdown	Rising: 155℃ Falling: 140℃	-	Controlled by "**FLT_OT_CTRL**" Shutdown when temperature>155℃ Restart when temperature<140℃
Thermal warning	Rising: 109℃ Falling: 94℃	-	Record to thermal warning bit.
OC	80%V_{set}	200μs	Hiccup mode
Output OVP	120%V_{set}	2μs	Stop switching when VOUT>126%Vset Resume switching when VOUT<126%Vset
Output UVP	40%V_{set}	10μs	Select by "**FLT_BUCKx_CTRL**" Latch off or hiccup, default hiccup mode.
Input OVP	5.8V	4μs	Shutdown when VIN>5.8V, restart when VIN<5.68V

5.1 Over-Temperature Protection

The device provides thermal warning function and thermal shutdown protection. If the junction temperature is higher than 109℃, the thermal warning [FLT_TEMP_DIE] bit is be set to 1. The bit can be reset to 0 after I^2C read if the temperature drops below 94℃. The thermal warning function is activated once the global EN pin is pulled high.

As the temperature goes even higher, the device goes into thermal shutdown when the junction temperature exceeds typically 155℃. In this mode, the HS switch and LS switch are turned off. When the junction temperature falls below typically 140℃, the buck is be re-enabled automatically.

The thermal fault detection is activated once the global EN pin is pulled high. The over-temperature protection can be disabled by Register "**FLT_OT_CTRL**".

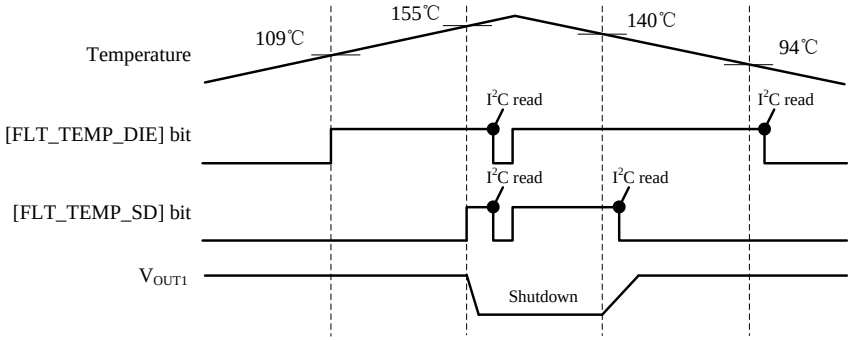


Fig.9 Thermal warning and thermal shutdown

5.2 Over current Protection Mode

The device implements cycle by cycle current limit to protect the device against over current. When the current in the high side MOSFET reaches its current limit, the high side MOSFET is turned off and the low side MOSFET is turned on. The regulator continues to limit the current on a cycle-by-cycle basis. As the load current increases, the output voltage will drop. As soon as the output voltage drops below 80%VSET for a duration of 1ms, the buck will be turned off for 7x soft start time. The buck will then restart. If the over load condition remains the buck will be

turned off for another 7x soft start time. This restart will continue until the over load condition is removed. The OC fault detection is disabled during the normal power up, shut down and DVS period.

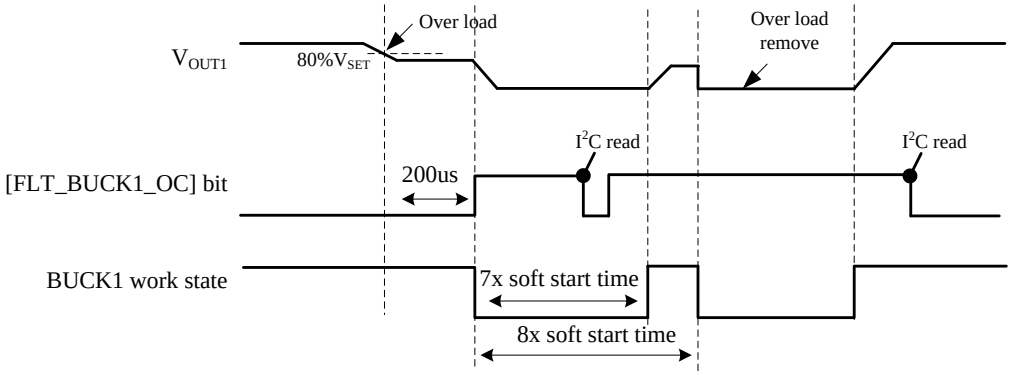


Fig.10 OCP function

5.3 Overvoltage (OV)/Undervoltage (UV) Protection

The SY21525A protects against output overvoltage and undervoltage fault conditions.

When the output voltage reaches 126% V_{SET} for a duration of 10µs, the buck converter will enter no switching mode. Both high side and low side MOSFETS are turned off until the output voltage drops below 126%V_{SET}. The OV fault detection is disabled during the normal power up, shut down and DVS period.

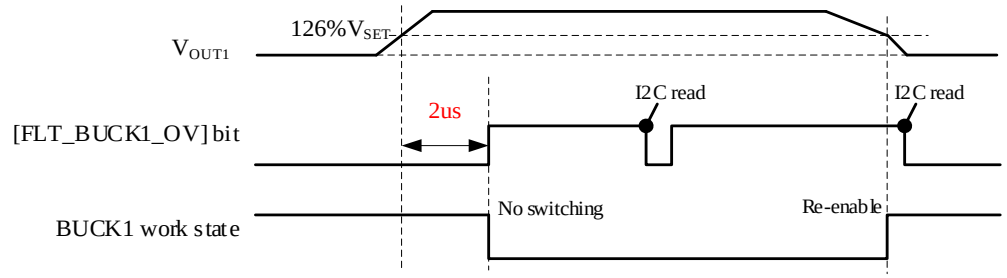
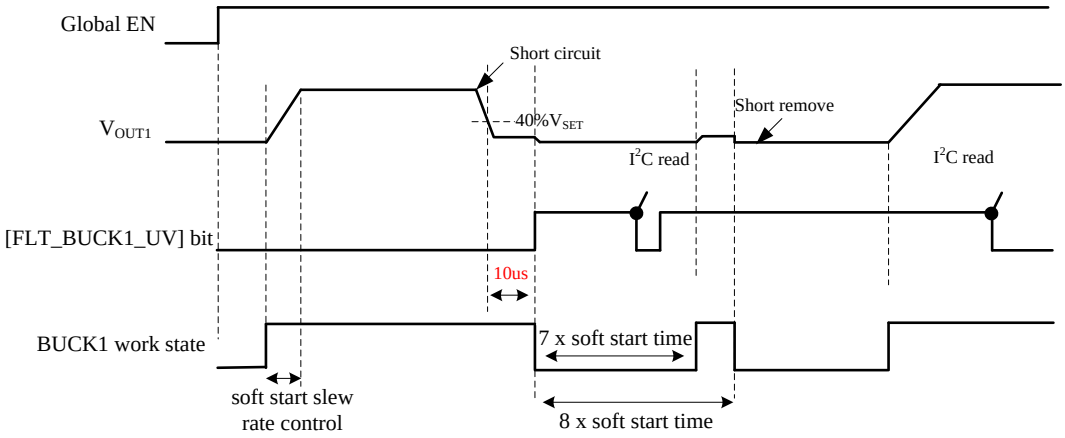
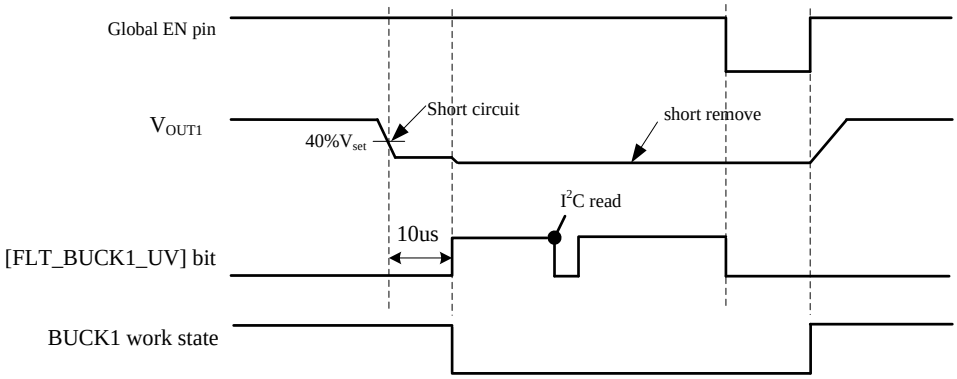


Fig.11 Output OVP function

When the output voltage drops below 60% V_{SET} for 50µs, the buck converter will be turned off. The device provides hiccup and latch off protection modes which is selected by register "**FLT_BUCK1_CTRL**". If latch off mode is selected, the buck converter will not re-enable after UV event. The state can only be cleared by recycling the PVIN/AVIN or by toggling the EN pin. When the UV hiccup mode is selected, the buck will restart after 7x soft start time. The UV fault detection is disabled during the normal power up, shut down and DVS period.



(a) UVP function, hic-cup mode



(b) UVP latch off

Fig.12 UVP function

5.4 Input OVP

The device provides input OVP function to protect the input from overvoltage. When PVIN exceeds 5.8V, the Buck will be turned off. When PVIN decreases to 5.68V, the Buck will restart. The input OV fault detection is activated once the global EN pin is pulled high.

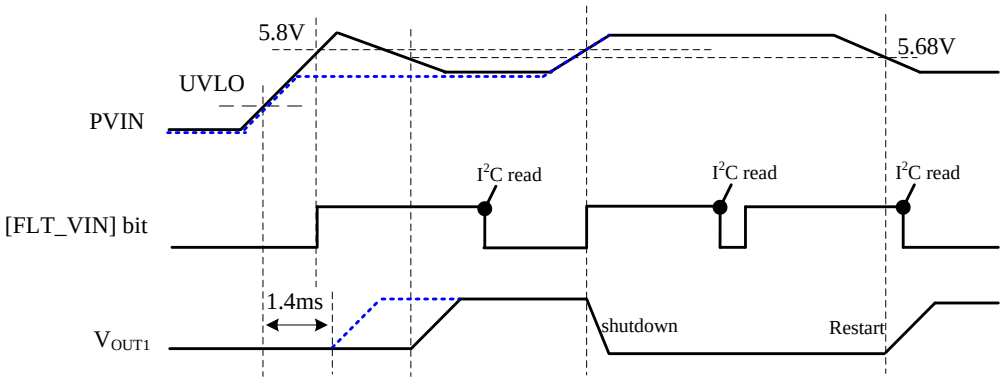


Fig.13. Input OVP function

6 Interrupt

The SY21525A can alert the host when a fault has occurred through an interrupt request signal (IRQ) with configurable masking options through a configurable interrupt (INT) pin. The interrupt pin is set as an active low, open drain output internally.

When a fault occurred, the corresponding fault record bit will be set to 1 until the fault is cleared. When the fault is cleared, the corresponding fault record bit will be set to 0 after read.

When a fault occurred and the corresponding fault record is not masked, the INT pin will be pulled low. And when all the fault record is cleared, the INT pin will be released to open drain. Fig.14 shows the interrupt tree structure.

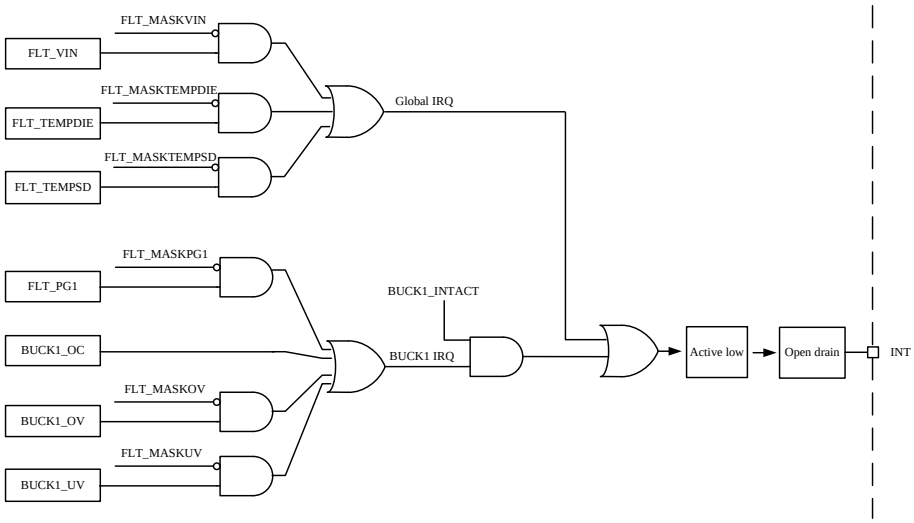


Fig.14 Interrupt tree

6.1 Input OVP Interrupt

The device provide a [FLT_VIN] bit in Register "FLT_RECORDTEMP" to indicate input OVP fault. If the input voltage is higher than OVP threshold, the bit will be set to 1 and pull INT pin to low level. The bit can be reset to 0 after read if the OVP state is cleared. This interrupt can be masked by [FLT_MASKVIN] bit in Register "FLT_MASKTEMP".

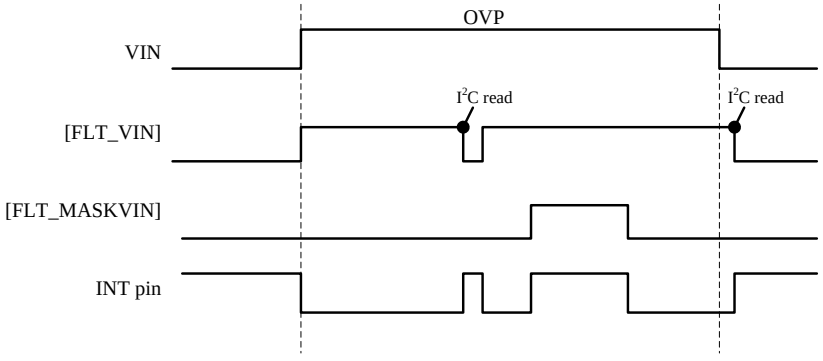


Fig.15 Input OVP interrupt function

6.2 Temperature Interrupt

The device provide a [FLT_TEMP_DIE] bit in Register "FLT_RECORDTEMP" for thermal warning record. If the temperature of the device is higher than 109℃, the bit will set to 1 and pull INT pin to low level. The bit can be reset to 0 after read if the temperature drops below 94℃. This interrupt can be masked by [FLT_MASKTEMP_DIE] bit in Register "FLT_MASKTEMP".

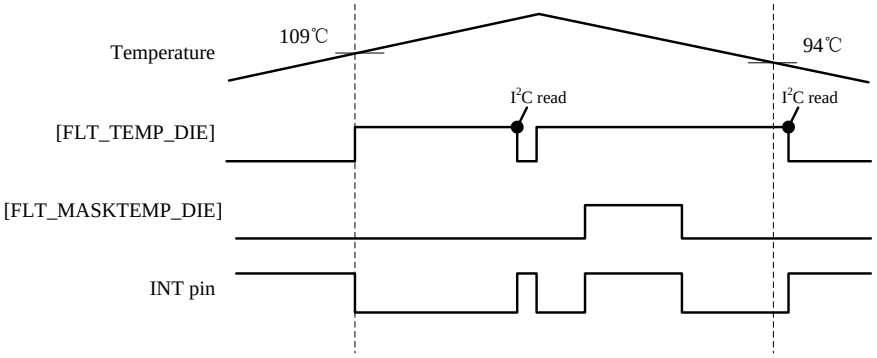


Fig.16 Thermal warning interrupt function

The device also provide a [FLT_TEMP_SD] bit in Register "FLT_RECORDTEMP" for thermal shutdown record. If the junction temperature is higher than 155℃, the bit will set to 1 and pull INT pin to low level. The bit can be reset to 0 after read if the temperature drops below 140℃. This interrupt can be masked by [FLT_MASKTEMP_SD] bit in Register "FLT_MASKTEMP".

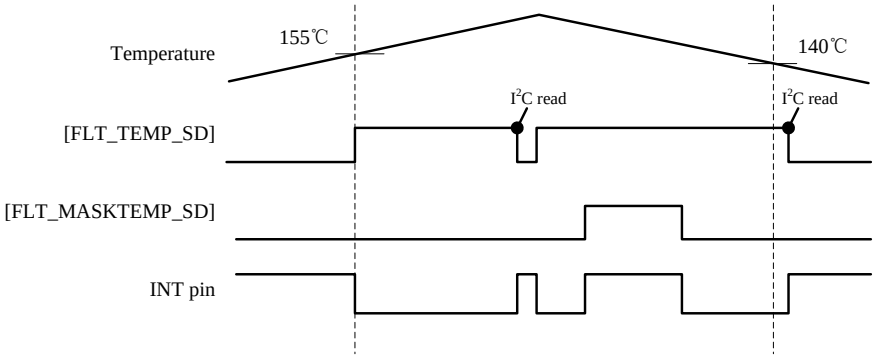


Fig.17 Thermal shutdown interrupt function

6.3 Fault Power Good Interrupt

The device provide a [FLT_PG1] bit in Register "FLT_RECORDBUCK1" to indicate power good state for each buck. If the output voltage is detected between 90%Vset and 110%Vset, the bit will set to 0, and if the output voltage is out of range, the bit will set to 1. The bit can be reset to 0 after read if the not power good state is clear. This interrupt can be masked by [FLT_MASKPG1] bit in Register "FLT_MASKBUCK1".

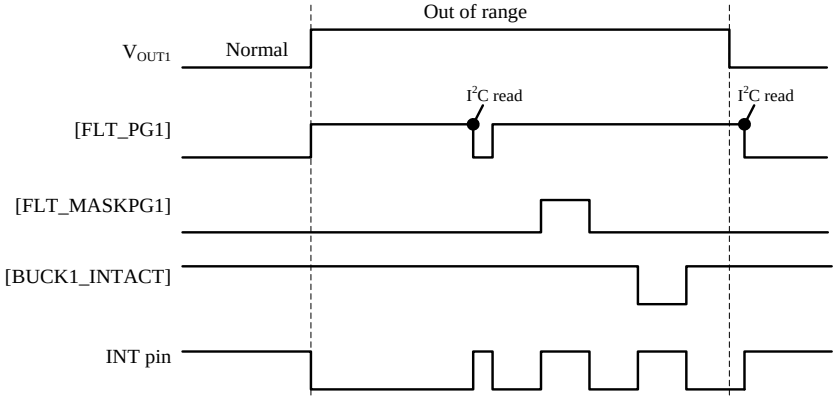


Fig.18 power good interrupt function

6.4 Over Current Interrupt

The device provide a [FLT_BUCK1_OC] bit in Register "FLT_RECORDBUCK1" to indicate over current state. If the over current state is detected, the bit will set to 1. The bit can be reset to 0 after read if the fault state is clear. This interrupt can only be masked by [BUCK1_INTACT] bit in Register "FLT_MASKBUCK1".

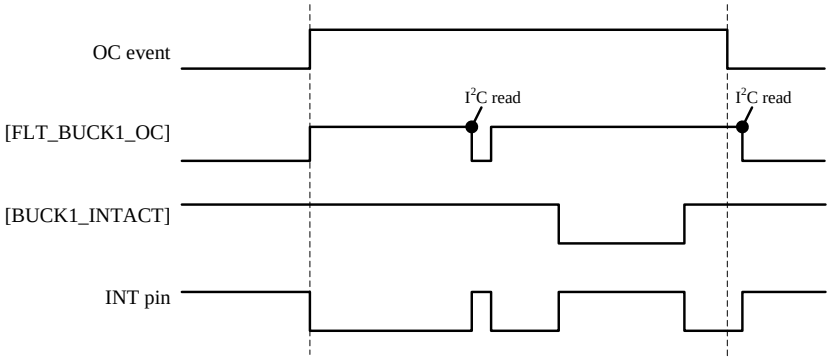


Fig.19 OCP interrupt function

6.5 Over Voltage Interrupt

The device provide a [FLT_BUCK1_OV] bit in Register "FLT_RECORDBUCK1" to indicate over voltage state. If the over voltage state is detected, the bit will set to 1. The bit can be reset to 0 after read if the fault state is clear. This interrupt can be masked by [FLT_BUCK1_MASKOV] bit and [BUCK1_INTACT] bit in Register "FLT_MASKBUCK1".

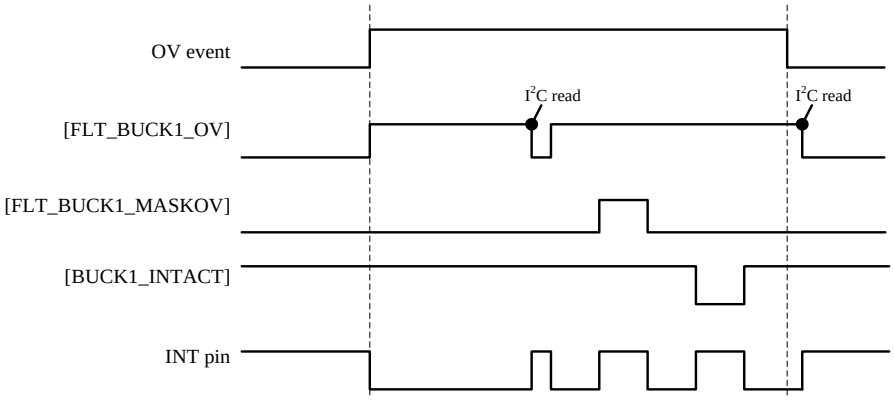


Fig.20 Input OVP interrupt function

6.6 Under Voltage Interrupt

The device provide a [FLT_BUCK1_UV] bit in Register "FLT_RECORDBUCK1" to indicate under voltage state. If the under voltage state is detected, the bit will set to 1. The bit can be reset to 0 after read if the fault state is clear. This interrupt can be masked by [FLT_BUCK1_MASKUV] bit and [BUCK1_INTACT] bit in Register "FLT_MASKBUCK1".

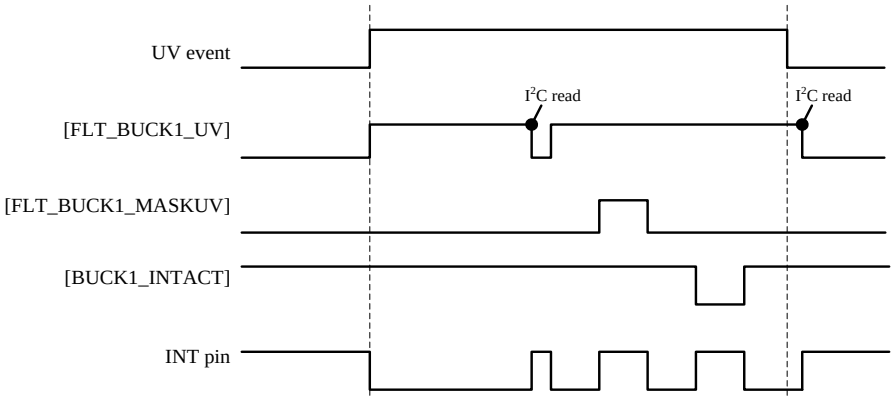


Fig.21 Input UVP interrupt function

6.7 Interrupt Condition During Power Sequencing

The global fault detection (input OVP, thermal warning, thermal shutdown) is activated once the global EN pin is pull high. The buck fault (PG, OC, OV, UV) detection is blocked during the normal power up, shut down and DVS period.

When the buck is turned off by toggling global EN pin, the fault record Registers "FLT_RECORDTEMP" and "FLT_RECORDBUCKx" will be reset to default value.

Shutdown the buck by software EN bit will not change the fault record Registers "FLT_RECORDTEMP" and "FLT_RECORDBUCKx".

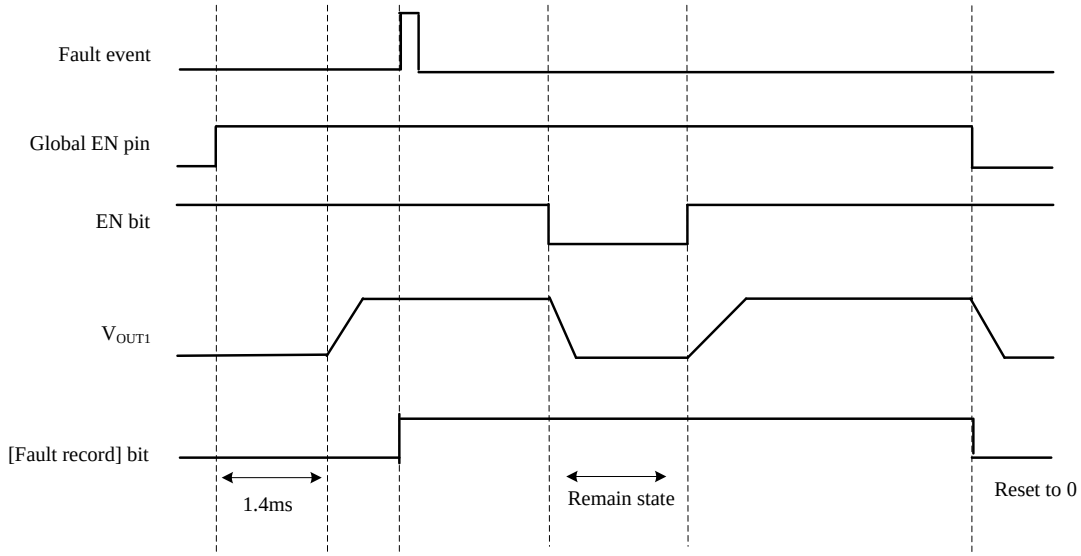


Fig.22 interrupt function during power up sequencing

7 Component Selection Guide

Assume that buck work in CCM and ignore capacitor's ESL, component selection guide is shown below.

7.1 Inductor Selection

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage.

Instant-PWM operates well over a wide range of inductor values. This flexibility allows for optimization to find the best trade-off of efficiency, cost and size for a particular application. Selecting a low inductor value will help reduce size and cost and enhance transient response, but increase peak inductor ripple current, reducing efficiency and increasing output voltage ripple. The low DC resistance (DCR) of these low value inductors may help reduce DC losses and increase efficiency. On the other hand, higher inductor values tend to have higher DCR and will slow transient response.

A reasonable compromise between size, efficiency, and transient response can be determined by selecting a ripple current (Δi_L) about 20% ~ 50% of the desired full output load current of each phase. Start calculating the approximate inductor value by selecting the input and output voltages, the operating frequency (f_S), the maximum output current (I_{omax}) and estimating Δi_L as some percentage of that current.

$$\Delta_{iL} = \frac{Vo}{f_s \cdot L} \cdot (1 - D) = \frac{Vin}{f_s \cdot L} \cdot D \cdot (1 - D)$$

$$iL_{peak} = Io + 0.5\Delta_{iL}$$

Where $D = \frac{Vo}{Vin}$.

The worst case condition is Vout=0.5Vin,and $\Delta_{iL} = \frac{Vin}{4f_s \cdot L}$, $iL_{peak} = I_{omax} + \frac{Vin}{8f_s \cdot L}$.

Select an inductor with a saturation current and thermal rating in excess of iL_{peak}

If FCCM light load operation is selected, make sure the inductor value is high enough to avoid reverse current limit is been triggered just under steady state if the load current is zero.

For highest efficiency, select an inductor with a low DCR that meets the inductance, size and cost targets. Low loss ferrite materials should be considered.

7.2 Inductor Design Example

Consider a typical design for a device providing $1.65V_O$ at 20A output current and 5A each phase from $3.3V_{IN}$, operating at 2MHz and using target inductor ripple current (ΔI_L) of 40% or 2A.

$$\Delta_{iL} = \frac{1.65V}{2MHz \cdot L} \cdot \left(1 - \frac{1.65V}{3.3V}\right) < 2A$$

Conclude from above equation, L>0.206uH.

For the inductor, 0.24uH low ESR inductor is suggested for each phase.

$$\Delta_{iL} = \frac{1.65V}{2MHz \cdot 0.24uH} \cdot \left(1 - \frac{1.65V}{3.3V}\right) = 1.72A$$

$$iL_{peak} = 5A + 0.5 \times 1.72A = 5.29A$$

The resulting 1.72A ripple current is 1.72A/5A is about 34.4%, well within the 20% ~ 50% target.

Finally, select an available inductor with a saturation current higher than the resulting iL_{peak} of 5.29A.

7.3 Input Capacitor Selection

Input filter capacitors are needed to reduce the ripple voltage on the input, to filter the switched current drawn from the input supply and to reduce potential EMI. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating above the system requirements. X5R or X7R series ceramic capacitors are most often selected due to their small size, low cost, surge current capability and high RMS current ratings over a wide temperature and voltage range. However, systems that are powered by a wall adapter or other long and therefore inductive cabling may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{RMS} \approx Io \cdot \sqrt{D \cdot (1 - D)}$$

$$\Delta_{Vin} = \frac{Io}{f_s \cdot Cin} \cdot D \cdot (1 - D) + iL_{max} \cdot ESR$$

Where $Io=I_{load}/4$.

The worst case condition is Vout=0.5Vin, and $\Delta_{Vin} = \frac{0.25Io}{f_s \cdot Cin}$, $I_{RMS} = 0.5Io$.

The capacitance value is less important than the RMS current rating. Take care to locate the ceramic input capacitor as close to the device IN and GND pin as possible.

For the input capacitor, one 10μF low ESR ceramic capacitors are suggested.

7.4 AVIN RC Filter Parameter Selection

The current of V_{IN} capacitor for buck is un-continuous which will generate large ripple voltage. The heavier the load, the larger the ripple voltage. So, it is necessary to add RC filter to decrease AVIN ripple voltage if AVIN connect to PVIN, especially when buck with heavy load. Proper RC filter is good for the stability of PMIC.

R/C parameter should satisfy

$$f_{cutoff} = \frac{1}{2\pi RC} < f_s$$

Generally, a R with 1~5 ohm and C with 0.1uF~1uF MLCC cap is suggested. The heavier of load, the larger of RC.

7.5 Output Capacitor Selection

Instant-PWM provides excellent performance with a wide variety of output capacitor types. Ceramic and POS types are most often selected due to their small size and low cost. Total capacitance is determined by the transient response and output voltage ripple requirements of the system.

$$\Delta_{Vo} = \Delta_{iL}(ESR + \frac{1}{8f_s \cdot C_o})$$

For the output capacitor, two 22µF low ESR ceramic capacitors are suggested for each phase, then totally 8 pcs 22uF output cap.

Consider a typical application with Δ_{iL} = 1.72A using eight 22µF ceramic capacitors, each with an ESR of 6mΩ for parallel total of 176µF and 0.75mΩ ESR, capacitor DC rating 29% at 1.65V.

$$\Delta_{Vo} = 1.72A \times \left(0.75m\Omega + \frac{1}{8 \times 2MHz \times 176uF \times 71\%}\right) = 2.15mV$$

7.6 Output Transient Undershoot/Overshoot

If very fast load transient must be supported, consider the effect of the output capacitor on the output transient undershoot and overshoot. Instant-PWM responds quickly to changing load conditions, however, some considerations must be needed, especially when using small ceramic capacitors which have low capacitance at low output voltages which results in insufficient stored energy for load transient. Output transient undershoot and overshoot have two causes: voltage changes caused by the ESR of the output capacitor and voltage changes caused by the output capacitance and inductor current slew rate.

ESR undershoot or overshoot may be calculated as $V_{ESR}=\Delta I_O \times ESR$. Using the ceramic capacitor example above and a fast load transient of ±16A, V_{ESR} = ±16A × 0.75mΩ = ±12mV.

Capacitive undershoot (load increasing) is a function of the output capacitance, the load step, the inductor value and the input-output voltage difference and the maximum duty factor. During a fast load transient, the maximum duty factor of instant-PWM is a function of t_{on} and the minimum t_{off} as the control scheme is designed to rapidly ramp the inductor current by grouping together many t_{on} pulses in this case. The maximum duty factor D_{max} may be calculated by

$$D_{max} = \frac{t_{on}}{t_{on}+t_{off,min}}$$

Given this, the capacitive undershoot may be calculated by

$$V_{undershoot} = -\frac{L \cdot \Delta I_O^2}{2C_o \cdot (V_{in,min} \cdot D_{max} - V_o)}$$

Consider a 16A load increase using the ceramic capacitor case when V_{IN} = 3.3V. At V_O = 1.65V, the result is t_{on} = 400ns, $t_{off,min}$ = 100ns, D_{max} = 400 / (400 + 100) =0.8 and capacitor DC rating 29% at 1.65V.

$$V_{undershoot} = -\frac{(\frac{0.24uH}{4}) \times (16A)^2}{2 \times 71\% \times 176uF \cdot (3V \times 0.8 - 1.65V)} = 82mV$$

In fact, t_{on} can be extended to longer and D_{max} larger, the load transient performance will be better than the calculated value.

Capacitive overshoot (load decreasing) is a function of the output capacitance, the inductor value and the output voltage.

$$V_{overshoot} = \frac{L \cdot \Delta I_O^2}{2C_o \cdot V_o}$$

Consider a 4A load decrease for each phase using the ceramic capacitor case above. At V_O = 1.65V the result is

$$V_{overshoot} = \frac{4\times0.24uH\times(4A)^2}{2\times71\%\times176uF\times1.65V} = 37.2mV$$

Combine the ESR and capacitive undershoot and overshoot to calculate the total overshoot and undershoot for a given application.

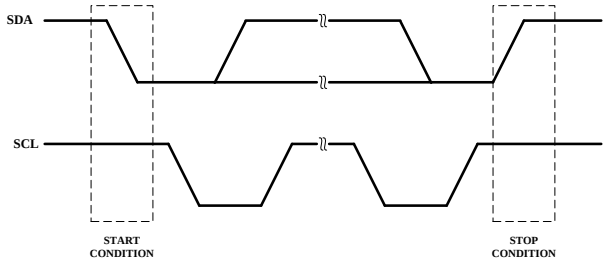
I²C Communication Interface

I²C interface is a simple, bidirectional 2-wire bus protocol, consisting of the Serial Clock Control (SCL) and the Serial Data Signal (SDA). The SY21525A hosts a slave I²C interface that supports data speeds up to 3.4Mbps. SCL is an input to the SY21525A and is supplied by the controller, whereas SDA is bidirectional. The SY21525A has an open-drain output to transmit data on SDA. An external pull-up resistor must be placed on the serial data line to pull the drain output high during data transmission.

The default address of the SY21525A is set to 0x1D(0011101x) by a one-time programmable fuse.

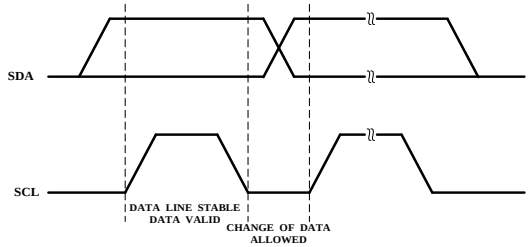
1 START and STOP Conditions

The device is controlled via an I²C compatible interface. The START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition. The I²C master always generates the START and STOP conditions.



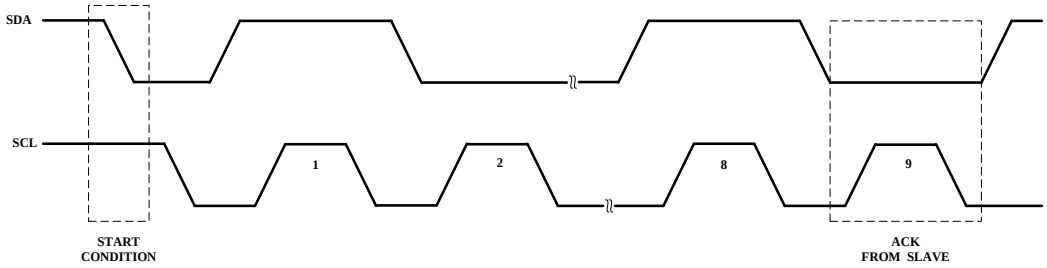
2 Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.



3 Acknowledge

Each address and data transmission uses 9-clock pulses. The ninth pulse is the acknowledge bit (ACK). After the START condition, the master sends 7-slave address bits and an $R/\overline{W}$ bit during the next 8-clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge. The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data.



4 Data Transactions

All transactions start with a control byte sent from the I²C master device. The control byte begins with a START condition, followed by 7-bits of slave address (0011101x) for the Device, this address can be changed if necessary) followed by the 8th bit, R/$\overline{W}$ bit. The R/$\overline{W}$ bit is 0 for a write or 1 for a read. If any slave devices on the I²C bus recognize their address, they will acknowledge by pulling the SDA line low for the last clock cycle in the control byte. If no slaves exist at that address or are not ready to communicate, the data line will be 1, indicating a Not Acknowledge condition. Once the control byte is sent, and the device acknowledges it, the 2nd byte sent by the master must be a register address byte. The register address byte tells the device which registers the master will write or read. Once the device receives a register address byte it responds with an acknowledge.

Write To A Register

S	SLAVE ADDR + W	A	REGISTER ADDR	A	DATA	A	P

Read From A Register

S	SLAVE ADDR + W	A	REGISTER ADDR	A	S	SLAVE ADDR + R	A	DATA	N	P

S	START	A	ACKNOWLEDGE		DRIVEN BY THE MASTER
P	STOP	N	NO ACKNOWLEDGE		DRIVEN BY THE SLAVE

Register Map

1 Register address map

No.	Address	Register
1	0x01	IO_CHIPNAME
2	0x02	IO_CHIPVERSION
3	0x0F	IO_SOFTRESET
4	0x13	FLT_RECORDTEMP
5	0x14	FLT_RECORDBUCK1
6	0x22	IO_I2CCFG
7	0x25	IO_RSTDVS
8	0x30	FLT_OT_CTRL
9	0x32	FLT_MASKTEMP
10	0x33	FLT_MASKBUCK1
11	0x37	FLT_BUCK1_CTRL
12	0x3E	BUCK1_RAMP
13	0x42	BUCK1_CFG0
14	0x48	BUCK1_DVS0CFG1
15	0x49	BUCK1_DVS0CFG0
16	0x4A	BUCK1_DVS1CFG1
17	0x4B	BUCK1_DVS1CFG0
18	0x54	BUCK1_RSPCFG
19	0x55	BUCK1_SLEWCTRL

2 Register description

IO_CHIPNAME				
Register Address:		0x01		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:0	11111111	CHIPNAME	R	Manufacturer Identification

IO_CHIPVERSION				
Register Address:		0x02		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:0	00000000	CHIPVERSION	R	Version Number Identification

IO_SOFTRESET				
Register Address:		0x0F		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:1	0000 000	-	-	-
0	0	SOFTRESET	R/W	Reset All Registers and Reload from OTP: 0: Do nothing 1: Reset and bit cleared

FLT_RECORDTEMP				
Register Address:		0x13		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	FLT_VIN	R	VIN OVP Occurred Record (cleared when read) 0: No fault, less than threshold. 1: Fault, greater than threshold, send interrupt request.
6:3	0000	-	-	-
2	0	FLT_TEMP_DIE	R	Over-Temperature Record For Die (109℃) (cleared when read) 0: No fault, less than threshold. 1: Fault, greater than threshold, send interrupt request
1	0	FLT_TEMP_SD	R	Over-Temperature Shutdown Record (155℃) (cleared when read) 0: No fault, less than threshold. 1: Fault, greater than threshold, send interrupt request
0	0	-	-	-

FLT_RECORDBUCK1				
Register Address:		0x14		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	FLT_PG1	R	Output Good For BUCK1 (cleared when read) 0: 110% V_{set} > VOUT1 > 90% V_{set}. 1: VOUT1 is out of range, send interrupt request
6	0	FLT_BUCK1_OC	R	Overcurrent For BUCK1 (cleared when read) 0: No fault, less than threshold. 1: Fault, greater than threshold, send interrupt request
5	0	FLT_BUCK1_OV	R	Overvoltage For BUCK1 (cleared when read) 0: No fault, less than threshold. 1: Fault, greater than threshold, send interrupt request
4	0	FLT_BUCK1_UV	R	Under Voltage For BUCK1 (cleared when read) 0: No fault, less than threshold. 1: Fault, greater than threshold, send interrupt request
3-0	0000	-	-	-

IO_I2CCFG				
Register Address:		0x22		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	Reserved		
6:0	001 1101	I2C_ADDRESS	R	I^2C device address setting, programmed by factory.

IO_RSTDVS				
Register Address:		0x25		
Bits	**Default**	**Signal Name**	**R/W**	**Description**

<table>
<tr><td>7:5</td><td>11</td><td>-</td><td>R/W</td><td>-</td></tr>
<tr><td>4</td><td>1</td><td>IO_RSTDVS_CTRL</td><td>R/W</td><td>Enable/disable Buck1 watchdog reset function
0: Disable
1: Enable</td></tr>
<tr><td>3</td><td>0</td><td>--</td><td>R/W</td><td>-</td></tr>
<tr><td>2:0</td><td>000</td><td>IO_DEBOUNCETIME</td><td>R/W</td><td>Delay before start reset DVS when WDG_RST pin is asserted
<table>
<tr><td></td><td>Delay time/ms</td></tr>
<tr><td>000</td><td>0 (default)</td></tr>
<tr><td>001</td><td>1.56</td></tr>
<tr><td>010</td><td>3.125</td></tr>
<tr><td>011</td><td>6.25</td></tr>
<tr><td>100</td><td>12.5</td></tr>
<tr><td>101</td><td>9</td></tr>
<tr><td>110</td><td>15.25</td></tr>
<tr><td>111</td><td>14.5</td></tr>
</table></td></tr>
</table>

FLT_OT_CTRL				
Register Address:		0x30		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:4	0000	-	-	-
3	0	FLT_OT_CTRL	R/W	Over temperature shutdown mode 0: Shutdown and auto recover 1: Do nothing
2:0	000	-	-	-

FLT_MASKTEMP				
Register Address:		0x32		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	FLT_MASKVIN	R/W	Mask IRQ for VIN OVP 0: Pass IRQ to INT pin. 1: Mask IRQ.
6:3	000	-	-	-
2	0	FLT_MASKTEMP_DIE	R/W	Mask IRQ for hot die 0: Pass IRQ to INT pin. 1: Mask IRQ
1	0	FLT_MASKTEMP_SD	R/W	Mask IRQ for thermal shutdown 0: Pass IRQ to INT pin. 1: Mask IRQ
0	0	-	-	-

FLT_MASKBUCK1				
Register Address:		0x33		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	FLT_BUCK1_MASKPG	R/W	Mask IRQ for FLT_PG1 0: Pass IRQ to INT pin. 1: Mask IRQ
6	0	BUCK1_INTACT	R/	Enable or disable Buck1 INT function

			W	0: Disable 1: Enable Default value metal change available
5	0	FLT_BUCK1_MASKOV	R/W	Mask IRQ for FLT_BUCK1_OV 0: Pass IRQ to INT pin. 1: Mask IRQ
4	0	FLT_BUCK1_MASKUV	R/W	Mask IRQ for FLT_BUCK1_UV 0: Pass IRQ to INT pin. 1: Mask IRQ
3:0	0000	-	-	-

FLT_BUCK1_CTRL				
Register Address:		0x37		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:4	0000	-	-	-
3	1	FLT_BUCK1_CTRL	R/W	Protection mode for UV 0: UV Shutdown 1: UV Hic-cup
2:0	000	-	-	-

BUCK1_RAMP				
Register Address:		0x3E		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	-	-	-
6	1	FCCM_DVS_UP	R/W	Work mode when DVS up 0: Auto phase 1: Full phase FCCM
5:3	00 0	-	-	-
2	1	FCCM_DVS_DN	R/W	Work mode when DVS down 0: Auto phase 1: Full phase FCCM
1:0	00	-	-	-

BUCK1_CFG0				
Register Address:		0x42		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:1	0000 000	-	-	-
0	1	VOUT_DISCHARGE_EN	R/W	Enable discharge resistor when shutdown 0:.Disable 1: Enable

BUCK1_DVS0CFG1				
Register Address:		0x48		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:0	0x8C	BUCK1_DVS0	R/W	8-bit DAC[7:0] value to generate VOUT for DVS Configuration 0.

DAC	Vo/V	DAC	Vo/V

				0000 0000	0.300	1100 1001	1.310
				0000 0001	0.305	1100 1010	1.320
				…	…	…	…
				1100 0111	1.295	1111 1110	1.840
				1100 1000	1.300	1111 1111	1.850

BUCK1_DVS0CFG0				
Register Address:		0x49		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:6	00	-	-	-
5	1	BUCK1_DVS0MODE	R/W	Buck1 DVS0 work mode 0: Automatic PFM/PWM 1: Forced PWM
4:1	0000	-	-	-
0	0	BUCK1_EN_DVS0	R/W	Enable or disable Buck1 DVS0 0: Disable, V_{OUT1}=0 1: Enable

BUCK1_DVS1CFG1				
Register Address:		0x4A		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:0	0x8C	BUCK1_DVS1	R/W	8-bit DAC[7:0] value to generate VOUT for DVS Configuration 0.

DAC	Vo/V	DAC	Vo/V
0000 0000	0.300	1100 1001	1.310
0000 0001	0.305	1100 1010	1.320
…	…	…	…
1100 0111	1.295	1111 1110	1.840
1100 1000	1.300	1111 1111	1.850

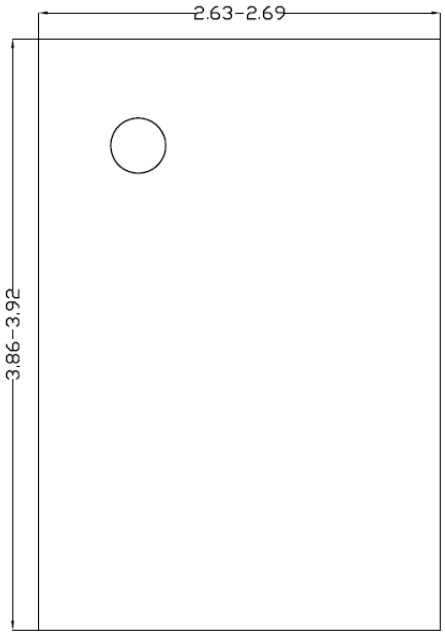
BUCK1_DVS1CFG0				
Register Address:		0x4B		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:6	00	-	-	-
5	1	WORK_MODE	R/W	BUCK1 DVS1 work mode 0: Automatic PFM/PWM 1: Forced PWM
4:1	0000	-	-	-
0	0	BUCK1_EN_DVS1	R/W	Enable or disable Buck1 DVS1 0: Disable, V_{OUT1}=0 1: Enable

BUCK1_RSPCFG				
Register Address:		0x54		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	-	-	-
6:4	001	BUCK1_RSPUP	R/	DVS up slew rate mV/μs

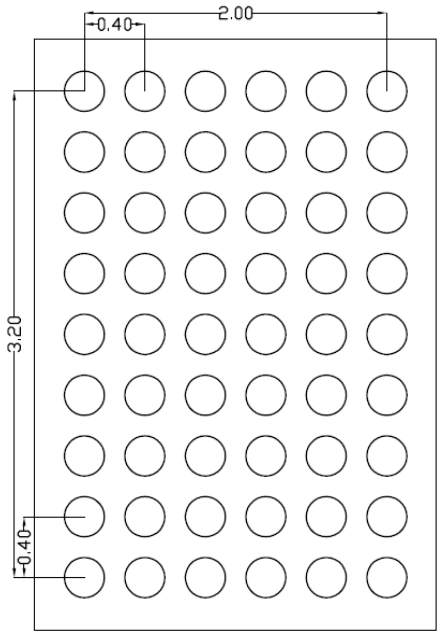
			W	001	16
				011	8
				100	4
				101	2
				110	1
				111	0.5
3	0	-	-	-	
2:0	100	BUCK1_RSPDN	R/W		DVS down slew rate mV/μs
				001	16
				011	8
				100	4
				101	2
				110	1
				111	0.5

BUCK1_SLEWCTRL				
Register Address:		0x55		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:6	00	-	-	-
5:4	00	BUCK1_POWERUP	R/W	Power up slew rate
				00	10 mV/μs
				01	5 mV/μs
				10	2.5 mV/μs
				11	1.25 mV/μs
3:0	0000	-	-	-

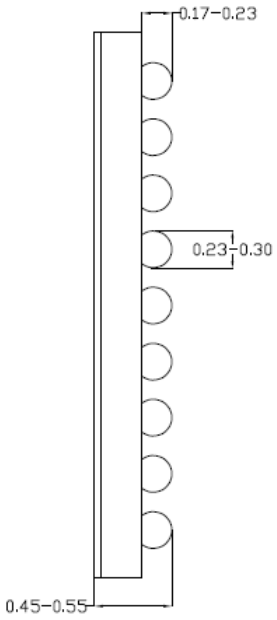
CSP2.66x3.89-54 Package Outline Drawing



Top view



Side view



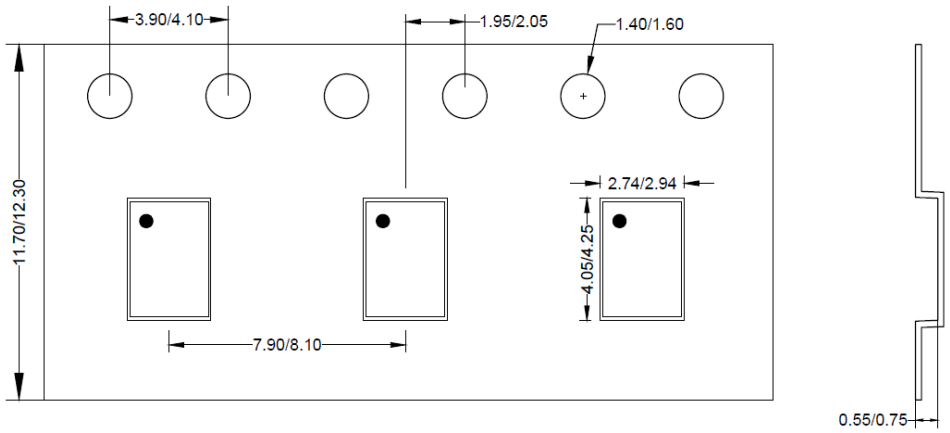
Bottom view

Notes: All dimensions are in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

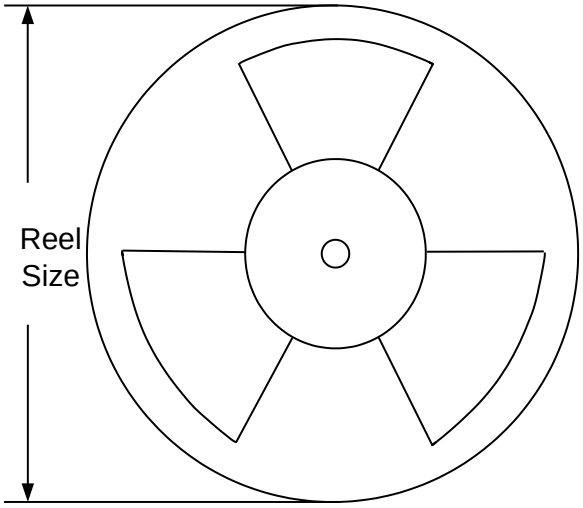
1. Taping orientation

CSP2.66x3.89



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
CSP2.66x3.89	12	8	13"	400	400	5000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Dec. 30, 2022	Revision 0.9	Initial Release.
Feb. 21, 2023	Revision 0.9A	The output voltage accuracy spec is changed from ±0.4% to ±0.5% @CCM, V_{OUT}>0.6V, T_A=+25℃, but the accuracy of full temperature is not affected. (Page 7)
Apr. 10, 2023	Revision 0.9B	1. Add current share accuracy at 10A/15A load. 2. Add switch frequency accuracy at 3T. 3. Data out hold time min 12ns. 4. Add support start-up with pre-bias voltage. 5. Add the LC selection guide. 6. Add both 1.8V and 3.3V can be connected to VIO. 7. AVIN add RC filter.
Jul. 17, 2025	Revision 1.0	Production release, no change.

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