SY7T501/SY7T502

Single-Phase Energy Measurement ICs with Relay and Dimming Controls

Data Sheet

General Description

The SY7T501 and SY7T502 are energy measurement ICs designed for monitoring any single-phase (2-wire) loads. The SY7T501 and SY7T502 are ideally suited for applications such as smart-plugs, smart appliances, lighting and building automation.

The UART interface supports low baud rates to allow low-cost isolation when required. Additionally, the UART includes an auto-baud function.

The analog front end (AFE) provides a differential analog input for current sensing and a single-ended input dedicated to voltage acquisition. A high-resolution delta-sigma converter feeds a fixed function digital signal processing block performing RMS, active power, and energy accumulation calculations. The analog front-end includes a comparator with a state machine that provides an accurate voltage zero-crossing (ZC) reference to internal blocks. The ZC signal is available on the DO0 output.

The devices feature a relay control block with user-programmable On/Off delays. The SY7T502 features relay contact feedback for continuous timing adjustment (closed loop control) and supports latching (single/dual coil) and non-latching relay types.

The devices include a user-programmable leading-edge dimmer control block

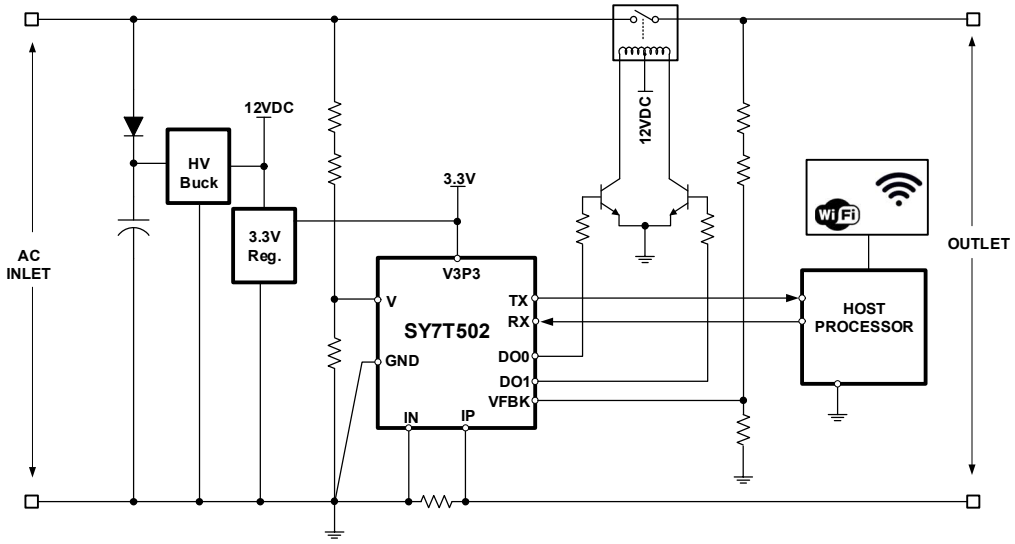
Features

- Small packages: MSOP-10 (SY7T502), SO-8 (SY7T501)
- High resolution Delta-Sigma ADC with two analog (sensor) inputs
- Internal precision voltage reference
- Internal trimmed timing reference
- Fixed-function Digital Signal Processing block
- UART interface with Auto-Baud Function
- Integrated control for latching and non-latching single and dual coil relays.
- Relay Contact sensing feedback
- Integrated dimmer control (Leading Edge)
- Integrated AC line Zero-Crossing (ZC) detector
- Digital I/O's individually configurable as open-drain or push-pull, 5V tolerant
- Control of all functions via registers that are accessible through the UART

Applications

- Smart-Plugs, Outlets and Dimmers
- Power-Strips and Power Distribution Units
- Connected Appliances

Typical Application



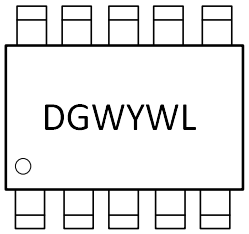
Introduction

This datasheet provides the ordering information, mechanical, electrical, and functional device characteristics of the SY7T501 and SY7T502. The SY7T501 offers a subset of the SY7T502's features. Many features and electrical specifications of both parts are identical. When features present in both parts are described in this data sheet, the parts are referred to as *devices*. Differences are flagged for features not available for the SY7T501.

Ordering Information

Ordering Number	Carrier Type	Temperature Range	Package	Top Mark
SY7T501FAC	Reel	-40°C to +85°C	SO-8	DGTYWL
SY7T502FBC	Reel	-40°C to +85°C	MSOP10	DGWYWL

Top Marking



DGW = SY7T502 Device ID

Y = Year ID (e.g., D = 2021)

W = Week Number ID (e.g., V = week 42)

L = Lot Number Code

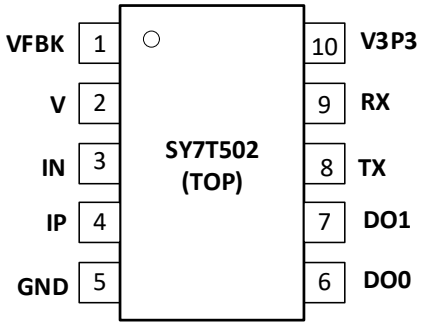
DGT = Device ID (DGT = SY7T501)

Y = year ID (i.e.: D = 2021)

W = Week Number ID for the specified year (i.e.: V = 42)

L = Lot Number ID for the specified Week

Pinout



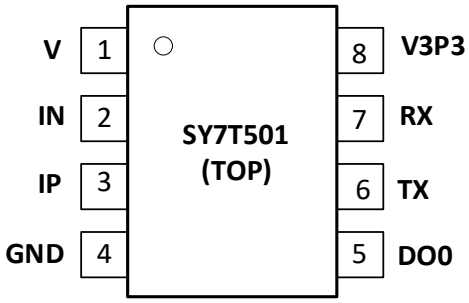


Table 1. Pin Description

Pin Name	Pin Number		Description
	SY7T501	SY7T502	
VFBK	--	1	Voltage Feedback (voltage after relay contact) †
V	1	2	Voltage Input
IN	2	3	Current Input (differential; positive)
IP	3	4	Current Input (differential; negative)
GND	4	5	Ground (Analog, Digital)
DO0	5	6	Digital Output 0 (Multi-Function, user configurable)
DO1	--	7	Digital Output 1 †
TX	6	8	UART Transmit Data
RX	7	9	UART Receive Data
V3P3	8	10	Supply (Analog, Digital)

†: Pin function available on the SY7T502 only

Block Diagrams

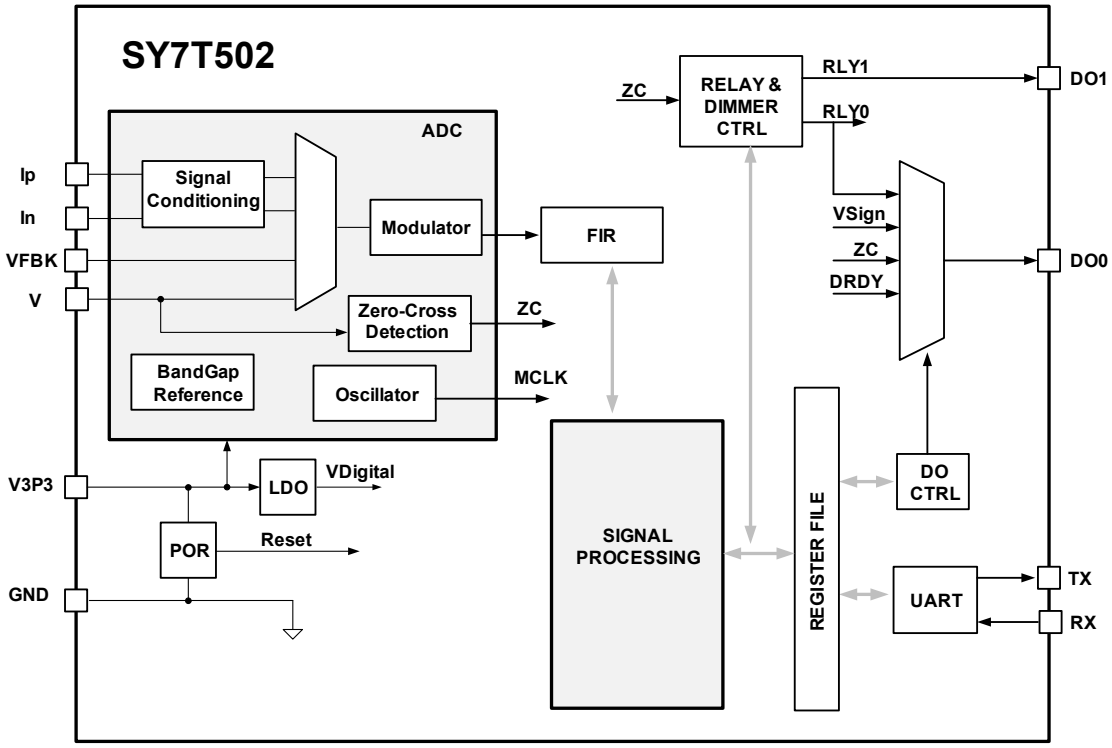


Figure 1. SY7T502 Block Diagram

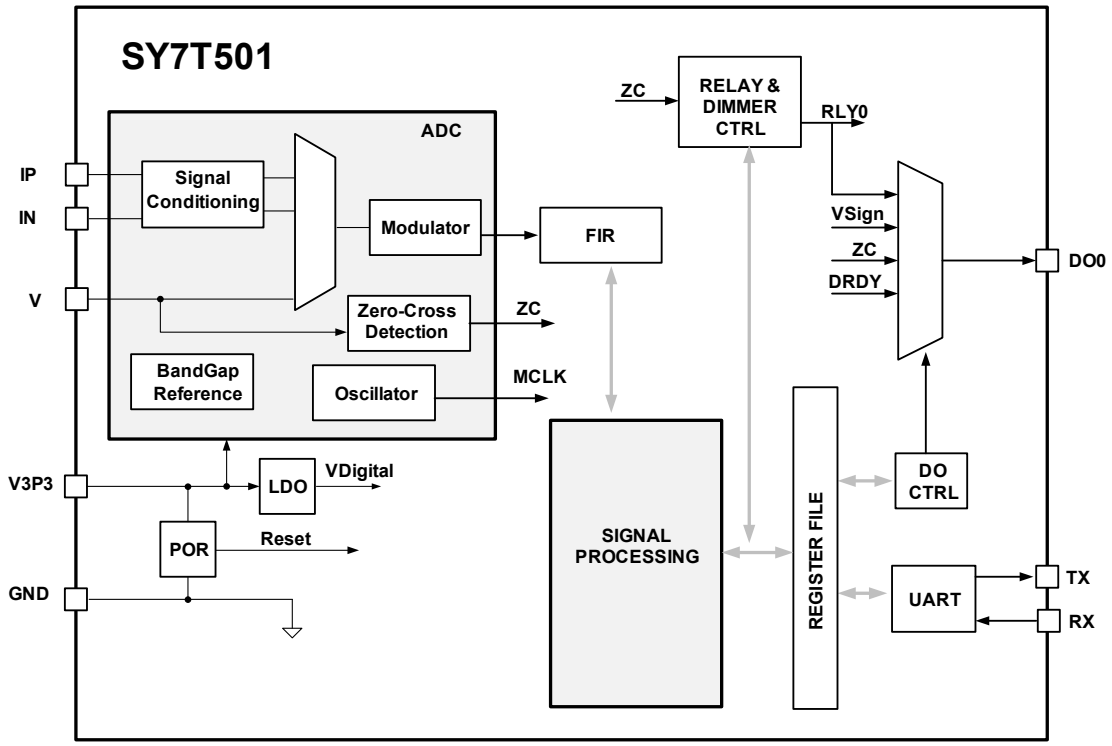
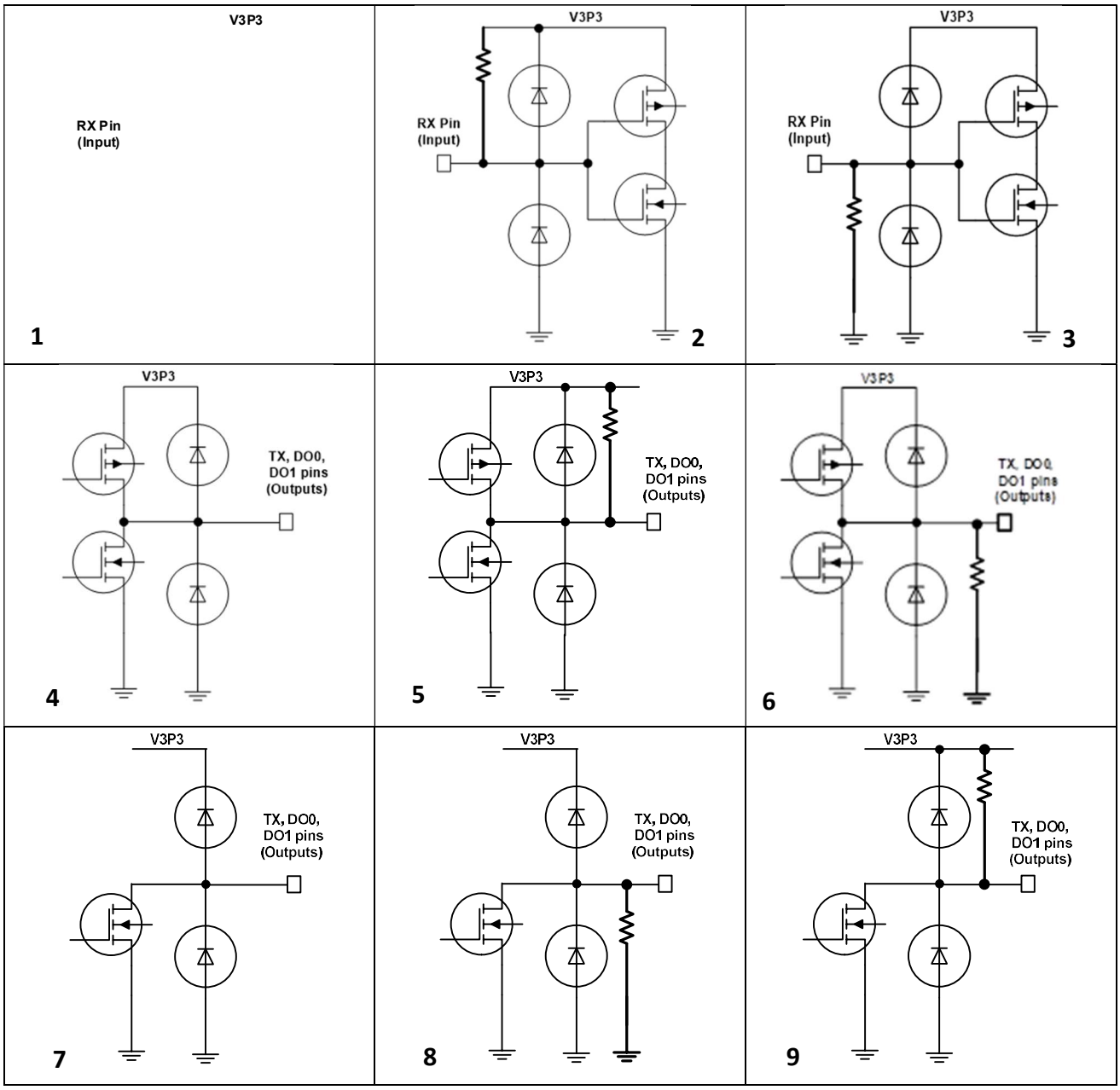


Figure 2. SY7T501 Block Diagram

Equivalent Circuits



UART RX pin (input) configurations: 1 = pull-up and pull-down disabled; 2 = pull-up enabled; 3= pull-down enabled.

UART TX, DO0 and DO1 (outputs) configurations: 4 = push-pull, pull-up, and pull-down disabled; 5 and 6 = push-pull with pull-up or pull-down enabled (configuration allowed however not useful); 7 = Open Drain, pull-up, and pull-down disabled; 8 = Open-Drain, pull-down enabled; 9 = Open-Drain, pull-up enabled.

Absolute Maximum Ratings (Note 1)

Description	Min	Max	Unit
Supply and Ground Pins			
V3P3	-0.5	4.6	V
GND	-0.1	0.1	V
Analog Input Pins			
V, VFBK (SY7T502 only)	-10	10	mA
	-0.5	V3P3+0.5	V
IP/IN	-10	10	mA
	-0.5	V3P3+0.5	V

Digital Pins			
Input (UART RX)	-10	10	mA
	-0.5	V3P3+ 0.5	V
Output (UART TX)	-10	10	mA
	-0.5	V3P3+ 0.5	V
Outputs (D0, D1)	-10	10	mA
	-0.5	V3P3+ 0.5	V

Temperature Ratings			
	Min	Max	Unit
Operating junction temperature, peak, 100ms		140	°C
Operating junction temperature, continuous		125	°C
Storage temperature	-45	165	°C
Maximum solder temperature, 30s duration per JEDEC J-STD-020		260	°C

Electrostatic Discharge					
Parameter	Symbol	Test Condition	Class	Value (Max)	Unit
Electrostatic discharge voltage (Human Body Model)	$V_{ESD(HBM)}$	TA = +25 °C, conforming to JESD22-A114	2	2000	V
Electrostatic discharge voltage (Charge Device Model)	$V_{ESD(CDM)}$	TA = +25 °C, conforming to ANSI/ESD STM5.3.1	II	500	V

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

Parameter	Symbol	Test Condition	Typ	Unit
Thermal resistance, Junction to Ambient	θ_{JA}	4-Layer PCB, Air velocity = 0 m/s	129	°C/W
Thermal resistance, Junction to Case (top)	θ_{JC}	4-Layer PCB, Air velocity = 0 m/s	76	°C/W

Recommended Operating Conditions (Note 2)

Parameter	Conditions	Min	Max	Unit
Supply Voltage (V3P3)		3.0	3.6	V
Operating Temperature		-40	+85	°C

Note 2: The device operations and performance are not guaranteed outside the recommended operating conditions.

Electrical Characteristics

Note that production tests are performed at room temperature.

Supply Current						
Parameter	Symbol	Test Conditions	Min	Typ.	Max	Unit
Supply Current (Quiescent)	I_{V3P3}	See Note 1		2.0	2.5	mA

Note 1: V3P3 = 3.3VDC; device in normal operations; Temperature = 25°C.

Input Logic Levels (UART RX)						
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Digital High-Level Input Voltage	V_{IH}		2	--	--	V
Digital Low-Level Input Voltage	V_{IL}		--	--	0.8	V
Input Leakage Current	I_H, I_{IL}	GND < V_{PIN} < V3P3, Pull-up/down disabled	-2		2	µA
Input Pull-Up Resistance	R_{pup}	Pull-up/down enabled		70		kΩ
Input Down Resistance	R_{pdn}			70		kΩ
Output Logic Levels (UART TX, DO, DO1)						
Digital High-Level Output Voltage	V_{OH}	I_{LOAD} = 1mA	V3P3 -0.4		V3P3	V
		I_{LOAD} = 15mA	V3P3 -1.1		V3P3	V
Digital Low-Level Output Voltage	V_{OL}	I_{LOAD} = 1mA	0		0.4	V
		I_{LOAD} = 15mA	0		0.8	V
Output Pull-Up Resistance	R_{pup}	Output configured as Open-Drain		70		kΩ
Output Down Resistance	R_{pdn}			70		kΩ

R/C Oscillator						
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Nominal Frequency		V3P3 =3.3V; Ta = 22°C		10.0		MHz
Frequency variation with temperature	RCO_{NOM}		-4.5		2.2	%
Frequency Variation with Supply		V3P3 = 3.0V to 3.6V (Ta = 22°C)	-0.75		0.75	%

Bandgap Voltage Reference (VREF)						
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Reference Voltage	V_{REF}	TA = +22°C	1.198	1.200	1.202	V
Power Supply Rejection		ΔVREF/ΔV3P3 (V3P3 2.8V to 3.6V)	-2		+2	mV/V
VREF(T) Deviation from VNOM(T) (7)		[(VREF(T) - VNONM(T)) x 10^6] /[VNOM(T) x 62)]	-40		+40	ppm/°C

Supply Voltage Monitor (POR)						
			Min	Typ	Max	Unit
V3P3 Threshold (Falling) (5)	POR_{TSD}			2.55		V
V3P3D Threshold (Rising) (6)				2.75		V

Notes:

5) Below this threshold the SY7T501/SY7502 is in reset mode (non-operating).

6) Above this threshold the SY7T501/SY7T502 is in “mission-mode” (normal operations).

7) Guaranteed by design, not production tested

Zero-Crossing Comparator						
			Min	Typ	Max	Unit
Comparator Threshold	VZC_{TH}		-5	0	+5	mV
Comparator Hysteresis	VZC_{HS}			0		mV

Delta-Sigma ADC						
ADC Settings						
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clock rate				2.5		MHz
Nominal sample rate				2,579.979		Hz
Full scale				8,388,608		LSB
IP/IN Input						
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Usable Range			-125		+125	mV
Input Impedance		VIN = 65Hz		60		kΩ
Input Offset (6)				10		mV
Common Mode Tolerance			-20		+20	mV
Total Harmonic Distortion at 125mVpk		125mVpk input, 55Hz, 64kpts FFT, Blackman-Harris window		-80		dB
Total Harmonic Distortion at 20mVpk		20mVpk input, 55Hz, 64kpts FFT, Blackman-Harris window		-85		dB
ADC Gain Error vs Percentage Power-Supply Variation $\frac{10^6\ \Delta Noutpk\ 357nV/VIN}{100\Delta V3P3\ /\ 3.3}$		VIN = 100mV peak, 65Hz; V3P3 = 3.0V, 3.6V			90	ppm/%
V Input(s)						
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Usable Range			-125		+125	mV
Input Impedance		f = 65Hz		60		kΩ
Input Offset (See note 6)				10		mV
Total Harmonic Distortion at 125mVpk		20mVpk input, 55Hz, 64kpts FFT, Blackman-Harris window		-80		dB
Total Harmonic Distortion at 20mVpk		125mVpk input, 55Hz, 64kpts FFT, Blackman-Harris window		-85		dB
ADC Gain Error vs %Power Supply Variation $\frac{10^6\ \Delta Nout_{PK}\ 357nV\ /\ V_{IN}}{100\Delta V3P3A/3.3}$		Vin=200mVpk, 65Hz, 3.0V -3.6V			90	ppm/%

Note 5: Guaranteed by design, not subject to test.

Note 6: Input Offset do not include post-processing compensation/cancellation.

Functional Description

Clock Generation

The devices feature an internal R/C oscillator. The on-chip oscillator is trimmed and designed to minimize the frequency variation over temperature and supply voltage.

Power-On Reset and Supply Monitor

The devices include a comparator with hysteresis to monitor the supply voltage. The comparator's output asserts a reset if the supply voltage (V3P3) level drops below the recommended operating range.

Metrology

The devices include a fixed function signal processing block. This block processes the ADC data, providing the following measurements:

- True RMS voltage
- True RMS current
- Active power
- Accumulated energy
- Line period

The figures below show the voltage and current signal processing and the active power calculation. The gray boxes indicate user-accessible registers.

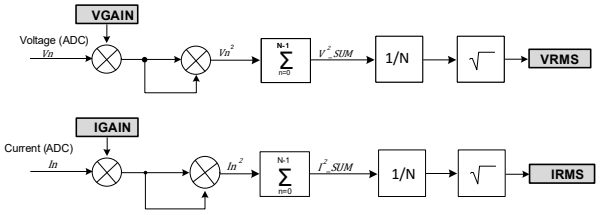


Figure 3. Voltage and Current RMS Calculations

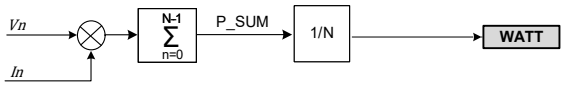


Figure 4. Active Power Calculations

For voltage and current RMS measurements the calculations are performed as indicated in the equations shown in Figure 4.

$$I_{RMS} = \sqrt{\frac{\sum_{n=0}^{N} i_n^2}{N}} \quad V_{RMS} = \sqrt{\frac{\sum_{n=0}^{N} v_n^2}{N}}$$

Figure 5. Irms and Vrms Equations

Accumulation Interval

The accumulation interval (T_{ACC}) is the amount of time (or number of ADC samples) over which the device performs and updates energy measurement calculations. The accumulation interval is configurable by the user through the *NSAMPLES* and *ACCUMCYC* registers and can either be a fixed number of line cycles (line-locked) or a fixed number of ADC samples (fixed interval).

The register *ACCUMSAM_X* reports the number of ADC samples within the given accumulation interval.

Fixed Interval

When the *ACCUMCYC* register is 0, the device operates on a fixed accumulation interval set by the *NSAMPLES* register. The *NSAMPLES* register contains an unsigned integer value representing the accumulation interval expressed in number of ADC samples.

$$T_{ACC} = \frac{NSAMPLES}{Sample\ Rate}$$

Line-Locked Interval

The accumulation interval can also be locked to the incoming line voltage cycles. When the *ACCUMCYC* register is set to a non-zero value, the accumulation interval will end after *ACCUMCYC* low-to-high zero crossings of the line voltage (see Zero-Crossing Detection) unless the maximum accumulation time has elapsed. This will cause the device to use an accumulation interval of *ACCUMCYC* line cycles regardless of the line frequency.

$$T_{ACC} = \text{MIN}\left(\frac{ACCUMCYC}{\text{Line Frequency}}, \frac{NSAMPLES}{Sample\ Rate}\right)$$

Frame Counter

The frame counter (*FRAME_X*) is an unsigned 32-bit counter that is incremented at the completion of each accumulation interval. The register rolls-over at 0xFFFFFFFF to a value of 0x00000000. The register is initialized to 0x00000000 at power-on and reset and is accessible for read and write operations. The user can initialize the Frame Counter register to any value in the range, the register will be incremented from it.

Zero-Crossing Detection

The devices include a comparator combined with a state machine and a filter to detect the line voltage zero-crossing for reducing spurious zero-crossing detection, e.g., from noise and harmonics. The filtered zero-crossing signal is utilized internally by the Relay and Dimmer controls, line period calculation, and other functional

blocks. It can also be output on the DO0 pin as line voltage sign or zero-crossing pulse.

AC Line Frequency and Period

The devices include line period calculations, the result is available in the *LF_PERIOD* register. The line period is calculated using a timer/counter, measuring the interval between zero crossings. The value of the line period is updated at each line voltage zero-crossing. The period is calculated as follows:

$$Line\ Period = 1.6E^{-6}\ s * LF\_PERIOD$$

For example, for a 50Hz line frequency the line period register value is expected to be 12500 (0x30D4).

Energy Accumulation

The devices include an energy accumulation function. The 32-bit signed registers *ENERGY* and *ENERGY_X* contains the net value of the accumulated energy. ENERGY contains the running energy accumulation over time whereas *ENERGY_X* contains a snapshot of *ENERGY* taken at the end of each accumulation interval. *ENERGY* and *ENERGY_X* are initialized to 0x00000000 at reset or power-on. The *ENERGY_X* is read only.

The rate of the energy counter can be configured by the user through the *CE_CONFIG* register (1 or 1/16).

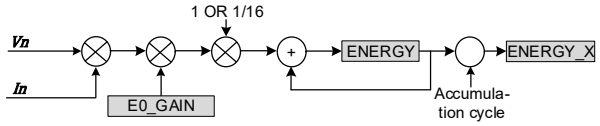


Figure 6. Energy Calculations

Power Sign

The devices allow setting the polarity of the power (sign of the power). This feature allows inverting the sign of the power, typically in cases where the current channel inputs connections to the sensor (shunt) are swapped. Refer to the *CE_CONFIG* register for setting of the power sign.

Current Input Boost

The devices include a configurable digital gain. The default gain is 1. Gains of 1, 2, 4 and 8 can be selected. Refer to the *CE_CONFIG* register for the digital gain settings.

Voltage High-Pass Filter

The signal processing of the Line Voltage input includes a high-pass filter that remove any DC components from the input signal. The filter is enabled by default, but it can be disabled by the user using the *CE_CONFIG* register.

Calibration Registers

The devices provide three calibration registers.

The V0GAIN and I0GAIN registers allow for compensation of the inaccuracies of the external sensors (i.e., voltage divider and current shunt) tolerances.

The register values can be determined as follows:

$$V0GAIN = \frac{(V_{Target} - V_{rms}) \cdot 2^{14}}{V_{rms}}$$

$$I0GAIN = \frac{(I_{Target} - I_{rms}) \cdot 2^{14}}{I_{rms}}$$

V_{Target} and I_{Target} are the expected RMS values for voltage and current, respectively. Vrms and Irms are the values calculated by the SY7T502 and available in the relevant registers.

The *E0GAIN* register allows a further correction of the energy being accumulated, as per the following equation (for power):

$$P = \Sigma(WATT_X \cdot \frac{2^{14} + E0GAIN}{2^{14}})$$

Scaling

The devices provide unscaled measurements. To convert the measurement value to physical values, such as Volts, Amperes, etc., it is necessary for the host processor to perform a simple scaling calculation.

$$Vrms = \frac{(VFS * 13.936)}{2^{30}} * VRMS$$

VRMS is the value contained in the VRMS register and VFS is the Full-Scale voltage (maximum Line Voltage corresponding to the full-scale of the ADC).

$$Irms = \frac{(IFS * 13.936)}{2^{30}} * IRMS$$

IRMS is the value contained in the IRMS register and IFS is the Full-Scale current (maximum Load Current corresponding to the full-scale of the ADC).

$$Power = \frac{(VFS * IFS * 13.936^2)}{2^{33}} * WATT\_X$$

WATT_X is the value contained in the *WATT_X* register while VFS and IFS are the Full-Scale voltage and current respectively.

$$Energy\ (Wh) = \frac{(VFS*IFS*13.936^2)}{(2^{17}*2580*3600)} * ENERGY$$

Example:

A generic system utilizes a resistive divider for line voltage sensing and a resistive shunt for current sensing, refer to Figure 6.

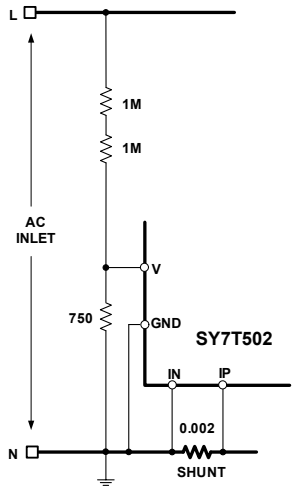


Figure 7. Voltage and Current Sense

In this case, the attenuation provided by the voltage divider is 3.75*10^{-4}, the full-scale voltage calculated on the ADC full scale (±125mV) is the following:

$$VFS = \frac{125 \cdot 10^{-3}\ V}{3.75 \cdot 10^{-4}} = 333V$$

$$IFS = \frac{125 \cdot 10^{-3}\ V}{2 \cdot 10^{-3}\ \Omega} \frac{1}{G} = 62.5A$$

G is the digital gain established by the *CE_CONFIG* register (1, 2, 4, or 8). G = 1 is used in the formula above. Calculated values are peak values.

Digital Output (DO0) Pin

The devices include a single digital output (pin DO) that can be configured by the user to output internally generated signals, as indicated in Table 2.

The DO0 pin can be configured as push-pull or open-drain. The DO polarity can be selected (active high or low) in order to adapt to the external circuitry (e.g., relay or TRIAC driver circuits). An internal weak pull-up and/or pull-down resistor can be enabled. All the DO0 pin configurations are through the *PAD_CNTL* register.

Table 2. Digital Output Configuration

***PAD_CNTL* Register DO0[2:0]**			**Description**
0	0	0	DO Disabled DO-HiZi (DEFAULT)
0	0	1	Line Voltage ZC (pulse)
0	1	0	Line Voltage Sign
0	1	1	DO Disabled DO-HiZi
1	0	0	RESERVED
1	0	1	Data Ready (RMS and Power data ready) DRDY
1	1	0	DO Disabled DO-HiZi
1	1	1	Relay/Dimmer Control

Relay Control

The devices comprise a relay control block for single-coil relays (latching and non-latching types). The SY7T502 has two relay control outputs and can therefore be used for dual-coil relays. The relay type is selectable through the *ZCRLY_CONTROL* register (Zero-Crossing and Relay Control Register).

Note: The relay control mechanism is based on the line voltage zero-crossing. In normal operation, a valid zero crossing signal must be present for a coil output to be activated. The DO0 and DO1 pins can also be directly controlled. See section *Forcing Relay Coil Activation* on page 14.

Relay activation (relay on) and de-activation (relay off) timing is individually configurable through dedicated user-accessible bit fields *RLY_ONTIME*[15:0] and *RLY_OFFTIME*[15:0] in the *RLY_TIME* register.

The 16-bit timer has a resolution of 1.6us, the relay activation time can be calculated as:

$$Activation\ Time = 1.6\mu s \cdot RLY\_ONTIME$$

Similarly, for the de-activation time:

$$DeActivation\ Time = 1.6\mu s \cdot RLY\_OFFTIME$$

The maximum activation and de-activation delays are 105ms.

In order to initiate a relay ON or OFF sequence it is necessary to set the relevant bit in the *ZC_RLY_CTLR* register.

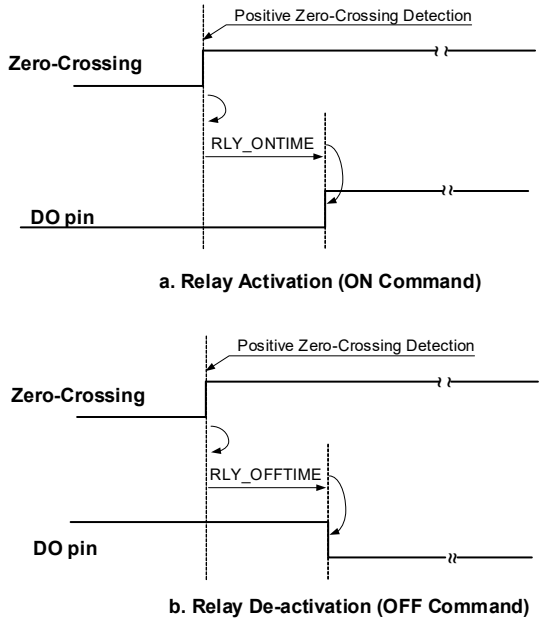


Figure 8. Relay Commands (non-latching)

When using latching relays, the activation and de-activation pulse width is selectable through the *T_PW*[7:0] bits of the *ZC_RLY_CNTL* register. The pulse width range is 0us to 52.22ms. The pulse width can be calculated as follows:

$$TPulseWidtht = 128 * T\_PW * 1.6\mu s$$

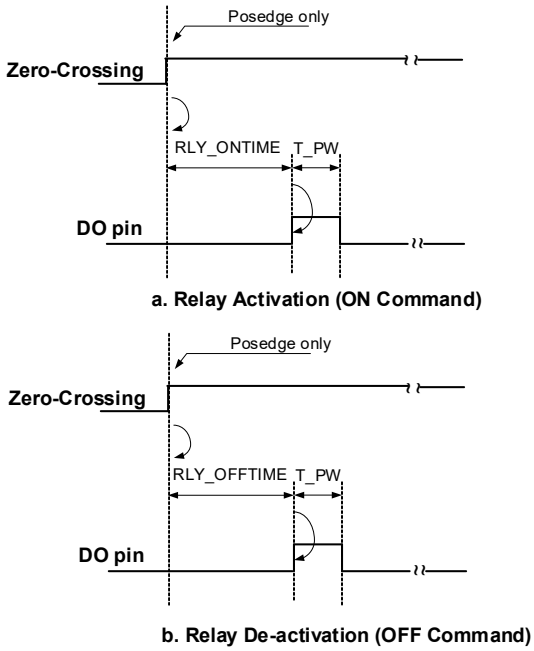


Figure 9. Relay Commands (latching)

For the SY7T502, the status of the relay's contact is reported in the *RLY_STATUS* register.

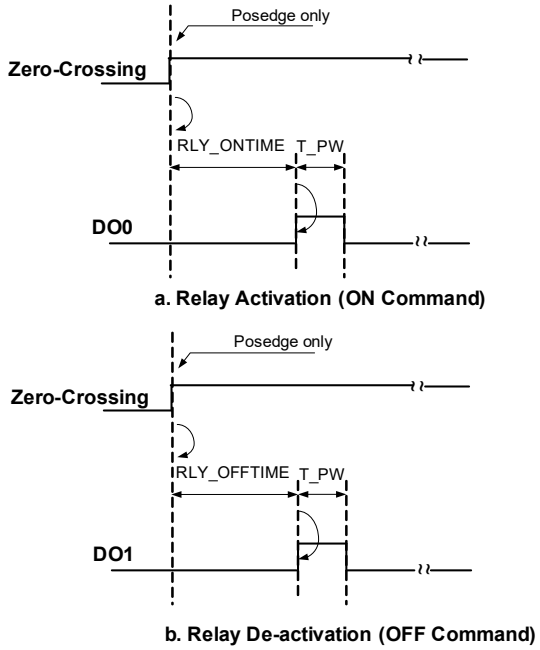


Figure 10. Relay Commands (dual-coil latching – SY7T502)

Closed Loop Relay Control

The SY7T502 includes an ADC input dedicated to relay contact sensing, i.e., to determine both open/close status and sensing of contact timing. The status of the relay contact is reported in the *RLY_STATUS* register. A reasonable AC voltage must be present at the relay contact for the detection mechanism to work.

Sensing of the mechanical actuation delays allows for continuous adjustment of the relay command delays (closed loop). For additional details on dynamic relay control, see Application Note AN7021 *Relay Control with the Silergy SY7T501 and SY7T502*, or contact Silergy at: support.em@silergy.com

Forcing Relay Coil Activation

In some cases, relay coils must be activated when no AC voltage is present. In safety applications, relays must be able to open or close immediately without the delay from a zero-crossing signal. The SY7T502 can activate DO0 and DO1 directly with the following sequences involving the *PAD_CNTL* register at address 0x1C:

Activate DO0 (Pulse):

1) Read and store value in 0x1F
2) Write 0x00 to 0x1F
3) Write 0x6F to *PAD_CNTL*
4) Wait for the time specified in *T_PW*
5) Write 0x67 to *PAD_CNTL*
6) Restore value at 0x1F

Activate DO1 (Pulse):

1) Read and store value in 0x1F
2) Write 0x00 to 0x1F
3) Write 0xE7 to *PAD_CNTL*
4) Wait for the time specified in *T_PW*
5) Write 0x67 to *PAD_CNTL*
6) Restore value at 0x1F

Dimmer Control

The devices include a leading-edge dimming control block.

The dimmer block shares the *RLY_ONTIME* and *T_PW* registers with the relay control block.

Leading-Edge Dimming

Referring to the Figure 11, the delay time or phase angle from the voltage positive and negative zero-crossing is set through the register *RLY_ONTIME*. The pulse width (DIM_{PW}) is set via the register *T_PW*.

The relevant times are calculated as follows:

$$DIM_{DLY} = 1.6\mu s \cdot RLY\_ONTIME$$

$$DIM_{PW} = 1.6\mu s \cdot T\_PW$$

The dimmer logic includes a control that prevents the control pulse from overflowing to the adjacent semi-period, for cases when the value DIM_{DLY} + DIM_{PW} exceeds the half line period time.

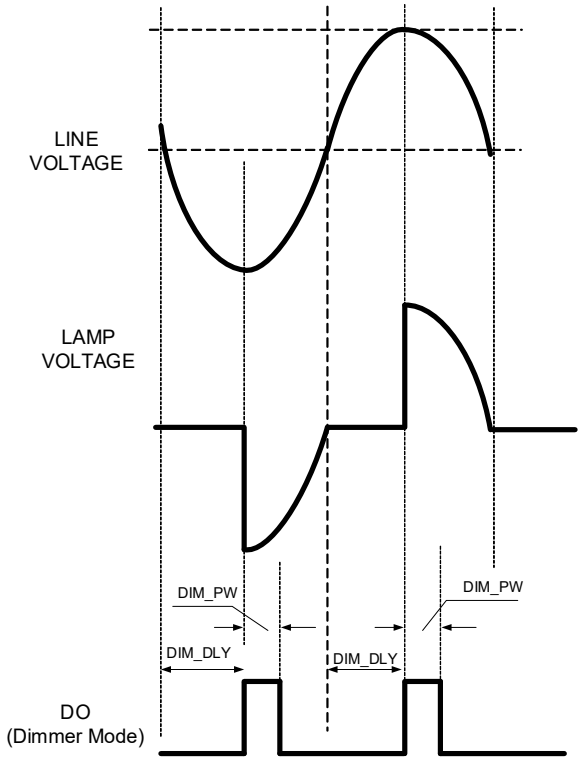


Figure 11. SY7T502 Dimmer Control

Trailing-Edge Dimming: Referring to Figure 12, the register *RLY_ONTIME* must be set to 0. The dimmer pulse is active at the zero-crossing. The DIM_{PW} pulse width is set via the register *T_PW*. The relevant time are calculated as follows:

$$DIM_{PW} = 1.6\mu s * T_{PW} * 32$$

The dimmer logic includes a control that prevents the dimmer pulse from overflowing to the adjacent semi-period, for cases when the DIM_{DLY} + DIM_{PW} time exceeds the half line period time.

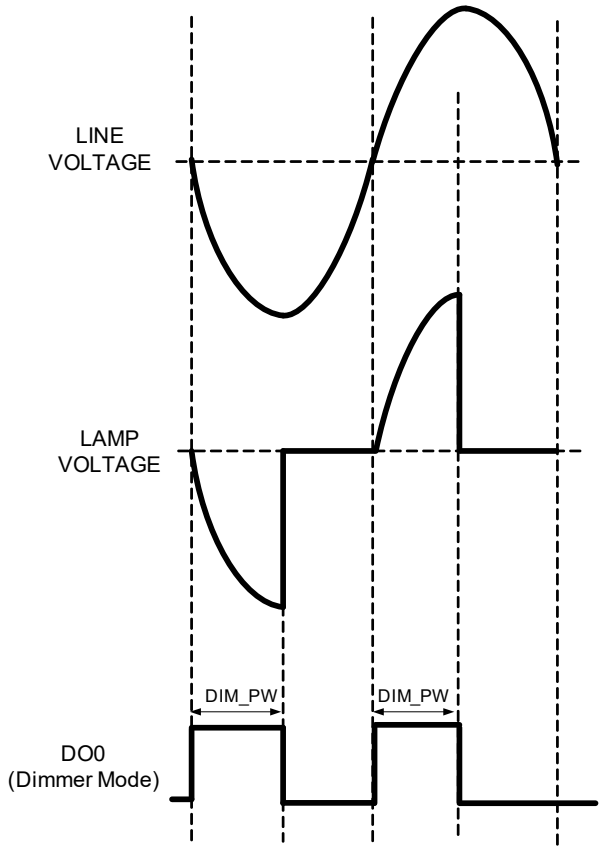


Figure 12. SY7T502 Dimmer Control (Trailing Edge)

UART

The devices feature a UART interface with a default data rate of 4800 Baud and 8-bit, no-parity, 1 start-bit and 1 stop-bit format. Baud rates of 600bd to 38,400bd are supported. The UART includes a fixed communication protocol and an auto-baud function. The auto-baud feature allows the host processor to set the interface to different baud rates including non-standard rates. Note that the UART starts at power-on/RESET in auto-baud mode. Therefore, it is recommended to issue a synchro-nization packet as indicated in the Auto-Baud section, before initiating the communication.

The register *UART_CTRL* allows to set the baud rate and to enable the auto-baud function. The recommended baud rates range from 600 to 38,400 Baud.

The baud rate can be set as follow:

$$uart\ baud\ rate = \frac{5{,}000{,}000}{BAUD[13:0]}$$

where *BAUD*[13:0] is a field in the *UART_CTRL* register.

Auto-Baud

The auto-baud function allows the UART interface to modify its baud rate upon receiving a synchronization message from the host processor.

The synchronization packet is a 0x55 character. The SY7T502 UART block only checks for synchronization packets following a reset or power-on or once the host processor re-enables the auto-baud function by setting the *AUTOBAUD_EN* bit in the *UART_CTRL* register.

Once a successful synchronization packet is detected, the UART will be set to the new baud rate and the *AUTOBAUD_OK* bit in the *UART_CTRL* register will be set. The autobaud function will be disabled until the *AUTOBAUD_EN* bit of the *UART_CTRL* register is set.

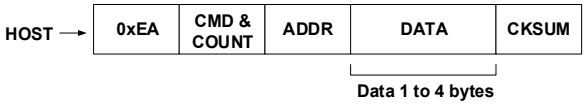
UART Protocol

The UART interface implements a fixed communication protocol that allows the host processor to access (read/ write) the internal registers and memory locations.

For a four-byte register value, the least significant byte is sent first, and the most significant byte is sent last.

Write Command

The write command packet consists of a header byte, the command and counter byte, an address byte, the payload (data) and the relevant checksum.



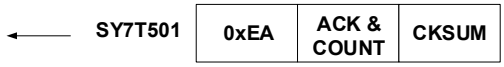
The following table contains a description of the write command from the host.

Byte	Data	Description
1	0xEA	Preamble
2	[7]: 1 [6:0]: 4	Command: 0=Read; 1=Write COUNT = 4
3	ADDR [7] ADDR [6:0]	0=Register; 1=Memory Register/Memory Address
4 ~ 7	DATA	Data (Payload): 4 bytes
8	CKSUM[7:0] (1)	Checksum of byte 1 - n

Notes:

(1) 8-bit checksum is the sum of preceding bytes (1 through n) including preamble, overflow discarded.

The expected reply from the device is the following:



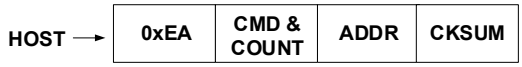
The following Table contains a description of the acknowledge from the SY7T501 or SY7T502.

Byte	Data	Description
1	0xEA	Preamble
2	[7] ACK [6:0] COUNT	ACK = 0: OK; ACK = 1: ERROR COUNT = 4
3	CKSUM[7:0] (1)	Checksum of byte 1 - 2

Note: 8-bit checksum is the sum of preceding bytes (1 and 2) including preamble, overflow discarded.

Read Command

The Read command packet consist of a header byte, command and counter byte, an address byte, and a checksum.



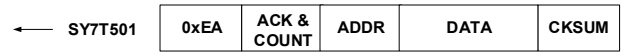
The table below describes the read command by the host processor:

Byte	Data	Description
1	0xEA	Preamble
2	[7] 1 [6:0] COUNT	Command: 0=Read; 1=Write Data (Payload) Size (2)
3	ADDR [7] ADDR [6:0]	0=Register; 1=Memory Register/Memory Address
4	CKSUM[7:0] (1)	Checksum of byte 1 - n

Notes:

(1) 8-bit checksum is the sum of preceding bytes (1 through n) including preamble, overflow discarded.

(2) If accessing registers (address bit = 0), the number of bytes can be set to 0 through 7CF. If accessing the memory (address bit = 1) the number of bytes is 4 through 60 in multiples of 4.



The table below contains a description of the reply of the part to a read command from the host.

Byte	Data	Description
1	0xEA	Preamble
2	[7] ACK [6:0] COUNT	ACK = 0: OK; ACK = 1: ERROR Data (Payload Count) (2)
3	ADDR [7] ADDR [6:0]	0: Register; 1: Memory Register/Memory Address
4 ~ n	DATA	Data (Payload)
n+1	CKSUM[7:0] 1)	Checksum of byte 1 - n

Notes:

(1) 8-bit checksum is the sum of preceding bytes (1 and 2) including preamble, overflow discarded

(2) The number of bytes is a multiple of 4, in the range 4 through 60 (up to 15 words) for memory accesses, and 4 through 124 (up to 31 words) for register accesses, in accordance with the value set in the relevant read command.

Register Description

All registers are four bytes wide. Table 1 lists the hardware registers, Table 2 lists RAM locations maintained by the signal processor that act as registers.

Table 1. Registers – for detailed descriptions, see individual tables following Table 2.

Address	Register	R/W	Default Value	Register Description
0x00	*UART_CTRL*	R/W	0x0004_1202	UART Control
0x04	*RESET*	R/W	0x0000_0000	Software Reset Command
0x08	*RLY_TIME*	R/W	0x0000_0000	Relay On and Off Time Delays
0x0C	*RLY_DELAY*	R	0x0000_0000	Sensed relay mechanical delays (for open and close actions) – SY7T502 only
0x10	*NSAMPLES*	R/W	0x0000_0AD9	Maximum number of ADC samples in an accumulation interval (2,777 decimal)
0x14	*LF_PERIOD*	R	0x0000_0000	Line Voltage Period (~10,450 with 16.6ms, 60Hz)
0x18	*ZC_RLY_CNTL*	R/W	0x0F01_0F00	Zero Crossing and Relay Control
0x1C	*PAD_CNTL*	R/W	0x060A_FF40	Digital Pin Control (TX, RX, DO)
0x20 -- 0x3E	Reserved	R/W	0x0000_0000	Reserved
0x40	*RLY_STATUS*	R	0x0000_0000	Relay contact state (open/closed) detection
0x44 Through 0x7E	Reserved	R/W	0x0000_0000	Reserved

Table 2. Data RAM – for detailed descriptions, see tables following Table 2.

0x80	ADC0	R	--	ADC reading from time slot 0 (I).
0x81	ADC1	R	--	ADC reading from time slot 1 (V).
0x82	ADC2	R	--	ADC reading from time slot 0 (VFBK) – SY7T502 only
0x83	*ACCUMCYC*	R/W	0x0000_0008	Maximum number of AC cycles per accumulation interval. For a 60Hz system, and accumulation interval is 133.3ms, for a 50Hz system it is 160ms.
0x84	*ZC_THR*	R/W	0x0080_0000	Voltage hysteresis threshold for ZC detection.
0x85	*RLY_THR*	R/W	0x0080_0000	Threshold for relay contact detection (ABS(VFBK – V)) – SY7T502 only
0x86	*RLY_HLD*	R/W	0x0000_0008	Number of samples required to change the detected relay status (RLY_STATUS)
0x87	*I0GAIN*	R/W	0x0000_0000	Current sensor gain calibration
0x88	*V0GAIN*	R/W	0x0000_0000	Voltage sensor gain calibration
0x89	Reserved	R/W	0x0000_0000	Reserved
0x8A	*E0GAIN*	*R/W*	0x0000_0000	Energy gain calibration
0x8B	*ACCUMSAM_X*	*R*	0x0000_0000	Number of samples in the last accumulation interval
0x8C – 0x8E	Reserved	R	0x0000_0000	Reserved
0x8F	*TSAMPLES*	R	0x0000_0000	Total of ADC samples since last reset

0x90	*FRAME_X*	R	0x0000_0000	Total of frames since the last reset. This counter can be used by the host to track energy accumulation (the energy of a frame should only be added to the accumulator if the frame counter has incremented by one).
0x91	*FREQ_LP*	R	0x0000_0000	Line frequency period (= *FREQ_LP**1.6µs)
0x92	*VRMS_X*	R	0x0000_0000	Voltage Root Mean Square
0x93	*IRMS_X*	R	0x0000_0000	Current Root Mean Square
0x94	*WATT_X*	R	0x0000_0000	Active Power
0x95	Reserved	R	0x0000_0000	Reserved
0x96	*ENERGY_X*	R/W	0x0000_0000	Accumulated Energy for the current accumulation interval, latched
0x97	*ENERGY*	R/W	0x0000_0000	Accumulated Energy for the current accumulation interval, updated at every sample
0x98	*CE_CONFIG*	R/W	0x0000_0000	CE Configuration Register
0x9A – 0xD9	Reserved	R	0x0000_0000	Reserved
0xDA	*PERIOD_LP*	R	0x0000_0000	Filtered measured period of the line voltage, generated by the signal processor. τ = *PERIOD_LP*/10,000

Register Details

***UART_CTRL* (R/W)**

Address	Bit	Definition	Access	Default	Description
0x00	[31:22]	Reserved	R only	0x00	Reserved
	[21:8]	*BAUD*	R/W	0x412	Baud rate selector [13:0]
	[7:2]	Reserved	R only		Reserved
	1	*AUTOBAUD_EN*	R/W	1	1 = auto-baud enabled 0 = auto-baud disabled
	0	*AUTOBAUD_OK*	R/W1C	0	Read 1: baud rate locked Read 0: baud rate not locked Write 1: reset autobaud block for new baud rate

Baud[13:0] — *Default 4800 Baud; Baud = 0x412 (decimal 1042); Baud[13:0] = 5,000,000/(Baud Rate) Example: For a baud rate of 4800 set Baud[13:0] = 5,000,000/4800 = 1041.667 = 1042*

AutoBaud_EN — *1 = set this bit to enable auto-baud mode*
0 = clear this bit to disable auto-baud mode

AutoBaud_OK — *AutoBaud_OK = 1 auto-baud sequence completed successfully, the baud rate is locked*
AutoBaud_OK = 0 an auto baud sequence has not started or has not been successful, and the baud rate is not locked.

***RESET* (R/W)**

Address	Bit	Definition	Access	Default	Description
0x04	[31:8]	Reserved	R only	0x0	Reserved
	[7:0]	*RESET_CMD*[7:0]	R/W	0x00	Write 0x81 to this register to initiate a reset sequence. Reads 0x0 when reset is completed.

***RELAY_TIME* (R/W) – Two Unsigned 16-Bit Integers**

Address	Bit	Definition	Access	Default	Description
0x08	[31:16]	*RLY_OFFTIME* [15:0]	R/W	0x00	Deactivation delay. Delay = 1.6µs * *RLY_OFFTIME*. The deactivation delay is relative to the line voltage zero-crossing.
	[15:0]	*RLY_ONTIME* [15:0]	R/W	0x00	Relay activation delay. Delay = 1.6µs * *RLY_ONTIME*.

***RLY_DELAY* (R) – Two Unsigned 16-Bit Integers**

Address	Bit	Definition	Access	Default	Description
0x0C	[31:16]	*RLY_OFFDEL* [15:0]	R/W	0x00	Relay ON-to-OFF mechanical delay: The relay's mechanical delay, as sensed from the OFF command to the first contact open feedback. The delay is in multiples of 1.6µs.
	[15:0]	*RLY_ONDEL* [15:0]	R/W	0x00	Relay OFF-to-ON mechanical delay: The relay's mechanical delay, sensed from the ON command to the first contact closure feedback. The delay is in multiples of 1.6µs.

Note: Values for this register are only calculated in the SY7T502. In the SY7T501 this register contains random values.

***NSAMPLES* (R/W) - Unsigned 16-Bit Integer**

Address	Bit	Definition	Access	Default	Description
0x10	[31:16]	Reserved	R only		Reserved
	[15:0]	*NSAMPLES*[15:0]	R/W	0x0AD9 (2,777)	Maximum number of ADC samples to be used for the RMS calculation (voltage, current) and Active Power. The value ranges from 0 to 0x3FFF

NSAMPLES[15:0] — *Default 0x0AD9 (decimal 2777). The NSAMPLES represents the number of ADC samples used in the accumulation interval. Note that the NSAMPLES is only used when the ACCUMCYC register is set to 0x0000.*

***LF_PERIOD* (R)**

Address	Bit	Definition	Access	Default	Description
0x14	[31:16]	Reserved			Reserved
	[15:0]	*LF_PERIOD*[15:0]	R only	--	AC Line Voltage Period; Period = 1.6µs * *LF_PERIOD*. Unsigned integer. Updated at each Voltage zero-crossing.

***ZC_RLY_CNTL* (R/W)**

Address	Bit	Definition	Access	Default	Description
0x18	[31:24]	*ZC_BLANK_TIME*	R/W	0x0F	Reserved; Contact Silergy for further information; do not change the default value.
	[23:16]	*ZC_DEGLITCH*	R/W	0x01	Reserved; Contact Silergy for further information; do not change the default value.
	[15:8]	*T_PW*[7:0]	R/W	0xF	*T_PW*: pulse width for the latching relays and for dimmer (unsigned 8-bit integer). Pulse width = *T_PW* * 128 * 1.6µs
	[7:6]	Reserved	R only	0x0	Reserved
	[5:4]	*RLY_TYP*	R/W	0x0	Relay Selection: [5:4] Relay Type 0 0 Single-Coil, non-latching 0 1 Single-Coil, latching 1 0 Dual-coil, latching 1 1 Single-Coil, non-latching
	[3]	Reserved	R only	0x0	Reserved
	[2]	*DM_MODE*	R/W	0x0	Dimmer mode Selection 0: Relay Mode (default) 1: Dimmer Mode
	[1]	*RLY_OFF*	R/W	0x0	Relay Command 0: No Command 1: Relay OFF Command
	[0]	*RLY_ON*	R/W	0x0	Relay Command 0: No Command 1: Relay ON Command

*T_PW[7:0] For relay control function (DM_MODE = 0), the relevant pulse width can be calculated as follows: TPulseWidth = 128 * T_PW * 1.6us. The pulse width range is 0ms to 52.22ms.*
*For dimmer control function (DM_MODE = 1), the relevant pulse width can be calculated as follows: TPulseWidth = T_PW * 1.6us * 32. The range is 0us to 13.056ms.*

PAD_CNTL (R/W)

Address	Bit(s)	Definition	Access	Default	Description
0x1C	31:27	Reserved	R only	0x0	0x0
	26:24	*OD*	R/W	0x7	Digital Outputs Mode: Bit Function [24]: UART_TX pin: 0 = push-pull; 1 = Open Drain [25]: DO0 pin: 0 = push-pull; 1 = Open Drain [26]: DO1 pin: 0 = push-pull; 1 = Open Drain
	23:16	PU_PD	R/W	0xA	Digital Pins pull-up/ pull-down: Bit Function [23:22]: Not Used [21]: DO0 pin: 0 = no pull-up; 1 = pull-up enabled [20]: DO0 pin: 0 = no pull-down; 1 = pull- down enabled [19]: RX pin: 0 = no pull-up; 1 = pull-up enabled [18]: RX pin: 0 = no pull-down; 1 = pull- down enabled [17]: TX pin: 0 = no pull-up; 1 = pull-up enabled [16]: TX pin: 0 = no pull-down; 1 = pull- down enabled
	15:8	Reserved	R/W	0xFF	Reserved, when writing to the PAD_CNTL register set these bits to 0xFF (default value).
	7	*DO1_POL*	R/W	0x0	DO1_POL Digital Output Polarity (SY7T502 only): DO1_POL = 0: Non-inverted/direct – Default DO1_POL = 1: Inverted
	6	*PAD_SMT*	R/W	0x1	Reserved, when writing PAD_CNTL register set this bit to 1
	5	*PAD_SR*	R/W	0x0	Reserved, when writing PAD_CNTL register set this bit to 0
	4	Reserved	R/W	0x0	Reserved
	3	*DO0_POL*	R/W	0x0	DO0_POL Digital Output Polarity: DO0_POL = 0: Non-inverted/direct - Default DO0_POL = 1: Inverted
	2:0	*DO0*	R/W	0x0	DO0 Output pin Function Selection [2:0] DO0 Output 0 0 0: Disabled (high impedance) - Default 0 0 1: Line Voltage Zero-Crossing (pulse at crossing) 0 1 0: Line Voltage Sign (DO0 high w/o AC voltage) 0 1 1: Disabled (high impedance) - Default 1 0 0: Reserved 1 0 1: Data Ready (RMS and Power data ready) 1 1 1: Relay and Dimmer Control

***RLY_STATUS* (R)**

Address	Bit	Definition	Access	Default	Description
0x40	[31:3]	Reserved	R only	0x00	Reserved
	2	*RLY_STATUS*	R only	0b1	Contact status: 0: Relay contact closed 1: Relay contact open
	1	*RLY_CLOSED*	R only	0b1	Relay contact status detected by comparing the voltages at the V and VFBK input pins: 1: Relay contact closed 0: Relay contact open
	0	*RLY_OPEN*	R only	0b0	Relay contact status detected by comparing the voltages at the V and VFBK input pins: 1: Relay contact open 0: Relay contact closed

Note: Values for this register are only calculated in the SY7T502. In the SY7T501 this register contains random values.

***ACCUMCYC* (R/W) – Unsigned 32-Bit Integer**

Address	Byte	Description
0x83	[31:0]	*ACCUMCYC* [31:0]. The maximum number of AC line cycles per accumulation interval.

***ZC_THR* (R/W)**

Address	Byte	Description
0x84	[31:0]	*ZC_THR* [31:0]. Zero-Crossing Hysteresis, the voltage hysteresis level required to detect zero crossings.

***I0GAIN* (R/W)**

Address	Byte	Default	Description
0x87	[31:0]	0x00000000	*I0GAIN*[31:0], Current sensor gain calibration. Signed integer. If the current is measured 1% too low, *I0GAIN*[31:0] should be set to 0xA4 (decimal 164). *Current Channel Gain* = $(2^{14} + IOGAIN)/2^{14}$

***V0GAIN* (R/W)**

Address	Byte	Default	Description
0x88	[31:0]	0x00000000	*V0GAIN*[31:0] Voltage sensor gain calibration. Signed integer. If the voltage is measured 1% too high, V0GAIN[31:0] should be set to 0xFF5C (decimal -164). *Voltage Channel Gain* = $(2^{14} + VOGAIN)/2^{14}$

***E0GAIN* (R/W)**

UART/I2C Address	Byte	Default	Description
0x8A	[31:0]	0x00000000	*E0GAIN*[31:0] Energy gain calibration. Signed integer. *Voltage Channel Gain* = $(2^{14} + VOGAIN)/2^{14}$

***ACCUMSAM_X* (R) – Unsigned 32-Bit Integer**

Address	Byte	Description
0x8B	[31:0]	*ACCUMSAM_X*[31:0]. The number of ADC samples in the last accumulation interval. The value is updated at the completion of each accumulation interval.

***TSAMPLES* (R/W) – Unsigned 32-Bit Integer**

Address	Byte	Description
0x8F	[31:0]	*TSAMPLES*[31:0]. The total number of ADC samples since reset.

***FRAME_X* (R/W) – Unsigned 32-Bit Integer**

Address	Byte	Description
0x90	[31:0]	*FRAME_X*[31:0]. The total number of accumulation intervals since reset.

***FREQ_LP* (R/W) – Unsigned 32-Bit Integer**

Address	Byte	Description
0x91	[31:0]	*FREQ_LP*[31:0]. The filtered measurement of the AC line voltage period. T = *FREQ_LP**1.6µs. At 60Hz, the value in *FREQ_LP* will be 10,417, equivalent to 16.67ms.

***VRMS_X* (R) – Unsigned 32-Bit Integer**

Address	Byte	Description
0x92	[31:0]	VRMS [31:0]. The voltage RMS measurement, updated at the completion of each accumulation interval.

***IRMS_X* (R) – Unsigned 32-Bit Integer**

Address	Byte	Description
0x93	[31:0]	IRMS [31:0]. The current RMS measurement, updated at the completion of each accumulation interval.

***WATT_X* (R) – Unsigned 32-Bit Integer**

Address	Byte	Description
0x94	[31:0]	WATT_X [31:0]. The current active power measurement, updated at the completion of each accumulation interval.

***ENERGY_X* (R) – Signed 32-Bit Integer**

Address	Byte	Description
0x96	[31:0]	*ENERGY_X*[31:0]. Accumulated Energy latched at each accumulation interval. The register contents represent the signed accumulated energy. Values between 0x1 and 0x7FFFFFFF indicate positive energy, values between 0xFFFFFFFF and 0x80000000 indicate negative energy. The rate of energy increase can be slowed down by a factor of 1/16 by setting the *RATE* bit in the *CE_CONFIG* register.

***ENERGY* – Signed 32-Bit Integer**

Address	Byte	Description
0x97	[31:0]	*ENERGY*[31:0]. Accumulated Energy as a running count, updated with each ADC sample. Otherwise, *ENERGY* has the same properties as *ENERGY_X*.

***CE_CONFIG* (R/W)**

Address	Bit(s)	Definition	Access	Default	Description
0x98	[31:6]	Reserved	RO	0x0	0x0
	5:4	Pre-Amp[1:0]	R/W	0x0	Current Channel Digital Pre-Amplifier [1:0] Pre-Amp Gain Setting: 0 0 Gain = 1 0 1 Gain = 2 1 0 Gain = 4 1 1 Gain = 8
	3	Reserved	R/W	0	Reserved
	2	*RATE*	R/W	0	Configuration of the Energy Accumulation Rate 0: Normal 1: Rate 1/16
	1	*PWR_SIGN*	R/W	0	Power Sign Selection 0: Normal 1: Inverted (swaps negative power to positive and vice versa. It reverses the energy accumulation in *ENERGY_X* and *ENERGY*.
	0	*V_HPF*	R/W	0x0	Voltage input High-Pass Filter Selection 0: Filter Enabled (default) 1: Filter Disabled

Application Examples

The SY7T501 and SY7T502 perform measurements and control function in different applications: These are smart dimmer and relay control. Both are described below.

Leading-Edge Dimmer with the SY7T502

The example shown in Figure 13 is a smart dimmer (leading-edge) that includes energy measurements and TRIAC control. The host processor communicates to the SY7T502 through the UART interface. It retrieves the energy measurement data by polling the registers of the SY7T502. The host processor controls the lamp by setting the firing angle of the dimmer via the relevant SY7T502 register. The energy measurement data is reported to the host processor and can be used to detect overload or malfunction of the connected load. The VFBK voltage input can be used as a generic ADC input (range ±125mV) by the host processor for auxiliary functions such as sensing the TRIAC temperature (typically using an NTC Thermistor) or, for example, to acquire the dimming phase from a potentiometer.

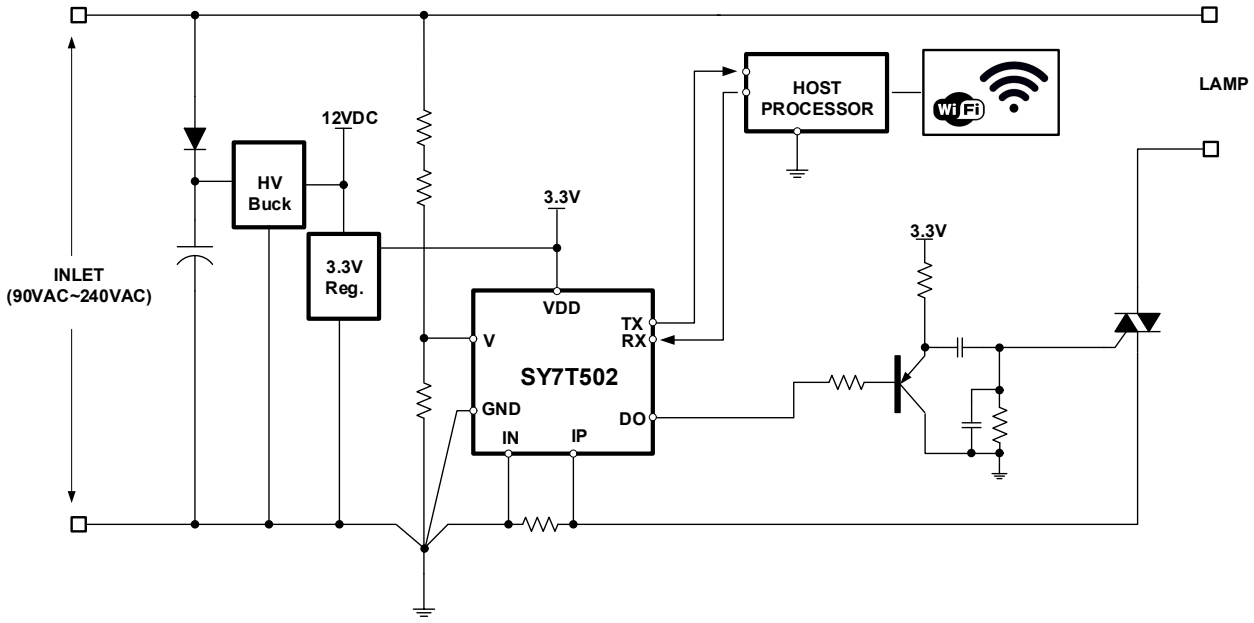


Figure 13. SY7T502 Leading Edge Dimmer and Measurements

Dual-Coil Relay Control with the SY7T502

The example shown in Figure 14 is a smart plug that includes energy measurements and relay control. In this example, the relay is a dual-coil latching type.

The host processor communicates to the SY7T502 through the UART interface. It retrieves the energy measurement data by polling the SY7T502 and it controls the relay by issuing the relay on/off commands to the SY7T502. The relay delays (on and off) are set by the host processor in order to have the relay contacts commutation close to the zero-crossings.

The energy measurement data is reported to the application and can be used by the host processor to detect overloads, eventually disconnecting the load to prevent overheating.

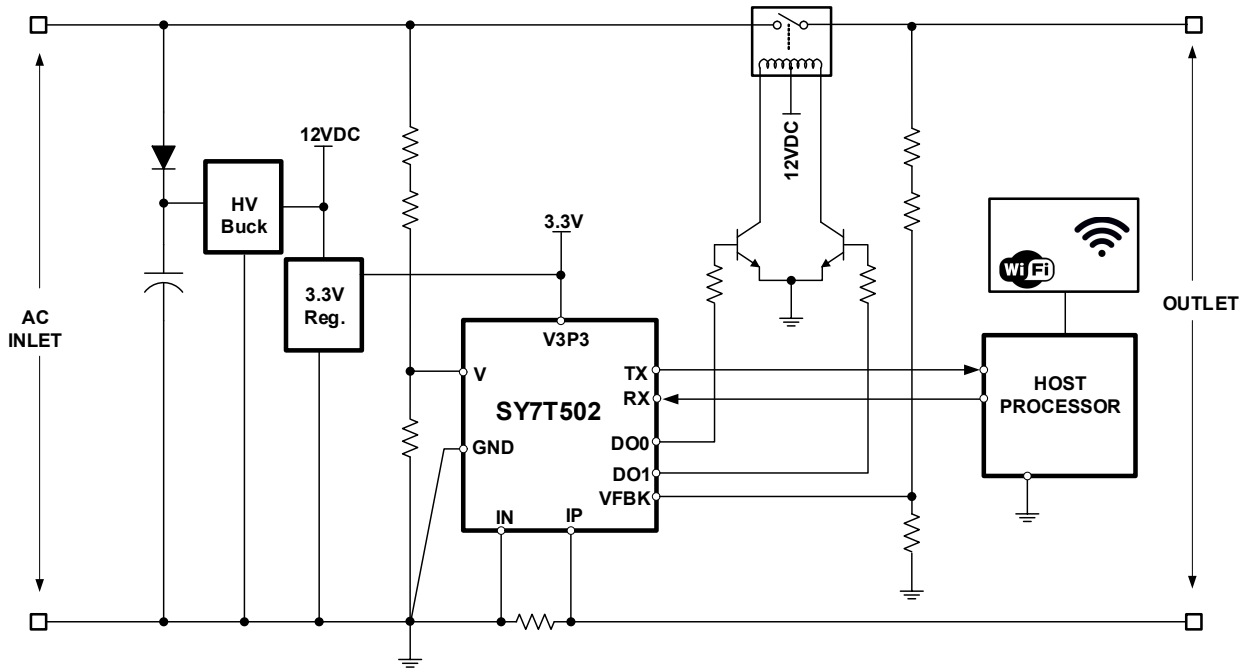


Figure 14. SY7T502 Relay Control and Measurements

Single-Coil Relay Control with the SY7T501

The example shown in Figure 15 is a smart plug application that includes energy measurements and relay control. In this example, the relay can be a single-coil latching or non-latching type.

The host processor communicates to the SY7T501 through the UART interface. It retrieves the energy measurement data by polling the registers of the SY7T501. The host processor controls the relay by issuing the relay on/off commands to the SY7T501. The relay delays (on and off) are set by the host processor in order to time the relay contacts commutation close to the voltage zero-crossings.

The energy measurement data is reported to the application interfacing the dimmer and can be used by the host processor to detect overloads, eventually disconnecting the load to prevent overheating.

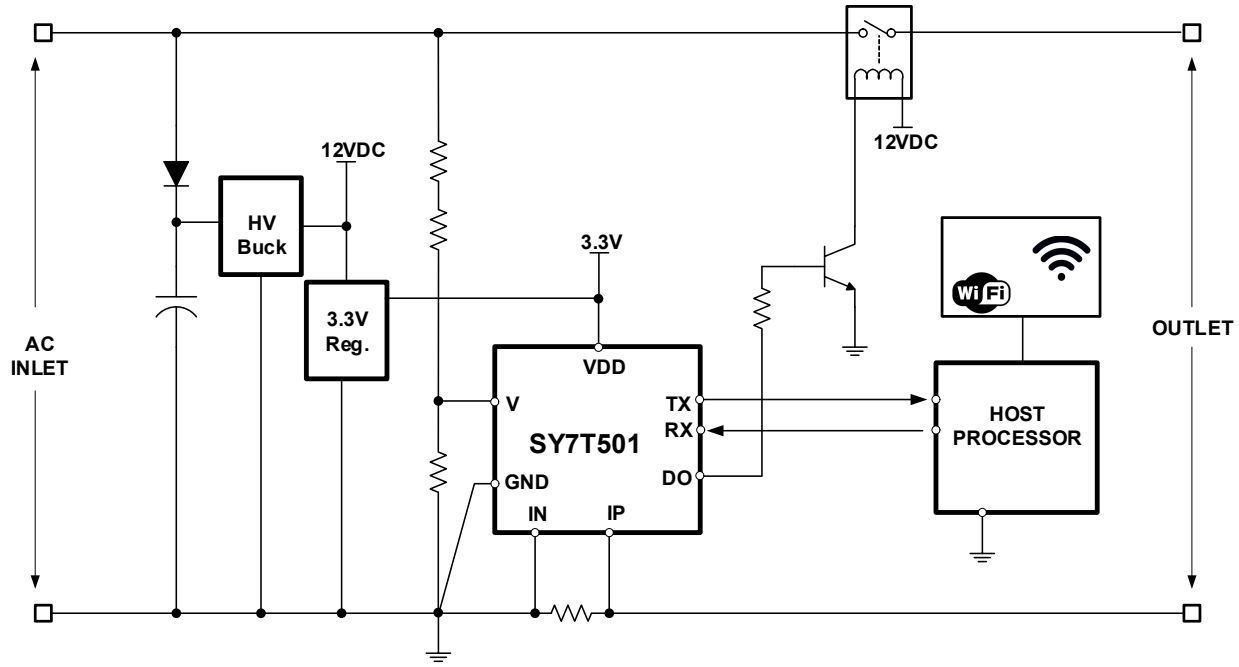


Figure 15. SY7T501 Relay Control and Measurement

Calibration

The devices are very accurate without calibration, and for typical applications, no calibration is required. If necessary, tolerances of current and voltage sensors can be compensated with the I0GAIN and V0GAIN registers. During calibration, known and accurate voltages and currents are applied to the devices, while the measurement outputs from the devices are recorded. The comparison of measured versus applied voltages and currents will yield error values. Based on these, settings for the *I0GAIN* and *V0GAIN* registers are then calculated as follows:

$$V0GAIN = 2^{14}\frac{-error_V(\%)}{100}$$

$$I0GAIN = 2^{14}\frac{-error_I(\%)}{100}$$

The SY7T501 and SY7T502 cannot store these registers nor any other registers such as those associated with relay timing. Upon cycling power, all registers will have the default values indicated in Table 1 and Table 2. The host must update all registers of interest in the SY7T501 and SY7T502 upon power up. It is recommended that the host checks and, if necessary, refreshes the registers in the SY7T501 and SY7T502 on a regular basis.

Typical Performance

Typical accuracy for an active power measurement is shown in Figure 16. Wh accuracy can be expected to be better than ±2.0% at current as low as 1/4,400 of the maximum current.

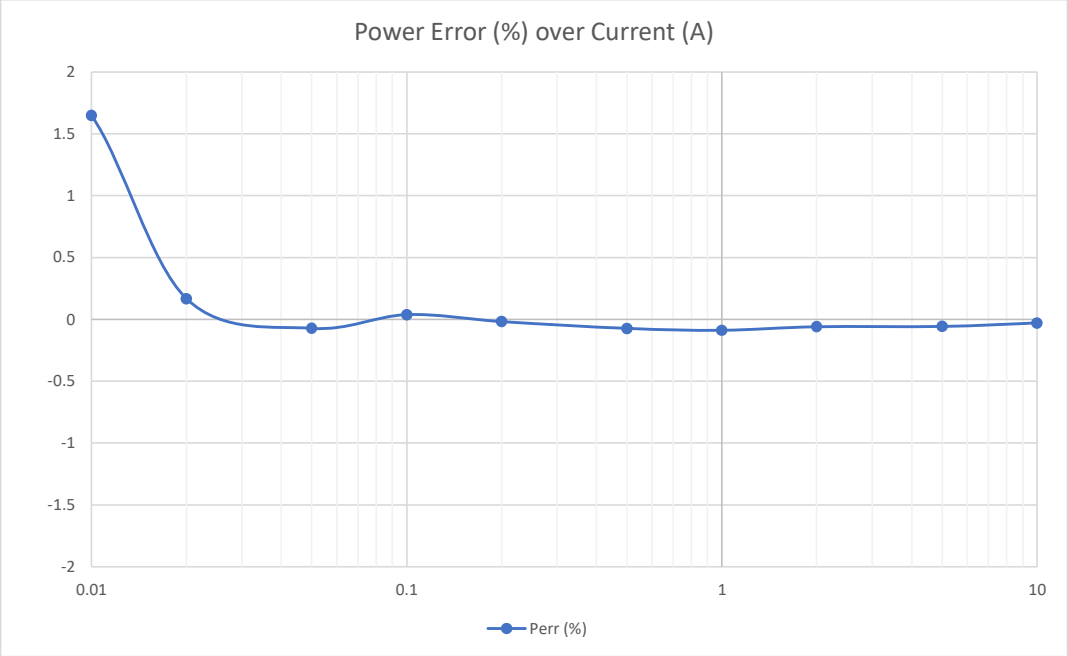


Figure 16. Power Measurement Accuracy

The conditions for the results in Figure 16 were:

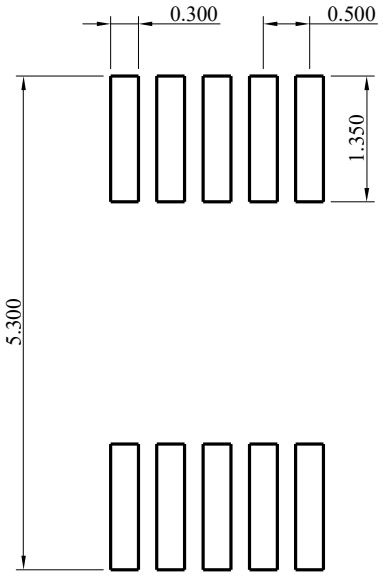
- 240Vrms AC voltage, 60Hz
- Current 10Arms to 0.01Arms at 0° phase angle
- Current sensor: 2mΩ shunt for maximum current of 42.2Arms
- Accumulation interval (frame): 8 cycles at 60Hz, or 133.3ms. Outputs averaged over 10 frames (1.33s).
- Test equipment: Fluke 6100A

Repeatability of each power measurement (based on one cycle at 60Hz or 16.67ms) with the conditions listed above applied is listed in Table 3, expressed as standard deviation of the measurement error (maximum current = 44A).

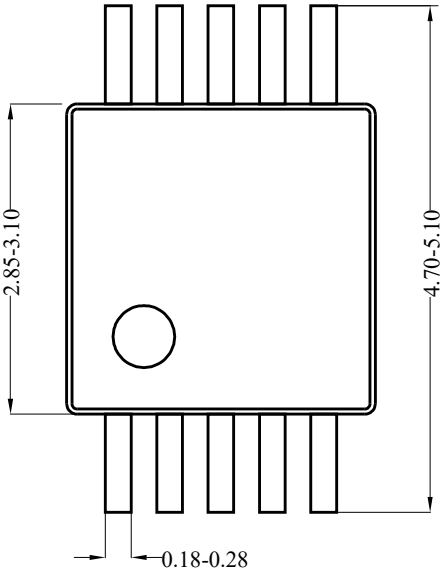
Table 3. Standard Deviation of Power Error as a Function of Current.

I (A)	Imax/I	P (W)	Stddev (Perr)		I (A)	Imax/I	P (W)	Stddev (Perr)
10	4.42	2400	0.036%		0.1	442	24	0.138%
5	8.84	1200	0.029%		0.05	884	12	0.372%
2	22.1	480	0.049%		0.02	2210	4.8	1.329%
1	44.2	240	0.035%		0.01	4420	2.4	1.996%
0.5	88.4	120	0.053%		0.005	8840	1.2	4.061%
0.2	221	48	0.126%					

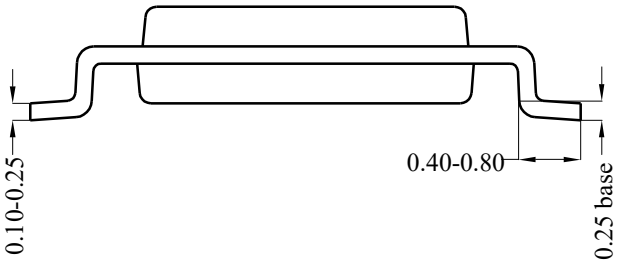
Package Information – SY7T502



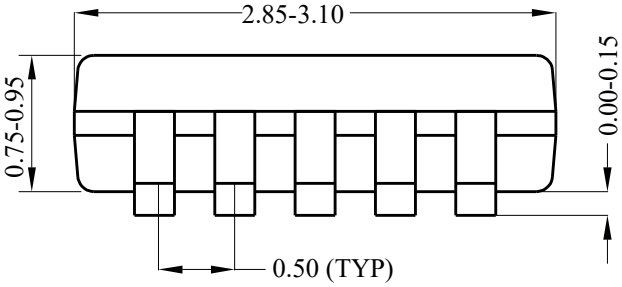
Recommended Pad Layout



Top view



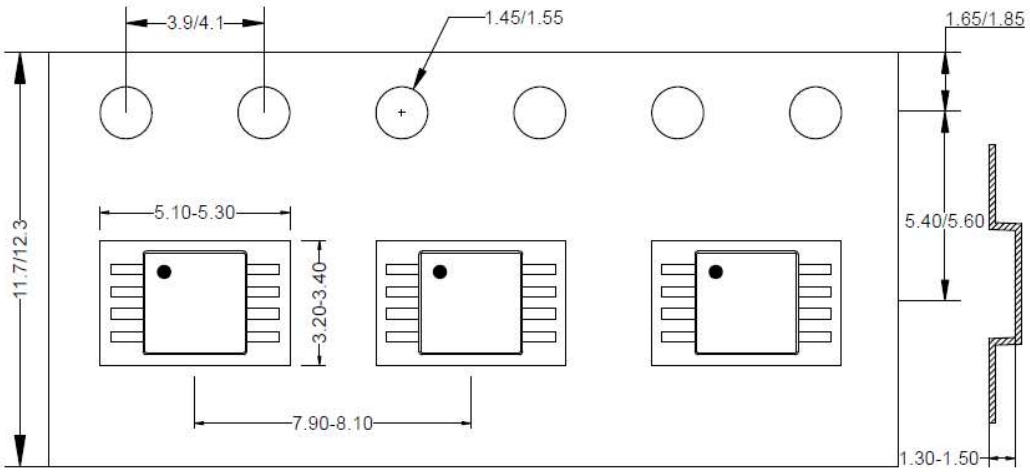
Front view

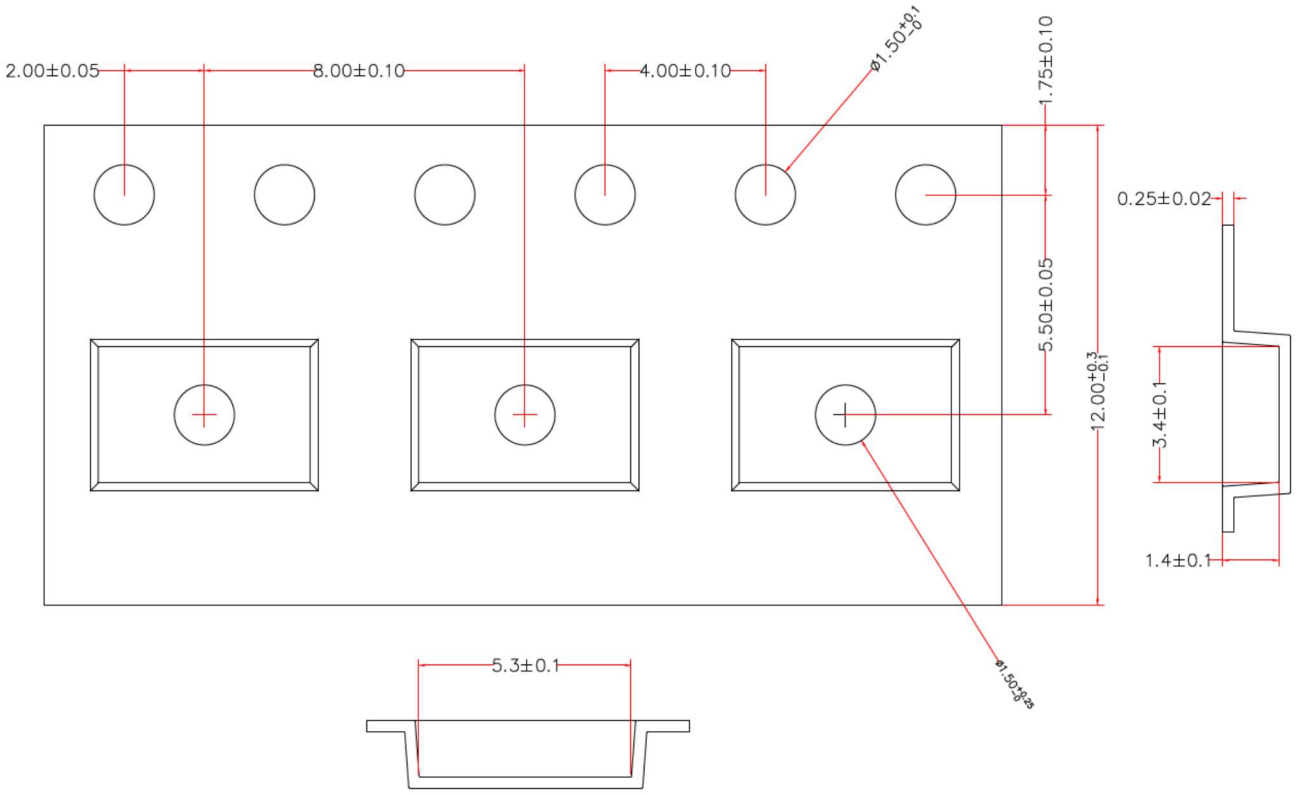


Side view

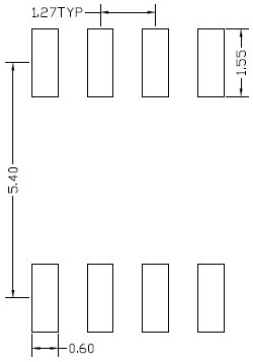
Note: All dimension shown in millimeter

Tape and Reel Orientation and Dimensions

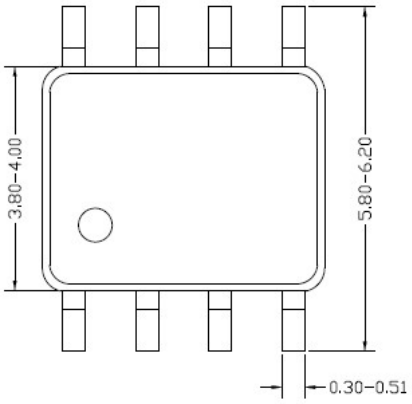




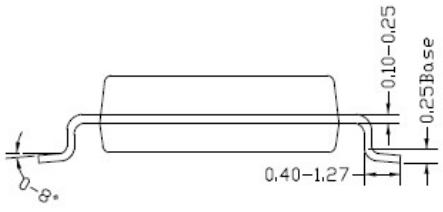
Package Information – SY7T501

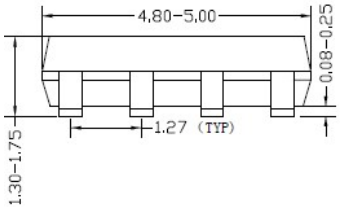


Recommended Pad Layout



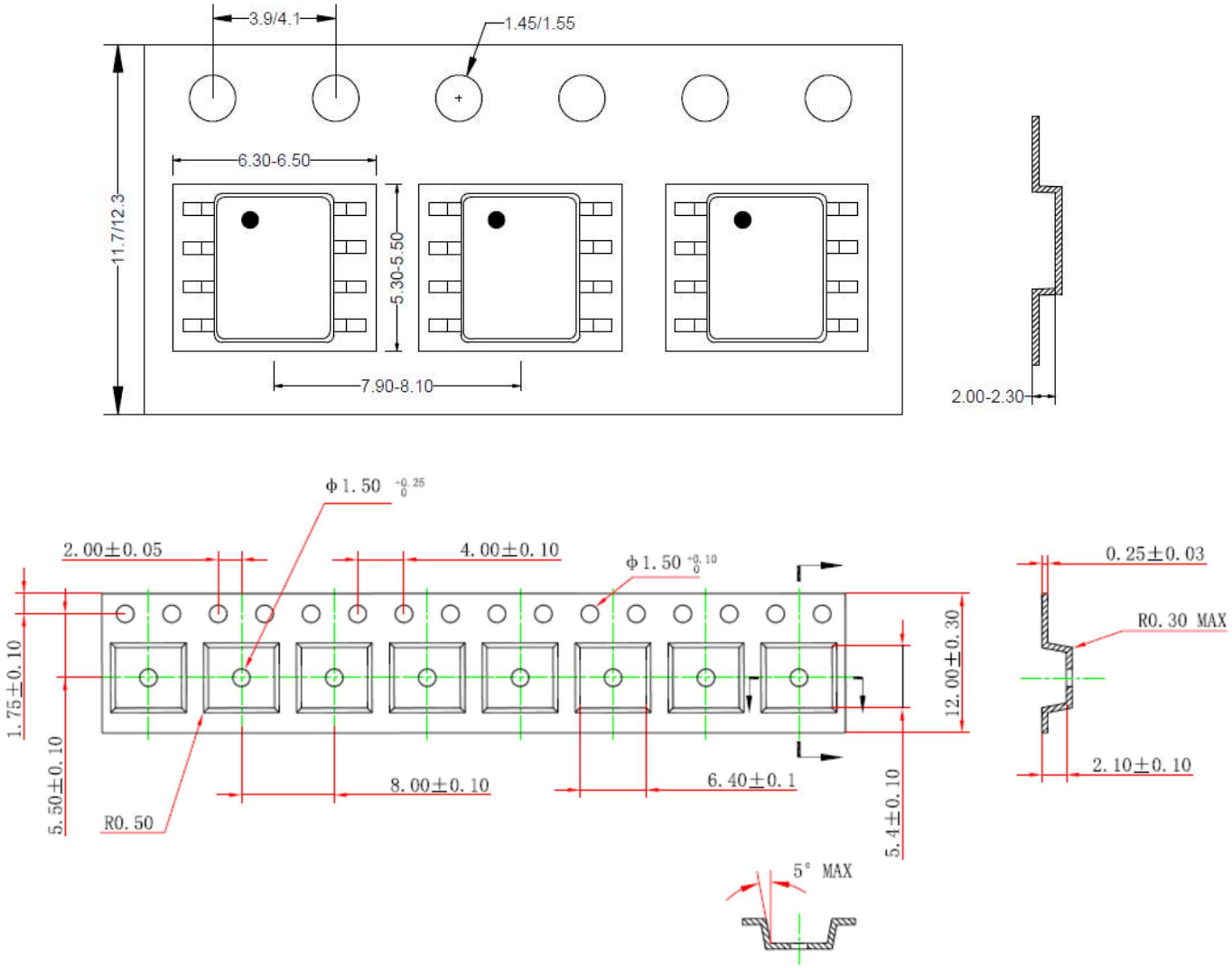
Top view



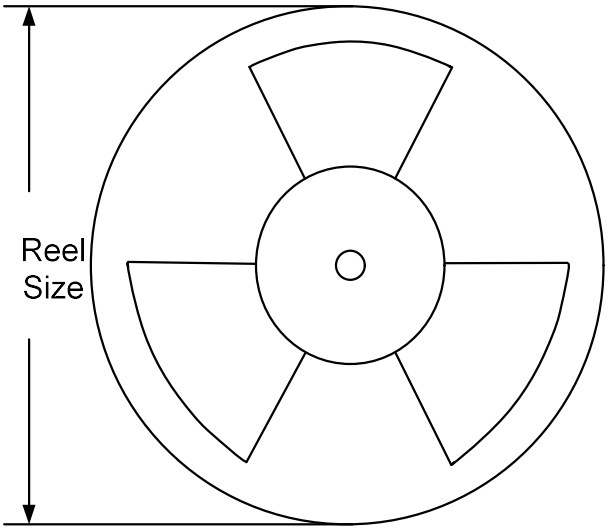


Note: All dimension shown in millimeter

Tape and Reel Orientation and Dimensions



Tape and Reel Data



Package Type	Tape Width (mm)	Pocket Pitch (mm)	Reel Size	Leader Length (mm)	Trailer Length (mm)	Parts per Reel
SO8	12	8	13”	400	400	2,500
MSOP10	12	8	13”	400	400	3,000

Contact Information

For more information about the SY7T501 and SY7T502 or other Silergy products, contact technical support at support.em@silergy.com

Revision History

Revision Number	Revision Date	Description	Pages changed
0.9	10/11/2023	First release	All
0.91	1/2/2024	Added ADC settings Added reference to AN7021 Updated register descriptions Updated baud rate information	9 14 17, 18, 21 15
0.92	2/26/2024	Added ADC full scale definition Improved Functional Description Updated description of relay control Added section on forcing coil activation Updated register descriptions Added page 'Typical Performance' Changed spelling of register and bit names	9 10 – 16 12 14 17 – 24 28 all
1.0	5/16/2025	Removed tray packaging option from Ordering Information table Updated packaging and dimensions for tape and reel	2 29 - 32
1.1	1/21/2026	Changed PAD_CNTL register bit 26 description Changed PAD_CNTL bit [26:24] default value	19 19

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