SY28637F

Single-channel, Adjustable Voltage Monitor in Ultra-small Package

General Description

The SY28637F is a compact supervisory circuit that monitors voltages greater than 500mV with 0.25% threshold accuracy. The output assertion delay time can be adjusted using an external capacitor. The device features a logic high enable pin to control the power on and off the internal logic.

Operating within a voltage range of 1.7V to 6.5V, the SY28637F has a typical quiescent current of 9μA and an open-drain output rated at 18V.

The device is available in an ultra-small DFN 1.45mm×1.0mm–6pin package and is fully specified for operation over a temperature range of T_J=-40°C to 125°C.

Features

- Operating Voltage Range: 1.7V to 6.5V
- Adjustable Threshold Down to 500mV
- Threshold Accuracy: 1% Over temperature
- Capacitor-adjustable Delay Time
- Low Quiescent Current: 9μA (typ.)
- External Enable Input
- Open Drain Output (Rated at 18V)
- Temperature Range: -40°C to 125°C
- RoHS Compliant and Halogen Free
- Compact Package: DFN1.45×1-6

Applications

- Notebook and Desktop Computers
- Microcontrollers, DSPs, and Microprocessors
- Portable and Battery-Powered Products
- FPGAs and ASICs

Typical Application

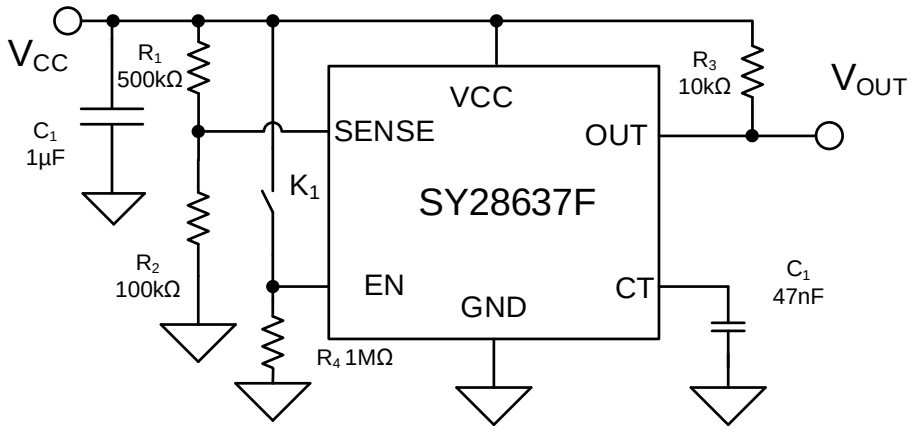


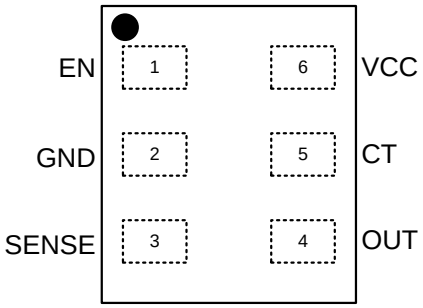
Figure1. Schematic Diagram

Ordering Information

Ordering Number	Package Type	Top Mark
SY28637FDTD	DFN1.45×1-6 RoHS Compliant and Halogen Free	***txyz***

Device code: t
x=year code, y=week code, z= lot number code

Pinout (Top View)



(DFN1.45×1-6)

Pin Name	Pin NO.	I/O	Pin Description
EN	1	I	Active high input. Driving EN low immediately makes OUT go low, independent of V_{SENSE}. With V_{SENSE} already above V_{IT+}, drive EN high to make OUT go high after 0.2µs.
GND	2		Ground pin.
SENSE	3	I	This pin is connected to the voltage that is monitored with the use of an external resister. The output asserts after the capacitor-adjustable delay time when VSENSE rises above 0.5V and EN is asserted. The output de-asserts after a minimal propagation delay (16µs) when VSENSE falls below V_{IT+} - V_{HYS}.
OUT	4	O	OUT is an open drain output that is immediately driven low after V_{SENSE} falls below (V_{IT+} - V_{HYS}) or the EN input is low. OUT goes high after the capacitor-adjustable delay time when V_{SENSE} is greater than V_{IT+} and the EN pin is high. Open drain device can be pulled up to 18V independent of VCC; Pull-up resisters are required for these devices.
CT	5	I	Capacitor-adjustable delay. The CT pin offers a user-adjustable delay time. Connecting this pin to a ground referenced capacitor sets the delay time for SENSE rising above 0.5V to OUT asserting. $t_{pd(r)}(s) = [C_{CT}(\mu F) \times 4] + 40\mu s$
VCC	6	I	Supply Voltage Input. Connect a 1.7V to 6.5V supply to VCC to power the device. It is good analog design practice to place a 0.1µF ceramic capacitor close to this pin.

Block Diagram

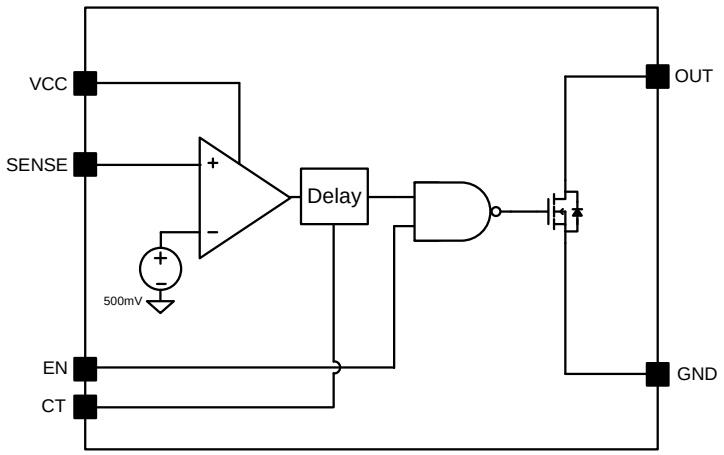


Figure2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VCC, EN, SENSE	-0.3	7	V
CT	-0.3	VCC + 0.3	
OUT (Open Drain)	-0.3	20	
OUT Current	-10	10	mA
Lead Temperature (Soldering, 10s)		260	°C
Junction Temperature, Operating	-40	125	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	293.8	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	165.1	
P_D Power Dissipation T_A = 25°C	0.34	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VCC	1.7	6.5	V
CT, EN, SENSE	0	6.5	
OUT (Open Drain)	0	18	
OUT Current	0.0003	1	mA

Electrical Characteristics

($1.7V < V_{CC} < 6.5V$, typical values are at $T_J = 25°C$ and $V_{CC} = 3.3V$, unless otherwise noted. The values are guaranteed by test, design or statistical correlation.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{CC}		1.7		6.5	V
Power on Reset Voltage	V_{POR}	V_{OL} (max) =0.2V, I_{OUT} =15μA (Note 4)		0.72		V
Supply Current (into VCC pin)	I_{CC}	V_{CC}=3.3V, T_A=25°C, no load		9	12	μA
		V_{CC}=3.3V, T_A=125°C, no load		12	14	μA
		V_{CC}=6.5V, T_A=25°C, no load		11	13.5	μA
		V_{CC}=6.5V, T_A=125°C, no load		14	16	μA
Positive-going Input Threshold Voltage	V_{IT+}	V_{SENSE} rising, -40°C <T_J < 125°C	0.495	0.5	0.505	V
Hysteresis Voltage	V_{HYS}	V_{SENSE} falling		5		mV
SENSE Input Current	I_{SENSE}	V_{SENSE} = 0V to V_{CC} (Note 5)	-15		15	nA
CT Pin Charge Current	I_{CT}		260	310	360	nA
CT Pin Comparator Threshold Voltage	V_{CT}		1.18	1.238	1.299	V
CT Pin Down Resistance	R_{CT}			200		Ω
Low-level Input Voltage	V_{IL}				0.4	V
High-level Input Voltage	V_{IH}		1.4			V
Under Voltage Lockout	V_{UVLO}	V_{CC} falling, (Note 6)	1.3		1.7	V
EN Leakage		EN/#EN = V_{CC} or GND	-100		100	nA
Low-level Output Voltage	V_{OL}	V_{CC} ≥ 1.2V, I_{SINK} = 90μA			0.3	V
		V_{CC} ≥ 2.25V, I_{SINK} = 0.5mA			0.3	V
		V_{CC} ≥ 4.5V, I_{SINK} = 1mA			0.4	V
Open-drain Output Leakage Current	$I_{LKG(OD)}$	V_{OUT} high impedance = 18V		20		nA

Timing Requirements

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SENSE (rising) to OUT Propagation Delay	$t_{PD(r)}$	V_{SENSE} rising, C_{CT} = open		40		μs
		V_{SESNE} rising, C_{CT} = 0.047μF		190		ms
SENSE (falling) to OUT Propagation Delay	$t_{PD(f)}$	V_{SENSE} falling		16		μs
Start-up Delay		(Note 7)		50		μs
EN Pin Minimum Pulse Duration	t_W		1			μs
EN Glitch Rejection	t_{EN_GLH}			100		ns
EN to OUT Delay Time (Output Disable)	t_{d_off}	EN de-asserted to output de-asserted		200		ns
EN to VOUT Delay Time	t_{d_fix}	EN asserted to output asserted delay		200		ns

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions

Note 4: The lowest supply voltage (VCC) at which output is active (OUT is low); t_{r_VCC} > 15μs/V. below V_{POR}, the output cannot be determined.

Note 5: Specified by design.

Note 6: When VCC falls below the UVLO threshold, the output de-asserts (OUT goes low). Below V_{POR}, the output cannot be determined

Note 7: During power on, V_{CC} must exceed 1.7 V for at least 50μs (plus propagation delay time, $t_{PD(r)}$) before output is in the correct state.

Timing Sequence:

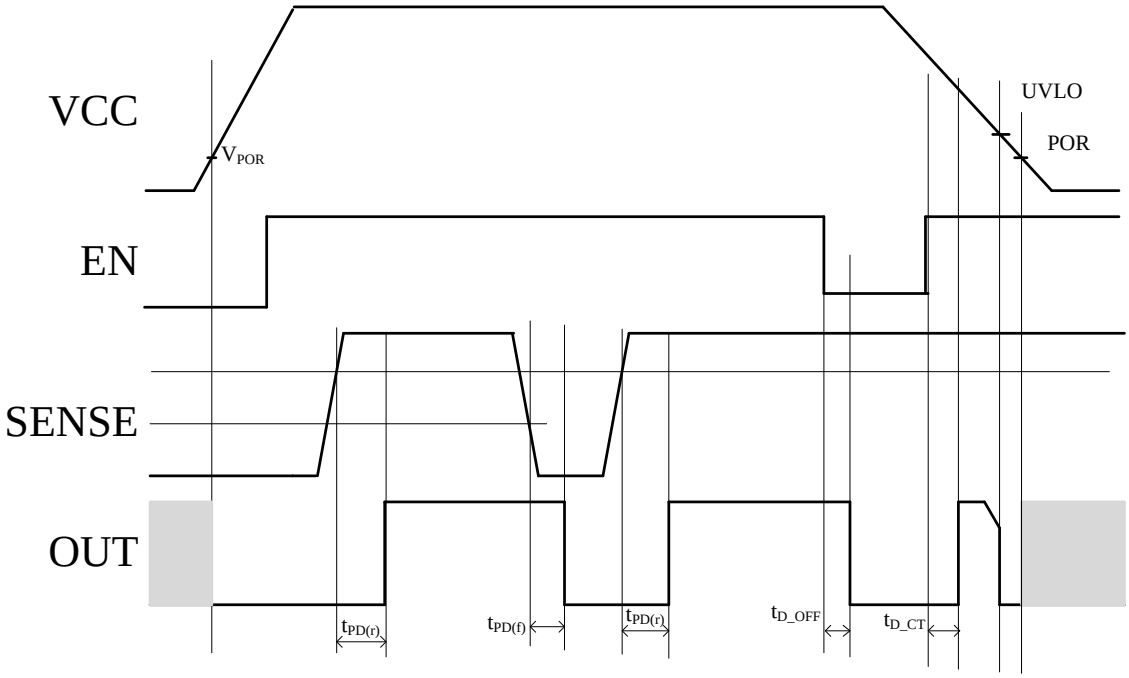
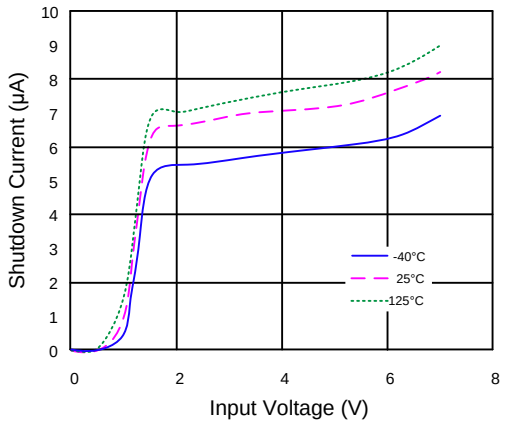


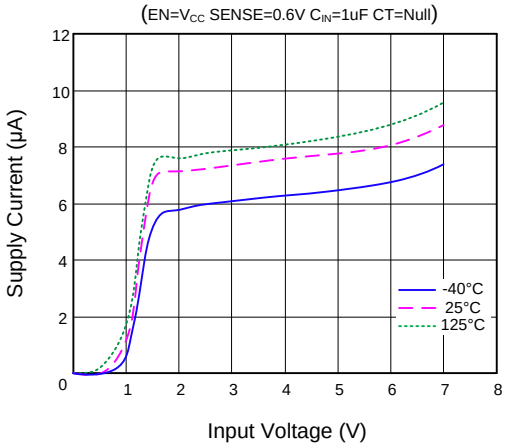
Figure3. SY28637F Timing Sequence

Typical Operating Characteristics

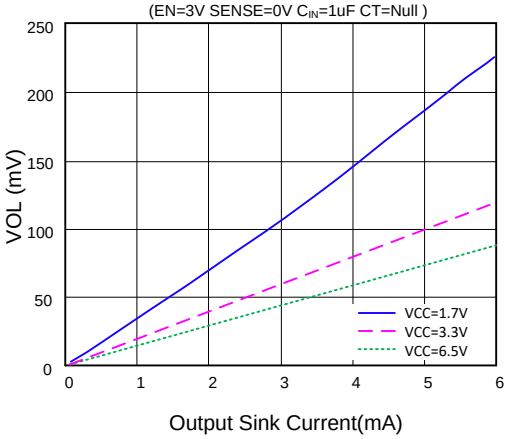
Shutdown Current vs. Input Voltage
(EN=0V SENSE=0V C_{IN}=1uF CT=Null)



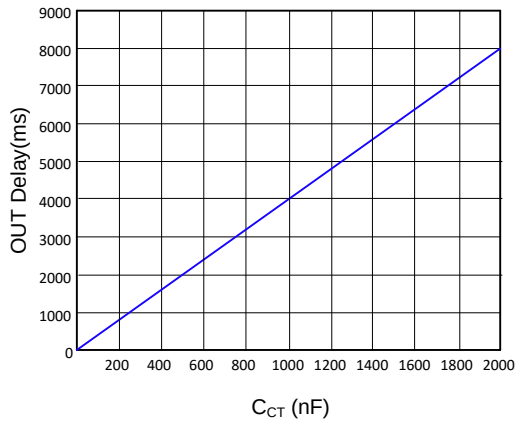
Supply Current vs. Input Voltage
($EN=V_{CC}$ SENSE=0.6V C_{IN}=1uF CT=Null)



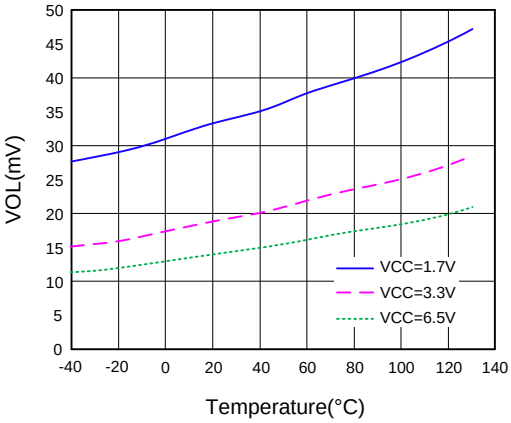
Output Voltage Low vs. Output Sink Current
(EN=3V SENSE=0V C_{IN}=1uF CT=Null)



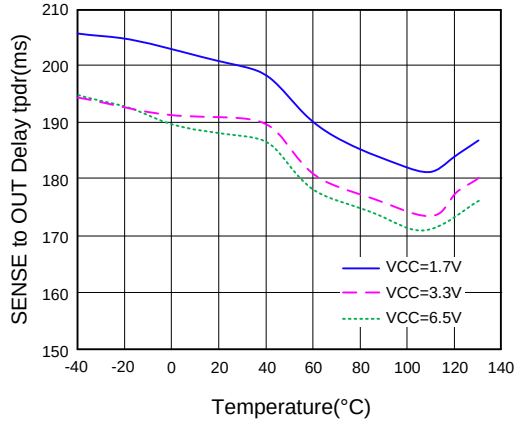
SENSE to OUT Delay vs. C_{CT}
(V_{CC}=3.3V EN=3V SENSE=0.6V C_{IN}=1uF)



Output Voltage Low vs. Temperature
(EN=3V SENSE=0V C_{IN}=1uF CT Null Output sink current=1mA)

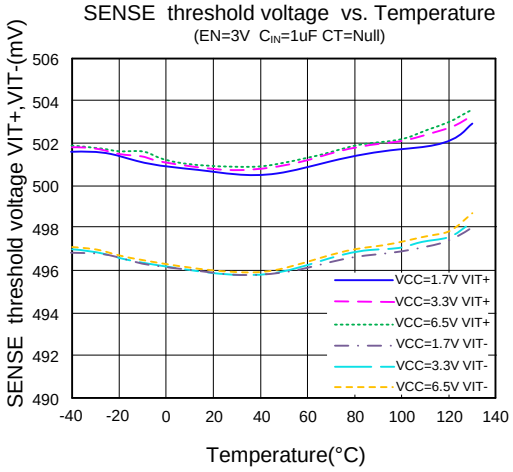


SENSE to OUT Delay vs. Temperature
(EN=3V SENSE=0VC_{IN}=1uF CT=47nF Output sink current=1mA)



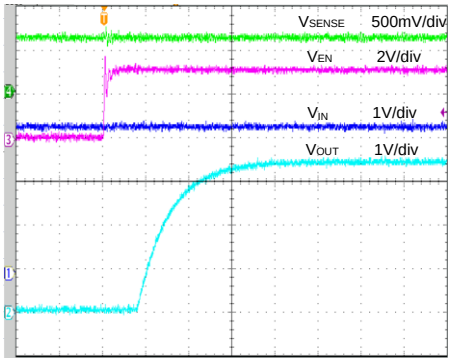
SENSE threshold voltage vs. Temperature

(EN=3V C_{IN}=1uF CT=Null)



Startup from Enable

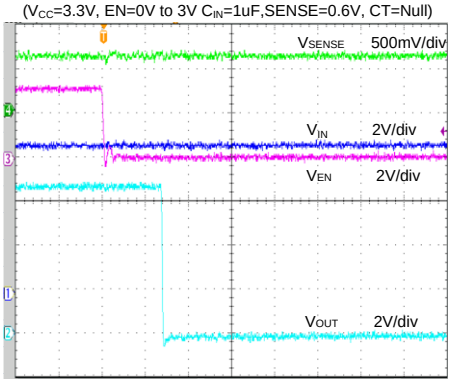
(V_{CC}=3.3V, EN=0V to 3V C_{IN}=1uF,SENSE=0.6V, CT=Null)



Time (200ns/div)

Shutdown from Enable

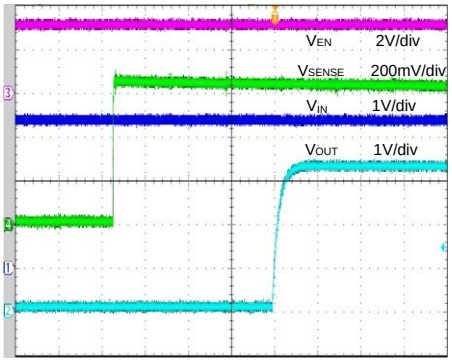
(V_{CC}=3.3V, EN=0V to 3V C_{IN}=1uF,SENSE=0.6V, CT=Null)



Time (100ns/div)

Startup from SENSE

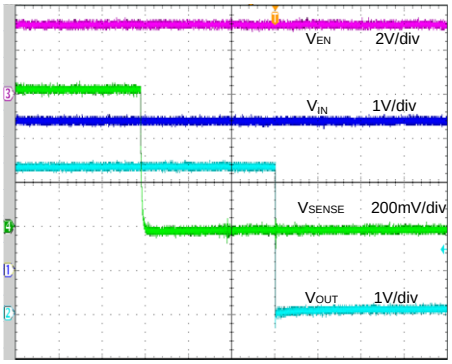
(V_{CC}=3.3V, EN=3V,SENSE=0V to 0.6V, C_{IN}=1uF, CT=Null)



Time (10μs/div)

Shutdown from SENSE

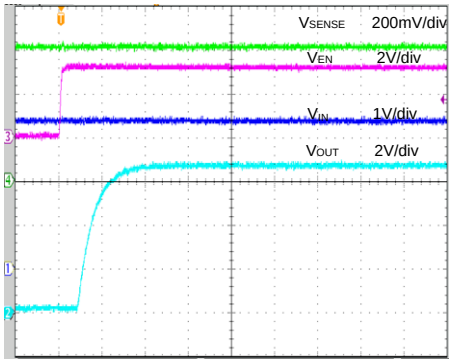
(V_{CC}=3.3V, EN=3V,SENSE=0.6V to 0V, C_{IN}=1uF, CT=Null)



Time (2μs/div)

Startup from Enable

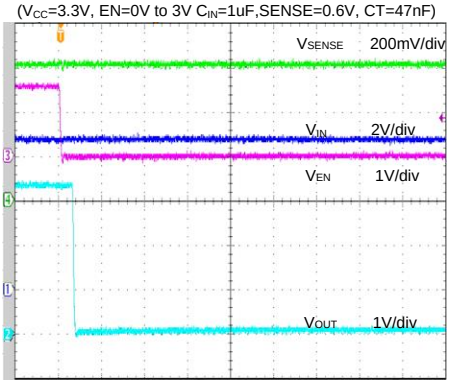
(V_{CC}=3.3V, EN=0V to 3V C_{IN}=1uF,SENSE=0.6V, CT=47nF)



Time (200ns/div)

Shutdown from Enable

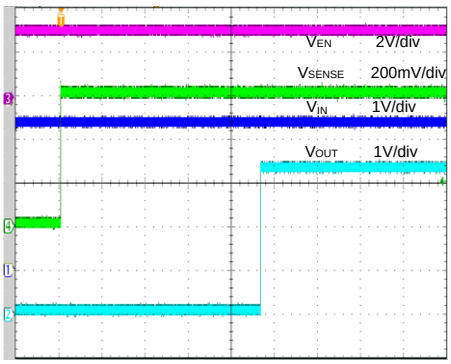
(V_{CC}=3.3V, EN=0V to 3V C_{IN}=1uF,SENSE=0.6V, CT=47nF)



Time (400ns/div)

Startup from SENSE

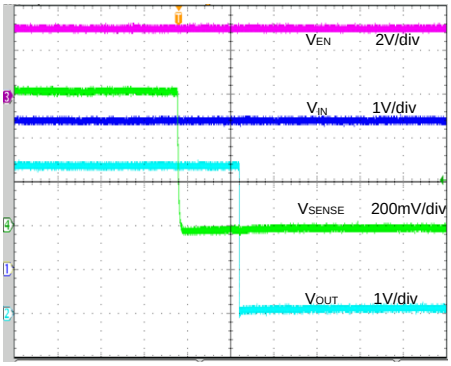
(V_{CC}=3.3V, EN=3V,SENSE=0V to 0.6V, C_{IN}=1uF, CT=47nF)



Time (40ms/div)

Shutdown from SENSE

(V_{CC}=3.3V, EN=3V,SENSE=0.6V to 0V, C_{IN}=1uF, CT=47nF)



Time (4μs/div)

Application Information

The SY28637F is a compact supervisory circuit that monitors voltages greater than 500mV with 0.25% threshold accuracy. The output assertion delay time can be adjusted using an external capacitor. The device features a logic high enable pin to control the power on and off the internal logic.

Operating within a voltage range of 1.7V to 6.5V, the SY28637F has a typical quiescent current of 9μA and an open-drain output rated at 18V.

The device is available in an ultra-small DFN 1.45mm×1.0mm–6pin package and is fully specified for operation over a temperature range of T_J=-40°C to 125°C.

Table1. SY28637F Truth Table

Conditions		Output	Status
ENABLE = high	SENSE < VIT+	OUT = low	Output not asserted
ENABLE = low	SENSE < VIT+	OUT = low	Output not asserted
ENABLE = low	SENSE > VIT+	OUT = low	Output not asserted
ENABLE = high	SENSE > VIT+	OUT = high	Output asserted after delay

SENSE Input Pin

The SENSE input pin is designed to monitor system voltages greater than 0.5V. When the voltage on this pin reaches the threshold voltage (VIT+), and the ENABLE input is high, the output will be asserted after a delay set by a capacitor-adjustable timer. The output is de-asserted when the voltage at the SENSE pin falls below (VIT+ - Vhys).The comparator features built-in hysteresis to ensure smooth transitions between output assertions and de-assertions. While not typically necessary, a 1nF to 10nF bypass capacitor at the SENSE input is recommended for high noise environments, in order to mitigate sensitivity to transients and layout parasitics. The desired threshold voltage can be calculated using the following equation:

$V_{TARGET}=(1+R_1/R_2)\times0.5(V)$ (1)

CT Output Delay Time

The delay time can be programmed by adding an external capacitor between the CT pin and the ground. If the CT pin is floating, the device will use the internally set delay of 40μs. If required, the delay time can be extended to a value determined by the following equation:

$tpd(r)\ (s) = [C_{CT}(\mu F)\times4] + 40\ \mu s$ (2)

The reset delay time is determined by the duration required for the on-chip, precision 310nA current source to charge an external capacitor to 1.24V. The internal current source is enabled when the voltage on the SENSE pin exceeds VIT+ and ENABLE is set high, initiating the charging of the external capacitor. Once the voltage across a capacitor reaches 1.24V, the OUT signal will be asserted. The use of a good dielectric ceramic capacitor is recommended for most applications. Note that stray capacitance around this pin could introduce errors when compared with the calculated reset delay time.

Output Pin (OUT)

In a typical application, the output is connected to a reset/enable input of the processor (DSP, CPU, FPGA, ASIC, etc.) or to the enable input of a voltage regulator.

The SY28637Ffeatures an open-drain output. A pull-up resistor must be used to ensure proper interfacing between the OUT pin and the circuit it controls. By connecting the pull-up resistor to an adequate voltage rail, OUT can be connected to other devices using different interface voltage levels. The outputs can be pulled up to 18V independent of the supply voltage (VCC). To ensure proper voltage levels, some thought should be given to choosing the correct pull-up resistor value. The ability to sink current is determined by the supply voltage; as an example, if VCC = 5V and the desired output pull-up rails is 18 V, then to obtain a sink current of 1 mA or less (as mentioned in the Electrical Characteristics section), the pull-up resistor value should be greater than 18 kΩ. Multiple devices can be used to monitor different voltage levels in a system and their outputs can be OR-wired, to create a single logic control signal.

Enable Function

An external logic signal from processors can control the enable input of the SY28637F, turning the output on or off. The SY28637F features an active-high enable input (ENABLE). When ENABLE is driven high, the OUT pin will be in high-impedance state. The threshold levels for ENABLE are 0.4V (maximum) when low, and 1.4V (minimum) when high, allowing it to be driven by a system supply of 1.5V or higher.

Active high input. Driving ENABLE low immediately makes OUT go low-impedance. With VSENSE greater than VIT+, driving ENABLE high causes OUT to go high-impedance after 0.2μs.

PCB Layout Guide

For best performance of the SY28637F, the following guidelines must be strictly followed:

1. Place the VCC decoupling capacitor close to the device.

2. Input and output capacitors should be placed closed to the IC and connected to ground plane to reduce noise coupling.

3. SENSE pin is a sensitive pin. Keep SENSE trace far away from the trace or plane that has large dv/dt. The divider resistor should be placed as close as possible to the SENSE pin.

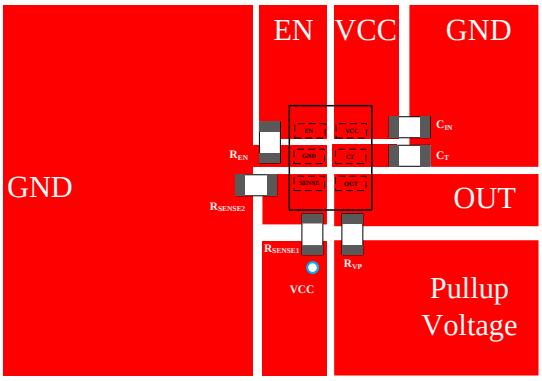
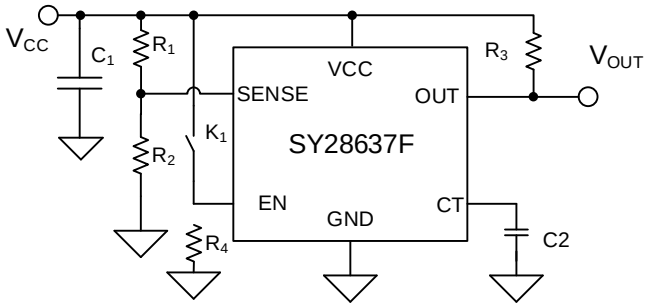


Figure4. PCB Layout Suggestion

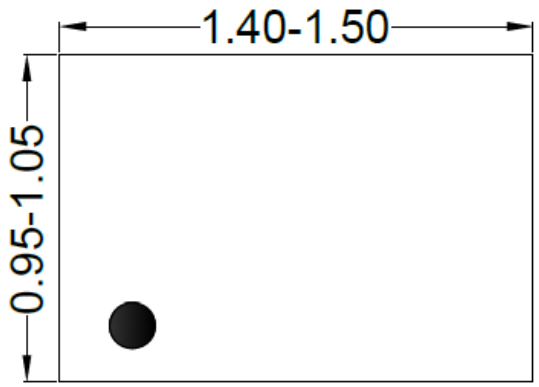
Schematic



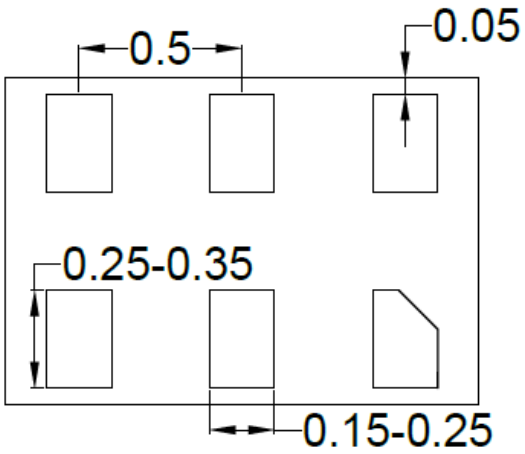
BOM List

Designator	Description	Part Number	Manufacturer
C1	1μF/50V, 0603, X5R	GRM188R61H105K	Murata
C2	47nF/25V,0603,X5R	GRM188R71H473K	Murata
R1	500kΩ, 0603		
R2	100kΩ, 0603		
R3	10kΩ, 0603		
R4	1MΩ, 0603		

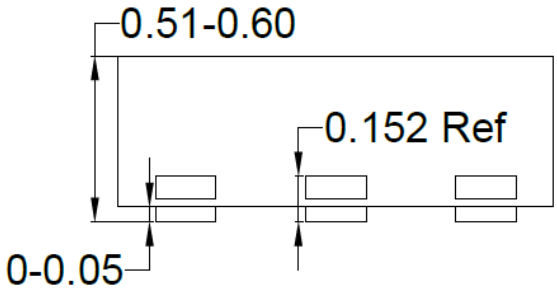
DFN1.45×1-6 Package Outline Drawing



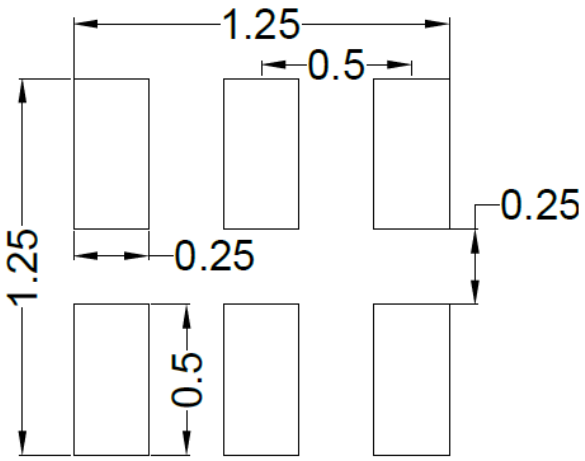
Top View



Bottom View



Side View

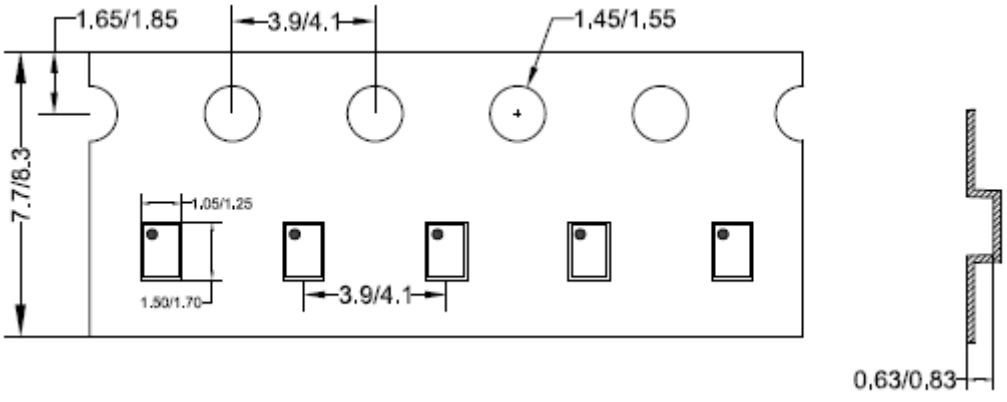


Recommended PCB Layout
(only for reference)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

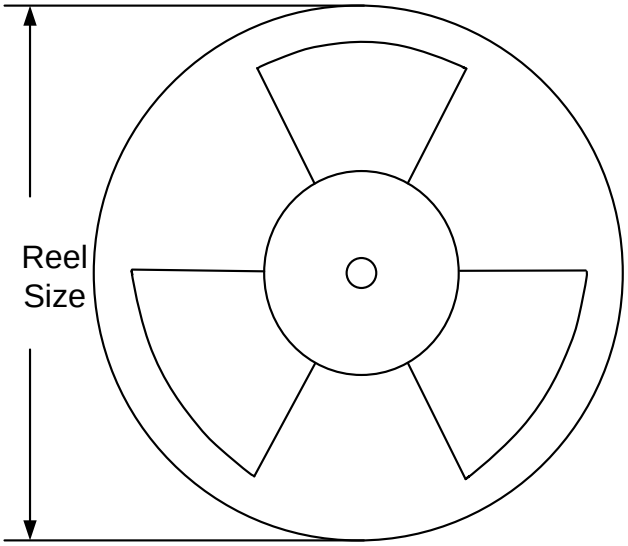
Tape and Reel Information

1. Tape Dimensions and Pin1 Orientation



Feeding direction ⟶

2. Reel Dimensions



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN1.45×1	8	4	7"	400	160	3000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
July 10, 2025	Revision 1.0A	1. The logic gate in the Block Diagram changed from AND gate to NAND gate (Page 3) 2. Language improvements for clarity.
Jan.04, 2023	Revision 1.0	Initial Production Release
Jan.04, 2022	Revision 0.9	Initial Release

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