SY20798

PD3.0, QC3.0/2.0, SCP, FCP, AFC and Apple 2.4A, High Voltage and Current, Bi-directional Regulator for Li-Ion Battery Power Bank Application

1 General Description

The SY20798 is a 4.6-13V input bi-directional regulator designed for single cell Li-Ion battery power bank application. It supports multiple charging protocols, including PD3.0, QC3.0/2.0, SCP, FCP, AFC and Apple 2.4A. It also integrates the Battery Fuel Gauge Indicator, Light Load Detection and Load Insert Detection to provide a fully scheme for power bank application.

Advanced bi-directional energy flow control is adopted to achieve battery charging and discharging alternately. If the external power supply is present, the SY20798 will run in Charging Mode with fully protection function; if the external power supply is absent, the SY20798 will run in Discharging Mode with total output capability up to 22.5W.

The SY20798 integrates 4 N-Channel MOSFETs for 4 Ports to achieve charging and discharging path management. A half bridge with quasi-fixed high switching frequency is integrated to achieve power conversion for battery charging and battery discharging. All of them adopt N-Channel MOSFETs with 18V rating and extremely low $R_{DS(ON)}$ to optimize operation efficiency and extend the life of battery.

The SY20798 is available in QFN5×5-32 package to minimize the size of PCB layout for wide portable applications.

Ordering Information

SY20798 □(□□□)

- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY20798QEQ	QFN5×5-32	----

2 Features

- Integrated 6 N-Channel MOSFETs with 18V Voltage Rating and Extremely Low $R_{DS(ON)}$
- Maximum 5A Battery Charging Current
- Maximum 22.5W Output Power
- Trickle Current / Constant Current / Constant Voltage for Charging
- Programmable Constant Charge Voltage and Termination Current
- USB Port Identifier for Various Input Current Limit
- Programmable Battery Internal Resistor Compensation for Battery Fuel Gauge Indicator
- Up to 4 LEDs Battery Fuel Gauge Indicator with Programmable Threshold
- Support BC1.2 and PD3.0 for Input Ports
- Support Fast Charging Protocols PD3.0, QC3.0/2.0, SCP, FCP, AFC and Apple 2.4A for Output Ports
- Support Type-C DRP with Try.SRC
- Support TCPC Interface for the Update of PD Protocol
- Load Insert Detection
- Light Load Auto-Sleep
- Integrated Input OVP/UVP Protection
- Integrated Output OVP/OCP/SCP Protection
- Battery UTP/OTP/SCP/OVP Protection
- Thermal Shutdown Protection
- Max 100uA Quiescent Current in Sleep Mode

3 Applications

- Single Cell Li-Ion Power Bank
- Portable Device with Single Cell Battery Pack

4 Typical Applications

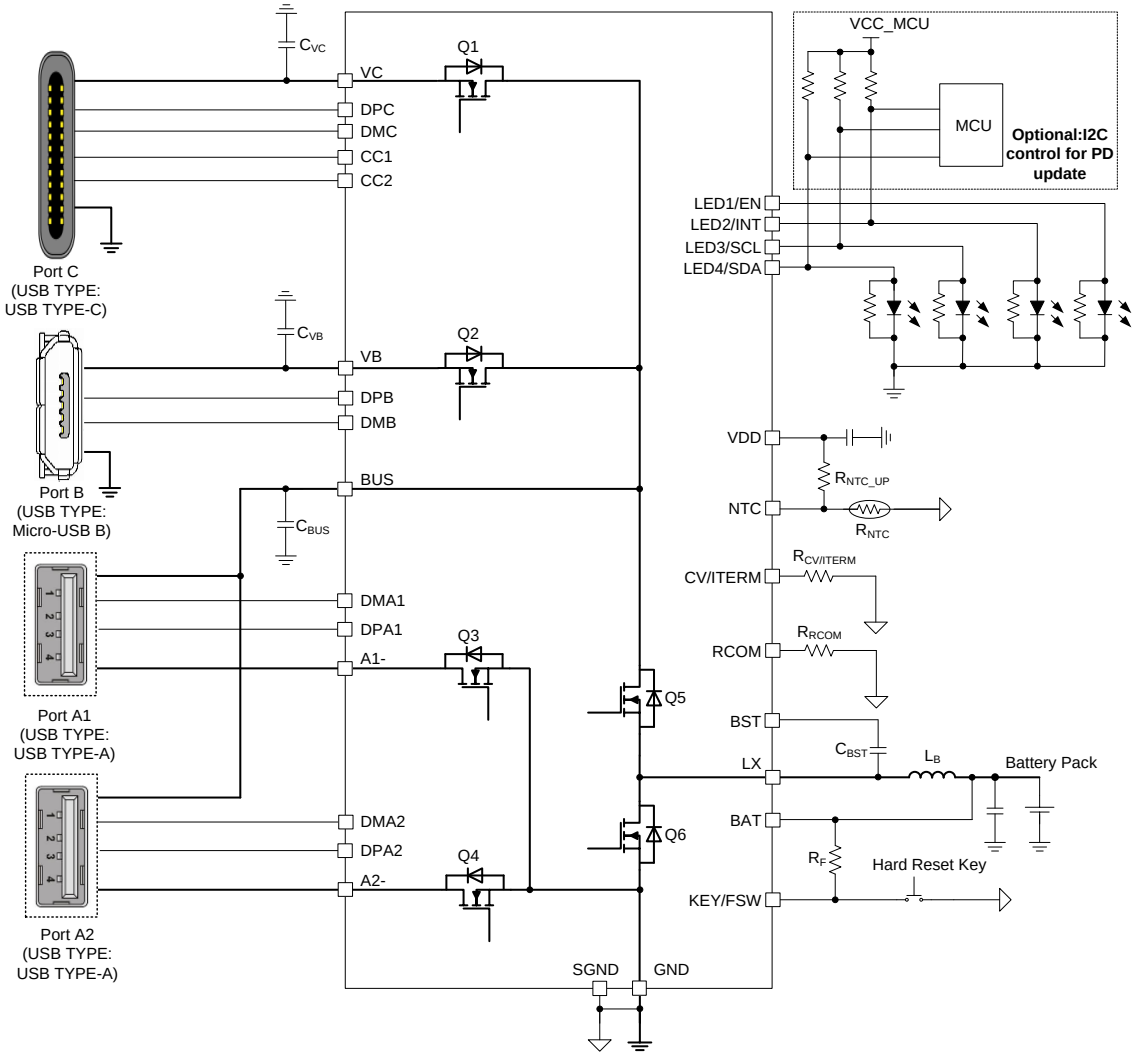

Figure 1. Application for Single Cell Li-Ion Power Bank

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5 Pin Configuration and Functions

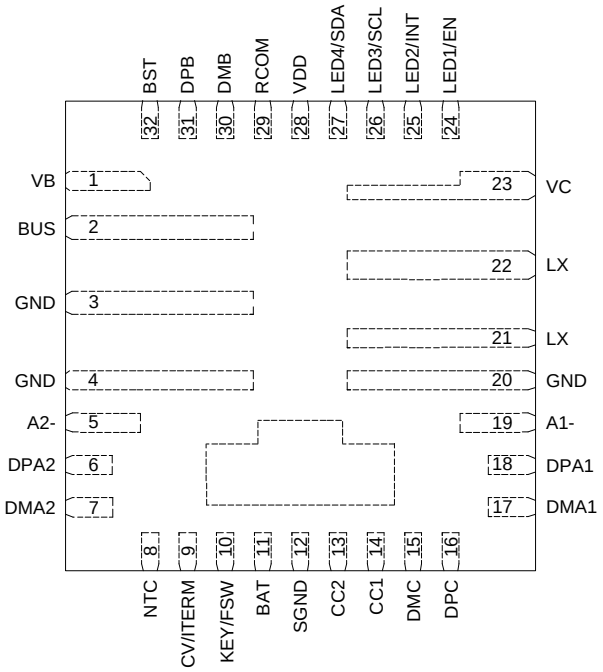


Figure 2. QFN5×5-32 in top view

Top Mark: FTC*xyz* (device code: **FTC**, ***x=year code, y=week code, z= lot number code)***

Table 1. Pin Functions

Name	PIN Number	Description
VB	1	Positive power supply pin for the input Port B. Connect a MLCC from this pin to ground to decouple high frequency noise.
BUS	2	Input or output point of half bridge. Connect a MLCC from this pin to ground to decouple high frequency noise.
GND	3,4,20	Power ground pins.
A2-	5	Negative power pin for the output Port A2.
DPA2	6	D+ pin for the output Port A2.
DMA2	7	D- pin for the output Port A2. DPA2 and DMA2 support QC3.0/2.0, SCP, FCP, AFC and Apple 2.4A.
NTC	8	Battery thermal protection sense pin.
CV/ITERM	9	Battery constant charging voltage and termination charging current set pin.
KEY/FSW	10	Function1: KEY pin. Connect a key from this pin to ground. Function2: Switching frequency set pin. Connect a resistor from BAT to KEY to set the switching frequency of boost converter.
BAT	11	Battery positive pin. Also connect to the inductor terminal.
SGND	12	Signal ground pin. Keep star-connected to power ground pin.
CC2	13	Multifunction configuration channel interface pin for the input and output Port C. Functions include connector polarity, end-device connection detect, current capabilities, and PD communication.
CC1	14	Multifunction configuration channel interface pin for the input and output Port C. Functions include connector polarity, end-device connection detect, current capabilities, and PD communication.

DMC	15	D- pin for the input and output Port C. DPC and DMC support QC3.0/2.0, SCP, FCP, AFC and Apple 2.4A in Discharging Mode. Support BC1.2 detection in Charging Mode.
DPC	16	D+ pin for the input and output Port C.
DMA1	17	D- pin for the output Port A1. DPA1 and DMA1 support QC3.0/2.0, SCP, FCP, AFC and Apple 2.4A.
DPA1	18	D+ pin for the output Port A1.
A1-	19	Negative power pin for the output Port A1.
LX	21,22	Switch node pins. These pins are shorted internally. Connect an external inductor between LX and BAT.
VC	23	Positive power pin for the input and output Port C. Connect a MLCC from this pin to ground to decouple high frequency noise.
LED1/EN	24	Function1: LED1 driver for Battery Fuel Gauge Indicator. It is also used as Battery Level Threshold adjustment. Function2: Battery Depletion Threshold set pin. Function3: TCPC Interface enable pin.
LED2/INT	25	Function1: LED2 driver for Battery Fuel Gauge Indicator. It is also used as Battery Level Threshold adjustment. Function2: Open-drain Interrupt output when the TCPC Interface is enabled. Connect LED2/INT to the logic rail through a 10kΩ resistor. Low: Alert. IC indicates that Alert Status change has occurred. The MCU shall read the Alert Register to determine what event is triggered. High: No Alert.
LED3/SCL	26	Function1: LED3 driver for Battery Fuel Gauge Indicator. It is also used as Battery Level Threshold adjustment. Function2: I2C Interface clock when the TCPC Interface is enabled. Connect SCL to the logic rail through a 10kΩ resistor.
LED4/SDA	27	Function1: LED4 driver for Battery Fuel Gauge Indicator. It is also used as Battery Level Threshold adjustment. Function2: I2C Interface data when the TCPC Interface is enabled. Connect SDA to the logic rail through a 10kΩ resistor.
VDD	28	Internal Linear Regulator output. VDD is the output of 3.3V Linear Regulator. Connect a 1μF ceramic capacitor from VDD to GND.
RCOM	29	Battery Internal Resistor Compensation pin. This pin is used to compensate the voltage drop caused by battery internal resistor for Battery Fuel Gauge Indicator in Discharging Mode.
DMB	30	D- pin for the input Port B. DPB and DMB support BC1.2 detection.
DPB	31	D+ pin for the input Port B.
BST	32	Boot strap pin. Connect a 0.1μF MLCC from this pin to LX.
Thermal Pad	-	Exposed pad beneath the IC. Always solder thermal pad to the board, and have vias on the thermal pad plane connecting to power ground planes. It serves as a thermal pad to dissipate the heat.

6 Functional Block Diagram

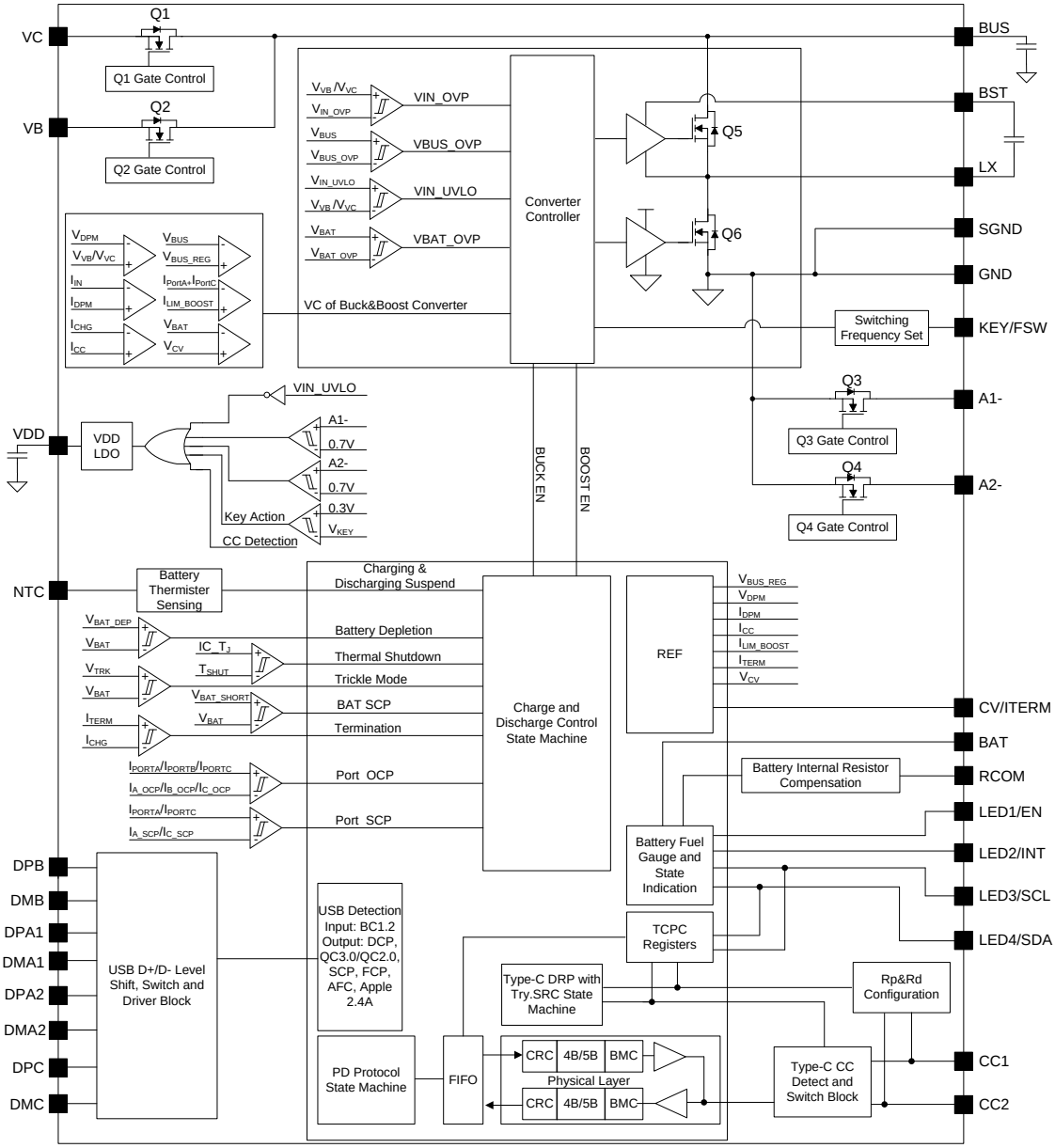


Figure 3. Functional Block Diagram

7 Specifications

7.1 Absolute Maximum Ratings (Note 1)

VB, VC, BUS, LX, A1-, A2-, RCOM, CV/ITERM---------- -0.5V to 18V
CC1, CC2, DPA1, DMA1, DPA2, DMA2, DPB, DMB, DPC, DMC ---------- -0.5V to 18V
LED1/EN, LED2/INT, LED3/SCL, LED4/SDA ---------- -0.5V to 18V
VDD, BST-LX, NTC ---------- -0.5V to 3.6V
KEY/FSW, BAT ---------- -0.5V to 5.5V
Package Thermal Resistance (Note 2)
Θ_{JA} ---------- 43 °C/W
Θ_{JC} ---------- 16 °C/W
Junction Temperature Range ---------- -40°C to +150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 125°C

7.2 Recommended Operating Conditions (Note 3)

VB, VC, BUS, A1-, A2-, LED1/EN, LED2/INT, LED3/SCL, LED4/SDA ---------- 0V to 16V
CC1, CC2, DPA1, DMA1, DPA2, DMA2, DPB, DMB, DPC, DMC ---------- 0V to 16V
LX ---------- -0.3V to 16V
KEY/FSW, BAT ---------- 0V to 5V
Others ---------- 0V to 3.3V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

7.3 Electrical Characteristics

(T_A=25°C, T_A=T_J, L_B=2.2μH, C_{BUS}=30μF, C_{VB}=10μF, C_{VC}=10μF, R_{NTC_UP}=10kΩ, R_{NTC}=10kΩ(103-AT), unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Quiescent Current						
I_{BAT}	Battery discharge current in Sleep Mode	V_{BAT}=4.2V, Sleep Mode, V_{BUS}≤V_{BAT}			100	μA
I_{BUS}	Input quiescent current of Port B and Port C	Charging disabled, measured from VB or VC, V_{VB}>V_{IN_UVLO} or V_{VC}>V_{IN_UVLO}		3.8		mA
Port B and Port C Power Up						
V_{IN_UVLO}	VB and VC UVLO threshold	Rising edge	4.2		4.55	V
V_{IN_UVHYS}	VB and VC UVLO hysteresis	Falling edge		100		mV
LDO Output						
V_{VDD}	VDD LDO output voltage	V_{BUS}=5V	3.2	3.3	3.4	V
I_{VDD}	VDD LDO current limit	V_{VDD}=3V	80			mA
Ports Management and Protection						
$V_{IN\_OVP\_5V}$	VB and VC OVP threshold in 5V Mode	Rising edge	5.7		6	V
$V_{IN\_OVP\_HYS\_5V}$	VB and VC OVP hysteresis in 5V Mode	Falling edge		0.1		V
$V_{IN\_OVP\_9V}$	VB and VC OVP threshold in 9V Mode	Rising edge	9.8		10.3	V
$V_{IN\_OVP\_HYS\_9V}$	VB and VC OVP hysteresis in 9V Mode	Falling edge		0.22		V
$V_{IN\_OVP\_12V}$	VB and VC OVP threshold in 12V Mode	Rising edge	13		13.7	V
$V_{IN\_OVP\_HYS\_12V}$	VB and VC OVP hysteresis in 12V Mode	Falling edge		0.29		V
I_{A_OCP}	Port A1 and Port A2 output OCP threshold	Rising edge	3.1	3.4	3.8	A
I_{C_OCP}	Port C input OCP threshold	Rising edge	3.6	4	4.4	A
I_{B_OCP}	Port B input OCP threshold	Rising edge	3.6	4	4.4	A
I_{LIGHT}	Port A1 and Port A2 light load threshold	Falling edge	25	50	75	mA
Port FET						
R_{PORTC}	$R_{DS(ON)}$ of Port C blocking NFET Q1			25		mΩ
R_{PORTB}	$R_{DS(ON)}$ of Port B blocking NFET Q2			35		mΩ
R_{PORTA1}	$R_{DS(ON)}$ of Port A1 blocking NFET Q3			25		mΩ
R_{PORTA2}	$R_{DS(ON)}$ of Port A2 blocking NFET Q4			25		mΩ
Half-Bridge Power MOSFET						
R_{HSFT}	$R_{DS(ON)}$ of High-Side NFET Q5			8		mΩ
R_{LSFT}	$R_{DS(ON)}$ of Low-Side NFET Q6			5		mΩ
Half-Bridge in Buck Mode						
Voltage Bias						
V_{CHG_OP}	Supply voltage for battery charging		4.6		13	V

Input Voltage and Current Regulation						
V_{DPM}	Input voltage regulation in Charging Mode	V_{DPM}=4.5V	4.44	4.5	4.56	V
	Input voltage regulation in Bypass Mode and output ports are both DCP	V_{DPM}=4.75V	4.65	4.75	4.825	V
	Input voltage regulation in Bypass Mode and at least one output port is Apple 2.4A	V_{DPM}=4.815V	4.76	4.815	4.875	V
I_{DPM}	Input current limit	I_{DPM}=0.5A	0.4	0.45	0.5	A
		I_{DPM}=1A	0.8	0.9	1	A
		I_{DPM}=2A	1.7	1.9	2.1	A
		I_{DPM}=3A	2.7	2.85	3	A
Timer						
T_{TC}	Trickle charge timeout			2		hrs
T_{FC}	Fast charge (CC and CV) timeout		20			hrs
Switching Frequency						
f_{SWBK}	Buck switching frequency			400		kHz
Battery Charging						
V_{CV}	Battery constant charge voltage	In CV mode, constant charge voltage is set to 4.2V	4.157	4.178	4.2	V
		In CV mode, constant charge voltage is set to 4.35V	4.306	4.328	4.35	V
ΔV_{RCH}	Recharge threshold voltage	V_{BAT} falling edge		100		mV
V_{BAT_OVP}	Battery OVP threshold	V_{BAT} rising edge	103%	105%	107%	V_{CV}
$V_{BAT\_OVP\_HYS}$	Battery OVP hysteresis	V_{BAT} falling edge		2%		V_{CV}
V_{TRK}	Battery trickle charge voltage threshold	V_{BAT} rising edge	2.7	2.8	2.9	V
I_{CC}	Battery constant charge current	V_{VB} or V_{VC}=5V, V_{BAT}=3.5V	4.5	5	5.5	A
I_{TC}	Battery trickle charge current	V_{VB} or V_{VC}=5V, V_{BAT}=2.5V	0.4	0.5	0.6	A
I_{TERM}	Termination current threshold	$R_{CV/ITERM}$=25kΩ(4% I_{CC})	0.14	0.2	0.24	A
		$R_{CV/ITERM}$=75kΩ(8% I_{CC})	0.32	0.4	0.48	A
Battery Short Circuit Protection						
V_{BAT_SHORT}	Battery SCP threshold	V_{BAT} falling edge	1.8		2	V
f_{FB}	Frequency fold back when battery SCP	V_{BAT}< V_{BAT_SHORT}		12.5%		f_{SWBK}
Half-Bridge in Boost Mode						
Voltage and Current Bias						
V_{BAT_DEP}	Battery depletion voltage threshold	V_{BAT} falling edge, R_{LED1}=100kΩ	3		3.15	V
		V_{BAT} falling edge, R_{LED1}=50kΩ	2.55		2.7	V
$V_{BAT\_DEP\_HYS}$	Battery depletion voltage threshold hysteresis	V_{BAT} rising edge		200		mV
V_{BUS_REG}	BUS voltage regulation in boost mode	5V mode	5.14	5.2	5.25	V
		9V mode	8.9	9	9.15	V
		12V mode	11.9	12	12.2	V
V_{BUS_OVP}	BUS OVP threshold in boost mode	V_{BUS} rising edge	107%	110%	113%	V_{BUS_REG}
$V_{BUS\_OVP\_HYS}$	BUS OVP hysteresis in boost mode	V_{BUS} falling edge		2%		V_{BUS_REG}
I_{LIM_BOOST}	Output current limit of boost converter without fast charging protocols implemented		3.6	4	4.7	A
	Output current limit of boost converter in PD3.0 mode	Current limit is set to 1A	0.85	1	1.15	A
		Current limit is set to 2A	1.85	2	2.15	A
		Current limit is set to 3A	2.85	3	3.15	A

Switching Frequency						
f_{SWBST}	Boost switching frequency	Boost frequency is set to 330kHz, R_F=56K	264	330	396	kHz
Cold/Hot Thermistor Comparator(Use 103-AT thermistor)						
Battery NTC Thermal Protection in Charging Mode						
V_{COLD},V_{T1}	Cold (0℃,T1) threshold	Rising edge	72.8%	73.4%	74%	V_{VDD}
	Cold hysteresis	Falling edge		4%		
V_{COOL},V_{T2}	Cool (15℃,T2) threshold	Rising edge	58.9%	59.5%	60.1%	
	Cool hysteresis	Falling edge		2%		
V_{HOT},V_{T3}	Hot (45℃,T3) threshold	Falling edge	32.3%	32.9%	33.5%	
	Hot hysteresis	Rising edge		4%		
Battery NTC Thermal Protection in Boost Mode						
V_{COLD}	Cold (-20℃,T_{COLD}) threshold	Rising edge	87.1%	87.6%	88.1%	V_{VDD}
	Cold hysteresis	Falling edge		0.8%		
V_{HOT}	Hot (60℃,T_{HOT}) threshold	Falling edge	22.6%	23.15 %	23.7%	
	Hot hysteresis	Rising edge		0.8%		
KEY Active Voltage						
V_{KEY}	KEY active low voltage	Falling edge			0.3	V
QC3.0/QC2.0/SCP/FCP/AFC/Apple 2.4A						
Output Apple 2.4A						
$V_{DP\_2.7V}$	D+ output voltage		2.6	2.7	2.8	V
$V_{DM\_2.7V}$	D- output voltage		2.6	2.7	2.8	V
R_{DP_PAD1}	D+ output impedance	I_{DP} =-5μA	24	30	36	kΩ
R_{DM_PAD1}	D- output impedance	I_{DM} =-5μA	24	30	36	kΩ
Output QC3.0/QC2.0						
$V_{BUS\_CONT\_RANGE}$	BUS output voltage range		5		12	V
$V_{BUS\_CONT\_STEP}$	Voltage per step in continuous mode		0.15	0.2	0.25	V
V_{DAT_REF}	Threshold for D+ to detect the presence of portable device		0.25	0.325	0.4	V
V_{SEL_REF}	Threshold for output voltage selection		1.8	2	2.2	V
Output SCP/FCP/AFC						
V_{FC_VOH}	D- valid output High	I_{DM} =-200μA	85%			V_{VDD}
V_{FC_VOL}	D- valid output Low	I_{DM} =200μA			0.4	V
V_{FC_VIH}	D- valid input High		1.4			V
V_{FC_VIL}	D- valid input Low				1	V
PD3.0						
Transmitter and Receiver Specifications (CC1, CC2)						
$V_{(TXHI)}$	Transmit High voltage	Applies to both no load condition and under the load condition	1.05	1.125	1.2	V
$V_{(TXLO)}$	Transmit Low voltage		-75		75	mV
Timing Requirements						
t_{UI}	Bit unit interval	1/f Bit rate	3.03	3.3	3.70	μs
tFall	Fall time		300			ns
fBitRate	Bit rate		270	300	330	kbps
tRise	Rise time		300			ns
I2C Logic Level and Timing						
V_{LOW}	SCL,SDA Low Level Threshold				0.4	V
V_{HIGH}	SCL,SDA High Level Threshold		1.2			V
F_{SCL}	I2C clock frequency				1000	kHz

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

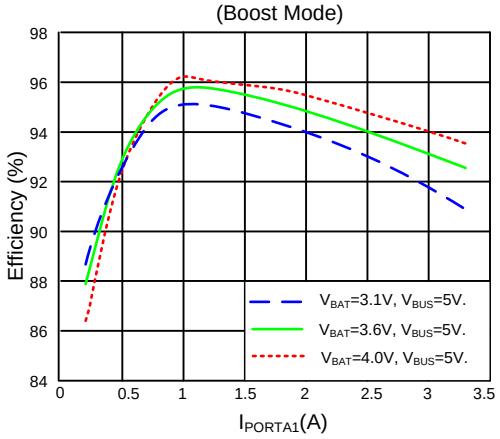
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective four-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

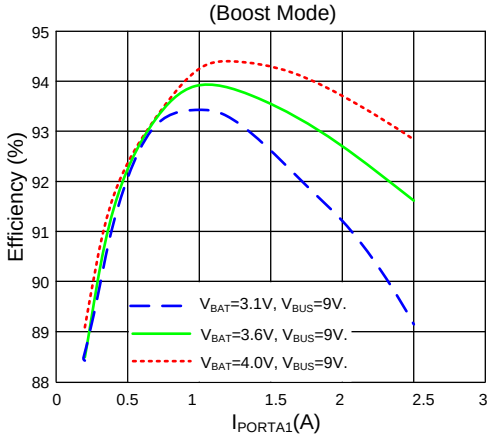
7.4 Typical Performance Characteristics

(T_A=25°C, V_{VC}=5V or V_{VB}=5V, unless otherwise specified.)

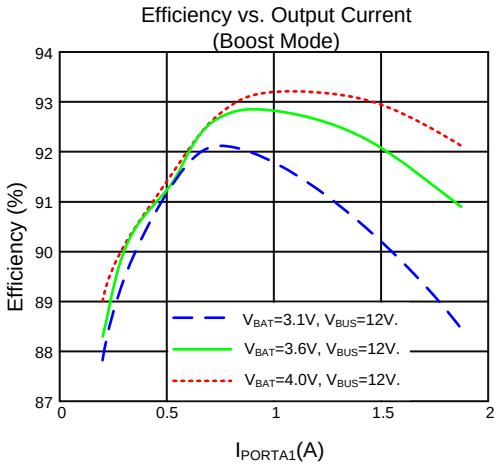
Efficiency vs. Output Current
(Boost Mode)



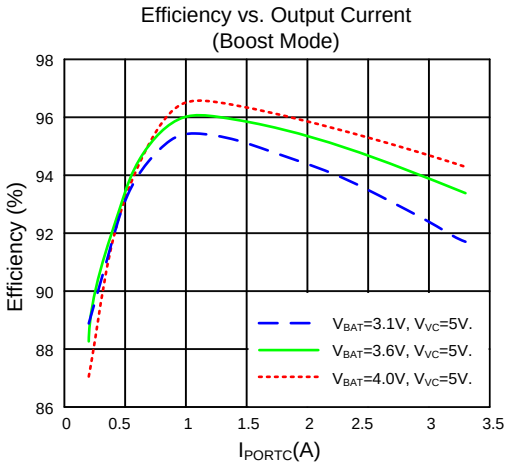
Efficiency vs. Output Current
(Boost Mode)



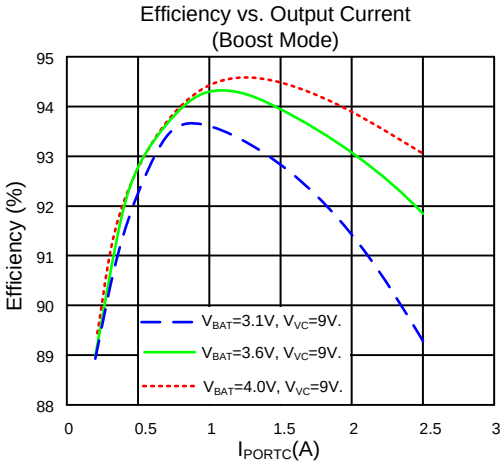
Efficiency vs. Output Current
(Boost Mode)



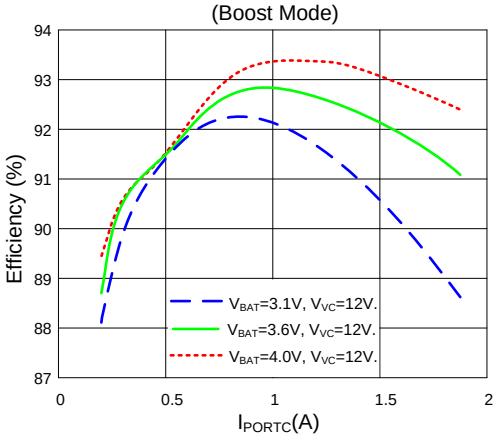
Efficiency vs. Output Current
(Boost Mode)



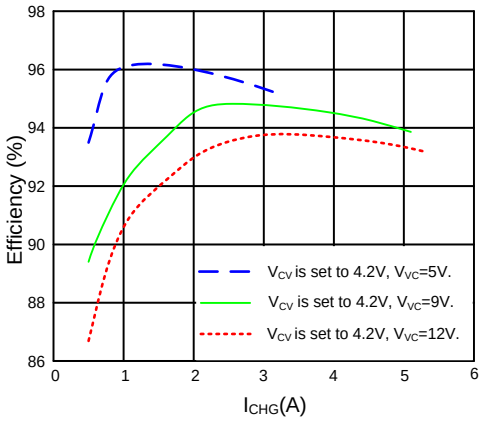
Efficiency vs. Output Current
(Boost Mode)



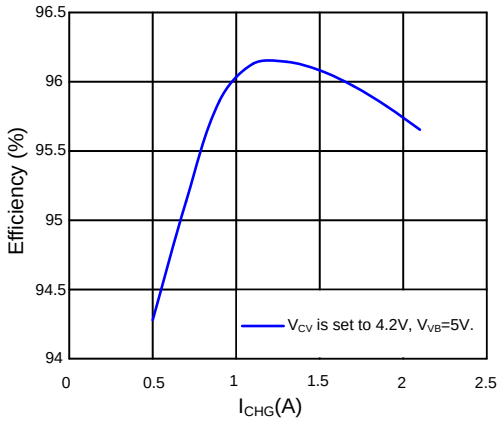
Efficiency vs. Output Current
(Boost Mode)



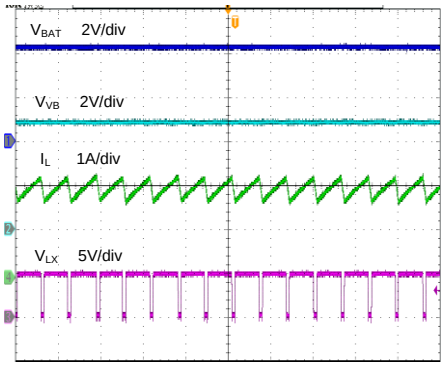
Efficiency vs. Charging Current
(Buck Mode)



Efficiency vs. Charging Current
(Buck Mode)

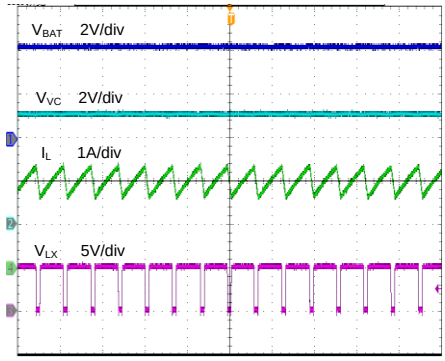


Buck Steady State
(V_{VB}=5V, I_{CHG}=2A, CV mode)



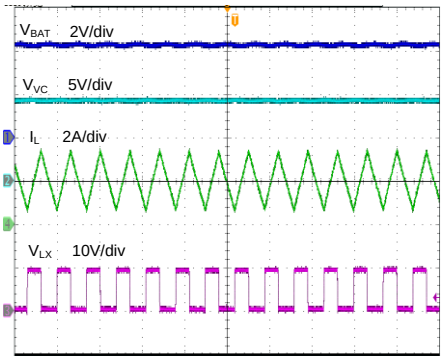
Time (4μs/div)

Buck Steady State
(V_{VC}=5V, I_{CHG}=2A, CV mode)



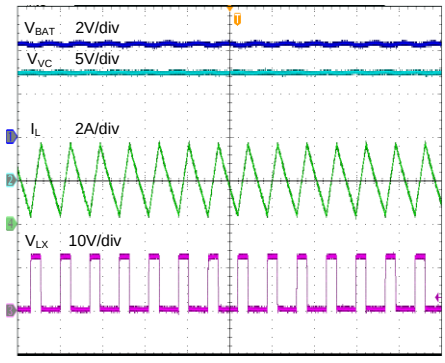
Time (4μs/div)

Buck Steady State
(V_{VC}=9V, I_{CHG}=2A, CV mode)



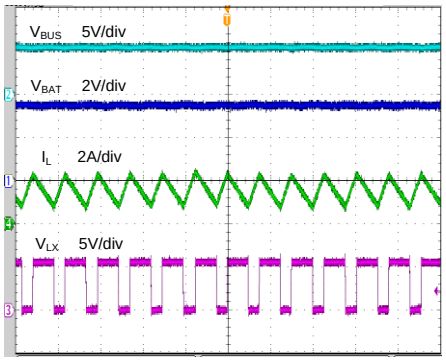
Time (4μs/div)

Buck Steady State
(V_{VC}=12V, I_{CHG}=2A, CV mode)



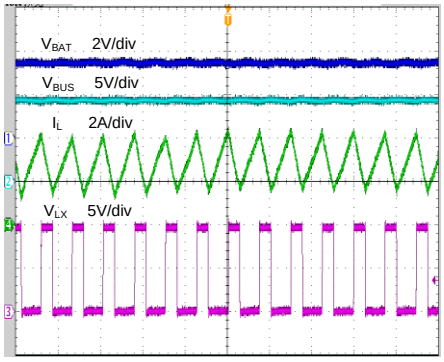
Time (4μs/div)

Boost Steady State
(V_{BAT}=3.5V, I_{PORTA1}=1A, V_{BUS}=5V)



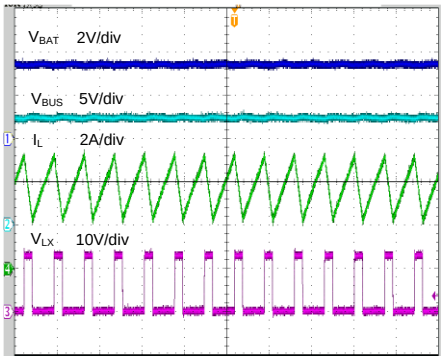
Time (4μs/div)

Boost Steady State
(V_{BAT}=3.5V, I_{PORTA1}=1A, V_{BUS}=9V)



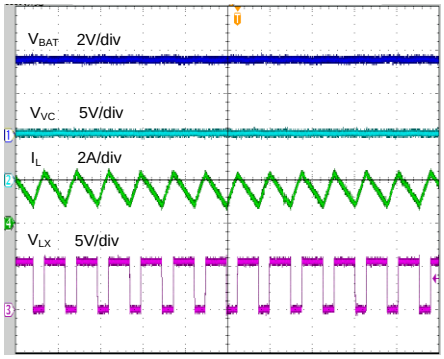
Time (4μs/div)

Boost Steady State
(V_{BAT}=3.5V, I_{PORTA1}=1A, V_{BUS}=12V)



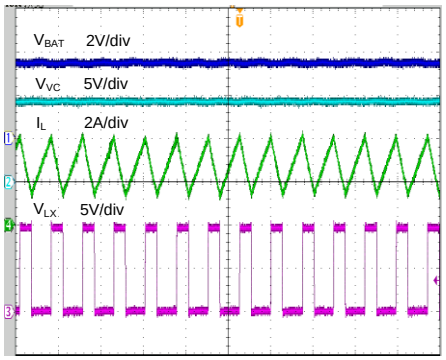
Time (4μs/div)

Boost Steady State
(V_{BAT}=3.5V, I_{PORTC}=1A, V_{VC}=5V)



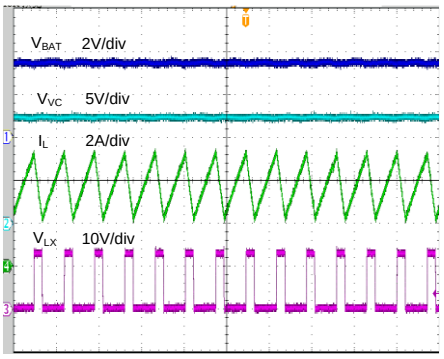
Time (4μs/div)

Boost Steady State
(V_{BAT}=3.5V, I_{PORTC}=1A, V_{VC}=9V)



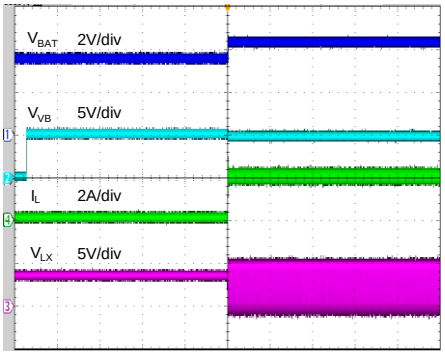
Time (4μs/div)

Boost Steady State
(V_{BAT}=3.5V, I_{PORTC}=1A, V_{VC}=12V)



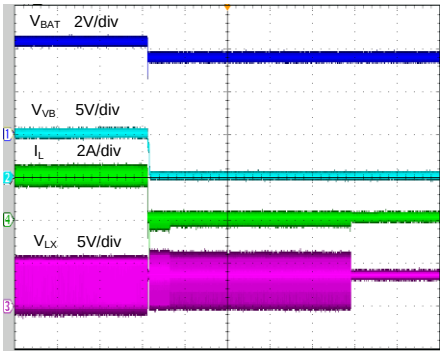
Time (4μs/div)

Buck VB Power On
(V_{VB}=5V, I_{CHG}=2A, CV mode)



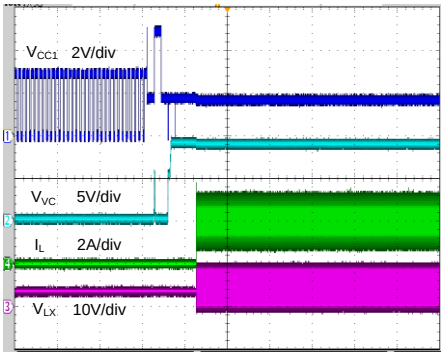
Time(200ms/div)

Buck VB Power Off
(V_{VB}=5V, I_{CHG}=2A, CV mode)



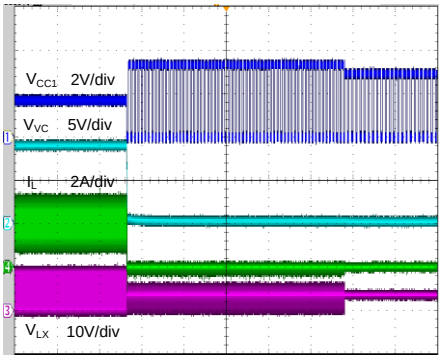
Time(1s/div)

Buck VC Power On
(V_{VC}=9V, I_{CHG}=2A, CV mode (Attach PD Adapter))



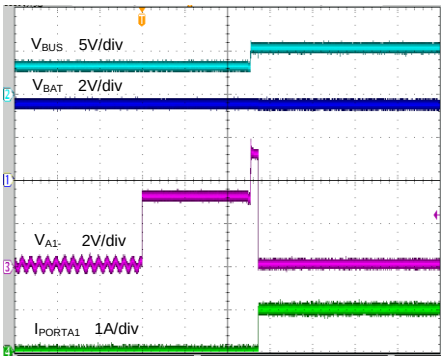
Time(1s/div)

Buck VC Power Off
(V_{VC}=9V, I_{CHG}=2A, CV mode (Detach PD Adapter))



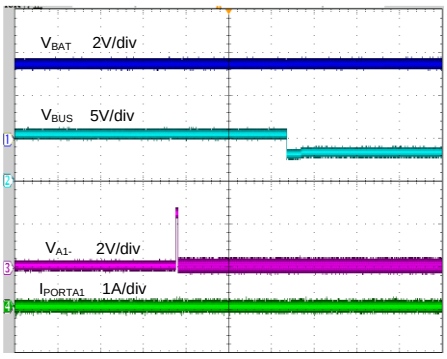
Time(1s/div)

Port A1 Power On
(V_{BAT}=3.5V, R_{PORTA1}=5Ω(Attach Load))



Time(100ms/div)

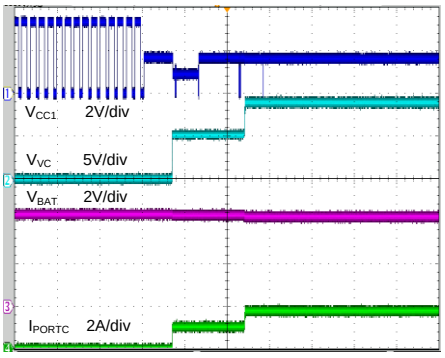
Port A1 Power Off
(V_{BAT}=3.5V, R_{PORTA1}=5Ω(Detach Load))



Time(2s/div)

Port C Output On

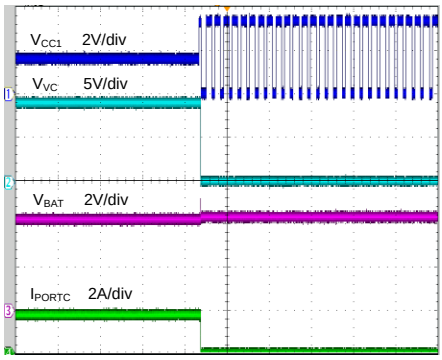
(V_{BAT}=4.2V, R_{PORTC}=5Ω(Attach PD Load))



Time(400ms/div)

Port C Output Off

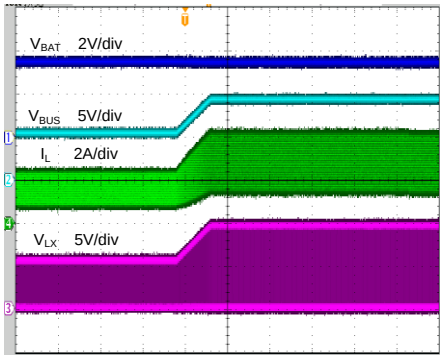
(V_{BAT}=4.2V, R_{PORTC}=5Ω(Detach PD Load))



Time(400ms/div)

Boost 5V to 9V

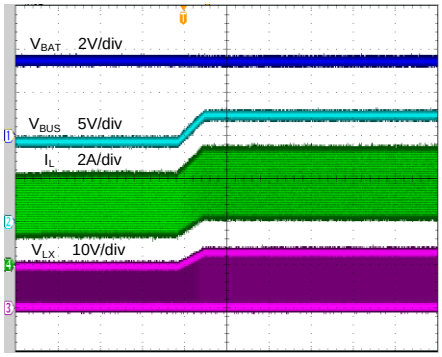
(V_{BAT}=3.5V, I_{PORTA1}=1A)



Time(10ms/div)

Boost 9V to 12V

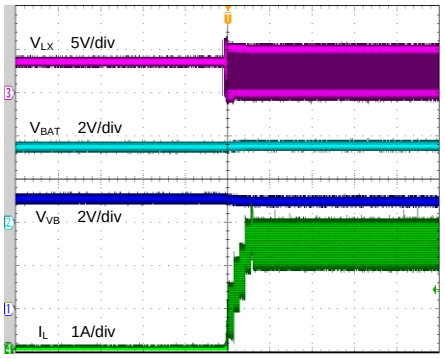
(V_{BAT}=3.5V, I_{PORTA1}=1A)



Time(10ms/div)

Inductor Current Soft Start of Battery Charging

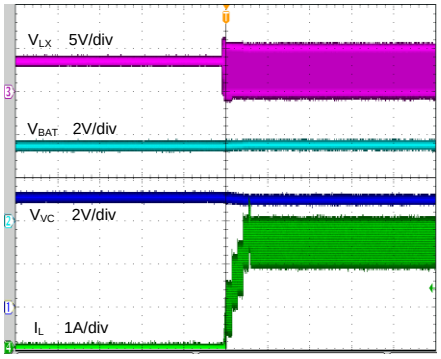
(V_{VB}=5V, V_{BAT}=3.5V, I_{DPM}=2A)



Time(10ms/div)

Inductor Current Soft Start of Battery Charging

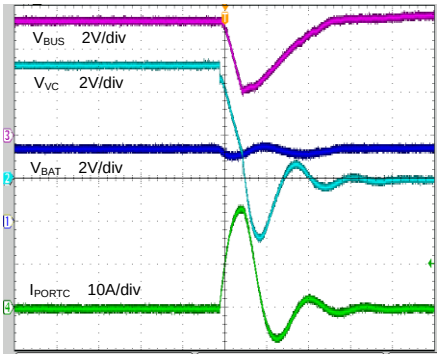
(V_{VC}=5V, V_{BAT}=3.5V, I_{DPM}=2A)



Time(10ms/div)

Port C SCP

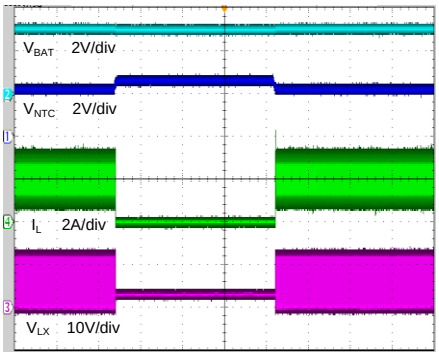
(V_{BAT}=3.5V, VC short to GND)



Time(10μs/div)

NTC Protection of Battery Charging -Temperature Changes from Cool to Cold then to Cool

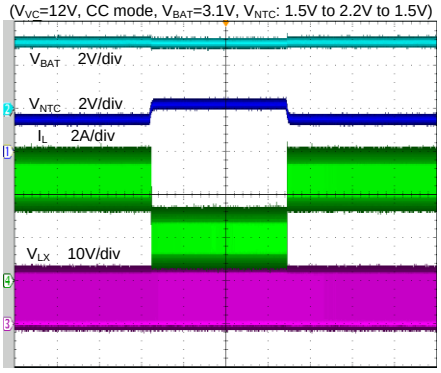
(V_{VC}=12V, CC mode, V_{BAT}=3.1V,V_{NTC}: 2.2V to 2.6V to 2.2V)



Time(1s/div)

NTC Protection of Battery Charging - Temperature Changes from Normal to Cool then to Normal

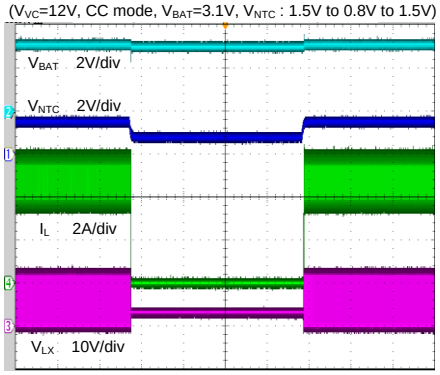
(V_{VC}=12V, CC mode, V_{BAT}=3.1V, V_{NTC}: 1.5V to 2.2V to 1.5V)



Time(1s/div)

NTC Protection of Battery Charging - Temperature Changes from Normal to Hot then to Normal

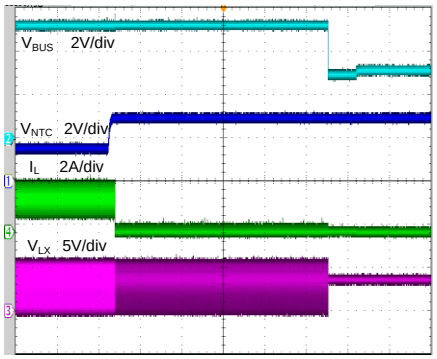
(V_{VC}=12V, CC mode, V_{BAT}=3.1V, V_{NTC} : 1.5V to 0.8V to 1.5V)



Time(1s/div)

NTC Protection of Battery Discharging - Temperature Changes from Normal to Cold

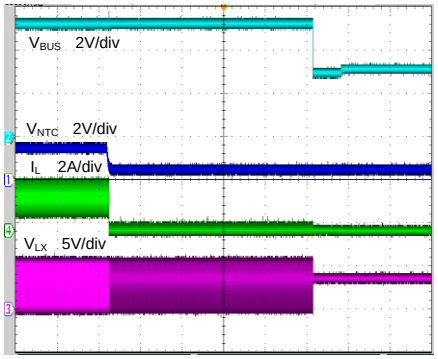
(V_{BAT}=3.5V, I_{PORTA1}=1A, V_{NTC}: 1.5V to 2.9V)



Time(1s/div)

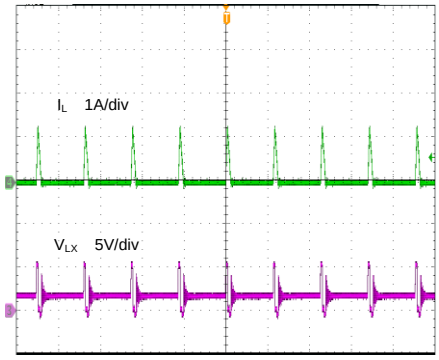
NTC Protection of Battery Discharging - Temperature changes from Normal to Hot

(V_{BAT}=3.5V, I_{PORTA1}=1A, V_{NTC}: 1.5V to 0.5V)



Time(1s/div)

Battery SCP in Charging Mode
(V_{VB}=5V, V_{BAT}=1.5V)



8 Function Description

The SY20798 adopts peak current mode control for buck and boost converter to implement the charging and discharging of battery. The peak current mode control simplifies the loop design of buck and boost converter, optimizes the stability and dynamic performance. There are 4 types of working mode in the SY20798: Charging Mode, Discharging Mode, Bypass Mode and Sleep Mode.

8.1 Charging Mode Description

The SY20798 works in Charging Mode when the input source is present on Port C (Port C is configured as input port automatically) or Port B and all output ports are off.

To meet the various input source type, the SY20798 integrates VDPM, IDPM, CC and CV loops in Charging Mode. When the adapter is inserted to Port C or Port B, the SY20798 starts the source type detection automatically; the SY20798 sets appropriate input voltage, I_{CC}, V_{CV}, V_{DPM}, I_{DPM}, I_{TERM} in order to minimize the charging time. The SY20798 stops charging to measure V_{BAT} for 480ms per 20s for the Battery Fuel Gauge Indicator in the normal charging cycle.

8.1.1 Input Voltage Dynamic Power Management

When input voltage drops to $V_{DPM,}$ the input voltage is limited to V_{DPM} by regulating the duty cycle of buck converter. The VDPM loop takes control of the buck converter until the input voltage rises above V_{DPM}.

V_{DPM} is 90% of the set input voltage in Charging Mode, 95% of the set input voltage when all the output ports are DCP in Bypass Mode, 96% of the set input voltage when at least one output port is Apple 2.4A in Bypass Mode.

8.1.2 Input Current Dynamic Power Management

After the input USB type detection, the SY20798 sets the input current limit automatically. When the input current reaches I_{DPM}, the input current will be limited to I_{DPM} by regulating the duty cycle of buck converter. The IDPM loop takes control of the buck converter until the input current decreases under I_{DPM}. The minimum I_{DPM} of Port C is 0.5A and the maximum I_{DPM} of Port C is 3A. The minimum I_{DPM} of Port B is 0.5A and the maximum I_{DPM} of Port B is 2A.

8.1.3 Constant Charging Current

The constant charging current I_{CC} of the SY20798 is 5A.

8.1.4 Constant Charging Voltage

The constant charging voltage V_{CV} of the SY20798 can be set to 4.2V or 4.35V by CV/ITERM pin (Described in Table 2).

8.1.5 Termination Current

The termination current I_{TERM} of the SY20798 can be set to 4%I_{CC} or 8%I_{CC} by CV/ITERM pin (Described in Table 2).

Table 2. V_{CV} and I_{TERM} Setting

Resistance connected between CV/ITERM and GND	V_{CV}	I_{TERM}
$R_{CV/ITERM}$<30kΩ	4.2V	4% I_{CC}
60kΩ< $R_{CV/ITERM}$<90kΩ	4.35V	8% I_{CC}
130kΩ< $R_{CV/ITERM}$<160kΩ	4.35V	4% I_{CC}
$R_{CV/ITERM}$>240kΩ	4.2V	8% I_{CC}

8.2 Discharging Mode Description

The SY20798 works in Discharging Mode when the input source is absent and at least one of the output ports is on. A quasi-fixed peak current mode boost converter is employed to step-up voltage in Discharging Mode. The maximum output power is up to 22.5W.

The SY20798 starts the boost converter and turns on the port's NMOS when the load insertion signal is detected. The SY20798 can identify the charging protocol of the portable device and change the output voltage and current limit according to the request of the portable device. The SY20798 supplies the output ports with 5V only when at least two output ports are on.

8.2.1 Battery Internal Resistor Compensation

The SY20798 uses RCOM pin to compensate the battery internal resistor in Discharging Mode. The compensation voltage will be added to the battery voltage on BAT pin to get the OCV of battery for Battery Fuel Gauge Indicator.

The compensated battery internal resistance is calculated by the following equation:

$$R_{BAT\_INTER} = 45 \times 10^{-6} \times R_{RCOM}$$

Where R_{RCOM} is the resistance connected to RCOM pin.

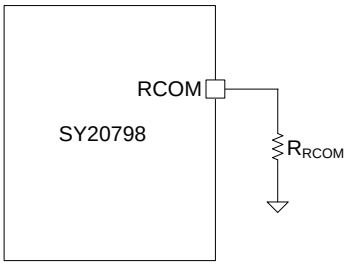


Figure 4. Battery Internal Resistor Compensation Circuit

8.2.2 Switching Frequency Control

The switching frequency of SY20798 can be programmed by the pull-up resistor on KEY/FSW pin in Discharging Mode.

The frequency is calculated by the following equation:

$$F_{SW} = \frac{18.5\times10^{9}\Omega \times 1Hz}{R_F}$$

Where R_F is the resistance connected from BAT pin to KEY/FSW pin.

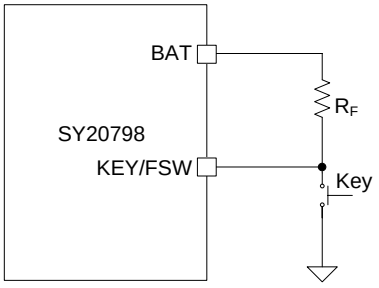


Figure 5. Switching Frequency Set Circuit

8.2.3 Output Current Limit of Boost Converter

When the output current of boost converter exceeds I_{LIM_BOOST}, the current is limited to I_{LIM_BOOST} by regulating the duty cycle of boost converter. The boost CC loop takes control of the boost converter until the output current of boost converter is lower than I_{LIM_BOOST}.

8.2.4 Battery Depletion Threshold Set

The SY20798 stops discharging and enters into Sleep Mode to prohibit the battery from being over discharged when V_{BAT} is lower than V_{BAT_DEP} in Discharging Mode. V_{BAT_DEP} is set to 3.15V when R_{LED1} is higher than 90kΩ and is set to 2.7V when R_{LED1} is lower than 60kΩ.

8.3 Bypass Mode Description

The SY20798 works in Bypass Mode when the input source is present and at least one output port turns on.

When both the adapter and the portable device are present, the SY20798 charges the battery and delivers power to the output port from the adapter at the same time.

In Bypass Mode, the SY20798 disables the fast charging protocols.

8.4 Sleep Mode Description

The SY20798 turns off the PortA1, PortA2, Port B, Port C, VDD, buck and boost converter to enter into Sleep Mode when the adapter and the portable device are all absent. The Port C features DRP with Try.SRC and toggles between Source and Sink in Sleep Mode.

8.5 Load Insert Detection

The insertion of the portable device on Port A1, Port A2 and Port C will trigger the Load Insert Detection. The SY20798 starts the boost converter and turns on the port's NMOS when the load insertion signal is detected.

8.6 Light Load Detection

If the output current of the Port A1 or Port A2 is lower than I_{LIGHT} for 25s, the SY20798 will turn off this port.

8.7 LED Status Indication Description

8.7.1 Battery Fuel Gauge and Charging/Discharging Status Indicator Description

The SY20798 integrates the Battery Fuel Gauge Indicator and Charging/Discharging Status Indicator through 4 LEDs (Described in Table 3).

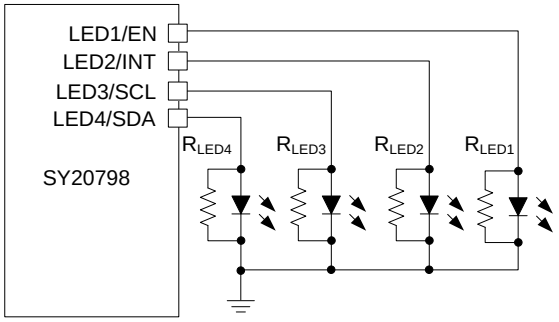


Figure 6. LED Indication Circuit

Table 3. LED Status

Operation Mode	Battery Fuel Gauge	V_{BAT}	LED Status			
			LED1	LED2	LED3	LED4
Charging	0-25%	< V_{TH1}	Flicker1	OFF	OFF	OFF
	25-50%	V_{TH1}~ V_{TH2}	ON	Flicker1	OFF	OFF
	50-75%	V_{TH2}~ V_{TH3}	ON	ON	Flicker1	OFF
	75-100%	V_{TH3}~V_{CV}	ON	ON	ON	Flicker1
	100%	≥V_{CV}	ON	ON	ON	ON
Discharging	0-25%	V_{DEP} ~ V_{TH1}	Flicker2	OFF	OFF	OFF
	25-50%	V_{TH1}~ V_{TH2}	Flicker2	Flicker2	OFF	OFF
	50-75%	V_{TH2}~ V_{TH3}	Flicker2	Flicker2	Flicker2	OFF
	75-100%	≥V_{TH3}	Flicker2	Flicker2	Flicker2	Flicker2
Sleep			OFF	OFF	OFF	OFF
Fault			Flicker1	Flicker1	Flicker1	Flicker1

Flicker1—ON 640mS, OFF 640mS.

Flicker2—ON 320mS, OFF 2240mS.

8.7.2 Battery Fuel Gauge Threshold Description

The resistors parallel to the LEDs are used to program the Battery Fuel Gauge Threshold.

R_{LED1}, R_{LED2}, R_{LED3} and R_{LED4} are used to program the Battery Fuel Gauge Threshold V_{TH1}, V_{TH2} and V_{TH3} (Described in Table 4).

Table 4. Battery Fuel Gauge Threshold

	Charging Mode	Discharging Mode
V_{TH1}	V_{TH1}=83%*V_{CV}+0.5V×R_{LED2}/R_{LED1}	V_{TH1}=80%*V_{CV}+ 0.5V×R_{LED2}/R_{LED1}
V_{TH2}	V_{TH2}=88%*V_{CV}+0.5V×R_{LED3}/R_{LED1}	V_{TH2}=85%*V_{CV}+ 0.5V×R_{LED3}/R_{LED1}
V_{TH3}	V_{TH3}=93%*V_{CV}+0.5V×R_{LED4}/R_{LED1}	V_{TH3}=90%*V_{CV}+ 0.5V×R_{LED4}/R_{LED1}

8.8 Key Function

There are 2 types of key action in the SY20798, 1-click action to reset the IC and 2-click action to disable the light load detection function for 2 hours.

8.9 Charging Protocols

The SY20798 supports multiple charging protocols. The Port B supports BC1.2. The Port C supports PD3.0 and BC1.2 when an adapter is present. The Port C supports PD3.0, QC3.0, QC2.0, SCP, FCP, AFC and Apple 2.4A when a portable device is present. The Port A1 and Port A2 support QC3.0, QC2.0, SCP, FCP, AFC and Apple 2.4A when a portable device is present.

8.10 Type-C DRP Function

The Port C of the SY20798 integrates three threshold comparators, three types of Rp and Rd which meet the USB Type-C specification 2.0 for CC1 and CC2 pins. The Port C is a DRP with Try.SRC, CC1 and CC2 toggle between Source

and Sink when the Port C is detached. It can identify the attach and detach of the Source and Sink automatically. The CC logic block is shown in Figure 7.

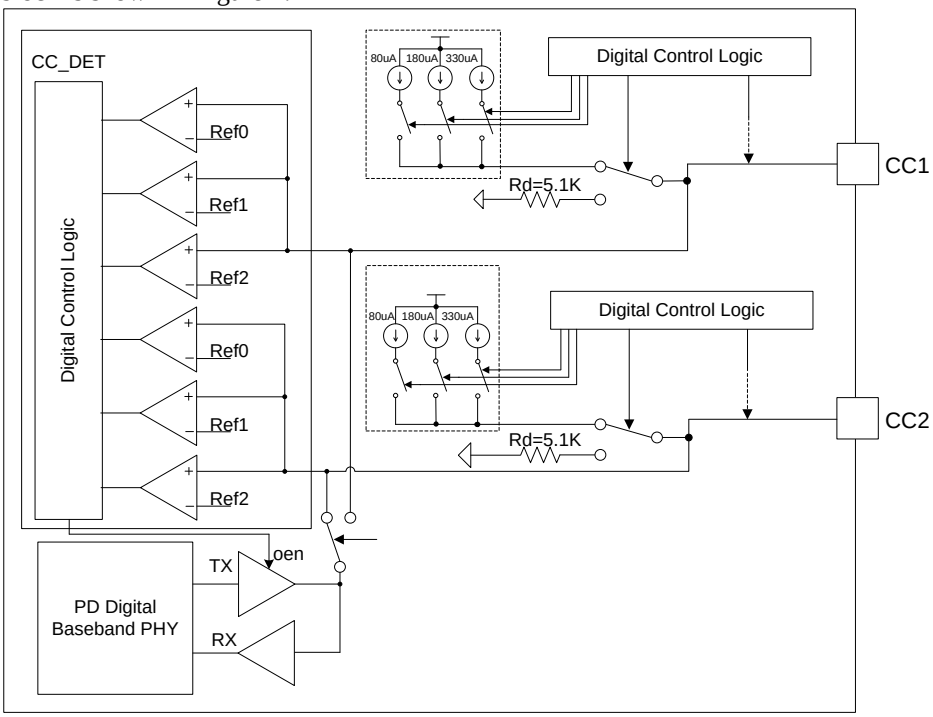


Figure 7. CC Logic Block

8.11 TCPC Interface

The SY20798 implements the USB Type-C Port Controller (TCPC) Interface for the update of PD protocol. The TCPC Interface uses I^2C protocol. When the resistance connected from LED1/EN pin to GND is lower than 100Ω, the TCPC Interface is enabled; the MCU can implement the full function of Type-C 2.0 and PD3.0 through the TCPC Interface.

When the TCPC Interface is enabled, the LED Status Indication function is disabled; LED2/INT pin is configured as Open-drain interrupt output; LED3/SCL is configured as the SCL pin of the I^2C Interface; LED4/SDA pin is configured as the SDA pin of the I^2C Interface.

8.12 Protection Description

During the half-bridge operating as synchronous buck mode, the SY20798 has Input Over Voltage Protection, Input Under Voltage Protection, BAT Over Voltage Protection, BAT Short Circuit Protection, Charging Timeout Protection, Thermal Shutdown Protection and NTC Protection for the Li-Ion battery and IC.

During the half-bridge operating as synchronous boost mode, the SY20798 has BUS Over Voltage Protection, BAT Depletion Protection, Port Short Circuit Protection, Port Over Current Protection, D+/D- short to BUS Protection, Thermal Shutdown Protection and NTC Protection for the Li-Ion battery and IC.

8.12.1 Input Over Voltage Protection

When V_{VC} or V_{VB} is higher than the over voltage protection threshold, the half bridge stops buck operation immediately. It recovers to normal work when the monitored voltage backs to normal level.

8.12.2 Input Under Voltage Protection

When V_{VC} or V_{VB} is lower than the under voltage protection threshold, the half bridge stops buck operation immediately. It recovers to normal work when the monitored voltage backs to normal level.

8.12.3 BAT Over Voltage Protection

When V_{BAT} is higher than the over voltage protection threshold, the half bridge stops buck operation immediately. It recovers to normal work when the monitored voltage backs to normal level.

8.12.4 BAT Short Circuit Protection

When V_{BAT} is lower than V_{BAT_SHORT}, the SY20798 wakes the battery up with a small charging current.

8.12.5 Charging Timeout Protection

The SY20798 has two kinds of timeout protection, 20-hour timeout protection for the fast charge mode and 2-hour timeout protection for the trickle charge mode. Once the timeout protection is triggered, the SY20798 stops the charge operation and latches off. Only re-plug in the input source can reset the latch logic and restart the normal charging work.

8.12.6 NTC Protection

The SY20798 adopts NTC pin to monitor the temperature of the battery to provide the protection of battery charging. The current setting at cool temperature (T1–T2) is 40% of the constant charging current. The SY20798 stops charging when the temperature of the battery is lower than T1 or higher than T3. Figure 8 describes the charging current vs battery temperature.

The SY20798 adopts NTC pin to monitor the temperature of the battery to provide the protection of battery discharging. The SY20798 stops discharging when the temperature of battery is lower than T_{COLD} or higher than T_{HOT} and enters into Sleep Mode.

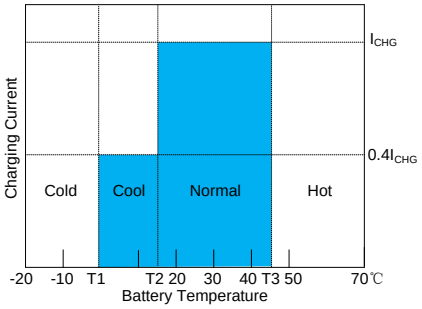


Figure 8. Charging Current vs Battery Temperature

8.12.7 Thermal Shutdown

The SY20798 shuts down the IC when the junction temperature exceeds 150℃. It recovers to normal work when the junction temperature drops to 130℃.

8.12.8 BUS Over Voltage Protection

When V_{BUS} is higher than the over voltage protection threshold, the half bridge stops boost operation immediately. It recovers to normal work when the monitored voltage backs to normal level.

8.12.9 Battery Depletion Protection

When V_{BAT} is lower than battery depletion voltage threshold, the SY20798 stops boost operation and then enters into Sleep Mode.

8.12.10 Port Short Circuit Protection

When port short circuit occurs, the SY20798 turns off the NMOS of the output port immediately. The SY20798 recovers to normal work when the fault removes.

8.12.11 Port Over Current Protection

When the current of the output port is over port OCP threshold, the SY20798 turns off the NMOS of the output port immediately. The SY20798 recovers to normal work when the fault removes.

8.12.12 D+/D- Short to BUS Protection

When DPA1, DMA1, DPA2, DMA2, DPC or DMC is shorted to BUS, the SY20798 disables the fast charging protocol function.

8.13 Registers

When the resistance connected from LED1/EN pin to GND is lower than 100Ω, the TCPC Interface is enabled.

The INT pin should be pulled low according to the TCPCI spec and the actions described in Register 84H to 85H.

Table 5. Register Summary

Address	Register Name	Read/Write
04h/05h	DEVICE_ID	R
10h/11h	ALERT	R/W
19h	TCPC_CONTROL	R/W
1Ah	ROLE_CONTROL	R/W
1Dh	CC_STATUS	R
1Eh	POWER_ STATUS	R
1Fh	FAULT_STATUS	R/W
20h	EXTENDED_STATUS	R
23h	COMMAND	W
2Eh	MESSAGE_HEADER_INFO	R/W
2Fh	RECEIVE_DETECT	R/W
30h	READABLE_BYTE_COUNT	R
	RX_BUF_FRAME_TYPE	R
	RX_BUF_BYTE_x	R
50h	TRANSMIT	R/W
51h	I2C_WRITE_BYTE_COUNT	W
	TX_BUF_BYTE_x	W
81h	BOOST_CTRL0	R/W
82h	BOOST_CTRL1	R/W
83h	BOOST_CTRL2	R/W
84h	CHG_DCHG_STAT0	R/W
85h	CHG_DCHG_STAT1	R/W

Table 6. DEVICE_ID Register (Register 04h/05h)

Bit	Bit Name	Type	Description
15-0	bcdDevice	R	A unique 16-bit unsigned integer assigned by the Vendor to identify the version of the TCPC.

Table 7. ALERT Register (Register 10h/11h)

Bit	Bit Name	Type	Description
15	Vendor Defined Alert	R/W	0: Cleared 1: A vendor defined alert has been detected. Read REG 2EH and 84H to 85H.
14-12	Reserved	R	Reserved
11	VBUS Sink Disconnect Detected BUS	R/W	0: Cleared 1: A VBUS Sink Disconnect Threshold crossing has been detected
10	Rx Buffer Overflow	R/W	0: TCPC Rx buffer is functioning properly 1: TCPC Rx buffer has overflowed. Future GoodCRC shall not be sent. Writing 1 to this register acknowledges the overflow. The overflow is cleared by writing to ALERT.ReceiveSOP*MessageStatus.
9	Fault	R/W	0: No fault 1: A fault has occurred. Read the FAULT_STATUS register.
8-7	Reserved	R	Reserved
6	Transmit SOP* Message Successful	R/W	0: Cleared 1: Reset or SOP* message transmission successful. GoodCRC response received on SOP* message transmission. Transmit SOP* message buffer registers are empty. Transmit SOP* Message Successful shall be asserted by TCPC after sending Hard Reset or Cable Reset.
5	Transmit SOP* Message Discarded	R/W	0: Cleared 1: Reset or SOP* message transmission not sent due to an incoming receive message. Transmit SOP* message buffer registers are empty.
4	Transmit SOP* Message Failed	R/W	0b: Cleared 1b: SOP* message transmission not successful, no GoodCRC response received on SOP* message transmission. Transmit SOP* message buffer registers are empty. Transmit SOP* Message Failed shall be asserted both by TCPC after sending Hard Reset or Cable Reset.
3	Received Hard Reset	R/W	0: Cleared 1: Received Hard Reset message
2	Received SOP* Message Status	R/W	0: Cleared 1: RECEIVE_BUFFER register changed
1	Power Status	R/W	0: Cleared 1: Power Status changed
0	CC Status	R/W	0: Cleared 1: CC Status changed

Note: Write 1 to corresponding bit in Alert to clear that bit.

Table 8. TCPC_CONTROL Register (Register 19h)

Bit	Bit Name	Type	Description
7-1	Reserved	R	Reserved
0	Plug Orientation	R/W	**0: Monitor the CC1 pin for BMC communications if PD messaging is enabled (default)** 1: Monitor the CC2 pin for BMC communications if PD messaging is enabled

Table 9. ROLE_CONTROL Register (Register 1Ah)

Bit	Bit Name	Type	Description
7	Reserved	R	Reserved
6	DRP	R/W	**0: No DRP. Bits B3..0 determine Rp/Rd/Ra or open settings (default)** 1: DRP The TCPC toggles CC1 & CC2 after receiving COMMAND.Look4Connection and until a connection is detected. Upon connection, the TCPC shall resolve to either an Rp or Rd and report the CC1/CC2 State in the CC_STATUS register. The CC pins shall stay in Potential_Connect_as_Src or Potential_Connect_as_Sink until directed otherwise.
5-4	Rp Value	R/W	**00: Rp default current (default)** 01: Rp 1.5A 10: Rp 3.0A 11: Reserved
3-2	CC2	R/W	00: Reserved 01: Rp (Use Rp definition in Bit5-4) **10: Rd (default)** 11: Reserved
1-0	CC1	R/W	00: Reserved 01: Rp (Use Rp definition in Bit5-4) **10: Rd (default)** 11: Reserved

Table 10. CC_STATUS Register (Register 1Dh)

Bit	Bit Name	Type	Description
7-6	Reserved	R	Reserved
5	Looking4Connection	R/W	**0: TCPC is not actively looking for a connection. A transition from '1' to '0' indicates a potential connection has been found (default)** 1: TCPC is looking for a connection (toggling as a DRP or looking for a connection as Sink/Source only condition)
4	ConnectResult	R	**0: The TCPC is presenting Rp (default)** 1: The TCPC is presenting Rd

3-2	CC2 State	R	If (ROLE_CONTROL.CC2=Rp) or (ConnectResult=0) **00: SRC.Open** 01: SRC.Ra 10: SRC.Rd 11: ReservedIf (ROLE_CONTROL.CC2=Rd) or (ConnectResult=1) **00: SNK.Open** 01: SNK.Default 10: SNK.Power1.5 11: SNK.Power3.0 If ROLE_CONTROL.CC2=Open, this field is set to 00 This field always returns 00 if (Looking4Connection=1). Otherwise, the returned value depends upon ROLE_CONTROL.CC2.

1-0	CC1 State	R	If (ROLE_CONTROL.CC1 = Rp) or (ConnectResult=0)
			00: SRC.Open
			01: SRC.Ra
			10: SRC.Rd
			11: Reserved
			If (ROLE_CONTROL.CC1 = Rd) or ConnectResult=1)
			00: SNK.Open
			01: SNK.Default
			10: SNK.Power1.5
			11: SNK.Power3.0
			If ROLE_CONTROL.CC1=Open, this field is set to 00
			This field always returns 00 if Looking4Connection=1. Otherwise, the returned value depends upon ROLE_CONTROL.CC1.

Table 11. POWER_STATUS Register (Register 1Eh)

Bit	Bit Name	Type	Description
7	Reserved	R	Reserved
6	TCPC Initialization Status	R	**0: The TCPC has completed initialization and all registers are valid (default)** 1: The TCPC is still performing internal initialization and the only registers that are guaranteed to return the correct values are 00h...0Fh
5-3	Reserved	R	Reserved
2	VC Present	R	**0: VC Disconnected (default)** 1: VC Connected The TCPC shall report VC present when TCPC detects V_{VC} rises above 4V. The TCPC shall report V_{VC} is not present when TCPC detects V_{VC} falls below 3.5V.
1-0	Reserved	R	Reserved

Table 12. FAULT_STATUS Register (Register 1Fh)

Bit	Bit Name	Type	Description
7	AllRegistersResetToDefault	R	This bit is asserted when the TCPC resets all registers to their default value. This happens at initial power up or if an unexpected power reset occurs.
6	Reserved	R	Reserved
5	Auto Discharge Failed	R/W	**0: No discharge failure (default)** 1: Discharge by the TCPM failed The TCPC shall report discharge fails if VBUS is not below vSafe0V within 650ms(max).
4-1	Reserved	R	Reserved
0	I2C Interface Error	R/W	**0:No Error (default)** 1:I^2C error has occurred Some of the conditions for asserting this bit: 1.TCPM writes to TRANSMIT requesting a transmission that is not Hard Reset, Cable reset or BIST Carrier Mode2 and there are less than 2 bytes in the TX_BUF_BYTE_x register; 2. I^2C writing number is not consistent with I2C_WRITE_BYTE_COUNT.

Table 13. EXTENDED_STATUS Register (Register 20h)

Bit	Bit Name	Type	Description
7-1	Reserved	R	Reserved
0	vSafe0V	R	0: V_{VC} is not at vSafe0V **1: V_{VC} is at vSafe0V (default)** The TCPC shall report V_{VC} is at vSafe0V when TCPC detects V_{VC} is below 0.8V.

Table 14. COMMAND Register (Register 23h)

Bit	Bit Name	Type	Description
7-0	COMMAND	W	0001 0001: **WakeI2C** (no action is taken other than to wake the I^2C interface) 1001 1001: **Look4Connection** Start DRP Toggling if ROLE_CONTROL.DRP=1. If ROLE_CONTROL.CC1/CC2= 01 start with Rp, if ROLE_CONTROL.CC1/CC2 =10 start with Rd. If ROLE_CONTROL.CC1/CC2 are not both 01 or 10, then do not start toggling. The TCPM shall issue COMMAND.Look4Connection to enable the TCPC to restart Connection Detection in cases where the ROLE_CONTROL contents will not change. 1101 1101: **ResetTransmitBuffer** The TCPC resets the pointer of the TRANSMIT_BUFFER register to offset 1 and the contents of TRANSMIT_BUFFER becomes invalid when this command is issued by the TCPM. 1110 1110: **ResetReceiveBuffer** The TCPC resets the pointer of RX_BUFFER when this command is issued by the TCPM. Writing this command would reset the pointer to 1.

			TCPC does not clear the content of the buffer upon receiving this command. The TCPM issues this command in order to re-read the RECEIVE_BUFFER.RX_BUF_BYTE_x. 1111 1111: **I2C Idle** This command would make IC enter Sleep Mode if all ports are not operating.

Table 15. MESSAGE_HEADER_INFO Register (Register 2Eh)

Bit	Bit Name	Type	Description
7	QC_12V_A	R	**0: Portable device in Port A is not requesting 12V through QC2.0 (default)** 1: Portable device in Port A is requesting 12V through QC2.0 Vendor Defined Alert will be generated when this bit changes.
6	QC_9V_A	R	**0: Portable device in Port A is not requesting 9V by QC2.0 (default)** 1: Portable device in Port A is requesting 9V by QC2.0 Vendor Defined Alert will be generated when this bit changes.
5	BYPASS_QC_A_EN	R/W	**0: Disable Port A QC2.0 when the adapter is present in Port C in Bypass Mode (default)** 1: Enable Port A QC2.0 when the adapter is present in Port C in Bypass Mode
4	Reserved	R	Reserved
3	Data Role	R/W	**0: UFP (default)** 1: DFP
2-1	USB PD Specification Revision	R/W	00: Revision 1.0 01: Revision 2.0 **10: Revision 3.0 (default)** 11: Reserved
0	Power Role	R/W	**0: Sink (default)** 1: Source

Table 16. RECEIVE_DETECT Register (Register 2Fh)

Bit	Bit Name	Type	Description
7-6	Reserved	R	Reserved
5	Enable Hard Reset	R/W	**0: TCPC does not detect Hard Reset signaling (default)** 1: TCPC detects Hard Reset signaling
4	FC_CTRL	R/W	**0: Enable all fast charging protocols including PD in Discharging Mode (default)** 1: Disable fast discharging protocols except PD in Discharging Mode
3-2	Reserved	R/W	Reserved
1	Enable SOP’ message	R/W	**0: TCPC does not detect SOP’ message (default)** 1: TCPC detects SOP’ message

0	Enable SOP message	R/W	**0: TCPC does not detect SOP message (default)** 1: TCPC detects SOP message

Table 17. READABLE_BYTE_COUNT Register (Register 30h)

Bit	Bit Name	Type	Description
7-0	READABLE_BYTE_COUNT	R	Indicates the number of bytes in the RX_BUF_BYTE_x registers plus one (for the RX_BUF_FRAME_TYPE). The content of this register is undefined when the RECEIVE_BUFFER is cleared. The value in this register shall be less than or equal to 31.

Table 18. RX_BUF_FRAME_TYPE Register (Register 30h)

Bit	Bit Name	Type	Description
7-3	Reserved	R	Reserved
2-0	Received SOP* Message	R	**000: Received SOP (default)** 001: Received SOP' All others are reserved. These registers are "hidden" and can only be accessed by reading at address 30h.

Table 19. RX_BUF_BYTE_x Register (Register 30h)

Bit	Bit Name	Type	Description
7-0	RX_BUFFER	R	Receive Buffer Bytes. These registers are "hidden" and can only be accessed by reading at address 30h.

Table 20. TRANSMIT Register (Register 50h)

Bit	Bit Name	Type	Description
7-6	Reserved	R	Reserved
5-4	Retry Counter	R/W	**00: No message retry is required (default)** 01: Automatically retry message transmission once 10: Automatically retry message transmission twice 11: Automatically retry message transmission three times
3	Reserved	R	Reserved
2-0	Transmit SOP* message	R/W	**000: Transmit SOP (default)** 001: Transmit SOP' 010: Reserved 011: Reserved 100: Reserved 101: Transmit Hard Reset 110: Transmit Cable Reset 111: Transmit BIST Carrier Mode 2 (TCPC shall exit the BIST mode no later than 45ms(max))

Table 21. I2C_WRITE_BYTE_COUNT Register (Register 51h)

Bit	Bit Name	Type	Description
7-0	I2C_WRITE_BYTE_COUNT	W	The number of bytes the TCPM intends to write to the TX_BUF_BYTE_x in the given I^2C transaction. The TCPM shall write as many bytes in the buffer as defined in this register in one I^2C write transaction. The TCPC shall ignore the I^2C transaction if I2C_WRITE_BYTE_COUNT is more than 30.

Table 22. TX_BUF_BYTE_x Register (Register 51h)

Bit	Bit Name	Type	Description
7-0	TRANSMIT_BUFFER	W	Transmit Buffer Bytes. These registers are “hidden” and can only be accessed by writing to address 51h.

Table 23. BOOST_CTRL0 Register (Register 81h)

Bit	Bit Name	Type	Description
7-0	VBUS_SET_H	R/W	BUS voltage set high 8 bits, V_{BUS}= VBUS_SET_H*80mV+ VBUS_SET_L*10mV. While VBUS is set higher than 12.55V, VBUS_SET_H and VBUS_SET_L keep unchanged (VBUS_SET_H + VBUS_SET_L=100 1110 0111 is the max value). V_{BUS} is set to 5.18V in default. 0000 0000:0V(Disable boost) … **0100 0000:5.12V (default)** … 1001 1100:12.48V(max)

Table 24. BOOST_CTRL1 Register (Register 82h)

Bit	Bit Name	Type	Description
7-5	VBUS_SET_L	R/W	BUS voltage set low 3 bits, VBUS= VBUS_SET_H*80mV+ VBUS_SET_L*10mV. While VBUS is set higher than 12.55V, VBUS_SET_H and VBUS_SET_L keep unchanged (VBUS_SET_H + VBUS_SET_L=100 1110 0111 is the max value). V_{BUS} is set to 5.18V in default. 000:0.00V 001:0.01V … **110:0.06V (default)** 111:0.07V
4	PD_DET_OVERTIME	R/W	Port C PD detection overtime control bit. **0: PD detection is not overtime (default)** 1: PD detection is overtime
3	CHG_EN_C	R/W	Charge enable bit when the adapter is present in Port C. 0: Disable charge when the adapter is present in Port C **1: Enable charge when the adapter is present in Port C (default)**

2	BLEED_DISCHG_EN_C	R/W	Port C Bleed Discharge EN control bit. **0: Disable Port C Bleed Discharge (default)** 1: Enable Port C Bleed Discharge
1	PORTB_EN	R/W	Port B on/off control bit. **1: Turn on Port B (default)** 0: Turn off Port B
0	PORTC_EN	R/W	Port C on/off control bit. **1: Turn on Port C (default)** 0: Turn off Port C

Table 25. BOOST_CTRL2 Register (Register 83h)

Bit	Bit Name	Type	Description
7-1	IBOOST	R/W	Boost current limit setting when FC_CTRL bit is 1. 0000000: 0mA 0000001: 50mA … **0111100: 3000mA (default)** … 1010000: 4000mA 1010001: Reserved … 1111111: Reserved
0	RESET	R/W	Write 1 to reset all the registers to default value, auto clear.

Table 26. CHG_DCHG_STAT0 Register (Register 84h)

Bit	Bit Name	Type	Description
7-6	CHG_STAT	R	Charging status indication bits. **00: Ready (default)** 01: Charging in progress 10: Charging done (Termination) 11: Charging fault (VIN OVP, BAT OVP, BAT SCP, NTC fault) INT signal will be generated when CHG_STAT changes.
5-4	DCHG_STAT	R	Discharging status indication bits. **00: Ready (default)** 01: Discharging in progress 10: Discharging fault (BAT DEP, BUS OVP, BUS SCP/OCP, NTC fault will make chip enter into sleep mode) 11: Reserved INT signal will be generated when DCHG_STAT changes.
3-0	IDPM_SET	R/W	IDPM_SET of Port C when PD_DET_OVERTIME bit is 0. **0000~0100:0.5A (default)** 0101:0.75A 0110:1A 0111:1.5A 1000:1.75A 1001:2.0A 1010:2.25A 1011:2.5A

			1100:2.75A 1101~1111:3A

Table 27. CHG_DCHG_STAT1 Register (Register 85h)

Bit	Bit Name	Type	Description
7	PORTA_STAT	R	Port A on/off status indication bit. **0: All Ports A are off (default)** 1: At least one Port A is on INT signal will be generated when this changes.
6	ONE_KEY_CLICK	R/W	One key click indication bit. **0: No one key click (default)** 1: One key click happens INT signal will be generated when this bit changes. Write 1 to clear this Bit.
5	DOUBLE_KEY_CLICK	R/W	Double key click indication bit. **0: No double key click (default)** 1: Double key click happens INT signal will be generated when this bit changes. Write 1 to clear this Bit.
4	KEY_STAT	R	KEY status indication bit. **0: KEY is high (default)** 1: KEY is low INT signal will be generated when this bit changes.
3	PORTB_PRES	R	Port B status indication bit. **0: The adapter is not present in Port B (default)** 1: The adapter is present in Port B INT signal will be generated when this bit changes.
2	QC_HV_A_C	R	Port A and Port C QC status indication bit. **0: Port C or Port A is not in QC HV mode (default)** 1: Port C or Port A is in QC HV mode (V_{BUS} is not set to 5V mode.) INT signal will be generated when this bit changes.
1-0	VIN_SET_C	R/W	Port C input voltage set bits. V_{DPM} and input OVP threshold change with VIN_SET_C. **00: 5V (default)** 01: Reserved 10: 9V 11: 12V

8.14 I²C Interface

The SY20798 uses I²C compatible interface for flexible charging parameter programming and instantaneous device status reporting. Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address 6BH, receiving control inputs from the master device like micro controller or a digital signal processor (The device address should be left shift 1 bit for write and read operation, the device address after left shift 1 bit is D6H). The I²C interface supports both standard mode (up to 100kbits), and fast mode (up to 400kbits).

Both SDA and SCL are bi-directional lines, connecting to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain.

8.14.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

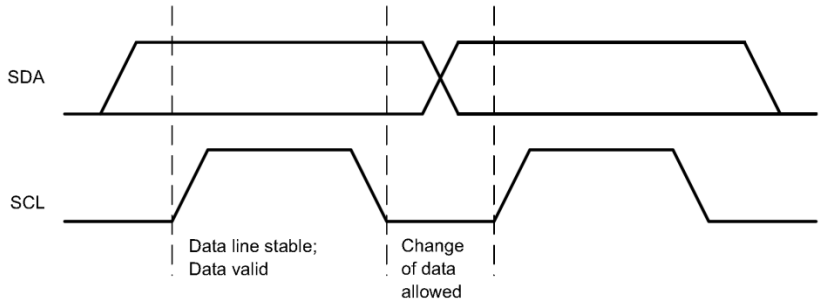


Figure 9. Bit Transfer on the I2C Bus

8.14.2 START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

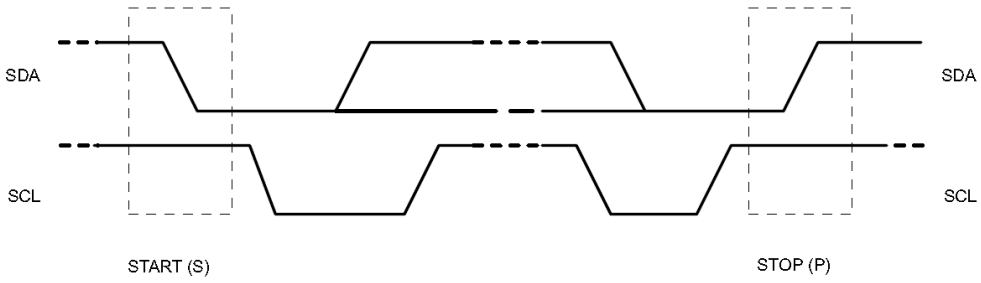


Figure 10. START and STOP conditions

8.14.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first.

If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

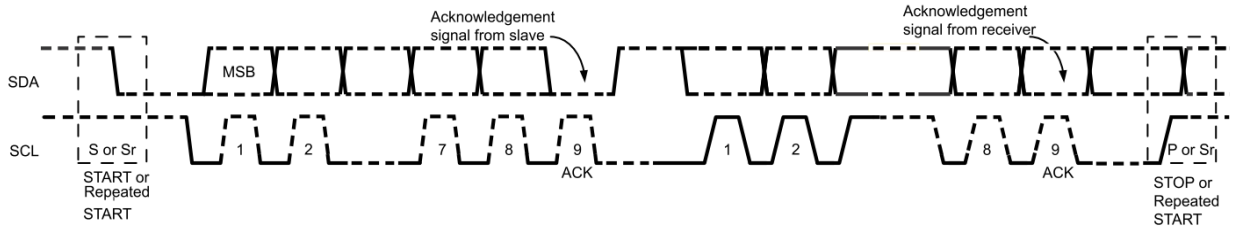


Figure 11. Data Transfer on the I2C Bus

8.14.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the 9th clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

8.14.5 Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

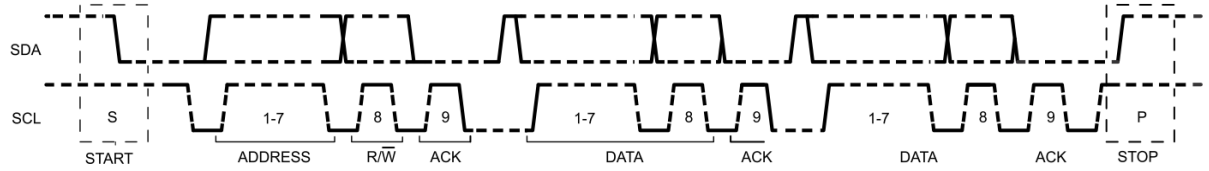


Figure 12. Complete Data Transfer

8.14.6 Single Read and Write

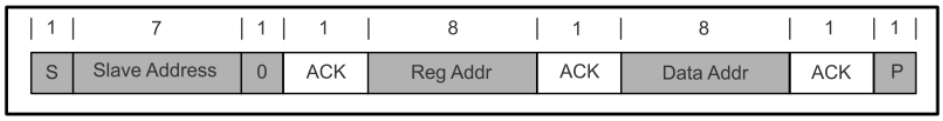


Figure 13. Single Write

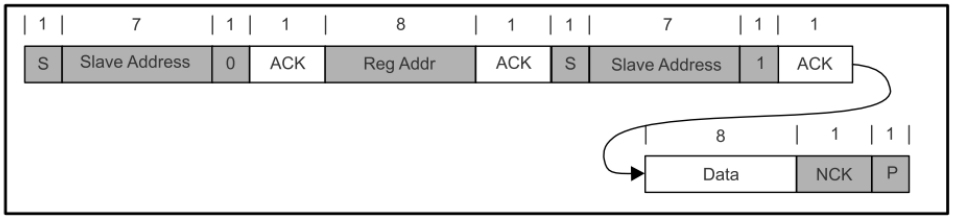


Figure 14. Single Read

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

8.14.7 Multi-Read and Multi-Write

The charger device supports multi-read and multi-write.

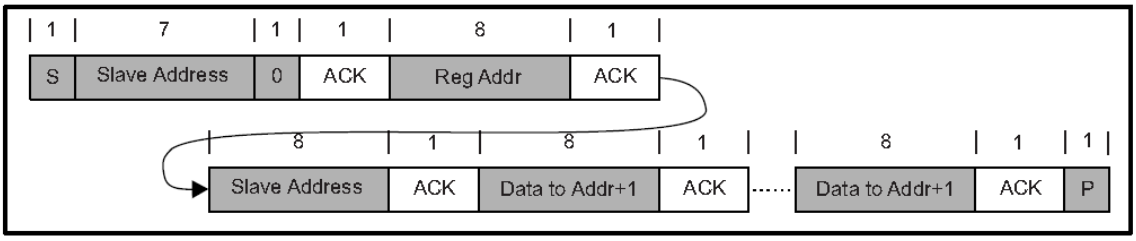


Figure 15. Multi-Write

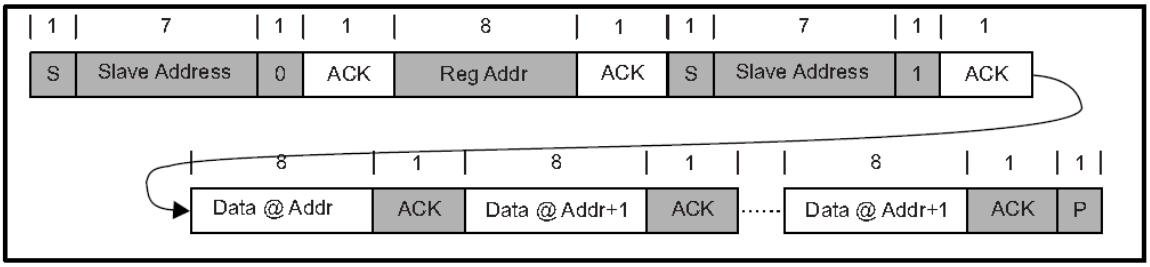


Figure 16. Multi-Read

9 Applications Information

Because of the high integration of the SY20798, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{VB}/C_{VC}, BUS capacitor C_{BUS}, battery capacitor C_{BAT}, inductor L_B, need to be selected for the targeted application specifications.

9.1 Input Capacitor C_{VB}/C_{VC}:

The input capacitor reduces the surge current drawn from the input and the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent high-frequency-switching current from passing to the input.

To minimize the potential noise problem, place a typical X7R or better grade ceramic capacitor really close to the VB/VC and GND pins. Care should be taken to minimize the loop area formed by C_{VB}/C_{VC}, VB/VC and GND pins. 10uF ceramic capacitor is suggested.

9.2 Bus Capacitor C_{BUS}:

1. Buck mode

The capacitor C_{BUS} acts as the input capacitor of the buck converter. The input current ripple RMS value is:

$$I_{CBUS\_RMS} = I_{CHG}\sqrt{D(1-D)}$$

Where I_{CHG} is the charge current and D is the duty cycle of the buck converter.

2. Boost mode

C_{BUS} is the output capacitor of boost converter. C_{BUS} reduces the bus voltage ripple and ensures the stability of the boost converter. The output current ripple RMS value is:

$$I_{CBUS\_RMS} = I_{BUS}\sqrt{\frac{D}{1\text{-}D}}$$

Where I_{BUS} is the output current of the boost converter and D is its duty cycle.

At least 30uF ceramic capacitor is suggested.

9.3 Battery Capacitor C_{BAT}:

1. Buck mode

The battery capacitor C_{BAT} acts as the output capacitor of the buck converter. C_{BAT} is selected to handle the output ripple noise requirements. For the best performance, it is recommended to use X7R or better grade ceramic capacitor. The output voltage ripple is calculated as below:

$$V_{RIP\_BAT\_BUCK} = \frac{(1-D)\times V_{BAT}}{8C_{BAT}F_{SW}{}^2L_B}$$

Where F_{SW} is the switching frequency of the buck converter, D is its duty cycle and L_B is its output inductance.

2. Boost mode

C_{BAT} acts as the input capacitor of the boost converter. The input voltage ripple is calculated as below:

$$V_{RIP\_BAT\_BOOST} = \frac{D\times V_{BAT}}{8C_{BAT}F_{SW}{}^2L_B}$$

Where F_{SW} is the switching frequency of the boost converter, D is its duty cycle and L_B is its input inductance.

At least 20uF ceramic capacitor is suggested.

9.4 Inductor L_B:

The inductor selection trades off between cost, size, and efficiency. A lower inductance value corresponds with smaller size, but results in higher ripple currents, higher magnetic hysteretic losses, and higher output capacitances. However, a higher inductance value benefits from lower ripple current and smaller output filter capacitors, but results in higher inductor DC resistance (DCR) loss. An inductor must not saturate under the worst-case condition.

1. Buck mode

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the average input current. The inductance is calculated as:

$$L_B = \frac{V_{BAT}(1-V_{BAT}/V_{IN\_MAX})}{F_{SW}\times I_{CHG\_MAX}\times 40\%}$$

Where F_{SW} is the switching frequency of the buck converter, I_{CHG_MAX} is the maximum charge current and V_{IN_MAX} is the maximum input voltage.

The SY20798 is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT\_MIN} > I_{CHG\_MAX} + \frac{V_{BAT}(1 - V_{BAT}/V_{IN\_MAX})}{2 \times F_{SW} \times L_B}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement.

2. Boost mode

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the average input current. The inductance is calculated as:

$$L_B = \frac{V_{BAT}(1 - V_{BAT}/V_{BUS\_MAX})}{F_{SW} \times I_{DIS\_MAX} \times 40\%}$$

Where F_{SW} is the switching frequency of the boost converter, I_{DIS_MAX} is the maximum discharge current and V_{BUS_MAX} is the maximum boost output voltage.

The SY20798 is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT\_MIN} > I_{DIS\_MAX} + \frac{V_{BAT}(1 - V_{BAT}/V_{BUS\_MAX})}{2 \times F_{SW} \times L_B}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement.

9.5 Layout Design

The layout design of the SY20798 regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{VB}, C_{VC}, C_{BUS}, L_B.

1. It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed a ground plane is highly desirable.

2. C_{BUS} must get close to Pins BUS and GND. The loop area formed by C_{BUS}, BUS and GND pins must be minimized.

3. C_{VB}/C_{VC} must get close to Pins VB/VC and GND. The loop area formed by C_{VB}/C_{VC}, VB/VC and GND pins must be minimized. Figure 17 is the recommended layout design.

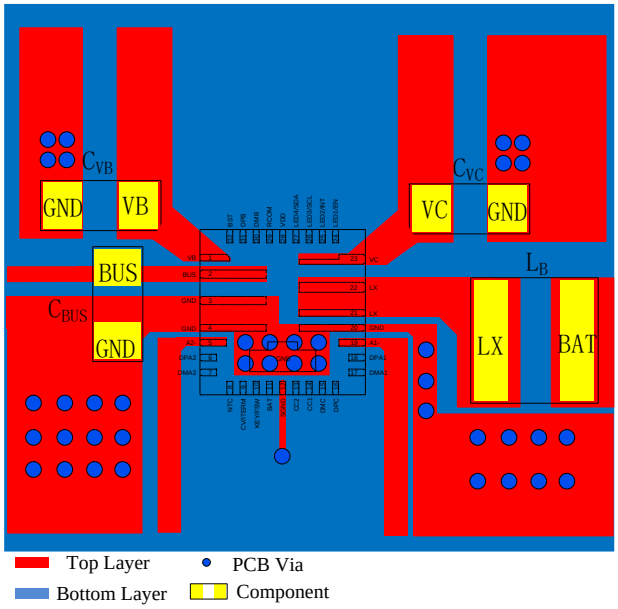
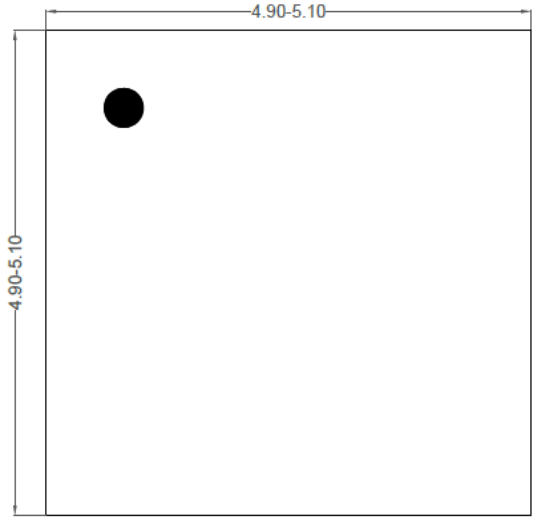


Figure 17. PCB Layout

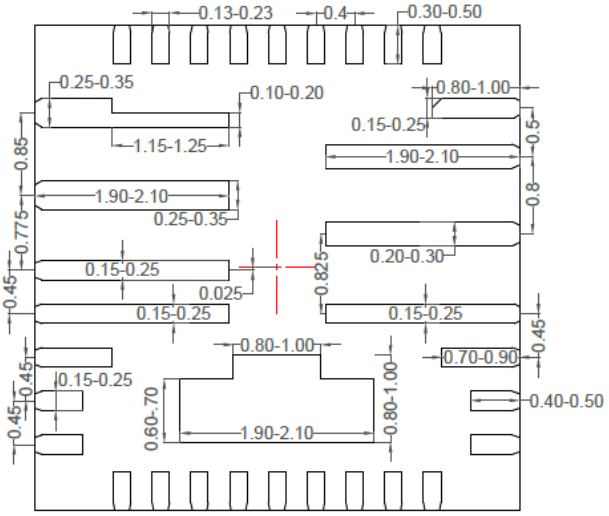
4. The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

5. In high current applications, a RC snubber circuit is suggested to be placed between LX and GND for better EMI.

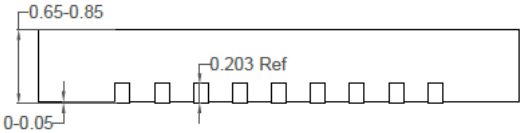
QFN5×5-32 Package Outline Drawing



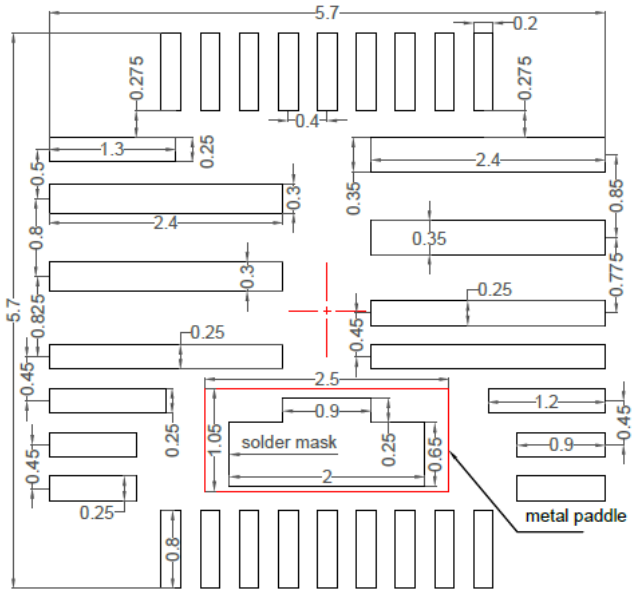
Top view



Bottom view



Side view



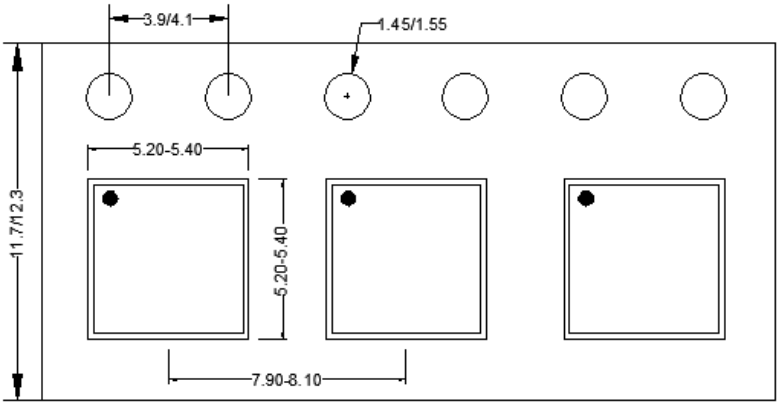
Recommended PCB layout
(Reference only)

Notes: 1, All dimension in millimeter and exclude mold flash & metal burr;

Taping & Reel Specification

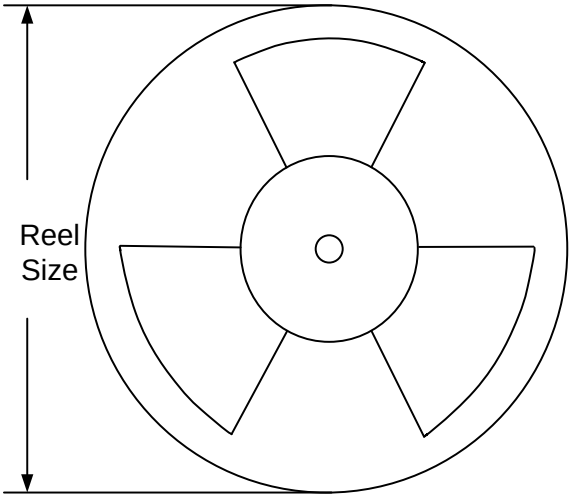
1. Taping Orientation

QFN5×5-32



Feeding Direction

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
QFN5×5-32	12	8	13"	400	400	5000

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