



# SY20794

## USB Type-C Port Controller

### 1 General Description

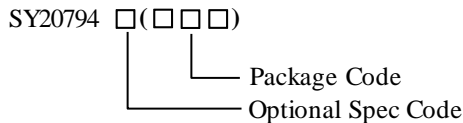
The SY20794 is a Type-C Port Controller (TCPC) which encapsulates USB Type-C CC logic, USB PD BMC Physical Layer, VBUS detection and VCONN power control.

The SY20794 integrates the CC logic for the USB Type-C connector. Under the control of the TCPM, the SY20794 enables the Port-C with fully port attach/detach, cable orientation, role detection, and USB Type-C current capability advertising function. It can be configured as DFP, UFP or DRP, depending on the application.

The SY20794 integrates the physical layer of the USB BMC power delivery protocol to allow up to 100W of power and role swap. The BMC PD block enables full support for alternative interfaces of the Type-C specification.

The SY20794 integrates 2 independent 700mΩ switches to control the VCONN power for an active cable. It also provides over voltage protection and programmable over current protection for VCONN.

### Ordering Information



Ordering Number	Package type	Note
SY20794VWS	CSP1.29*1.25-9	----

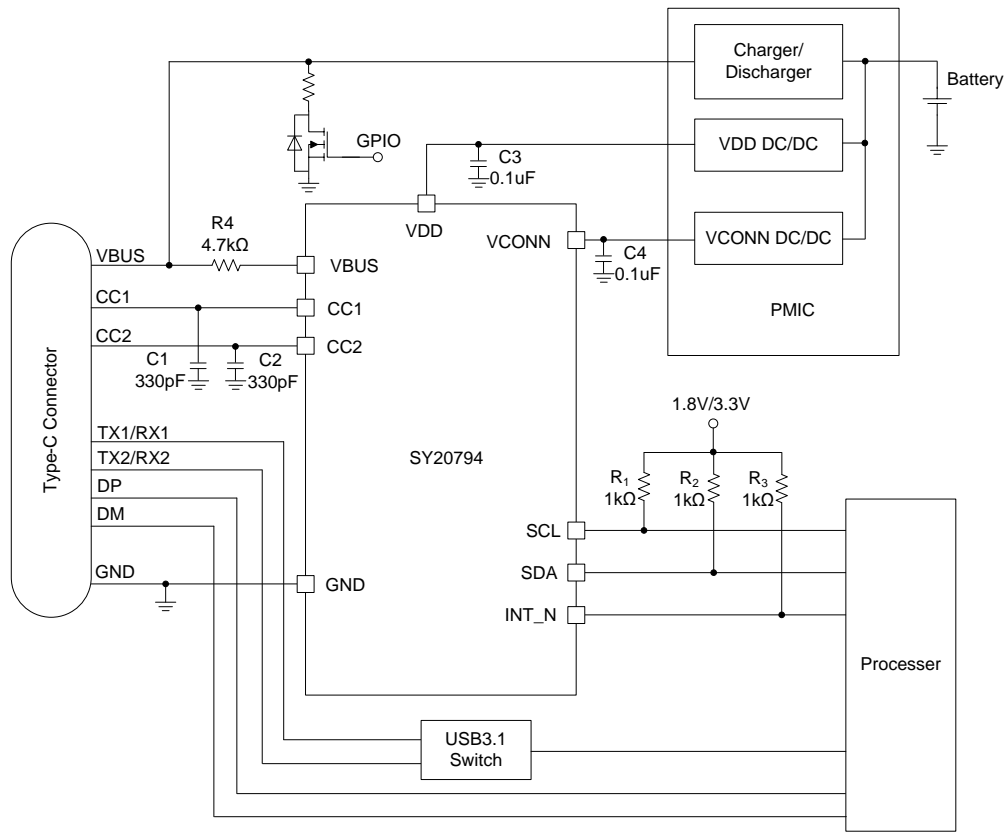
### 2 Features

- USB PD3.0 PHY with I<sup>2</sup>C Interface
- Current Capability Advertising and Detection
- CC Attach/Detach Detection as DFP, UFP and DRP
- Active Cable Detection
- Cable Orientation Detection
- BIST Mode Support
- VBUS Detection Support
- VCONN Power Control Support
- VCONN OVP, SCP and Programmable OCP
- Dead Battery Support
- Low Power Consumption: typical 11uA with DRP in Low Power Mode
- VDD range:3-5.5V
- Thermal Shutdown
- CSP1.29×1.25-9 Package

### 3 Applications

- Smartphones
- Tablets, Notebooks
- Laptops
- Adapters, Power Banks

## 4 Typical Applications



**Figure 1. Application Schematic for Smartphone**

**Table of Contents**

**1 General Description** ..... 1

**2 Features** ..... 1

**3 Applications** ..... 1

**4 Typical Applications** ..... 2

**5 Pin Configuration and Functions** ..... 4

**6 Functional Block Diagram** ..... 5

**7 Specifications** ..... 6

    7.1 Absolute Maximum Ratings ..... 6

    7.2 Recommended Operating Conditions ..... 6

    7.3 Electrical Characteristics ..... 7

    7.4 Typical Performance Characteristics ..... 10

**8 Function Description** ..... 11

    8.1 Type-C CC logic ..... 11

    8.2 PD Physical Layer with BMC ..... 12

    8.3 PD Protocol Layer Control ..... 12

    8.4 Dead Battery Mode ..... 14

    8.5 VCONN Power Control and Protection ..... 14

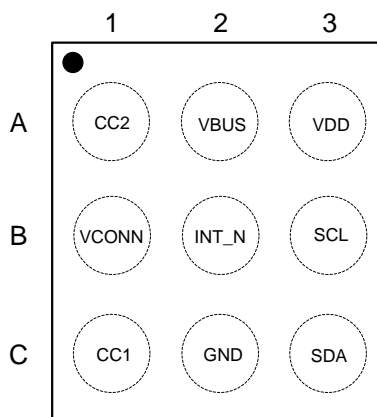
    8.6 Interrupts ..... 14

    8.7 Registers ..... 15

    8.8 I<sup>2</sup>C Interface ..... 33

**9 Applications Information** ..... 36

## 5 Pin Configuration and Functions



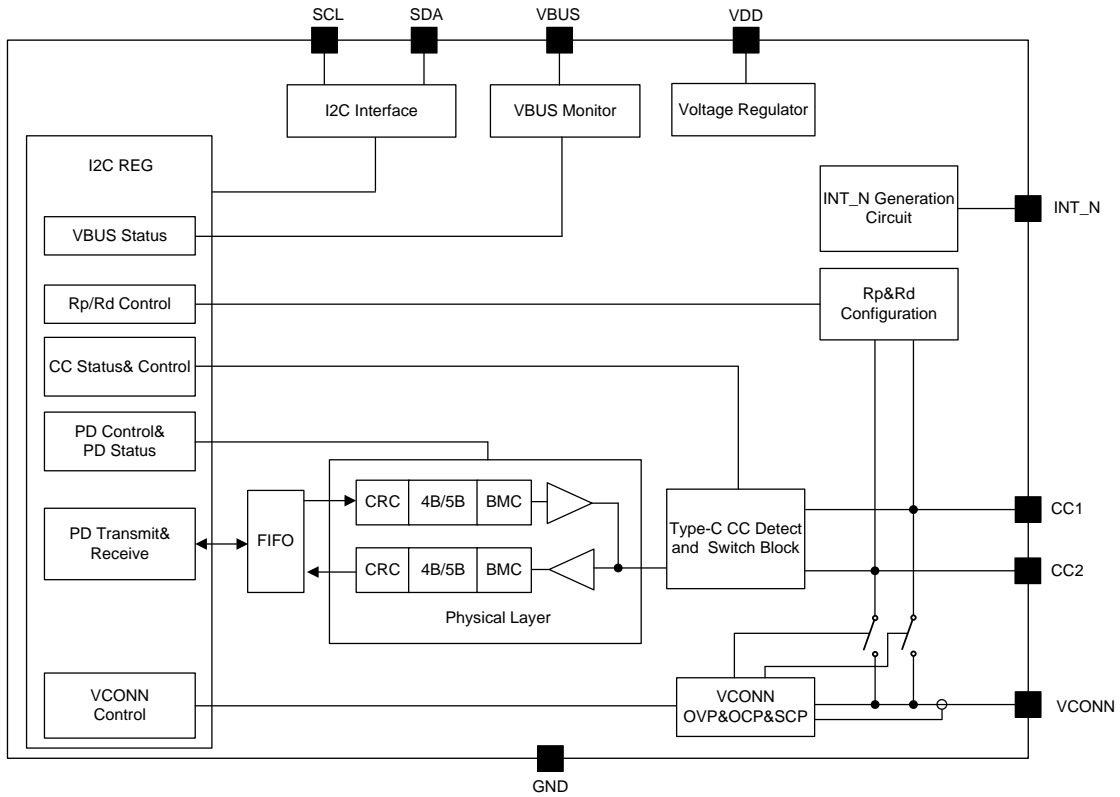
**Figure 2. CSP1.29×1.25-9 in top view**

**Top Mark: m6xyz** (device code: **m6**, *x*=year code, *y*=week code, *z*=lot number code)

**Table 1. Pin Functions**

Name	PIN Number	Description
CC2	A1	Type-C connector configuration channel pin. It is used for connector polarity, end-device connection detection, current capabilities, and PD communication.
VBUS	A2	VBUS input pin. Connect to VBUS of Type-C connector.
VDD	A3	Input supply voltage. Connect a 100nF ceramic capacitor from VDD to GND.
VCONN	B1	Power supply pin of VCONN. VCONN is switched to the correct CC pin to power Type-C full-featured cables and other accessories. If VCONN support is not required in the system, VCONN can be left floating or shorted to GND.
INT_N	B2	Open drain output. Asserted low to indicate the status change occurs. Connect INT_N to the logic rail through a pull-up resistor.
SCL	B3	I2C Interface clock. Connect SCL to the logic rail through a pull-up resistor.
CC1	C1	Type-C connector configuration channel pin. It is used for connector polarity, end-device connection detection, current capabilities, and PD communication.
GND	C2	Ground pin.
SDA	C3	I2C Interface data. Connect SDA to the logic rail through a pull-up resistor.

## 6 Functional Block Diagram



**Figure 3. Functional Block Diagram**

## 7 Specifications

### 7.1 Absolute Maximum Ratings (Note 1)

VDD/VCONN	-----	-0.3V- 6V
CC1/CC2	-----	-0.3V-24V
VBUS	-----	-0.3V-28V
SDA/SCL/INT_N	-----	-0.3V- 6V
Package Thermal Resistance (Notes 2)		
$\Theta_{JA}$	-----	85°C/W
$\Theta_{JC}$	-----	8°C/W
Junction Temperature Range	-----	-40°C to +150°C
Lead Temperature (Soldering, 10 sec.)	-----	260°C
Storage Temperature Range	-----	-65°C to 150°C

### 7.2 Recommended Operating Conditions (Note 3)

VBUS, CC1, CC2	-----	0V-20V
VDD	-----	3.0V-5.5V
VCONN	-----	3.3V-5.5V
SCL, SDA, INT_N	-----	0V-5.5V
Junction Temperature Range	-----	-40°C to 125°C
Ambient Temperature Range	-----	-40°C to 85°C

### 7.3 Electrical Characteristics

(T<sub>A</sub>=25°C, T<sub>A</sub>=T<sub>J</sub>, V<sub>VDD</sub> = 3V to 5.5V, V<sub>VCONN</sub>=3.3V to 5.5V, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Power Consumption</b>						
I <sub>SHIP</sub>	VDD consumption current in shipping mode; CC1 and CC2 are both Rd			9	15	μA
I <sub>LPR</sub>	VDD consumption current in Low Power Mode with CC1 and CC2 toggling as DRP			11	20	μA
I <sub>IDLE</sub>	VDD consumption current in active mode with 24M OSC disabled			100	150	μA
I <sub>ACTIVE</sub>	VDD consumption current in active mode with 24M OSC enabled			1.1	1.5	mA
<b>Transmitter and Receiver Specifications (CC1, CC2)</b>						
V <sub>(TXHI)</sub>	Transmit high voltage		1.05	1.125	1.2	V
V <sub>(TXLO)</sub>	Transmit low voltage		-75		80	mV
R <sub>TX</sub>	Transmitter output resistance		33	45	75	Ω
z <sub>BmcRX</sub>	Receiver input impedance		1			MΩ
<b>Timing Requirements</b>						
t <sub>UI</sub>	Bit unit interval		3.03	3.3	3.7	μs
f <sub>BitRate</sub>	Bit Rate		270	300	330	kbps
P <sub>BitRate</sub>	Maximum difference between the bit-rate during the part of the packet following the Preamble and the reference bit-rate				0.25	%
t <sub>InterFrameGap</sub>	Time from the end of last bit of a Frame until the start of the first bit of the next Preamble		25			μs
t <sub>StartDrive</sub>	Time before the start of the first bit of the Preamble when the transmitter shall start driving the line		-1		1	μs
t <sub>EndDriveBMC</sub>	Time to cease driving the line after the end of the last bit of the Frame				23	μs
t <sub>Fall</sub>	Fall time		300			ns
t <sub>HoldLowBMC</sub>	Time to cease driving the line after the final high-to-low transition		1			μs
t <sub>Rise</sub>	Rise time		300			ns
<b>DFP Specifications(CC1, CC2)</b>						
V <sub>Detach_0.5</sub>	UFP detach threshold in default DFP mode	Rising edge	1.52	1.585	1.65	V
	Hysteresis	Falling edge		0.02		V
V <sub>Detach_1.5</sub>	UFP detach threshold in 1.5A DFP mode	Rising edge	1.52	1.585	1.65	V
	Hysteresis	Falling edge		0.02		V

V <sub>Detach_3.0</sub>	UFP detach threshold in 3.0A DFP mode	Rising edge	2.50	2.625	2.75	V
	Hysteresis	Falling edge		0.02		V
V <sub>Ra_0.5</sub>	Ra detection threshold in default DFP mode	Falling edge	0.15	0.2	0.23	V
	Hysteresis	Rising edge		0.02		V
V <sub>Ra_1.5</sub>	Ra detection threshold in 1.5A DFP mode	Falling edge	0.35	0.4	0.43	V
	Hysteresis	Rising edge		0.02		V
V <sub>Ra_3.0</sub>	Ra detection threshold in 3.0A DFP mode	Falling edge	0.75	0.8	0.83	V
	Hysteresis	Rising edge		0.02		V
I <sub>Rp_0.5</sub>	Rp pull-up current in default DFP mode		64	80	96	μA
I <sub>Rp_1.5</sub>	Rp pull-up current in 1.5A DFP mode		166	180	194	μA
I <sub>Rp_3.0</sub>	Rp pull-up current in 3.0A DFP mode		304	330	356	μA
<b>UFP Specifications (CC1, CC2)</b>						
R <sub>d</sub>	Pull down resistor		4.6	5.1	5.6	kΩ
V <sub>Rp_0.5</sub>	Default DFP source current capability detection threshold	Falling edge	0.15	0.19	0.23	V
	Hysteresis	Rising edge		0.02		V
V <sub>Rp_1.5</sub>	1.5A DFP source current capability detection threshold	Falling edge	0.61	0.66	0.68	V
	Hysteresis	Rising edge		0.02		V
V <sub>Rp_3.0</sub>	3.0A DFP source current capability detection threshold	Falling edge	1.16	1.23	1.29	V
	Hysteresis	Rising edge		0.02		V
V <sub>DBL</sub>	UFP pull-down voltage for the default DFP and 1.5A DFP in dead battery mode	V <sub>VDD</sub> = 0V			1.1	V
V <sub>DBH</sub>	UFP pull-down voltage for the 3.0A DFP in dead battery mode	V <sub>VDD</sub> = 0V			2.45	V
<b>VCONN</b>						
I <sub>VCONN</sub>	VCONN consumption current without supplying to CC1/CC2	V <sub>VDD</sub> =3V, V <sub>VCONN</sub> =5.5V		3.2	6	μA
V <sub>VCONN_PRESNET</sub>	Threshold for detecting VCONN present on CC1 or CC2	V <sub>CC1</sub> or V <sub>CC2</sub> Rising edge	2.55	2.75	2.9	V
V <sub>VCONN_PRESNET_HYS</sub>	Threshold hysteresis for detecting VCONN present on CC1 or CC2			0.5		V
V <sub>VCONN_OVP</sub>	VCONN input voltage OVP threshold	Rising edge	5.6	5.85	6.1	V
R <sub>ON</sub>	On resistance for VCONN switch	V <sub>VCONN</sub> =3V to 5.5V		0.7	1	Ω

I <sub>OCP</sub>	VCONN OCP threshold	V <sub>VDD</sub> = 3.3V, V <sub>VCONN</sub> = 5.5V, OCP setting 200mA	135	205	275	mA
		V <sub>VDD</sub> = 3.3V, V <sub>VCONN</sub> = 5.5V, OCP setting 300mA	240	310	380	mA
		V <sub>VDD</sub> = 3.3V, V <sub>VCONN</sub> = 5.5V, OCP setting 400mA	345	415	485	mA
		V <sub>VDD</sub> = 3.3V, V <sub>VCONN</sub> = 5.5V, OCP setting 500mA	450	520	590	mA
		V <sub>VDD</sub> = 3.3V, V <sub>VCONN</sub> = 5.5V, OCP setting 600mA	550	625	695	mA
t <sub>Soft_VCCON_3.3V</sub>	Soft-start time for VCONN switch on with 3.3V voltage	V <sub>VDD</sub> = 3.3V, V <sub>VCONN</sub> = 3.3V	350	450	750	μs
t <sub>Soft_VCCON_5V</sub>	Soft-start time for VCONN switch on with 5V voltage	V <sub>VDD</sub> = 3.3V, V <sub>VCONN</sub> = 5V	430	540	900	μs
<b>VBUS detection</b>						
vSafe0V	Safe operating voltage at “zero volts”	Falling edge	0		0.8	V
V <sub>BUS_PRESENT</sub>	BUS voltage detection threshold for the present of BUS	Rising edge			4	V
		Falling edge	3.5			V
<b>I<sup>2</sup>C Electrical Characteristic</b>						
I2C_VDD	I2C BUS Supply voltage		1.5		5.5	V
V <sub>IL</sub>	LOW-Level voltage threshold				0.4	V
V <sub>IH</sub>	HIGH-Level voltage threshold	V <sub>VDD</sub> = 3V to 5.5V	1.3			V
V <sub>OL</sub>	LOW-Level output voltage	V <sub>VDD</sub> = 3V to 5.5V			0.4	V
f <sub>SCL</sub>	SCL Clock Frequency	V <sub>VDD</sub> = 3V to 5.5V			3400	kHz

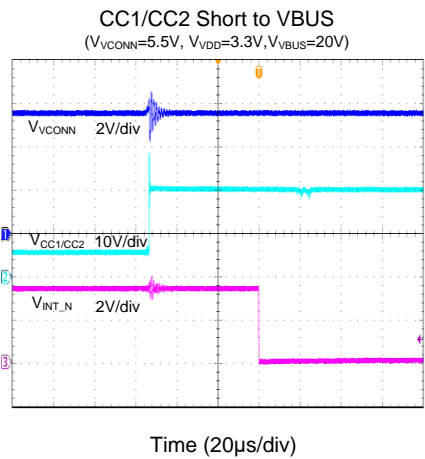
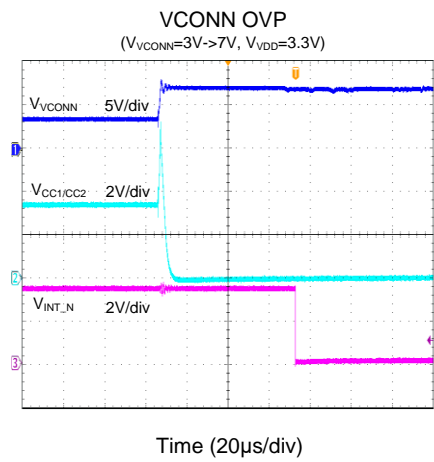
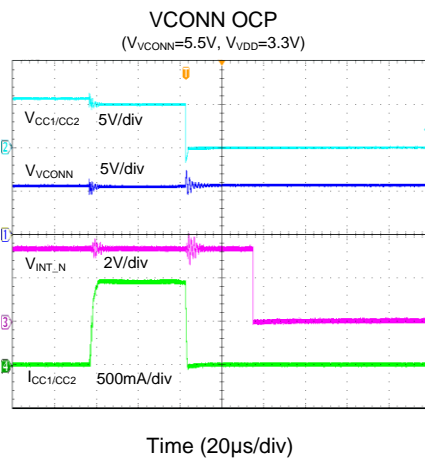
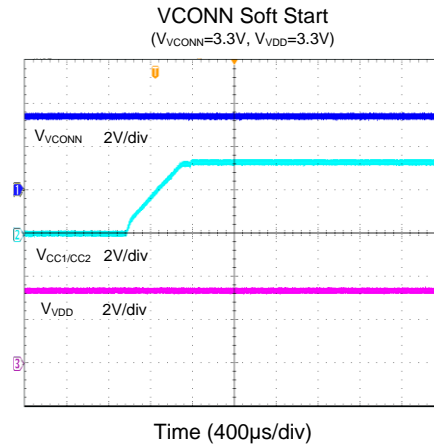
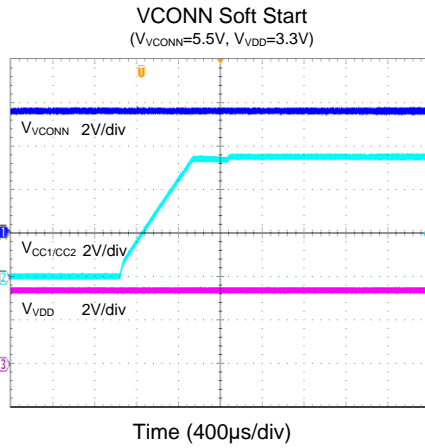
**Note 1:** Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

**Note 2:** θ<sub>JA</sub> is measured in the natural convection at T<sub>A</sub> = 25°C on a low effective four layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

**Note 3:** The device is not guaranteed to function outside its operating conditions.

### 7.4 Typical Performance Characteristics

(TA=25°C, unless otherwise specified.)



## 8 Function Description

The SY20794 is a USB Type-C Port Controller with TCPC Interface (TCPCI). The TCPC is a functional block which encapsulates VBUS detection, VCONN power control, USB Type-C CC logic, and the USB PD BMC Physical Layer. Under the control of an external microprocessor (TCPM), the SY20794 can determine port (DFP and UFP) attach and detach, transmit and receive PD message through CC line, and auto respond GoodCRC if the received message is valid and enabled. The SY20794 shall also notify the TCPM of its status change including power status, fault status by asserting the interrupt pin (INT\_N).

### 8.1 Type-C CC logic

The SY20794 integrates three threshold comparators, three types of Rp and Rd which meet the USB Type-C specification 2.0 for each CC pin. It can be configured as DFP, UFP or DRP through I2C.

When the SY20794 is configured as a UFP, one of the status including “Unattached, Rp\_default\_attached, Rp\_1.5A\_attached, Rp\_3A\_attached” shall be updated in the **CC\_STATUS Register**. When the SY20794 is configured as a DFP, one of the status including “Unattached, Ra\_attached, Rd\_attached” shall be reported. When the SY20794 is configured as a DRP, both CC1 and CC2 toggle between Rp(source) and Rd(sink). The toggle period and duty cycle of source can be programmed by the **TDRP Register** and **DCSRCDRP Register**. The CC logic block is shown in Figure 4.

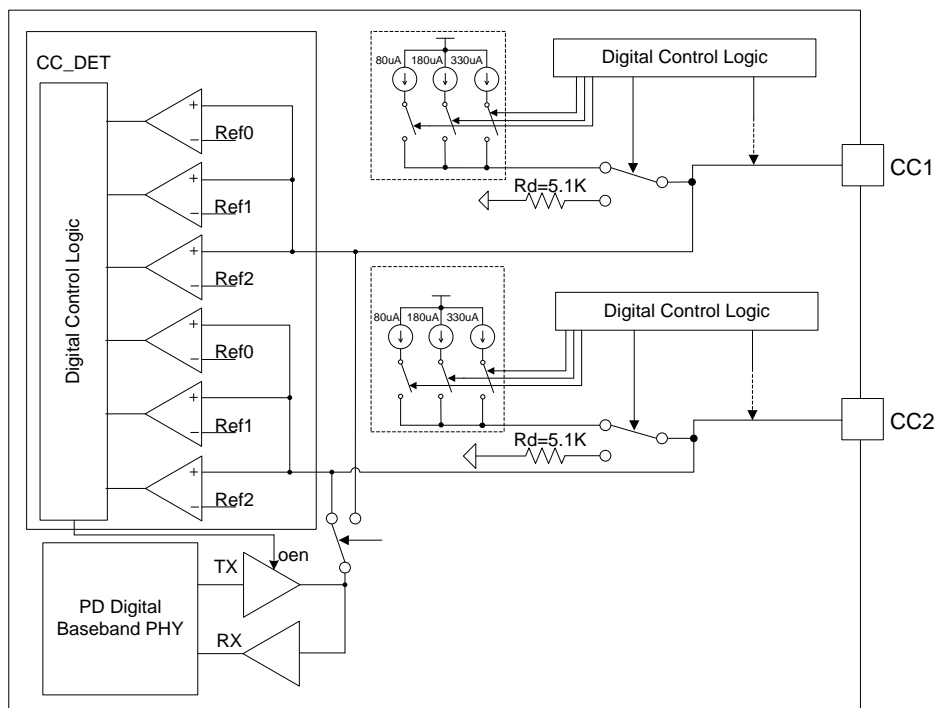


Figure 4. CC Logic Block

#### 8.1.1 DRP Configure

To start toggling between source and sink, the I2C operation is as follows:

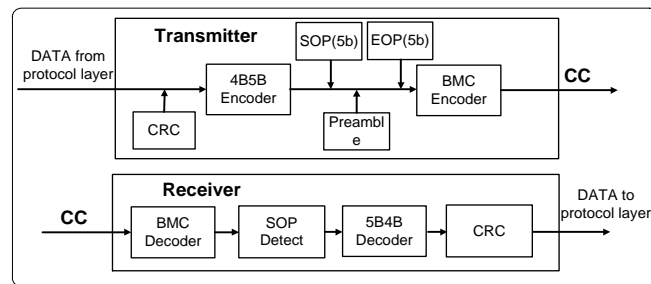
1. Upon power-up, the SY20794 is in shipping mode. The TCPM needs to wake up the SY20794 by writing 1 to the **SHIPPING\_QUIT** bit in the **VENDER\_CONTROL1 Register** and **BG\_EN** bit in the **VENDER\_POWER Register**.
2. The TCPM reads the **ALERT Register** to determine the reason for INT\_N assertion.

3. The TCPM clears the **CC Status** bit in the **ALERT Register** by writing 1 to the bit. If both CC1 and CC2 are unattached, the TCPM programs the SY20794 to present Rd on both CC pins by writing 0x6A to the **ROLE\_CONTROL Register**.
4. The TCPM writes **Look4Connection** command to the **COMMAND Register**, CC1 and CC2 toggle between Rp(source) and Rd(sink) .
5. For low power consumption, the SY20794 can enter Low Power Mode when the **LPR\_EN** bit is 1, the **BG\_EN** bit is 0, and the **OSC\_24M\_EN** bit is 0 by writing the **VENDER\_POWER Register**. Because any un-cleared INT shall set the **OSC\_24M\_EN** bit to 1, so it is necessary to clear all unmasked INTs.

## 8.2 PD Physical Layer with BMC

The PD function of the SY20794 complies with USB Power Delivery Specification, Revision 3.0 and the latest Type-C Port Controller Interface Specification. Some “Not support” functions are listed in the register.

The SY20794 implements the entire USB PD Physical Layer with BMC encoding and a part of portions of the USB PD Protocol Layer. The PD Physical Layer has two sections: Transmitter and Receiver. Its block diagram is shown in Figure 5.



**Figure 5. Physical Layer Block**

The transmitter shall receive packet data from the register, then encode the packet data including the CRC (i.e. the payload), transmit the Packet (Preamble, SOP\*, payload, CRC and EOP) across the channel using Bi-phase Mark Coding (BMC) over CC.

The receiver is responsible for detecting the SOP\* type and decoding the received data including the CRC. If the CRC is valid and the SOP\* type is enabled in the **RECEIVE\_DETECT Register**, the chip shall reply GoodCRC automatically, and then deliver the packet data to the **RX\_BUFFER Registers** and pull down INT\_N to notify the TCPM to read. If the CRC is invalid, flush the received data.

## 8.3 PD Protocol Layer Control

The SY20794 integrates the following portions of the USB PD Protocol Layer:

1. CRCReceiveTimer.
2. RetryCounter.
3. MessageID is not checked in the TCPC when a non-GoodCRC message is received. Retried messages that are received are passed to the TCPM via I2C.
4. A received GoodCRC must match the transmitted MessageID and SOP\* type before it is considered valid. Two things allow the TCPM to track the MessageID even when asynchronous messages are received.
  - a) If the **Receive SOP\* Message Status** bit is not cleared when the TCPM requests a TRANSMIT, then the **I2C Interface Error** shall be asserted.
  - b) If a message is received before the SY20794 has processed a transmit request, it asserts the **Transmit SOP\* Message Discarded** bit in the **ALERT Register**.

5. BIST handling shall be as follows: Each incoming BIST message may be passed up to the policy engine as is any other incoming USB PD Message, or responded to with a GoodCRC without passing to the policy engine. The SY20794 provides a mechanism to allow the policy engine to send a BIST Continuous Carrier Mode 2 message for tBistContMode.

### **8.3.1 I2C Operation to Transmit an SOP\* Message**

The **TX\_BUF\_BYTE\_x Registers** hold the content of the SOP\* USB PD message to be transmitted. The SY20794 automatically increments the **TX\_BUF\_BYTE\_x** offset when the TCPM writes to the **TX\_BUF\_BYTE\_x Registers**. The TCPM can write the **TX\_BUF\_BYTE\_x** beginning at offset 1 by writing the **ResetTransmitBuffer** command.

The steps for transmitting an SOP\* Message are as follows:

1. Upon power-up, the SY20794 is in shipping mode, the TCPM needs to wake up the SY20794 by writing 1 to the **SHIPPING\_QUIT** bit in the **VENDER\_CONTROL1 Register** and writing 1 to the **BG\_EN** bit in the **VENDER\_POWER Register**.
2. The TCPM reads the **ALERT Register** to determine the reason for INT\_N assertion. Before sending any SOP\* PD message, the TCPM clears corresponding INTs including **Transmit SOP\* Message Successful**, **Transmit SOP\* Message Discarded**, **Transmit SOP\* Message Failed** and **Received SOP\* Message Status**.
3. The TCPM enables specific SOP\* type in the **RECEIVE\_DETECT Register**. Otherwise, the received GoodCRC cannot be passed and processed correctly.
4. The TCPM writes the content of the message to be transmitted into the transmit buffer. As **TX\_BUF\_BYTE\_x** are hidden and can only be accessed by writing the **I2C\_WRITE\_BYTE\_COUNT Register (Register 51h)**, the TCPM shall write as many bytes in the TX buffer as defined in **I2C\_WRITE\_BYTE\_COUNT** in one I2C write transaction. Otherwise, a **FAULT\_STATUS.I2CInterfaceError** bit will be generated.
5. The TCPM writes the **TRANSMIT Register** to request a SOP\* transmission.
6. The outcome of the transmission may be one of three indications after asserting the INT\_N: **Transmit SOP\* Message Successful**, **Transmit SOP\* Message Discarded**, **Transmit SOP\* Message Failed**.

### **8.3.2 Transmit a Hard Reset Message**

The steps for transmitting a Hard Reset message are as follows:

1. Upon power-up, the SY20794 is in shipping mode, the TCPM needs to wake up the SY20794 by writing 1 to the **SHIPPING\_QUIT** bit in the **VENDER\_CONTROL1 Register** and writing 1 to **BG\_EN** bit in **VENDER\_POWER Register**.
2. The TCPM writes the **TRANSMIT Register** to request a Hard Reset transmission.
3. After the transmission, both **Transmit SOP\* Message Successful** and **Transmit SOP\* Message Failed** INTs are asserted. The **RECEIVE\_DETECT** and **READABLE\_BYTE\_COUNT Registers** are automatically cleared by the SY20794 to disable the USB PD message passing.

### **8.3.3 I2C Operation to Read the SOP\* Message**

When the **Received SOP\* Message Status** INT is asserted, **READABLE\_BYTE\_COUNT**, **RX\_BUF\_FRAME\_TYPE** and **RX\_BUF\_BYTE\_x** shall be prepared well in registers. As **RX\_BUF\_FRAME\_TYPE** and **RX\_BUF\_BYTE\_x** are hidden and can only be accessed by reading at address 30h, the SY20794 shall automatically increment the pointer of **RX\_BUF\_BYTE\_x** as the TCPM reads **RX\_BUF\_BYTE\_x**. The TCPM can re-read **RX\_BUF\_BYTE\_x** at a zero offset by writing to **COMMAND.ResetReceiveBuffer (0xEE)**. However, the pointer of **RX\_BUF\_BYTE\_x** would not increment if the TCPM reads **READABLE\_BYTE\_COUNT** or **RX\_BUF\_FRAME\_TYPE**.

The **RX\_BUF\_BYTE** is sized to hold two 30 bytes SOP\* messages, so the TCPM should read **RX\_BUF\_BYTE\_x** and clear the **Received SOP\* Message Status** INT timely.

The steps for receiving an SOP\* Message are as follows:

1. Upon power-up, the SY20794 is in shipping mode, the TCPM needs to wake up the SY20794 by writing 1 to the **SHIPPING\_QUIT** bit in the **VENDER\_CONTROL1 Register** and **BG\_EN** bit in the **VENDER\_POWER Register**.
2. The TCPM enables specific SOP\* type in the **RECEIVE\_DETECT Register** to ensure no SOP\* message is missed.
3. The TCPM reads the **ALERT Register** to determine the reason for INT\_N assertion. If **Received SOP\* Message Status** is asserted, the TCPM firstly reads 2 bytes from Address 30h to get **READABLE\_BYTE\_COUNT** and **RX\_BUF\_FRAME\_TYPE**.
4. The TCPM reads **n+2** bytes continuously from address 30h (n=value of **READABLE\_BYTE\_COUNT**).
5. The TCPM clears the INT by writing 1 to the **Received SOP\* Message Status** bit. If another PD message is stored in RX buffer, the INT\_N would be pulled low for **Received SOP\* Message Status** again. When two messages are stored in RX buffer and waiting for read, the **Rx Buffer Overflow INT** would be asserted. At this condition, no future GoodCRC would be sent if the **BIST\_TEST\_MODE** bit is 0.

## 8.4 Dead Battery Mode

When VDD is power off, the PD communication and Type-C detection function can no longer be maintained. To guide the VBUS from USB TYPE-C to charge the battery or power the system, Rd shall be presented in both CC pins. This condition is called as Dead Battery Mode.

## 8.5 VCONN Power Control and Protection

VCONN is required by active cables, emarker, and VCONN powered accessories like Alt Mode adapters. These types of devices or cables present Ra on one CC pin and Rd on the other CC pin. VCONN must be enabled when any of device or cable requiring VCONN is connected to a Type-C port and the SY20794 is operating as a DFP or DFP in DRP mode. The TCPM can also enable the VCONN switch when the SY20794 is a UFP during a VCONN\_SWAP sequence.

### 8.5.1 VCONN OCP and SCP

The SY20794 implements the VCONN switch with programmable OCP. The OCP threshold range is from 200mA to 600mA. When VCONN OCP happens, the VCONN switch would be closed quickly to avoid VCONN damage. The control bit **EN\_VCONN** would be cleared and the **VCON\_OC** INT would be asserted. The TCPM has to write 1 to the **VCON\_OC** bit in the **FAULT\_STATUS Register** and then write 1 to clear the **ALERT.Fault** bit.

The short circuit protection (SCP) of VCONN switch is also supported in the SY20794 and the protection actions are almost same with those of OCP.

### 8.5.2 VCONN OVP

To avoid chip damage, the SY20794 integrates OVP protection. When the voltage in CC pins, or VCONN is over  $V_{VCONN\_OVP}$ , the VCONN switch shall be turned off immediately and VCONN discharge is applied automatically. The control bit **EN\_VCONN** would be reset to 0 simultaneously and the **VCON\_OV** bit would be set. Similar with the OCP, to clear the **ALERT.Fault**, the OVP has to be cleared firstly by writing 1 to the **VCON\_OV** bit in the **FAULT\_STATUS Register**.

### 8.5.3 Thermal Shutdown

When the junction temperature of the IC exceeds 150°C, the SY20794 turns off the VCONN switch until the temperature decreases to 130°C.

## 8.6 Interrupts

The SY20794 asserts the INT\_N pin low when an unmasked event occurs. Upon assertion of the interrupt, the TCPM should read the **ALERT Register** to determine the reason for interrupt. Upon reading the Alert register, the TCPM should clear the interrupt by writing 1 to the appropriate field in the Alert register. If the **FAULT** flag is set in the **ALERT Register**, the TCPM must first read the **FAULT\_STATUS Register** to determine the reason for

fault, and then clear the appropriate field in the **FAULT\_STATUS Register** by writing 1. Once all fields in **FAULT\_STATUS Register** are cleared, the TCPM can then clear the flag in the **ALERT Register** by writing 1.

## 8.7 Registers

The SY20794's slave address is 1001 110B in 7-bit format.

The SY20794 integrates all the necessary registers which can standardize and simplify the USB Type-C and PD protocol control. The registers are listed as following.

**Table 2. Register Summary**

Address	Register Name	Read/Write
00h/01h	VENDOR_ID	R
02h/03h	PRODUCT_ID	R
04h/05h	DEVICE_ID	R
06h/07h	USBTYPESPEC_REV	R
08h/09h	USBPD_REV	R
0Ah/0Bh	PD_INTERFACE	R
10h/11h	ALERT	R/W
12h/13h	ALERT_MASK	R/W
14h	POWER_STATUS_MASK	R/W
15h	FAULT_STATUS_MASK	R/W
19h	TCPC_CONTROL	R/W
1Ah	ROLE_CONTROL	R/W
1Bh	FAULT_CONTROL	R/W
1Ch	POWER_CONTROL	R/W
1Dh	CC_STATUS	R
1Eh	POWER_STATUS	R
1Fh	FAULT_STATUS	R/W
23h	COMMAND	W
24h	DEVICE_CAPABILITIES_1L	R
25h	DEVICE_CAPABILITIES_1H	R
26h	DEVICE_CAPABILITIES_2L	R
27h	DEVICE_CAPABILITIES_2H	R
28h	STANDARD_INPUT_CAPABILITIES	R
29h	STANDARD_OUTPUT_CAPABILITIES	R
2Eh	MESSAGE_HEADER_INFO	R/W
2Fh	RECEIVE_DETECT	R/W
30h	READABLE_BYTE_COUNT	R
	RX_BUF_FRAME_TYPE	R
	RX_BUF_BYTE_x	R
50h	TRANSMIT	R/W
51h	I2C_WRITE_BYTE_COUNT	W
	TX_BUF_BYTE_x	W
90h	VENDER_POWER	R/W

93h	VCONN_OC	R/W
97h	VENDER_STATUS	R
98h	VENDER_INT	R/W
99h	VENDER_MASK	R/W
9Bh	VENDER_CONTROL1	R/W
9Fh	VENDER_CONTROL2	R/W
A0h	VENDER_CONTROL3	R/W
A2h	TDRP	R/W
A3h	DCSRCDRP_L	R/W
A4h	DCSRCDRP_H	R/W

**Table 3. VENDOR\_ID Register (Register 00h/01h)**

Bit	Bit Name	Type	Description
15-0	Vendor ID (VID)	R	A unique 16-bit unsigned integer assigned by the USB-IF to the Vendor. <b>Set to 0x3FAB</b>

**Table 4. PRODUCT\_ID Register (Register 02h/03h)**

Bit	Bit Name	Type	Description
15-0	USB Product ID (PID)	R	A unique 16-bit unsigned integer. Assigned uniquely by the Vendor to identify the TCPC. <b>Set to 0xC608</b>

**Table 5. DEVICE\_ID Register (Register 04h/05h)**

Bit	Bit Name	Type	Description
15-0	bcdDevice	R	A unique 16-bit unsigned integer assigned by the Vendor to identify the version of the TCPC. <b>Set to 0x3C02</b>

**Table 6. USBTYPEC\_REV Register (Register 06h/07h)**

Bit	Bit Name	Type	Description
15-8	Reserved	R	Reserved
7-0	bcdUSBTYPEC Release	R	0001 0001- Release 1.1

**Table 7. USBPD\_REV Register (Register 08h/09h)**

Bit	Bit Name	Type	Description
15-8	bcdUSBPD Revision	R	0010 0000-Revision 2.0
7-0	bcdUSBPD Version	R	0001 0001 -Version 1.1

**Table 8. PD\_INTERFACE Register (Register 0Ah/0Bh)**

Bit	Bit Name	Type	Description
15-8	bcd USB-PD Inter-Block Specification Revision	R	0001 0000 – Revision 1.0
7-0	bcd USB-PD Inter-Block Specification Version	R	0001 0000 – Version 1.0 (this release)

**Table 9. ALERT Register (Register 10h/11h)**

Bit	Bit Name	Type	Description
15	RX_CABLE_RESET	R/W	<b>0: Cleared (default)</b> 1: Received Cable Reset message
14	Alert Extended	R	Not Supported
13	Extended Status	R	Not Supported
12	Beginning SOP* Message Status	R	Not Supported
11	VBUS Sink Disconnect Detected	R	Not Supported
10	Rx Buffer Overflow	R/W	<b>0: TCPC Rx buffer is functioning properly (default)</b> 1: TCPC Rx buffer has overflowed. Future GoodCRC shall not be sent. Writing 1 to this register acknowledges the overflow. The overflow is cleared by writing to ALERT.Receive SOP* Message Status.
9	Fault	R/W	<b>0: No fault (default)</b> 1: A fault has occurred. Read the FAULT_STATUS register.
8	VBUS Voltage Alarm Lo	R	Not Supported
7	VBUS Voltage Alarm Hi	R	Not Supported
6	Transmit SOP* Message Successful	R/W	<b>0: Cleared (default)</b> 1: Reset or SOP* message transmission successful. GoodCRC response received on SOP* message transmission. Transmit SOP* message buffer registers are empty. Transmit SOP* Message Successful shall be asserted after sending Hard Reset or Cable Reset.
5	Transmit SOP* Message Discarded	R/W	<b>0: Cleared (default)</b> 1: Reset or SOP* message transmission not sent due to an incoming receive message. Transmit SOP* message buffer registers are empty.
4	Transmit SOP* Message Failed	R/W	<b>0: Cleared (default)</b> 1: SOP* message transmission not successful, no GoodCRC response received on SOP* message transmission. Transmit SOP* message buffer registers are empty. Transmit SOP* Message Failed shall be asserted after sending Hard Reset or Cable Reset.
3	Received Hard Reset	R/W	<b>0: Cleared (default)</b> 1: Received Hard Reset message
2	Received SOP* Message Status	R/W	<b>0: Cleared (default)</b> 1: RECEIVE_BUFFER register changed
1	Power Status	R/W	<b>0: Cleared (default)</b> 1: Power Status changed

0	CC Status	R/W	<b>0: Cleared (default)</b> 1: CC Status changed
---	-----------	-----	---

Note: Write 1 to corresponding bit in Alert to clear that bit.

**Table 10. ALERT\_MASK Register (Register 12h/13h)**

Bit	Bit Name	Type	Description
15	M_RX_Cable_Reset_Alert	R/W	0: Interrupt masked <b>1: Interrupt unmasked (default)</b>
14	M_Alert_Extended	R	Not Supported
13	M_Extended_Status	R	Not Supported
12	M_Beginning_SOP*_Message_Status	R	Not Supported
11	M_VBUS_Sink_Disconnect_Detected	R	Not Supported
10	M_RXBUF_OVFLOW	R/W	0: Interrupt masked <b>1: Interrupt unmasked (default)</b>
9	M_FAULT	R/W	0: Interrupt masked <b>1: Interrupt unmasked (default)</b>
8	M_VBUS_Voltage_Alarm_Lo	R	Not Supported
7	M_VBUS_Voltage_Alarm_Hi	R	Not Supported
6	M_Transmit_SOP*_Message_Successful	R/W	0: Interrupt masked <b>1: Interrupt unmasked (default)</b>
5	M_Transmit_SOP*_Message_Discarded	R/W	0: Interrupt masked <b>1: Interrupt unmasked (default)</b>
4	M_Transmit_SOP*_Message_Failed	R/W	0: Interrupt masked <b>1: Interrupt unmasked (default)</b>
3	M_RX_HARD_RESET	R/W	0: Interrupt masked <b>1: Interrupt unmasked (default)</b>
2	M_RX_SOP_MSG_STATUS	R/W	0: Interrupt masked <b>1: Interrupt unmasked (default)</b>
1	M_POWER_STATUS	R/W	0: Interrupt masked <b>1: Interrupt unmasked (default)</b>
0	M_CC_STATUS	R/W	0: Interrupt masked <b>1: Interrupt unmasked (default)</b>

**Table 11. POWER\_STATUS\_MASK Register (Register 14h)**

Bit	Bit Name	Type	Description
7	M_Debug_Accessory_Connected_Status	R	Not Supported

6	M_TCPC_INITIAL	R/W	0: Interrupt masked <b>1: Interrupt unmasked (default)</b>
5	M_Sourcing_High_Voltage_Status	R	Not Supported
4	M_Sourcing_VBUS_Status	R	Not Supported
3	M_VBUS_PRESENT_DETC	R/W	0: Interrupt masked <b>1: Interrupt unmasked (default)</b>
2	M_VBUS_PRESENT	R/W	0: Interrupt masked <b>1: Interrupt unmasked (default)</b>
1	M_VCONN_PRESENT	R/W	0: Interrupt masked <b>1: Interrupt unmasked (default)</b>
0	M_Sinking_VBUS_Status	R	Not Supported

**Table 12. FAULT\_STATUS\_MASK Register (Register 15h)**

Bit	Bit Name	Type	Description
7	M_VCON_OV	R/W	<b>0: Interrupt masked (default)</b> 1: Interrupt unmasked
6	M_Force_Off_VBUS_Interrupt_Status	R	Not Supported
5	M_Auto_Discharge_Failed	R	Not Supported
4	M_Force_Discharge_Failed	R	Not Supported
3	M_Internal_or_External_OCP_VBUS_Over_Current_Protection_Fault_Interrupt_Status	R	Not Supported
2	M_CC_UV_FAULT	R/W	<b>0: Interrupt masked (default)</b> 1: Interrupt unmasked
1	M_VCONN_OC	R/W	0: Interrupt masked <b>1: Interrupt unmasked (default)</b>
0	M_I2C_ERROR	R/W	0: Interrupt masked <b>1: Interrupt unmasked (default)</b>

**Table 13. TCPC\_CONTROL Register (Register 19h)**

Bit	Bit Name	Type	Description
7	Enable SMBus PEC	R	Not Supported
6	Enable Looking4Connection Alert	R	Not Supported
5	Enable Watchdog Timer	R	Not Supported

Bit	Bit Name	Type	Description
4	Debug Accessory Control	R	Not Supported
3-2	I2C Clock Stretching Control	R	Not Supported
1	BIST_TEST_MODE	R/W	<b>0: Normal Operation. Incoming messages enabled by RECEIVE_DETECT passed to TCPM via Alert. (default)</b> 1: BIST Test Mode. Incoming messages enabled by RECEIVE_DETECT result in GoodCRC response but may not be passed to the TCPM via Alert. TCPC may temporarily store incoming messages in the Receive Message Buffer, but this may or may not result in a Receive SOP* Message Status or a Rx Buffer Overflow alert.
0	Plug Orientation	R/W	<b>0: When VCONN is enabled, apply it to the CC2 pin. Monitor the CC1 pin for BMC communications if PD messaging is enabled.(default)</b> 1: When VCONN is enabled, apply it to the CC1 pin. Monitor the CC2 pin for BMC communications if PD messaging is enabled.

**Table 14. ROLE\_CONTROL Register (Register 1Ah)**

Bit	Bit Name	Type	Description
7	Reserved	R	Reserved
6	DRP	R/W	<b>0: No DRP. Bits B3..0 determine Rp/Rd/Ra or open settings (default)</b> 1: DRP The TCPC toggles CC1 & CC2 after receiving COMMAND.Look4Connection and until a connection is detected. Upon connection, the TCPC shall resolve to either an Rp or Rd and report the CC1/CC2 State in the CC_STATUS register. The CC pins shall stay in Potential_Connect_as_Src or Potential_Connect_as_Sink until directed otherwise.
5-4	Rp Value	R/W	<b>00: Rp default current (default)</b> 01: Rp 1.5A 10: Rp 3.0A 11: Reserved
3-2	CC2	R/W	00: Reserved 01: Rp (Use Rp definition in Bit5-4) <b>10: Rd (default)</b> 11: Z_Open
1-0	CC1	R/W	00: Reserved 01: Rp (Use Rp definition in Bit5-4) <b>10: Rd (default)</b> 11: Z_Open

**Table 15. FAULT\_CONTROL Register (Register 1Bh)**

Bit	Bit Name	Type	Description
7	DIS_VCON_OV	R/W	<b>0: Fault detection circuit enabled(default)</b> 1: Fault detection circuit disabled
6-5	Reserved	R	Reserved
4	Force Off VBUS (Source or Sink)	R	Not Supported
3	VBUS Discharge Fault Detection Timer	R	Not Supported
2	Internal or External OCP VBUS Over Current Protection Fault	R	Not Supported
1	Internal or External OVP VBUS Over Voltage Protection Fault	R	Not Supported
0	DIS_VCON_OC	R/W	<b>0: Fault detection circuit enabled(default)</b> 1: Fault detection circuit disabled

**Table 16. POWER\_CONTROL Register (Register 1Ch)**

Bit	Bit Name	Type	Description
7	Fast Role Swap Enable	R	Not Supported
6	VBUS_VOLTAGE Monitor	R	Not Supported
5	Disable Voltage Alarms	R	Not Supported
4	Auto Discharge Disconnect	R	Not Supported
3	Enable Bleed Discharge	R	Not Supported
2	Force Discharge	R	Not Supported
1	VCONN_POWER_SPT	R/W	<b>0: TCPC delivers at least 1W on VCONN(default)</b> 1: TCPC delivers at least the power indicated in Device_CAPABILITIES.VCONNPowerSupported
0	EN_VCONN	R/W	<b>0: Disable VCONN Source(default)</b> 1: Enable VCONN Source to CC

**Table 17. CC\_STATUS Register (Register 1Dh)**

Bit	Bit Name	Type	Description
7-6	Reserved	R	Reserved
5	Looking4Connection	R	<b>0: TCPC is not actively looking for a connection. A transition from '1' to '0' indicates a potential connection has been found (default)</b> 1: TCPC is looking for a connection (toggling as a DRP or looking for a connection as Sink/Source only condition)
4	ConnectResult	R	<b>0: The TCPC is presenting Rp (default)</b> 1: The TCPC is presenting Rd
3-2	CC2 State	R	If (ROLE_CONTROL.CC2=Rp) or (ConnectResult=0) <b>00: SRC.Open (default)</b> 01: SRC.Ra 10: SRC.Rd 11: Reserved If (ROLE_CONTROL.CC2=Rd) or (ConnectResult=1) <b>00: SNK.Open (default)</b> 01: SNK.Default 10: SNK.Power1.5 11: SNK.Power3.0 If ROLE_CONTROL.CC2=Open, this field is set to 00 This field always returns 00 if (Looking4Connection=1). Otherwise, the returned value depends upon ROLE_CONTROL.CC2.
1-0	CC1 State	R	If (ROLE_CONTROL.CC1 = Rp) or (ConnectResult=0) <b>00: SRC.Open (default)</b> 01: SRC.Ra 10: SRC.Rd 11: Reserved If (ROLE_CONTROL.CC1 = Rd) or ConnectResult=1) <b>00: SNK.Open (default)</b> 01: SNK.Default 10: SNK.Power1.5 11: SNK.Power3.0 If ROLE_CONTROL.CC1=Open, this field is set to 00 This field always returns 00 if Looking4Connection=1. Otherwise, the returned value depends upon ROLE_CONTROL.CC1.

**Table 18. POWER\_STATUS Register (Register 1Eh)**

Bit	Bit Name	Type	Description
7	Debug Accessory Connected	R	Not Supported
6	TCPC Initialization Status	R	<b>0: The TCPC has completed initialization and all registers are valid (default)</b> 1: The TCPC is still performing internal initialization and the only registers that are guaranteed to return the correct values are 00h...0Fh
5	Sourcing High Voltage	R	Not Supported

Bit	Bit Name	Type	Description
4	Sourcing VBUS	R	Not Supported
3	VBUS_PRESENT_DETC	R	0: VBUS Present detection disable 1: <b>VBUS Present detection enable (default)</b>
2	VBUS_PRESENT	R	<b>0: VBUS Disconnected (default)</b> 1: VBUS Connected The TCPC shall report VBUS present when TCPC detects VBUS rises above 4V. The TCPC shall report VBUS is not present when TCPC detects VBUS falls below 3.5V. The TCPC may report VBUS is not present if VBUS is between 3.5V and 4V.
1	VCONN_PRESENT	R	<b>0: VCONN is not present (default)</b> 1: This bit is asserted when VCONN voltage is applied to CC1 or CC2
0	Sinking VBUS	R	Not Supported

**Table 19. FAULT\_STATUS Register (Register 1Fh)**

Bit	Bit Name	Type	Description
7	VCON_OV	R/W	<b>0: not in an over-voltage protection state(default)</b> 1: Over-voltage fault latched Write 1 to clear this bit, then INT can be cleared by writing 1 to FAULT bit of Alert Reg.
6	Force Off VBUS (Source or Sink)	R	Not Supported
5	Auto Discharge Failed	R	Not Supported
4	Force Discharge Failed	R	Not Supported
3	Internal or External OCP VBUS Over Current Protection Fault	R	Not Supported
2	CC_UV_FAULT	R/W	<b>0: No fault detected (default)</b> 1: CC_UV fault happens (not latch)
1	VCON_OC	R/W	<b>0: No fault detected (default)</b> 1: Over-current VCONN fault latched Write 1 to clear this bit, then INT can be cleared by writing 1 to FAULT bit of Alert Reg.
0	I2C Interface Error	R/W	<b>0: No Error(default)</b> 1: I2C error has occurred some of the conditions for asserting this bit: 1. The TCPM writes to TRANSMIT requesting a transmission that is not Hard Reset, Cable reset or BIST Carrier Mode2 and there are less than 2 bytes in the TX_BUF_BYTE_x register; 2. I2C writing number is not consistent with recent I2C_WRITE_BYTE_COUNT. Write 1 to clear this bit, then INT can be cleared by writing 1 to

Bit	Bit Name	Type	Description
			FAULT bit of Alert Reg.

Table 20. COMMAND Register (Register 23h)

Bit	Bit Name	Type	Description
7-0	COMMAND	W	<p>1001 1001: <b>Look4Connection:</b> Start DRP Toggling if ROLE_CONTROL.DRP=1. If ROLE_CONTROL.CC1/CC2= 01 start with Rp, if ROLE_CONTROL.CC1/CC2 =10 start with Rd. If ROLE_CONTROL.CC1/CC2 are not both 01 or 10, then do not start toggling. The TCPM shall issue COMMAND.Look4Connection to enable the TCPC to restart Connection Detection in cases where the ROLE_CONTROL contents will not change.</p> <p>0010 0010: <b>DisableVbusDetect:</b> Disable Vbus present and vsafe0V detection.</p> <p>0011 0011: <b>EnableVbusDetect:</b> Enable Vbus present and vsafe0V detection.</p> <p>1101 1101: <b>ResetTransmitBuffer:</b> The TCPC resets the pointer of the TRANSMIT_BUFFER register to offset 1 and the contents of TRANSMIT_BUFFER becomes invalid when this command is issued by the TCPM.</p> <p>1110 1110: <b>ResetReceiveBuffer:</b> The TCPC resets the pointer of RX_BUFFER when this command is issued by the TCPM. Writing this command would reset the pointer to 1. TCPC does not clear the content of the buffer upon receiving this command. The TCPM issues this command in order to re-read the RECEIVE_BUFFER.RX_BUF_BYTE_x.</p>

Table 21. DEVICE\_CAPABILITIES\_1L Register (Register 24h)

Bit	Bit Name	Type	Description
7-5	ROLES_SUPPORT	R	<p>000: Type-C Port Manager can configure the Port as Source only or Sink only (not DRP) 001: Source only 010: Sink only 011: Sink with accessory support (optional) 100: DRP only 101: Source, Sink, DRP, Adapter/Cable all supported <b>110: Source, Sink, DRP (default)</b> 111: Not valid</p>
4	ALL_SOP_SUPPORT	R	<p>0: All SOP* except SOP*_DBG/SOP*_DBG <b>1: All SOP* messages are supported(default)</b></p>
3	SOURCE_VCONN	R	<p>0: TCPC is not capable of switching VCONN <b>1: TCPC is capable of switching VCONN (default)</b></p>
2	CPB_SINK_VBUS	R	<p><b>0: TCPC is not capable controlling the sink path to the system load(default)</b> 1: TCPC is capable of controlling the sink path to the system load</p>

Bit	Bit Name	Type	Description
1	SOURCE_HV_VBUS	R	<b>0: TCPC is not capable of controlling the source high voltage path to VBUS(default)</b> 1: TCPC is capable of controlling the source high voltage path to VBUS
0	SOURCE_VBUS	R	<b>0: TCPC is not capable of controlling the source path to VBUS (default)</b> 1: TCPC is capable of controlling the source path to VBUS

**Table 22. DEVICE\_CAPABILITIES\_1H Register (Register 25h)**

Bit	Bit Name	Type	Description
7	VBUS High Voltage Target	R	Not Supported
6	CPB_VBUS_OC	R	<b>0: VBUS OCP is not reported by the TCPC (default)</b> 1: VBUS OCP is reported by the TCPC
5	CPB_VBUS_OV	R	<b>0: VBUS OVP is not reported by the TCPC (default)</b> 1: VBUS OVP is reported by the TCPC
4	CPB_BLEED_DISC	R	<b>0: No Bleed Discharge implemented in TCPC (default)</b> 1: Bleed Discharge is implemented in the TCPC
3	CPB_FORCE_DISC	R	<b>0: No Force Discharge implemented in TCPC (default)</b> 1: Force Discharge is implemented in the TCPC
2	VBUS_MEASURE_ALARM	R	<b>0: No VBUS voltage measurement or VBUS Alarms (default)</b> 1: VBUS voltage measurement and VBUS Alarms
1-0	SOURCE_RP_SUPPORT	R	00: Rp default only 01: Rp 1.5A and default <b>10: Rp 3.0A, 1.5A, and default (default)</b> 11: Reserved Rp values which may be configured by the TCPM via the ROLE_CONTROL register

**Table 23. DEVICE\_CAPABILITIES\_2L Register (Register 26h)**

Bit	Bit Name	Type	Description
7	SINK_DISCONNECT_DET	R	<b>0: VBUS_SINK_DISCONNECT_THRESHOLD not implemented (default: Use POWER_STATUS.VbusPresent = 0 to indicate a Sink disconnect) (default)</b> 1: VBUS_SINK_DISCONNECT_THRESHOLD implemented
6	STOP_DISC_THD	R	<b>0: VBUS_STOP_DISCHARGE_THRESHOLD not implemented (default)</b> 1: VBUS_STOP_DISCHARGE_THRESHOLD implemented
5-4	VBUS_VOL_ALARM_LSB	R	00: TCPC has 25mV LSB for its voltage alarm and uses all 10 bits in VBUS_VOLTAGE_ALARM_HI_CFG and VBUS_VOLTAGE_ALARM_LO_CFG. 01: TCPC has 50mV LSB for its voltage alarm and uses only 9 bits. VBUS_VOLTAGE_ALARM_HI_CFG[0] and VBUS_VOLTAGE_ALARM_LO_CFG[0] are ignored by TCPC.

Bit	Bit Name	Type	Description
			10: TCPC has 100mV LSB for its voltage alarm and uses only 8 bits.VBUS_VOLTAGE_ALARM_HI_CFG[1:0] and VBUS_VOLTAGE_ALARM_LO_CFG[1:0] are ignored by TCPC. <b>11: Not support this function. (default)</b>
3-1	VCONN_POWER	R	000: 1.0W 001: 1.5W <b>010: 2.0W (default)</b> 011: 3W 100: 4W 101: 5W 110: 6W 111: External
0	VCONN_OCF	R	0: TCPC is not capable of detecting a VCONN fault <b>1: TCPC is capable of detecting a VCONN fault (default)</b>

**Table 24. DEVICE\_CAPABILITIES\_2H Register (Register 27h)**

Bit	Bit Name	Type	Description
7-0	Reserved	R	Reserved

**Table 25. STANDARD\_INPUT\_CAPABILITIES Register (Register 28h)**

Bit	Bit Name	Type	Description
7-5	Reserved	R	Reserved
4-3	Source Fast Role Swap	R	Not Supported
2	VBUS_EXT_OVF	R	<b>0: Not present in TCPC (default)</b> 1: Present in TCPC
1	VBUS_EXT_OCF	R	<b>0: Not present in TCPC (default)</b> 1: Present in TCPC
0	FORCE_OFF_VBUS_IN	R	<b>0: Not present in TCPC (default)</b> 1: Present in TCPC

**Table 26. STANDARD\_OUTPUT\_CAPABILITIES Register (Register 29h)**

Bit	Bit Name	Type	Description
7	VBUS Sink Disconnect Detect Indicator	R	<b>0: Not present in TCPC (default)</b> 1: Present in TCPC
6	CPB_DBG_ACC_IND	R	<b>0: Not present in TCPC (default)</b> 1: Present in TCPC
5	CPB_VBUS_PRESEN T_MNT	R	<b>0: Not present in TCPC (default)</b> 1: Present in TCPC
4	CPB_AUDIO_ADT_ACC_IND	R	<b>0: Not present in TCPC (default)</b> 1: Present in TCPC
3	CPB_ACTIVE_CABLE_IND	R	<b>0: Not present in TCPC (default)</b> 1: Present in TCPC

2	CPB_MUX_CFG_CTRL	R	<b>0: Not present in TCPC (default)</b> 1: Present in TCPC
1	CPB_CONNECT_PRESENT	R	<b>0: Not present in TCPC (default)</b> 1: Present in TCPC
0	CPB_CONNECT_ORIENT	R	<b>0: Not present in TCPC (default)</b> 1: Present in TCPC

**Table 27. MESSAGE\_HEADER\_INFO Register (Register 2Eh)**

Bit	Bit Name	Type	Description
7-5	Reserved	R	Reserved
4	Cable Plug	R/W	<b>0: Message originated from Source, Sink, or DRP (default)</b> 1: Message originated from a Cable Plug
3	Data Role	R/W	<b>0: UFP (default)</b> 1: DFP
2-1	USB PD Specification Revision	R/W	00: Revision 1.0 <b>01: Revision 2.0(default)</b> 10: Revision 3.0 11: Reserved
0	Power Role	R/W	<b>0: Sink (default)</b> 1: Source

**Table 28. RECEIVE\_DETECT Register (Register 2Fh)**

Bit	Bit Name	Type	Description
7	Reserved	R	Reserved
6	Enable Cable Reset	R/W	<b>0: TCPC does not detect Cable Reset signaling (default)</b> 1: TCPC detects Cable Reset signaling
5	Enable Hard Reset	R/W	<b>0: TCPC does not detect Hard Reset signaling (default)</b> 1: TCPC detects Hard Reset signaling
4	Enable SOP_DBG'' message	R/W	<b>0: TCPC does not detect SOP_DBG'' message (default)</b> 1: TCPC detects SOP_DBG'' message
3	Enable SOP_DBG' message	R/W	<b>0: TCPC does not detect SOP_DBG' message (default)</b> 1: TCPC detects SOP_DBG' message
2	Enable SOP'' message	R/W	<b>0: TCPC does not detect SOP'' message (default)</b> 1: TCPC detects SOP'' message
1	Enable SOP' message	R/W	<b>0: TCPC does not detect SOP' message (default)</b> 1: TCPC detects SOP' message
0	Enable SOP message	R/W	<b>0: TCPC does not detect SOP message (default)</b> 1: TCPC detects SOP message

**Table 29. READABLE\_BYTE\_COUNT Register (Register 30h)**

Bit	Bit Name	Type	Description
7-0	READABLE_BYTE_COUNT	R	Indicates the number of bytes in the RX_BUF_BYTE_x registers plus one (for the RX_BUF_FRAME_TYPE). The content of this register is undefined when the

			RECEIVE_BUFFER is cleared. The value in this register shall be less than or equal to 31.
--	--	--	---

**Table 30. RX\_BUF\_FRAME\_TYPE Register (Register 30h)**

Bit	Bit Name	Type	Description
7-3	Reserved	R	Reserved
2-0	Received SOP* Message	R	<b>000: Received SOP (default)</b> 001: Received SOP' 010: Received SOP'' 011: Received SOP_DBG' 100: Received SOP_DBG'' 110: Received Cable Reset All others are reserved.

**Table 31. RX\_BUF\_BYTE\_x Register (Register 30h)**

Bit	Bit Name	Type	Description
7-0	RX_BUFFER	R	Receive Buffer Bytes. These registers are “hidden” and can only be accessed by reading at address 30h.

**Table 32. TRANSMIT Register (Register 50h)**

Bit	Bit Name	Type	Description
7-6	Reserved	R	Reserved
5-4	Retry Counter	R/W	<b>00: No message retry is required (default)</b> 01: Automatically retry message transmission once 10: Automatically retry message transmission twice 11: Automatically retry message transmission three times
3	Reserved	R	Reserved
2-0	Transmit SOP* message	R/W	<b>000: Transmit SOP (default)</b> 001: Transmit SOP' 010: Transmit SOP'' 011: Transmit SOP_DBG' 100: Transmit SOP_DBG'' 101: Transmit Hard Reset 110: Transmit Cable Reset 111: Transmit BIST Carrier Mode 2 (TCPC shall exit the BIST mode no later than tBISTContMode max)

**Table 33. I2C\_WRITE\_BYTE\_COUNT Register (Register 51h)**

Bit	Bit Name	Type	Description
7-0	I2C_WRITE_BYTE_COUNT	W	The number of bytes the TCPM intends to write to the TX_BUF_BYTE_x in the given I <sup>2</sup> C transaction. The TCPM shall write as many bytes in the buffer as defined in this register in one I <sup>2</sup> C write transaction. The TCPC shall ignore the I <sup>2</sup> C transaction if I2C_WRITE_BYTE_COUNT is more than 30.

**Table 34. TX\_BUF\_BYTE\_x Register (Register 51h)**

Bit	Bit Name	Type	Description
7-0	TX_BUFFER	W	Transmit Buffer Bytes. These registers are “hidden” and can only be accessed by writing to address 51h.

**Table 35. VENDER\_POWER Register (Register 90h)**

Bit	Bit Name	Type	Description
7-6	Reserved	R	Reserved
5	VCONN_DISCHARGE_EN	R/W	VCONN OVP occurs and discharge path turn-on <b>0: No discharge (default)</b> 1: Discharge
4	LPR_RP_EN	R/W	Low power mode RP enable control bit <b>0: Low power mode RP disable (RD) (default)</b> 1: Low power mode RP Enable
3	LPR_EN	R/W	Low power mode enable <b>0: Active mode (default)</b> 1: Low power mode
2	BG_EN	R/W	BandGap enable control bit <b>0: BandGap off CC pin function disable (default)</b> 1: BandGap on; CC pin function enable
1	VBUS_DETEN	R/W	VBUS detection enable control bit 0: Measure off <b>1: Operation (default)</b>
0	OSC_24M_EN	R/W	24M oscillator for BMC communication 0: Disable 24M oscillator <b>1: Enable 24M oscillator (default)</b> 24M oscillator will be enabled automatically when INT occur.

**Table 36. VCONN\_OC Register (Register 93h)**

Bit	Bit Name	Type	Description
7-5	BMCIO_VCONOCP	R/W	VCONN over-current control selection 000: Current level = 200mA 001: Current level = 300mA 010: Current level = 400mA 011: Current level = 500mA <b>100: Current level = 600mA(default)</b> 101 to 111: Reserved If VCONN OCP trigger, the switch turns off timing under 55µs.
4	OCP_FAST_SPEED	R/W	<b>0: Fast (default)</b> 1: Slow
3	OCP_FAST_DISABLE	R/W	<b>0: OCP_Fast protection Enable (default)</b> 1: OCP_Fast protection Disable
2	SHORT_SPEED	R/W	<b>0: Fast (default)</b> 1: Slow
1	SHORT_DISABLE	R/W	<b>0: CC short protection Enable (default)</b> 1: CC short protection Disable

0	OVP_FAST_SPEED	R/W	<b>0: Fast (default)</b> 1: Slow
---	----------------	-----	-------------------------------------

**Table 37. VENDER\_STATUS Register (Register 97h)**

Bit	Bit Name	Type	Description
7-2	Reserved	R	Reserved
1	VBUS_80	R	<b>0: VBUS is over 0.8V</b> <b>1: VBUS is under 0.8V (default)</b>
0	Reserved	R	Reserved

**Table 38. VENDER\_INT Register (Register 98h)**

Bit	Bit Name	Type	Description
7-6	Reserved	R	Reserved
5	INT_RA_DETACH	R/W	<b>0: Cleared (default)</b> 1: Ra detach Write 1 to clear.
4-2	Reserved	R	Reserved
1	INT_VBUS_80	R/W	<b>0: Cleared (default)</b> 1: VBUS decrease under 0.8V happened Write 1 to clear.
0	INT_WAKEUP	R/W	<b>0: Cleared (default)</b> 1: Low power mode exited Write 1 to clear.

**Table 39. VENDER\_MASK Register (Register 99h)**

Bit	Bit Name	Type	Description
7-6	Reserved	R	Reserved
5	M_RA_DETACH	R/W	<b>0: Interrupt masked (default)</b> 1: Interrupt unmasked
4-2	Reserved	R	Reserved
1	M_VBUS_80	R/W	<b>0: Interrupt masked (default)</b> 1: Interrupt unmasked
0	M_WAKEUP	R/W	<b>0: Interrupt masked (default)</b> 1: Interrupt unmasked

**Table 40. VENDER\_CONTROL1 Register (Register 9Bh)**

Bit	Bit Name	Type	Description
7-6	Reserved	R	Reserved
5	SHIPPING_QUIT	R/W	<b>0: chip is in shipping mode(default)</b> 1: chip quits shipping mode
4	ENEXTMSG	R/W	<b>0: Disable Extended Bit Check when receiving GoodCRC (default)</b> 1: Enable Extended Bit Check when receiving GoodCRC

3	AUTOIDLE_EN	R/W	0: Auto enter idle mode disable <b>1: Auto enter idle mode enable (default)</b>
2-0	AUTOIDLE_TIMEOUT	R/W	Enter idle mode timeout time =(AUTOIDLE_TIMEOUT*2+1)*6.4ms Shortest time:6.4ms Longest time:15*6.4ms=96ms <b>000:6.4ms (default)</b>

**Table 41. VENDER\_CONTROL2 Register (Register 9Fh)**

Bit	Bit Name	Type	Description
7	WAKEUP_EN	R/W	0: Wakeup function disable <b>1: Wakeup function enable (default)</b>
6-1	Reserved	R	Reserved
0	I2C_ANTI_LOCK_EN	R/W	I2C anti-lock function control bit. If I2C anti-lock function is enabled, release SDA when SDA is pulled down above 20ms. 0: Disable I2C anti-lock function <b>1: Enable I2C anti-lock function(default)</b>

**Table 42. VENDER\_CONTROL3 Register (Register A0h)**

Bit	Bit Name	Type	Description
7-1	Reserved	R	Reserved
0	SOFT_RESET	R/W	Write 1 to trigger software reset

**Table 43. TDRP Register (Register A2h)**

Bit	Bit Name	Type	Description
7-4	Reserved	R	Reserved
3-0	TDRP	R/W	The period a DRP will complete a Source to Sink and back advertisement. (Period = TDRP * 6.4+ 51.2ms) 0000:51.2ms 0001:57.6ms 0010:64ms <b>0011:70.4ms (default)</b> ... 1110:140.8ms 1111:147.2ms

**Table 44. DCSRCDRP\_H Register (Register A3h)**

Bit	Bit Name	Type	Description
7-0	DCSRCDRP[7:0]	R/W	The percent of time that a DRP will advertise Source during tDRP. (DUTY = (DCSRCDRP[9:0] + 1) /1024) 0000000000 : 1/1024 0000000001 : 2/1024 ... <b>0101000111 : 328/1024 (default)</b> ... 1111111110 : 1023/1024 1111111111 : 1024/1024

			Note : Setting with 0xA4[9:8]
--	--	--	-------------------------------

**Table 45. DCSRCDRP\_L Register (Register A4h)**

Bit	Bit Name	Type	Description
7-2	Reserved	R	Reserved
1-0	DCSRCDRP[9:8]	R/W	<p>The percent of time that a DRP will advertise Source during tDRP. (DUTY = (DCSRCDRP[9:0] + 1) / 1024)</p> <p>000000000: 1/1024</p> <p>000000001: 2/1024</p> <p>...</p> <p><b>0101000111: 328/1024 (default)</b></p> <p>...</p> <p>111111110: 1023/1024</p> <p>111111111: 1024/1024</p> <p>Note: Setting with 0xA4[9:8]</p>

## 8.8 I<sup>2</sup>C Interface

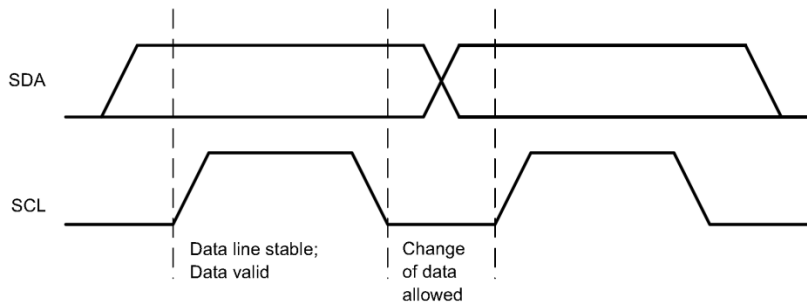
The SY20794 uses I<sup>2</sup>C compatible interface for flexible charging parameter programming and instantaneous device status reporting. Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address 4EH in 7-bit address format, receiving control inputs from the master device like micro controller or a digital signal processor.

Both SDA and SCL are bi-directional lines, connecting to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain.

### 8.8.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

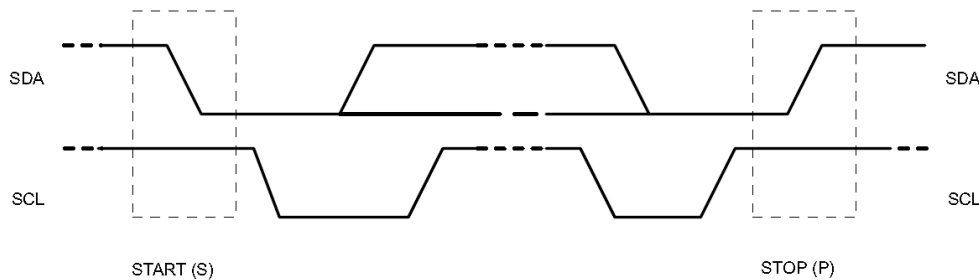


**Figure 6. Bit Transfer on the I2C Bus**

### 8.8.2 START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

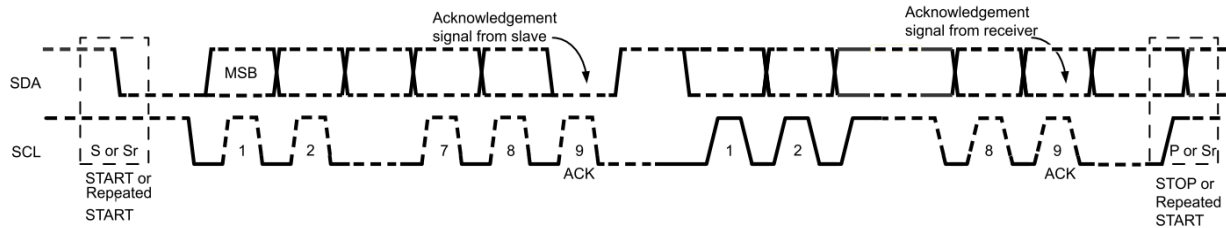


**Figure 7. START and STOP conditions**

### 8.8.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can

hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.



**Figure 8. Data Transfer on the I2C Bus**

**8.8.4 Acknowledge (ACK) and Not Acknowledge (NACK)**

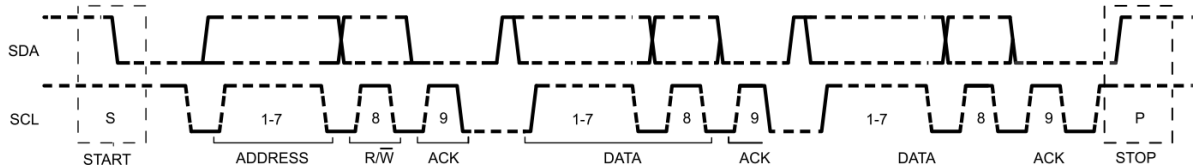
The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the 9th clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

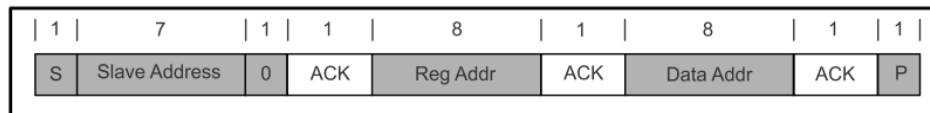
**8.8.5 Slave Address and Data Direction Bit**

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

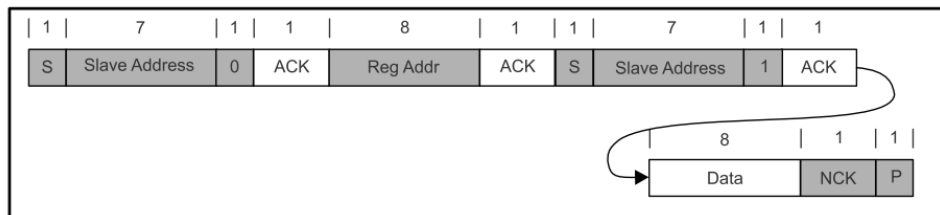


**Figure 9. Complete Data Transfer**

**8.8.6 Single Read and Write**



**Figure 10. Single Write**

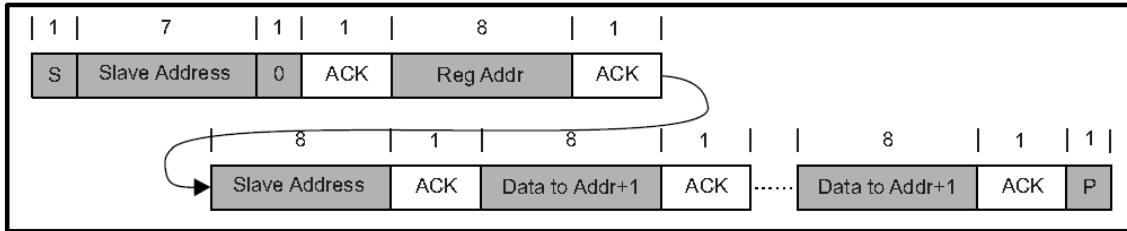


**Figure 11. Single Read**

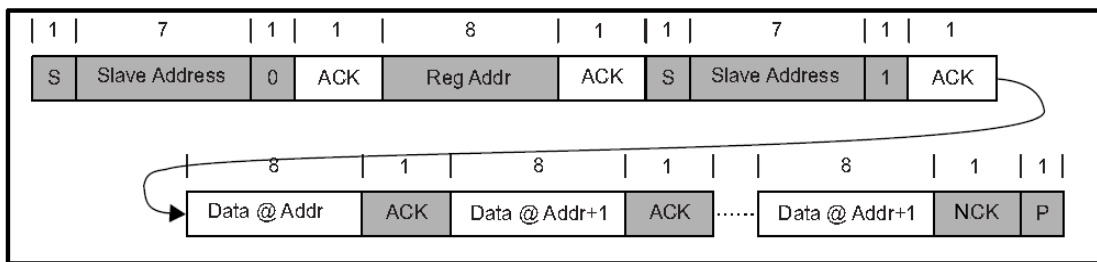
If the register address is not defined, the charger IC send back NACK and go back to the idle state.

**8.8.7 Multi-Read and Multi-Write**

The charger device supports multi-read and multi-write.



**Figure 12. Multi-Write**



**Figure 13. Multi-Read**

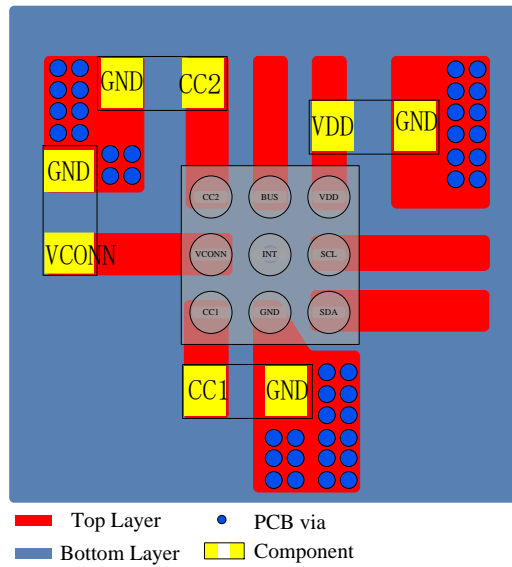
## 9 Applications Information

The I2C of SY20794 supports up to 3.4MHz at either 1.8V or 3.3V signal levels. The pull-up resistance in SDA and SCL should be chosen carefully to cooperate with the maximum I2C frequency and the I2C bus capacitance.

The layout design of the SY20794 regulator is relatively simple. For the best efficiency and minimum noise problems, the decoupling capacitor  $C_{VDD}$  should be placed as close as possible to the VDD pin of SY20794.

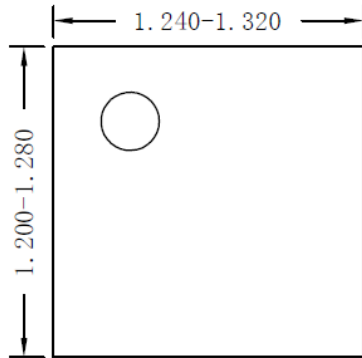
Trace width and thickness size of CC1, CC2, and VCONN should be designed based on maximum current limit.

Figure 14 is the recommended layout design.

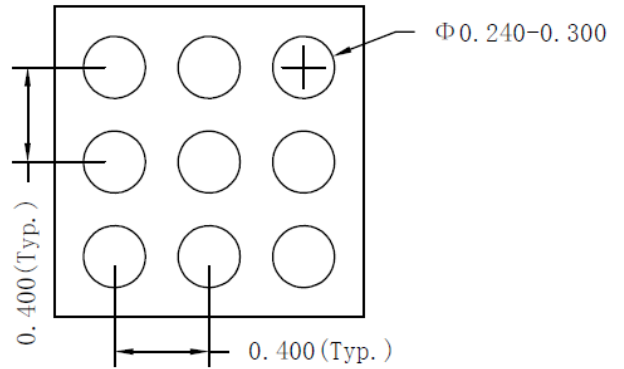


**Figure 14. PCB Layout**

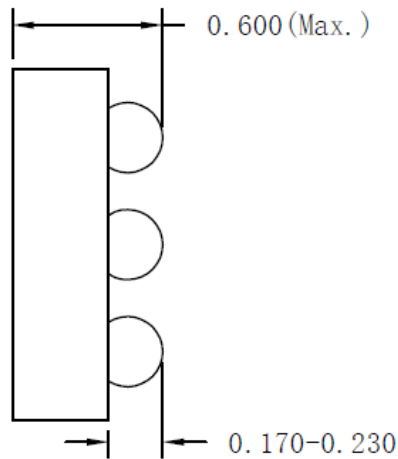
**CSP1.29×1.25-9 Package Outline Drawing**



**Top view**



**Bottom view**



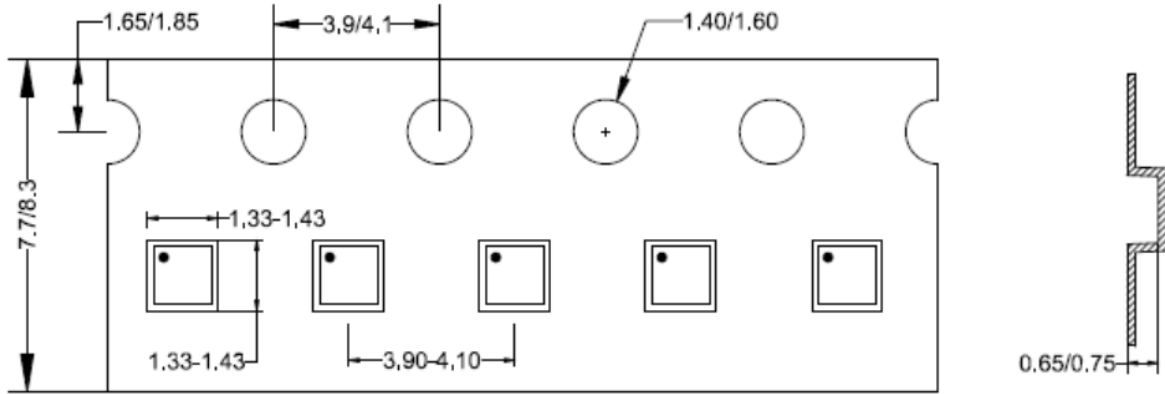
**Side view**

**Notes: 1, All dimension in millimeter and exclude mold flash & metal burr;**

## Taping & Reel Specification

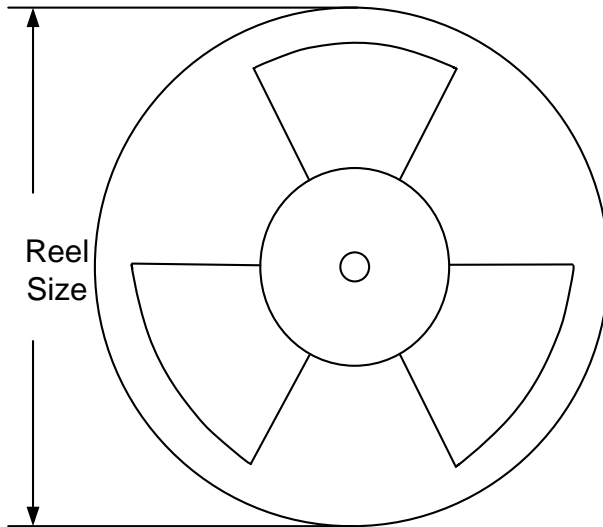
### 1. Taping Orientation

CSP1.29×1.25



**Feeding Direction** →

### 2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
CSP1.29×1.25	8	4	7"	400	160	3000

**IMPORTANT NOTICE**

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.
2. **Applications.** Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.
3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.
4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.
5. **Terms and conditions of commercial sale.** Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at <http://www.silergy.com/stdterms>, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.
6. **No offer to sell or license.** Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: [www.silergy.com](http://www.silergy.com)

© 2022 Silergy Corp.

**All Rights Reserved.**