SY21215

High Efficiency Fast Response
6A Continuous, 12A Peak, 28V Input
Synchronous Step Down Regulator

General Description

The SY21215 develops a high efficiency synchronous step-down DC-DC regulator capable of delivering 6A continuous, 12A peak current. The SY21215 operates over a wide input voltage range from 4V to 28V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The SY21215 adopts the instant PWM architecture to achieve fast transient responses for high step down applications and high efficiency at light loads. In addition, it operates at pseudo-constant frequency of 800kHz under continuous conduction mode to minimize the size of inductor and capacitor.

Ordering Information

SY21215 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY21215QNC	QFN3x3-10	--

Features

- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 40/20 mΩ
- Wide Input Voltage Range: 4-28V
- Instant PWM Architecture to Achieve Fast Transient Responses
- Internal 400μs Soft-start Limits the Inrush Current
- Pseudo-constant Frequency: 800kHz
- 6A Continuous/12A Peak Output Current Capability
- ±1.5% 0.6V Reference
- Programmable Peak Current Limit
- Power Good Indicator
- Output Discharge Function
- Short Circuit Latch Off Protection
- Over Voltage Latch Off Protection
- Input UVLO
- Over Temperature Protection
- RoHS Compliant and Halogen Free
- Compact Package: QFN3x3-10

Applications

- LCD-TV/Net-TV/3DTV
- Set Top Box
- Notebook
- High Power AP

Typical Applications

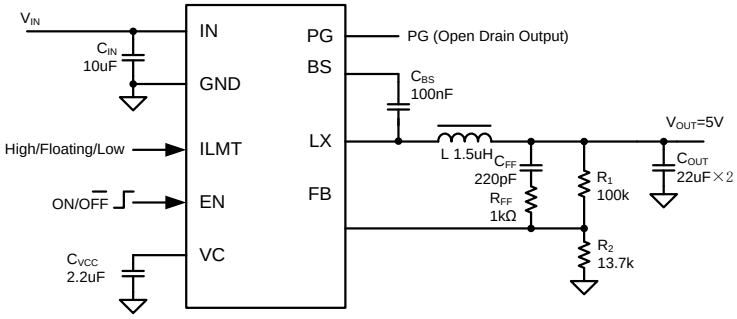

Figure 1 Schematic

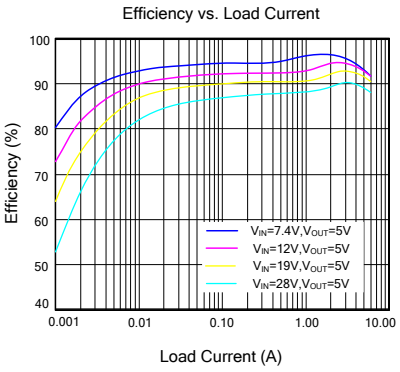

Figure 2. Efficiency

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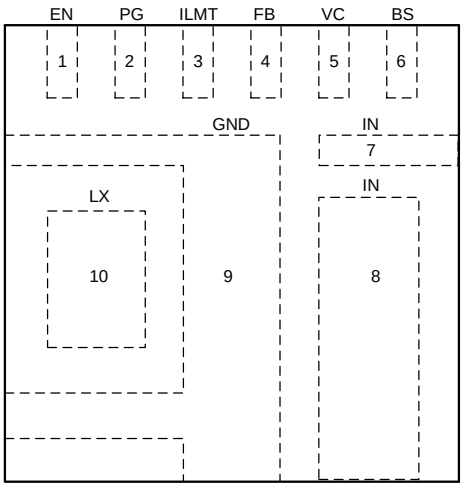
Pinout (top view)



(QFN3x3-10)

Top Mark: YV*xyz* (Device code: YV, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
EN	1	Enable control. Pull this pin high to turn on the IC. Do not leave this pin floating.
PG	2	Power good Indicator. Open drain output when the output voltage is within 90% to 120% of regulation point.
ILMT	3	Current limit setting pin. The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high respectively.
FB	4	Output Feedback Pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.6\times(1+R_1/R_2)$
VC	5	Internal 3.3V LDO output. Power supply for internal analog circuits and driving circuit. Bypass a capacitor to GND.
BS	6	Boot-strap pin. Supply high side gate driver. Decouple this pin to the LX pin with a 0.1μF ceramic cap.
IN	7,8	Input pin. Decouple this pin to the GND pin with at least a 10μF ceramic cap.
GND	9	Ground pin.
LX	10	Inductor pin. Connect this pin to the switching node of inductor.

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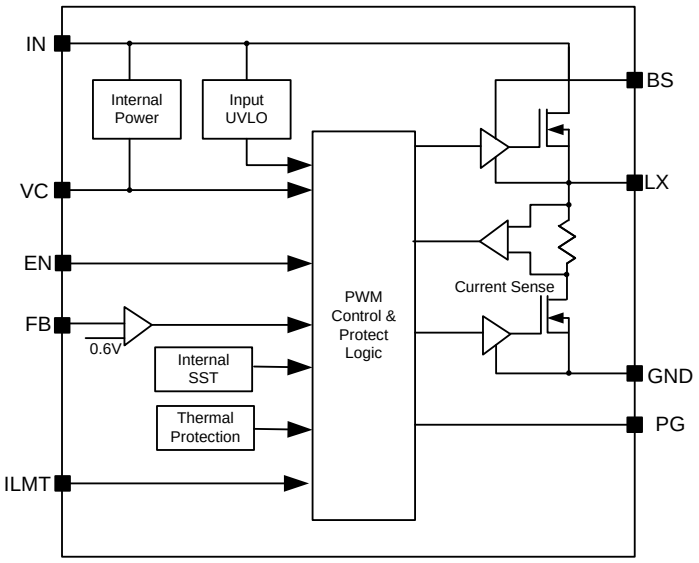
Block Diagram



Absolute Maximum Ratings (Note 1)

IN, LX, PG, EN ---------- -0.3V to 30V
BS-LX, FB, ILMT, VCC ---------- -0.3V to 4V
Power Dissipation, PD @ T_A = 25°C QFN3x3-10 ----------3.3W
Package Thermal Resistance (Note 2)
θ_{JA} ----------30°C/W
θ_{JC} ---------- 4°C/W
Junction Temperature Range ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
Dynamic LX voltage in 10ns Duration ---------- IN+3V to GND-5V

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 4V to 28V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

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Electrical Characteristics

(V_{IN} = 12V, V_{OUT} =5V, C_{OUT} = 100µF, T_A = 25°C, I_{OUT} = 2A unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.0		28	V
Quiescent Current	I_Q	I_{OUT}=0, V_{FB}=V_{REF}×105%		100		µA
Shutdown Current	I_{SHDN}	EN=0		3	10	µA
Feedback Reference Voltage	V_{REF}		0.591	0.6	0.609	V
FB Input Current	I_{FB}	V_{FB}=4V	-50		50	nA
Top FET RON	$R_{DS(ON)1}$			40		mΩ
Bottom FET RON	$R_{DS(ON)2}$			20		mΩ
Discharge Current	I_{DIS}			100		mA
Bottom FET Current Limit	I_{LIM}	I_{LMT}='0'	6		9	A
		I_{LMT}=Floating	9		12	
		I_{LMT}='1'	12		15	
ILMT Rising Threshold	V_{ILMTH}		Vcc-0.8		V_{CC}	V
ILMT Falling Threshold	V_{ILMTL}				0.8	V
ILMT Floating Threshold	V_{ILMIF}		1.3		2	V
Soft Start Time	T_{SS}			400		µs
EN Rising Threshold	V_{ENH}		0.8			V
EN Falling Threshold	V_{ENL}				0.4	V
EN Leakage Current	I_{EN}		-1		1	µA
Input UVLO Threshold	V_{UVLO}				3.9	V
UVLO Hysteresis	V_{HYS}			0.3		V
Oscillator Frequency	F_{OSC}	Vo=5V	0.68	0.8	0.92	MHz
Min ON Time	$t_{ON,MIN}$	V_{IN}=V_{INMAX}		50		ns
Min OFF Time	$t_{OFF,MIN}$			120		ns
VCC Output	V_{CC}	V_{IN}=4V	3.2	3.3	3.4	V
Output Over Voltage Threshold		V_{FB} Rising	115	120	125	%V_{REF}
Output Over Voltage Hysteresis				2		%V_{REF}
Output Over Voltage Delay Time				20		µs
Power Good Threshold		V_{FB} Rising	88	90	92	%V_{REF}
Power Good Hysteresis				2		%V_{REF}
Power Good Delay Time				10		µs
Maximum Duty Cycle	D_{MAX}			80		%
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown hysteresis	T_{HYS}			15		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Note 2: θJA is measured in the natural convection at T_A = 25°C on a four-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

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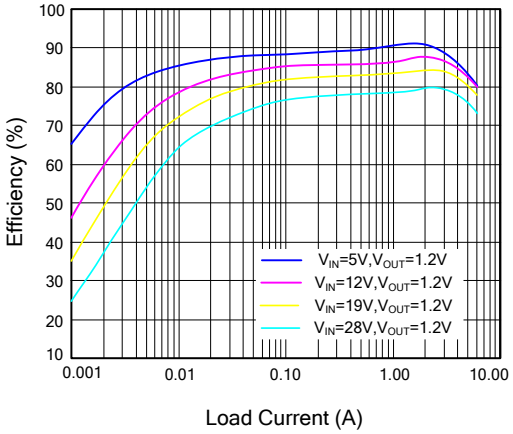
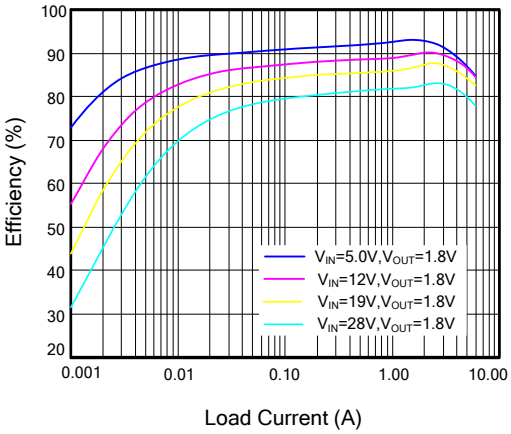
Typical Performance Characteristics

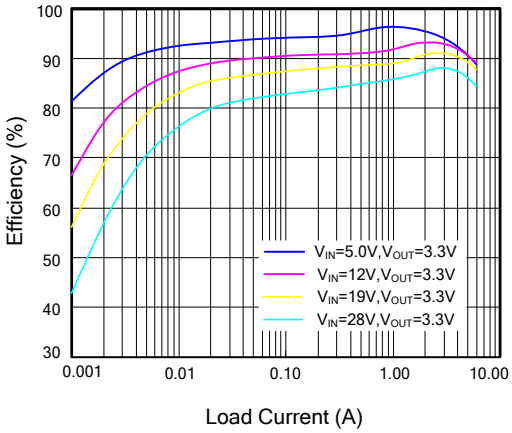
Efficiency vs. Load Current



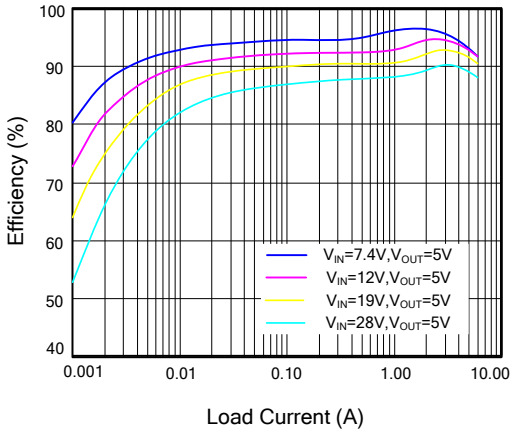
Efficiency vs. Load Current



Efficiency vs. Load Current

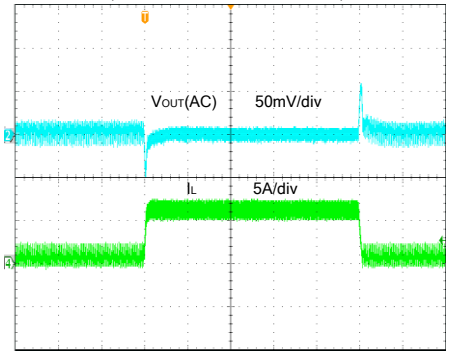


Efficiency vs. Load Current



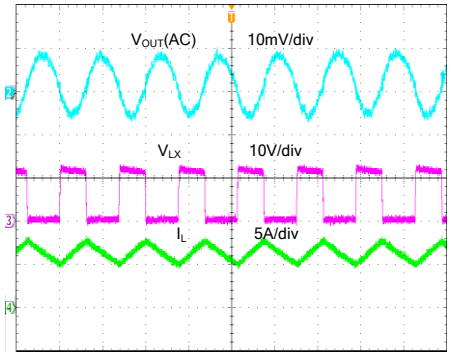
Load Transient

(V_{IN}=12V, V_{OUT}=5V, I_{LOAD}=0.6-6A)



Output Ripple

(V_{IN}=12V, V_{OUT}=5V, I_{LOAD}=6A)



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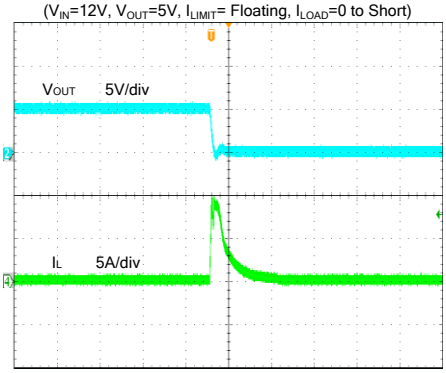
Short Circuit Protection

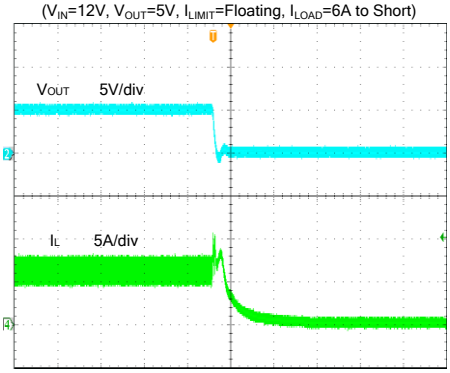
(V_{IN}=12V, V_{OUT}=5V, I_{LIMIT}= Floating, I_{LOAD}=0 to Short)



Time (100μs/div)

Short Circuit Protection

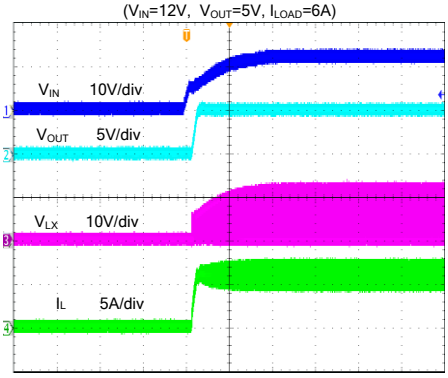
(V_{IN}=12V, V_{OUT}=5V, I_{LIMIT}=Floating, I_{LOAD}=6A to Short)



Time (100μs/div)

Startup from VIN

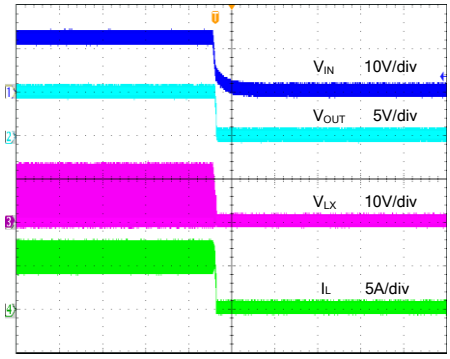
(V_{IN}=12V, V_{OUT}=5V, I_{LOAD}=6A)



Time (2ms/div)

Shutdown from VIN

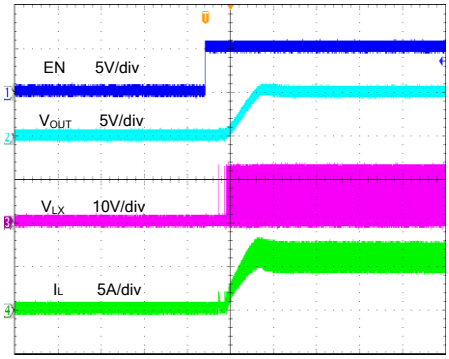
(V_{IN}=12V, V_{OUT}=5V, I_{LOAD}=6A)



Time (10ms/div)

Startup from Enable

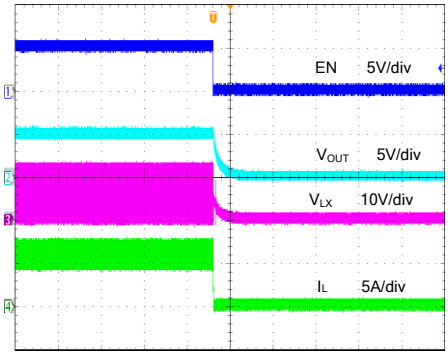
(V_{IN}=12V, V_{OUT}=5V, I_{LOAD}=6A)



Time (400μs/div)

Shutdown from Enable

(V_{IN}=12V, V_{OUT}=5V, I_{LOAD}=6A)



Time (400μs/div)

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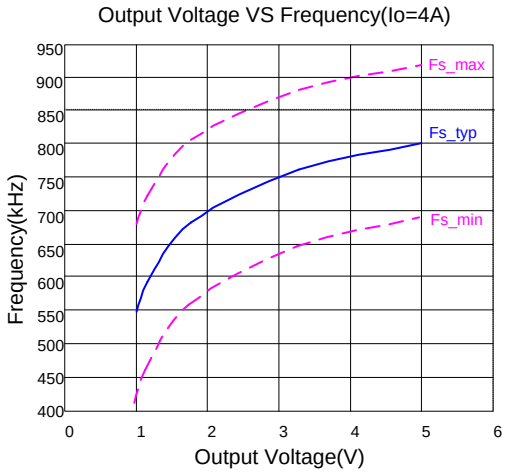

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Operation

The SY21215 develops a high efficiency synchronous step-down DC-DC regulator capable of delivering 6A continuous, 12A peak current. The SY21215 operates over a wide input voltage range from 4V to 28V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The SY21215 adopts the instant PWM architecture to achieve fast transient responses for high step down applications and high efficiency at light loads. In addition, it operates at pseudo-constant frequency of 800kHz under continuous conduction mode to minimize the size of inductor and capacitor.

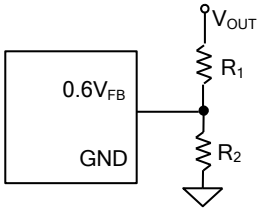
Applications Information

Because of the high integration in the SY21215, the application circuit based on this IC is rather simple. Only the input capacitor C_{IN}, the output capacitor C_{OUT}, the output inductor L and the feedback resistors (R_1 and R_2) need to be selected for the targeted applications specifications.

Feedback Resistor Dividers R_1 and R_2:

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10kΩ and 1MΩ is highly recommended for both resistors. If V_{OUT} is 3.3V, R_1=100k is chosen, then using following equation, R_2 can be calculated to be 22.1k:

$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} R_1 .$$



Input Capacitor C_{IN}:

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \cdot \sqrt{D(1-D)} \cdot$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins. In this case, a 10μF low ESR ceramic capacitor is recommended.

Output Capacitor C_{OUT}:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For most applications, an X5R or better grade ceramic capacitor greater than 66uF capacitance can work well. The capacitance derating with DC voltage must be considered.

Output Inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

where Fsw is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY21215 is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,\,MIN} > I_{OUT,\,MAX} + \frac{V_{OUT}(1\text{-}V_{OUT}/V_{IN,MAX})}{2 \cdot F_{SW} \cdot L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<10mΩ to achieve a good overall efficiency.

Current Limit Setting

The current limit is set to 6A, 9A or 12A when the ILMT pin is pull low, floating or pull high respectively.

Soft-start

The SY21215 has a built-in soft-start to control the rise rate of the output voltage and limit the input current surge during the IC start-up. The typical soft-start time is 400μs.

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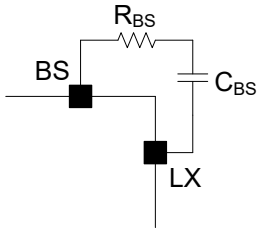
Enable Operation

Pulling the EN pin low (<0.4V) will shut down the device. During shutdown mode, the SY21215 shutdown current drops to lower than 10μA, driving the EN pin high (>0.8V) will turn on the IC again.

External Bootstrap Capacitor Connection (BS)

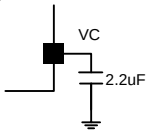
This device integrates a floating power supply for the gate driver that operates the high-side power switch. Proper operation requires a 100nF ceramic capacitor to be connected between BS and LX. This bootstrap capacitor provides the gate driver supply voltage for the high-side N-channel power MOSFET switch.

The high-side gate driver is optimized to achieve both better fast switching speed and low EMI. To further reduce the EMI of the converter, a proper resistor in series with bootstrap can be used. By doing this, the rising edge of LX node becomes slower and thus reduces the EMI, but the switching loss will become higher.



VCC LDO

The 3.3V VCC LDO provides the power supply for internal control circuit. Bypass this pin to ground with a 2.2uf ceramic capacitor.

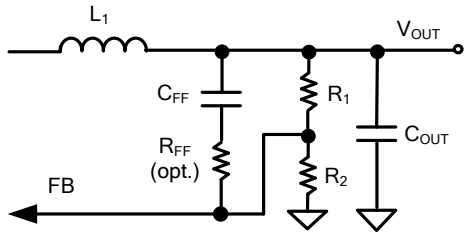


Power Good Indication

PG is an open drain output. This pin is externally pulled high when the FB voltage is within 90% to 120% of the internal reference voltage. Otherwise, is pulled low.

Load Transient Considerations:

The SY21215 adopts the instant PWM architecture to achieve good stability and fast transient responses. In applications with high step load current, adding an RC network R_{FF} and C_{FF} parallel with R1 may further speed up the load transient responses.



Layout Design:

The layout design of SY21215 regulator is relatively simple. For the best efficiency and minimum noise problem, we should place the following components close to the IC: C_{IN}, C_{VCC}, L, R_1 and R_2.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) C_{IN} must be close to pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

4) The components R_1, R_2, and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1Mohm resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

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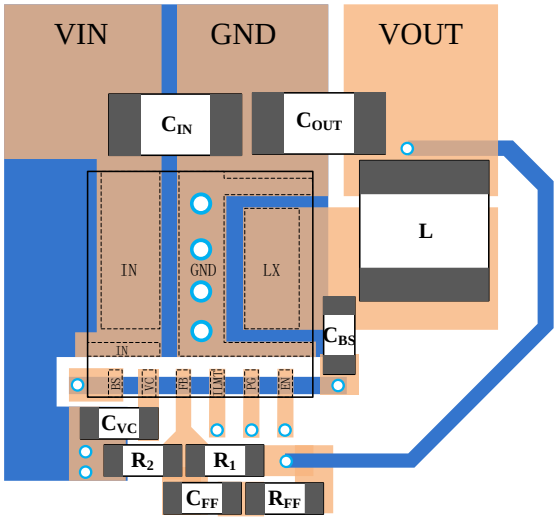

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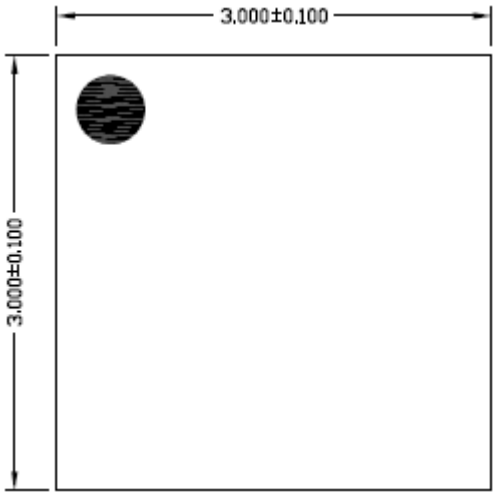
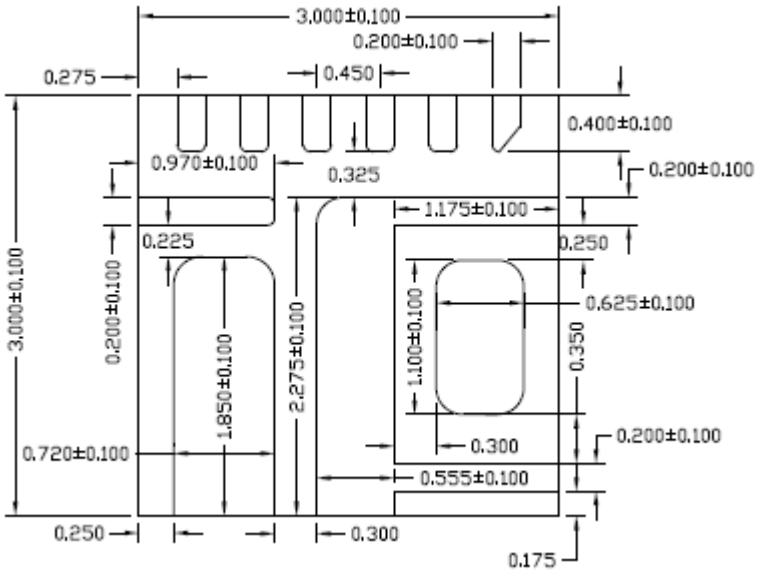
QFN3x3-10 Package Outline Drawing

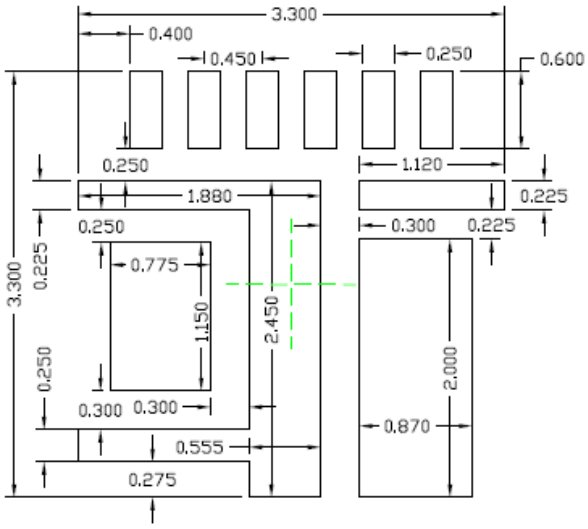


Top View



Bottom View

Side View



Recommended PCB Layout (Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr**

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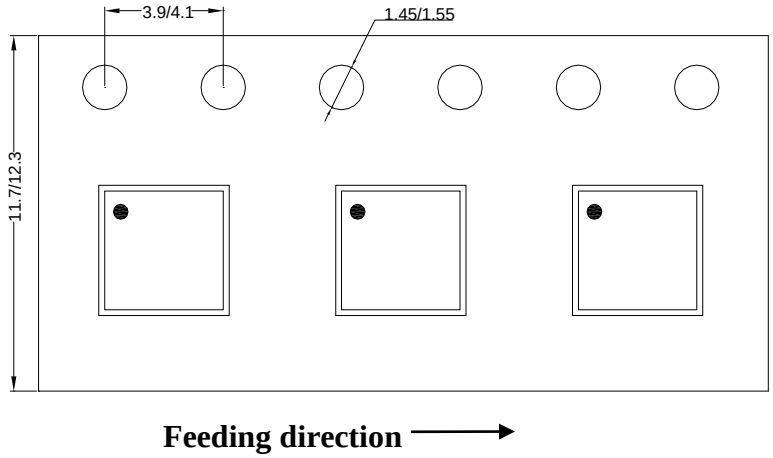
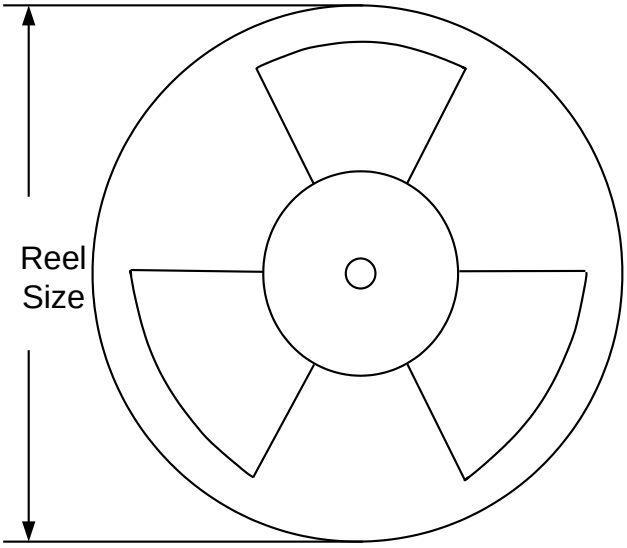
Taping & Reel Specification

1. QFN3x3-10 taping orientation



2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3x3	12	8	13"	400	400	5000

3. Others: NA

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