SY23565

Pseudo Fixed Frequency SSR Flyback Regulator
for High Input Voltage Application

General Description

SY23565 is a pseudo fixed frequency SSR Flyback regulator targeting at high input voltage applications. It integrates a 1200V MOSFET to process power up to 8W within DIP-7 package. SY23565's switching frequency is around 30 kHz. As load decreases, SY23565 will enter burst mode to achieve high efficiency under light load condition. SY23565 has frequency modulation function to facilitate EMI design. In addition, SY23565 integrates fast internal HV start-up circuit to minimize no-load loss and external components.

SY23565 provides comprehensive protections including OLP, VCC OVP, internal OTP, etc.

Ordering Information

SY23565□(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY23565FIC	DIP7	----

Features

- Integrated 1200V MOSFET
- 30kHz Pseudo Fixed Frequency
- Secondary Side Regulation
- Internal HV Start up
- Frequency Modulation to Facilitate EMI Design
- Burst Mode Control for Low No Load Power Consumption
- Reliable Protections for OLP, VCC OVP , OTP
- Compact Package: DIP7

Applications

- Power Supply for STB Home Appliances, Smart Power Meter and Other Appliances with High AC Input Voltage

Recommended operating output power	
Products	85-570Vac
SY23565FIC	12W

Typical Applications

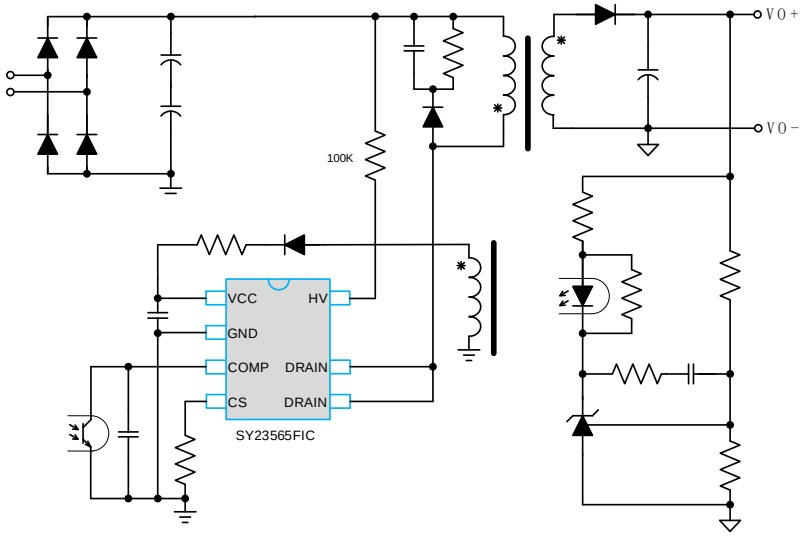
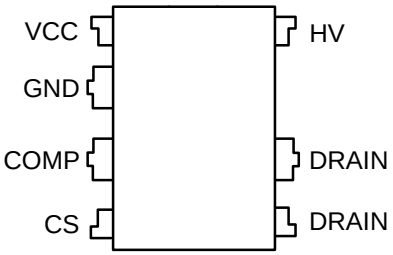


Fig.1 Typical Application Circuit

Pinout (top view)

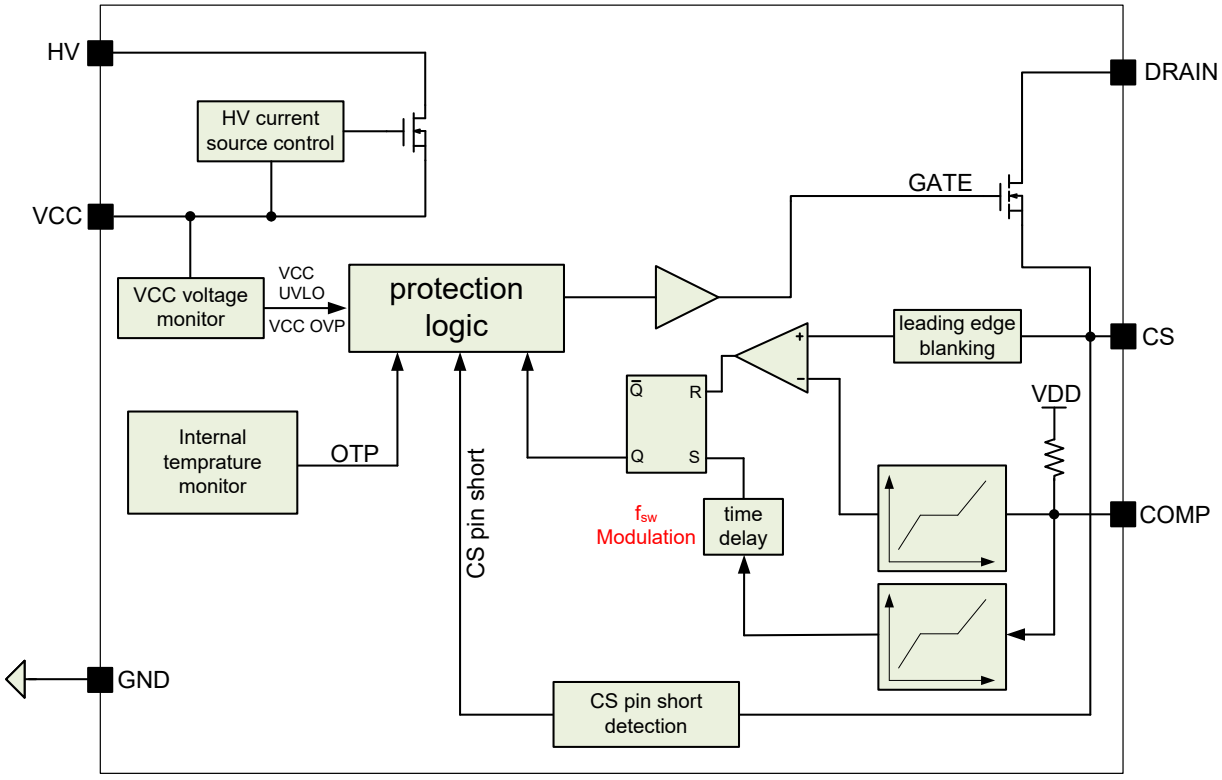


(DIP7)

Top Mark: CMF*xyz*(device code: CMF, ***x=year code, y=week code, z= lot number code***)

Pin	Name	Description
1	VCC	Power supply pin.
2	GND	Ground pin.
3	COMP	Output feedback pin. Directly Connect it to a opto-coupler
4	CS	Current sense pin. Connect this pin to the current sense resistor.
5~6	DRAIN	Drain of the internal power MOSFET.
7	HV	HV start up pin.

Block Diagram



Absolute Maximum Ratings (Note 1)

HV ---------- -0.3V~950V
VCC ---------- -0.3V~25V
COMP ---------- -0.3V~3.6V
CS ---------- -0.3V~3.6V
DRAIN ----------1200V
Power Dissipation, @ TA = 25°C DIP7 ---------- 1.5W
Package Thermal Resistance (Note 2)
DIP7, θ_{JA} ----------81°C/W
DIP7, θ_{JC} ----------48.5°C/W
Junction Temperature Range ---------- -45°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

VCC ---------- 12V~23V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 105°C

Electrical Characteristics

(V_{CC} = 12V (Note 3), T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
VCC Turn-on Threshold	V_{VCC_ON}	V_{CC} rising	19.5	21	22.5	V
VCC Turn-off Threshold (all logic reset)	V_{VCC_OFF}	V_{CC} falling	8	9	10	V
VCC OVP Voltage	V_{VCC_OVP}	V_{CC} rising	22.5	24	25.5	V
Operating Current	I_{VCC}			1.4		mA
Quiescent Current	I_Q	$V_{COMP} < V_{COMP,SLPIN}$	350	500	650	μA
CS Pin Section						
Maximum Peak Current Set Point	V_{CS_MAX}		0.9	1	1.15	V
Leading Edge Blanking Time	T_{LEB}			280		nS
Blanking Time for CS Short Detecting after MOS is Turned On	$T_{BLK\_CSSHORT}$			3		μS
Threshold for CS Short Detection	$V_{TH\_CSSHORT}$			50		mV
COMP Pin Section						
Internal Pull up Voltage	V_{COMP_HIGH}		2.15	2.5	2.85	V
Internal Pull up Resistor	R_{COMP}			21		kΩ
Threshold of Burst Operating Mode	V_{COMP_SLPIN}	V_{COMP} falling to enter burst mode	400	500	600	mV
	V_{COMP_SLPOUT}	V_{COMP} rising to exit burst mode	460	560	660	mV
OLP Threshold	V_{COMP_OLPOUT}			2		V
OLP Debounce Time	T_{OLP_DBC}	$V_{COMP}>V_{COMP,OLP}$	52	67	82	mS
HV Pin Section						
Off State HV Leakage Current	I_{HV_LK}	V_{HV}=1000V			10	μA
HV Pin Current Limit Level	I_{HV_LIMIT}	V_{HV}=1000V		0.3		mA
Power MOSFET Section						
Break-down Voltage	$V_{(BR)DSS}$	$I_{leakage}$=250μA	1200			V
ON-state Resistance	$R_{DS(ON)}$	V_{VCC}=12V, I_{DRAIN}=1A		5.26		Ω
Switching Frequency						
Nominal Switching Frequency	F_{NOM}		27	30	33	kHz
Modulation Amplitude	F_{MDL}			± 7%		
Frequency Modulation Period	T_{MDL}			4		mS
Internal OTP						
Internal OTP Threshold	T_{OTP}			160		℃
Hysteresis	T_{OTP_HYS}			17		℃

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause perm anent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

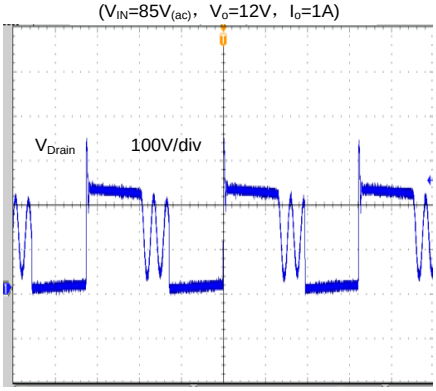
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a 2-layer test board of JESD 51-2 thermal measurement standard. Test condition: Device mounted on 2-layer PCB, 1oz copper, the board size is 76mm*60mm. θ_{JC} is measured on JESD51-14.

Note 3: Increase VCC pin voltage gradually higher than $V_{CC,ON}$ voltage then turn down to 12V.

Typical Performance Characteristics

Steady States

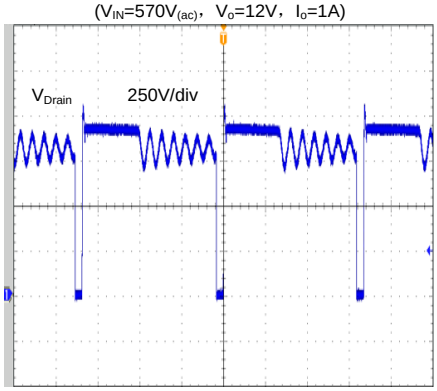
(V_{IN}=85$V_{(ac)}$, V_o=12V, I_o=1A)



Time (10μs/div)

Steady States

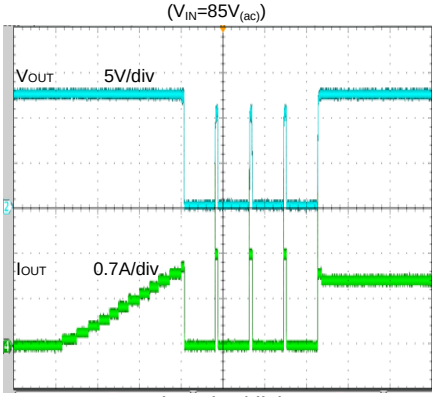
(V_{IN}=570$V_{(ac)}$, V_o=12V, I_o=1A)



Time (10μs/div)

OLP

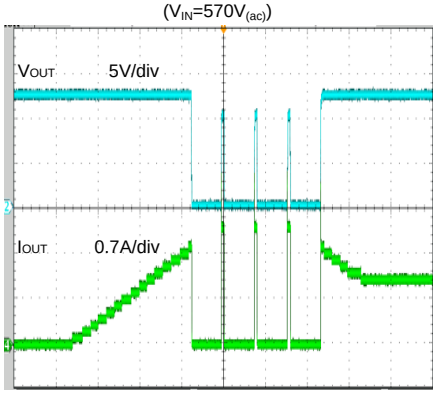
(V_{IN}=85$V_{(ac)}$)



Time (1s/div)

OLP

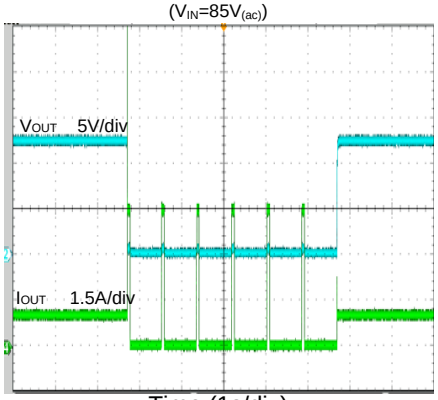
(V_{IN}=570$V_{(ac)}$)



Time (1s/div)

SCP

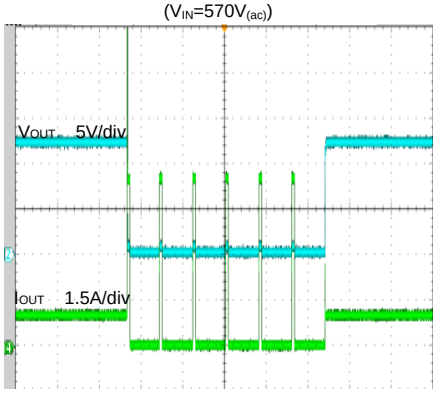
(V_{IN}=85$V_{(ac)}$)



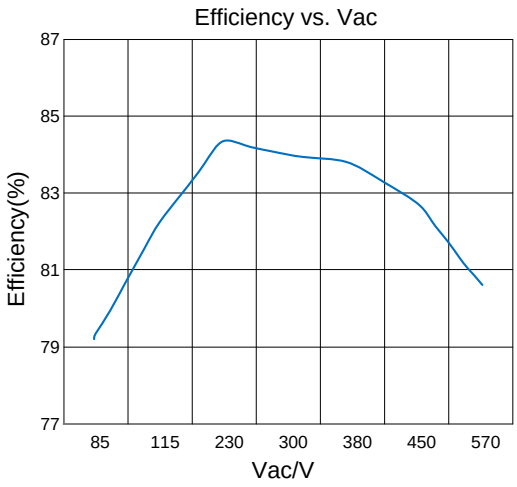
Time (1s/div)

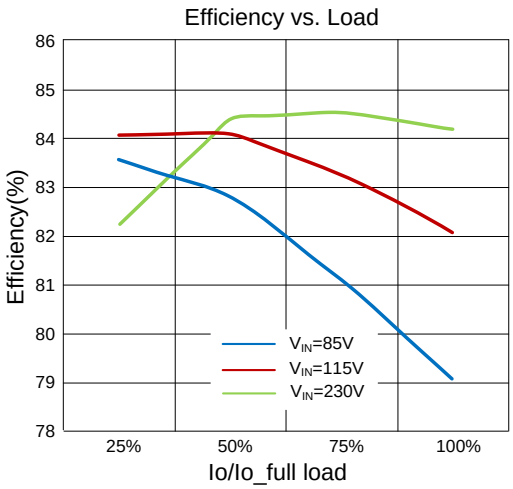
SCP

(V_{IN}=570$V_{(ac)}$)



Time (1s/div)





Applications Information

Pseudo fixed frequency control

SY23565 adopts Silergy's proprietary control method called pseudo fixed frequency control. Under steady state, the switching frequency is fixed value which is the same as traditional fixed frequency control method. The advantage of pseudo fixed frequency control method is that it can eliminate sub-harmonic oscillation during CCM when duty cycle is larger than 50%. So there is no need of slope compensation, design of flyback converter is simplified.

Burst mode control for light load

To achieve higher efficiency and lower power consumption at light load and no load condition respectively, SY23565 will enter burst mode when the load current decreases.

HV start up

SY23565 integrates high voltage start up on HV pin to achieve fast Vin start up speed and achieve very low no load power consumption.(Recommendation: minimum 100k resistor in series in application circuits.)

OLP

When over load condition happens, IC cannot further increase the output power due to max peak current limit. Due to the closed loop, COMP pin voltage will be pulled up to upper limit (~2.5V). SY23565 will compare COMP pin voltage with an internal OLP threshold (~2V), when V_{COMP} is higher than the OLP threshold, a timer will start to count, and if V_{COMP} is continuously higher than OLP threshold which result in OLP timer elapse, SY23565 will stop switching and enter auto-recovery mode.

Under output short circuit condition, VCC may drops to $V_{CC,MIN}$ before OLP timer elapse, SY23565 will also treat this condition as OLP.

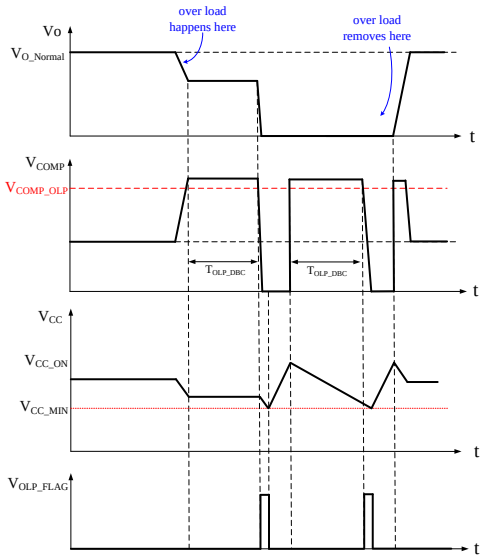


Fig.3 OLP protection

VCC OVP

Under abnormal conditions, such as opto-coupler open circuit or failure, VCC pin voltage may rises up to very high level. To avoid IC damage caused by VCC pin over voltage condition, SY23565 adopts an internal OVP threshold $V_{CC,OVP}$, when V_{CC} exceeds $V_{CC,OVP}$ threshold, SY23565 will stop switching and enter auto-recovery mode.

Internal OTP

SY23565 monitors die temperature under normal operating mode. Once die temperature rises above internal OTP threshold, IC will stop switching and enter auto-recovery mode.

Power Supply Design Guide

BUS capacitor calculation

Generally, bulk capacitor C_{BUS} is selected according to below rules:

1.5~2μF per watt (input power)

$C_{BUS,\ MIN}$=(1.5*P_{IN}) μF

$C_{BUS,\ MAX}$=(2*P_{IN}) μF

Minimum BUS voltage calculation

Minimum BUS voltage appears when input voltage V_{IN} is lowest and output current reaches the rated output current.

Minimum BUS voltage is calculated as:

$$V_{BUSMIN}=\sqrt{2*V_{INMIN}^{2}-\frac{P_O*(1-K_{CH})}{\eta*C_{BUS}*f_0}} \quad (3)$$

Where K_{CH} is BUS capacitor charge coefficient (generally K_{CH} is set to 0.2~0.3), η is converter efficiency, and f_0 is frequency of AC input.

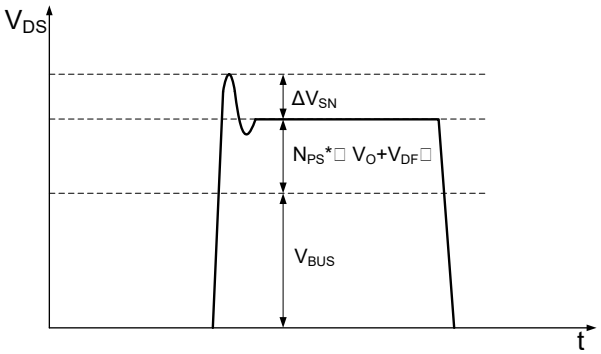
Transformer parameter calculation

1) Primary/secondary turns ratio: N_{PS}

N_{PS} is limited by the voltage stress of primary power MOSFET:

$$N_{PS}\le\frac{V_{MOSBR}*K_{DR}-\sqrt{2}V_{INMAX}-\Delta V_{SN}}{V_O+V_{DF}} \quad (4)$$

Where V_{MOSBR} is the breakdown voltage of primary MOSFET; K_{DR} is V_{DS} de-rating factor of power MOS; V_{DF} is forward voltage drop of secondary rectification diode; ΔV_{SN} is voltage spike during primary MOS turn off instant.



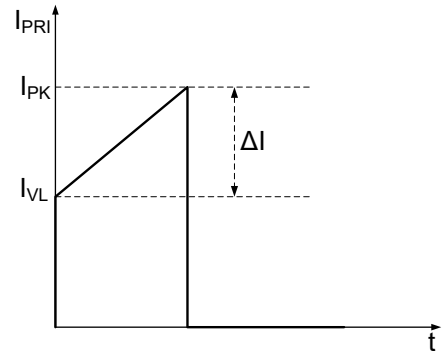
2) Primary inductance: L_M

Transformer primary inductance is related with primary current ripple. Generally, primary side current ripple is defined as shown in below figure. And current ripple factor is defined as below equation:

$$K_{BR}=\frac{0.5*\Delta I}{I_{PK}-0.5*\Delta I} \quad (5)$$

K_{BR}<1: CCM

K_{BR}=1: DCM



Generally, to get optimized transformer size, DCM operating is selected. K_{RP} =1. Once K_{RP} is selected, primary inductance of transformer is calculated as equation below:

$$L_M=\frac{V_{BUSMIN}^{2}\cdot D_{MAX}^{2}\cdot\eta}{2\cdot V_O\cdot I_O\cdot f_{SW}} \quad (6)$$

Where f_{SW} is rated switching frequency (30kHz), I_O is rated output current, η is converter efficiency. D_{MAX} is maximum duty cycle @ V_{BUSMIN} and rated output power, and D_{MAX} is calculated as below equation and it should be lower than 53% due to the max Ton limitation.

$$D_{MAX}=\frac{N_{PS}\cdot(V_O+V_{DF})}{V_{BUSMIN}+N_{PS}\cdot(V_O+V_{DF})} \quad (7)$$

3) Turns of primary winding: N_P

(a)Select the magnetic core type, identify the effective cross-sectional area A_E

(b)Preset the maximum magnetic flux density B_{MAX}

B_{MAX}=0.22T~0.28T

(c)Calculate maximum primary peak current I_{PK} @ rated output power:

$$I_{PK}=\frac{V_O\cdot I_O\cdot 2}{V_{BUSMIN}\cdot D_{MAX}\cdot\eta} \quad (8)$$

(d)Calculate primary turns: N_P

$$N_P=\frac{I_{PK}\cdot L_M}{B_{MAX}\cdot A_E} \quad (9)$$

4) Turns of secondary winding: N_S

$$N_S=\frac{N_P}{N_{PS}} \quad (10)$$

5) Turns of auxiliary winding: N_A

Before calculate auxiliary turns, VCC supply voltage $V_{CC(AUX)}$ by auxiliary winding should be predefined first.

Generally, $V_{CC(AUX)}$ is set to 12V~18V, then auxiliary turns is calculated as:

$$N_A = \frac{N_S \cdot V_{CC(AUX)}}{V_O} \quad (11)$$

Peak current sense resistor calculation

Maximum peak current appears under minimum BUS voltage and maximum load condition (OCP point); maximum peak current is calculated as:

$$I_{PKMAX} = \frac{V_O \cdot I_O \cdot K_{OCP} \cdot 2}{V_{BUSMIN} \cdot D_{MAX} \cdot \eta} \quad (12)$$

Where K_{OCP} is OCP proportion, K_{OCP} is generally set to 120%~130%. After maximum primary peak current has been calculated, the peak current sense resistor R_{CS} can be easily derived by equation below:

$$R_{CS} = \frac{V_{CSMAX}}{I_{PKMAX}} \quad (13)$$

Where V_{CSMAX} is the maximum allowed peak current sense voltage (typical=1.0V).

Note: Customer may need to adjust current sense resistor according to the converter OCP point. If OCP point is larger than target level, R_{CS} should be adjusted a little larger; If OCP point is smaller than target level, R_{CS} should be adjusted a little smaller.

Secondary Diode Selection

Under the conditions of the maximum BUS voltage and maximum output voltage, the reverse voltage of secondary rectification diode will reach the maximum level. The maximum value of diode reverse voltage (ignore voltage spike when primary MOS is turned on) is calculated as equation below:

$$V_{DRMAX} = \frac{\sqrt{2} \cdot V_{INMAX}}{N_{PS}} + V_O \quad (14)$$

Where V_{INMAX} is maximum AC input voltage (RMS), N_{PS} is the primary/secondary turns ratio of the transformer and V_O is output voltage, which is predefined by customer.

Maximum instantaneous forward current is calculated as equation below:

$$I_{DPKMAX} = I_{PKMAX} \cdot N_{PS} \quad (15)$$

Where I_{PKMAX} is the maximum primary peak current @ V_{BUSMIN} and OCP point.

Average forward current of diode

$$I_{DAVGMAX} = I_O \cdot K_{OCP} \quad (16)$$

Where I_O is rated output current, and K_{OCP} is OCP proportion to rated output current.

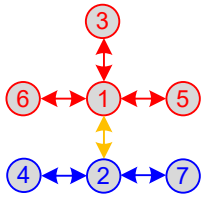
Layout Considerations

A proper PCB design must follow the below guidelines:

(a) To achieve a good EMI performance and to reduce the line frequency voltage ripples, the output of the bridge rectifier should be connected to the BUS line capacitor first, then to the switching circuit.

(b) The circuit loop of all switching circuit should be kept as small as possible: primary power loop, secondary loop and auxiliary power loop.

(c) The connection of primary ground is recommended as:



Ground ①: Ground of BUS capacitor
Ground ②: Ground of bias supply capacitor
Ground ③: Ground node of auxiliary winding
Ground ④: Ground of receiver of opto-coupler
Ground ⑤: Ground of primary side Y capacitor
Ground ⑥: Ground of current sense resistor.
Ground ⑦: Ground of controller IC.

(d) Bias supply trace should be connected to the bias supply capacitor first and then to the GND pin. The bias supply capacitor should be put right beside the IC.

(e) The switching loop formed by 'CS pin - current sense resistor - GND pin' should be kept as small as possible.

Design Example

A design example of typical application is shown below step by step.

Input/output Specification

Parameter	Symbol	Value	Unit
AC Input voltage range	V_{IN}	85~570	V
Rated output power	P_O	12	W
Rated output voltage	V_O	12	V
Rated output current	I_O	1	A
OCP proportion	K_{OCP}	120%	

Preset parameters

Parameter	Symbol	Value	Unit
Break down voltage of power MOS	V_{MOSBR}	1200	V
V_{DS} de-rating factor of power MOS	K_{DR}	90%	
Spike on V_{DS} during power MOS turn off	ΔV_{SN}	100	V
Converter efficiency	η	80%	
Primary current ripple factor@ V_{BUSMIN} & rated output power	K_{RP}	1	
BUS capacitor charge coefficient	K_{CH}	0.2	
Secondary diode forward voltage drop	V_{DF}	0.5	V
Transformer effective cross-sectional area (EF20)	A_E	33.5	mm^2

1) BUS capacitor selection

Calculate input power @ rated output power

$$P_{IN}=\frac{P_O}{\eta}=\frac{12}{0.8}=15W$$

Minimum BUS capacitor: $C_{BUSMIN}=1.5*15=22.5\mu F$

Maximum BUS capacitor: $C_{BUSMAX}=2*15=30\mu F$

Select BUS capacitor: $C_{BUS}=23.5\mu F$, install two 47μF/450V BUS caps in series.

2) Minimum BUS voltage calculation

BUS capacitor charge coefficient: $K_{CH}=0.2$

$$V_{BUSMIN}=\sqrt{2*V_{INMIN}^{2}-\frac{P_O*(1-K_{CH})}{\eta*C_{BUS}*f_0}}=\sqrt{2*85^2-\frac{12*(1-0.2)}{0.8*23.5*50*10^{-6}}}=65.1V$$

3) Transformer design

(a)Calculate primary/secondary turns ratio: N_{PS}

$$N_{PS}\le\frac{V_{MOSBR}*K_{DR}-\sqrt{2}V_{INMAX}-\Delta V_{SN}}{V_O+V_{DF}}=\frac{1200*0.9-\sqrt{2}*570-100}{12+0.5}=13.9$$

Select $N_{PS}=7$

(b) Calculate maximum duty cycle: D_{MAX}

$$D_{MAX}=\frac{N_{PS}\cdot(V_O+V_{DF})}{V_{BUSMIN}+N_{PS}\cdot(V_O+V_{DF})}=\frac{7*(12+0.5)}{65.1+7*(12+0.5)}=0.57$$

(c) Calculate primary inductance: L_M

$$L_M = \frac{V_{BUSMIN}^2 \cdot D_{MAX}^2 \cdot \eta}{2 \cdot V_O \cdot I_O \cdot f_{SW} * K_{RP}} = \frac{65.1^2 \cdot 0.57^2 \cdot 0.8}{2 \cdot 12 \cdot 1 \cdot 30 * 10^3 * 1} = 1.53mH$$

Select L_M=1.5mH

(d)Calculate primary peak current @ rated output power:

$$I_{PK} = \frac{V_O \cdot I_O \cdot 2}{V_{BUSMIN} \cdot D_{MAX} \cdot \eta} = \frac{12*1*2}{65.1 \cdot 0.57 \cdot 0.8} = 0.8A$$

(e)Calculate primary winding turns: N_P

$$N_P = \frac{I_{PK} \cdot L_M}{B_{MAX} \cdot A_E} = \frac{0.8 \cdot 1500}{0.26 \cdot 33.5} = 137.8$$

Select primary winding turns: N_P =133

(f)Calculate secondary winding turns: N_S

$$N_S = \frac{N_P}{N_{PS}} = \frac{133}{7} = 19$$

(g) Calculate auxiliary winding turns: N_A

VCC supply voltage from auxiliary winding is set to: $V_{CC(AUX)}$ =12V

$$N_A = \frac{N_S \cdot V_{CC(AUX)}}{V_O} = \frac{19*12}{12} = 19$$

Select auxiliary winding turns: N_A =19

4) Current sense resistor calculation:

$$I_{PKMAX} = \frac{V_O \cdot I_O \cdot K_{OCP} \cdot (1+K_{RP})}{V_{BUSMIN} \cdot D_{MAX} \cdot \eta} = \frac{12 \cdot 1 \cdot 120\% \cdot 2}{65.1 \cdot 0.57 \cdot 0.8} = 0.97A$$

$$R_{CS} = \frac{V_{CSMAX}}{I_{PKMAX}} = \frac{1}{0.97} = 1.03\Omega$$

5) Secondary diode selection

(a)Maximum reverse voltage calculation:

$$V_{DRMAX} = \frac{\sqrt{2} \cdot V_{INMAX}}{N_{PS}} + V_O = \frac{\sqrt{2}*570}{7} + 12 = 127.16V$$

Considering the voltage spike, reverse voltage rating of the diode is recommended to be greater than 150V.

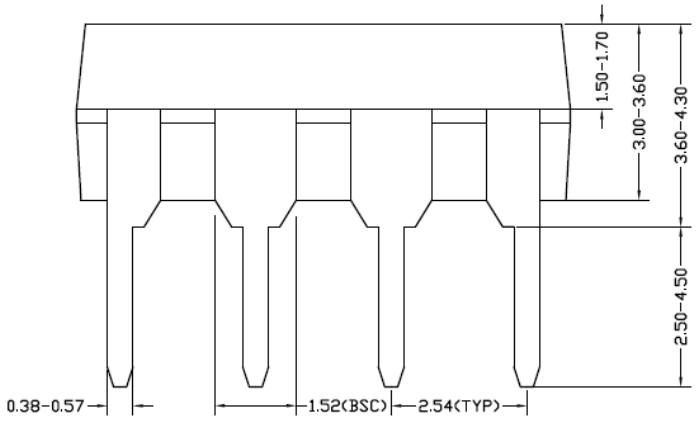
(b)Maximum instantaneous forward current:

$$I_{DPKMAX} = I_{PKMAX} \cdot N_{PS} = 0.97*7 = 6.79A$$

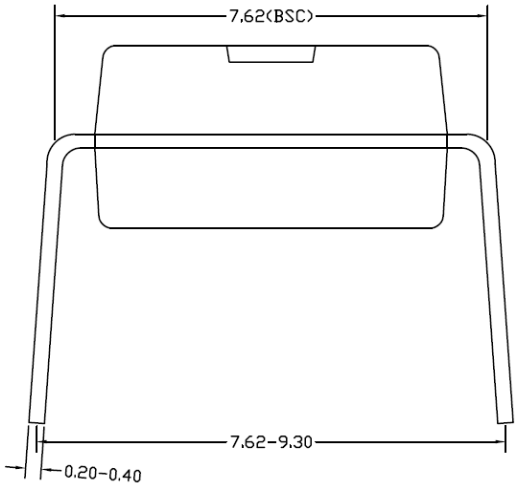
(c)Maximum average forward current:

$$I_{DAVGMAX} = I_O \cdot K_{OCP} = 1*120\% = 1.2A$$

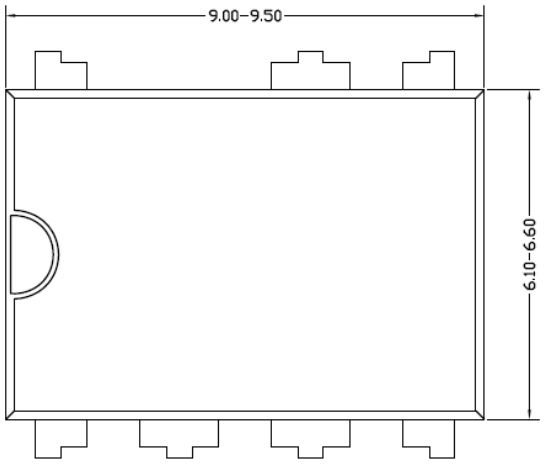
DIP7 Package Outline



Side view A



Side view B



Top view

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
	Revision 0.9	Initial Release

IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.

2. Applications. Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.

3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.

4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

5. **Terms and conditions of commercial sale**. Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at http://www.silergy.com/stdterms, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.

6. **No offer to sell or license**. Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com