SY22817A

Flyback Controller
With Primary Side CC/CV Control

General Description

SY22817A is a single stage Flyback controller targeting at Constant Current/Constant Voltage (CC/CV) applications. Both the output current and voltage are sensed on the primary side, eliminating the opto-isolator and the secondary side feedback circuitry, and minimizing the overall system cost.

SY22817A adopts the quasi-resonant operation and the adaptive PWM/PFM control to achieve the highest average efficiency and the best EMI performance. The no-load switching frequency can be as low as 500Hz, minimizing the no-load power loss.

SY22817A has programmable cable compensation to provide a better load regulation for the output voltage at the cable terminals.

SY22817A provides reliable protections including VIN Over Voltage Protection, Short Circuit Protection (SCP), Over Temperature Protection (OTP), Output voltage OVP/UVP (OVP/UVP), VSEN/ISEN pin short protection, VSEN pin upper divider resistor disconnect protection.

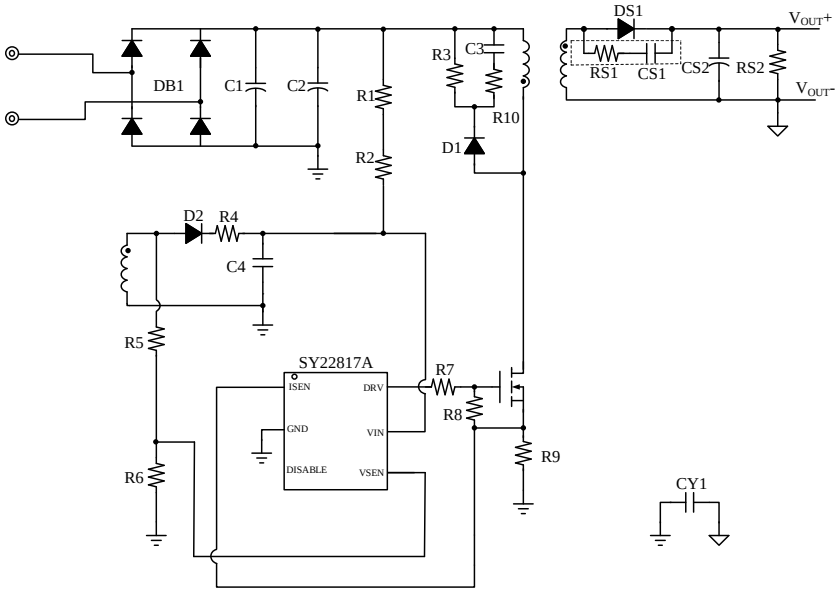
Features

- Tight PSR CC/CV Regulation Over Entire Operating Range
- QR-mode Operation for High Efficiency
- PWM/PFM Control for High Average Efficiency
- Fast Dynamic Load Transient Response
- Cable Compensation for Better Load Regulation
- Low Start Up Current: 5μA Max
- Minimum Frequency Limitation 500Hz
- Reliable Protections for OVP, UVP, SCP, OTP, OCP
- Reliable Protections for Safety Requirement
- Maximum Switching Frequency Limitation 125kHz
- RoHS Compliant and Halogen Free
- Compact Package: SOT23-6

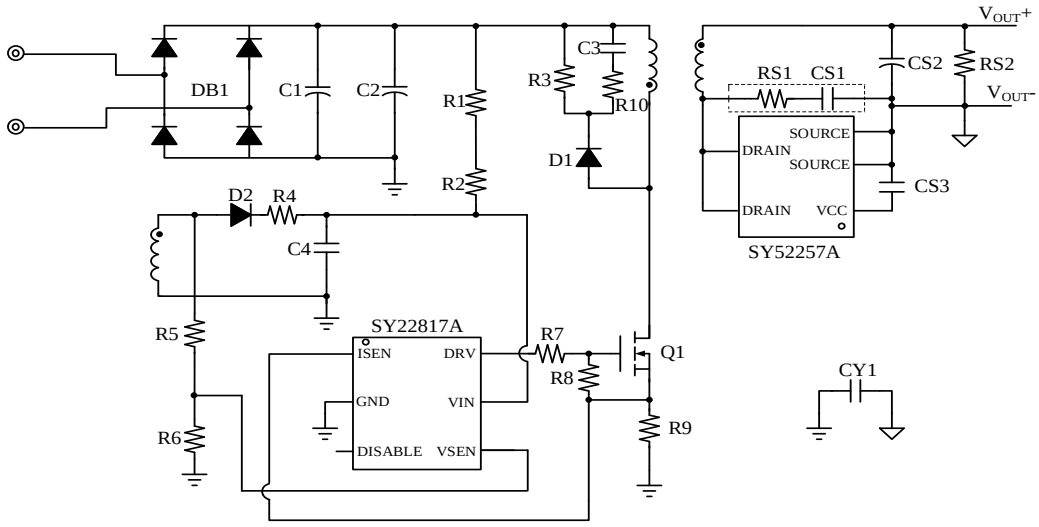
Applications

- AC/DC Adapters
- Battery Chargers

Typical Applications



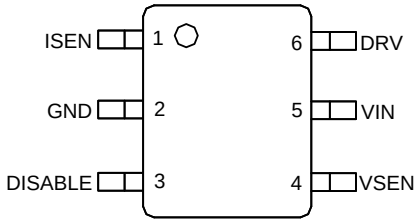
Typical Application Circuit



Typical Application Circuit Using SY52257A as the Secondary-Side Synchronous Rectifier

Ordering Information

SY22817□(□□)□
- Temperature Code
- Package Code
- Optional Spec Code



Pinout (Top view)

Ordering Number	Package	Top Mark
SY22817AABC	SOT23-6	2gxyz

x=year code, y=week code, z= lot number code

Pinout

Pin Number	Pin Name	Pin Description
1	ISEN	Current sense pin. Connect this pin to the source of the primary switch.
2	GND	Ground pin.
3	DISABLE	Disable control pin. Pull down to turn off. When this function is not used, it should be floating.
4	VSEN	Output voltage sense pin. This pin receives the auxiliary winding voltage by a resistor divider. The value of the resistor divider also programs the cable impedance. This pin also senses the winding voltage to provide the QR operation.
5	VIN	Power supply pin.
6	DRV	Gate driver pin. Connect this pin to the gate of primary MOSFET.

Absolute Maximum Ratings (Note 1)

VIN---------- -0.3V~26V
DRV ---------- -0.3V~15V
Supply Current I_{VIN} ---------- 20mA
VSEN ---------- -1V (*1) ~7V
ISEN---------- -0.3V~3.6V
DISABLE---------- -0.3V~3.6V
Power Dissipation, @ T_A = 25°C SOT23-6 ---------- 0.6W
Package Thermal Resistance (Note 2)
SOT23-6, θ_{JA} ---------- 170°C/W
SOT23-6, θ_{JC} ---------- 130°C/W
Temperature Range ---------- -45°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
(*1) Dynamic VSEN Negative Voltage in 50us Duration---------- -1V
Dynamic VSEN Negative Current in 50us Duration---------- -2mA
Human Body Model ESD, ANSI/ESDA/JEDEC JS-001-2014 (Note 3) ---------- ±2kV
Latch-up Test Per JEDEC STANDARD NO.78D NOVEMBER 2014 (Note 3) ---------- ±100mA

Recommended Operating Conditions

VIN---------- 9V~20V
ISEN---------- 0V~1V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 105°C

Electrical Characteristics

(V_{VIN} = 12V (Note 4), T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
VIN Turn-on Threshold	V_{VIN_ON}	V_{VIN} increasing	19.5	21.2	22.9	V
VIN Turn-off Threshold	V_{VIN_OFF}	V_{VIN} decreasing	6.7	7.7	8.7	V
VIN OVP Voltage	V_{VIN_OVP}	V_{VIN} increasing	22.7	24.0	25.6	V
VIN OVP Voltage Hysteresis	$V_{VIN\_OVP\_HYS}$	V_{VIN_OVP} - V_{VIN_ON}	2	3	4.5	V
VIN OVP Blanking time (Note 5)	T_{VIN_OVP}		85	128	152	μs
Start Up Current	I_{ST}	V_{VIN}<V_{VIN_OFF}	0.5	2	5	μA
Operating Current (Note 6)	I_{VIN}	f=100kHz, C_{DRV}=800pF	-	3	-	mA
Quiescent Current (Note 6)	I_Q	f=500Hz, C_{DRV}=800pF	-	170	-	μA
Discharge Current in OVP Mode	I_{VIN_OVP}	V_{VIN} =12V	3.9	5.2	6.6	mA
Current Feedback Modulator Section						
Internal Reference Voltage	V_{REF}		0.41	0.42	0.43	V
ISEN Pin Section						
Current Limit Voltage	V_{ISEN_LIM}	V_{FBV}<0.4V V_{ISEN} increasing	0.7	0.75	0.8	V
		V_{FBV}>0.4V V_{ISEN} increasing	0.92	0.95	0.98	V
Current Min Voltage	V_{ISEN_MIN}		0.22	0.26	0.30	V
Min ON Time	T_{ON_MIN}	DRV min width	340	430	520	ns
Voltage Threshold for V_{ISEN_LIM} Switch	V_{ISEN_SWITCH}	V_{ISEN} increasing	310	400	510	mV
Detection Time for V_{ISEN_LIM} Switch	T_{ISEN_SWITCH}		1.2	1.8	2.4	μs
CC Feedforward Resistor (Note 5)	R_{INT}		280	320	360	Ω
Voltage Threshold for ISEN Pin Short	V_{ISEN_SHORT}		95	150	205	mV
Time Threshold for ISEN Pin Short (Note 5)	T_{ISEN_SHORT}		2.4	3.6	4.8	μs
Enable Time for ISEN Pin Short (Note 5)	$T_{ISEN\_SHORT\_EN}$	Timer start V_{VIN_ON}	49	62	78	ms
Peak Current Modulation						
Modulation Minimum Range (Note 5)	$V_{ISEN\_JITTER\_MIN}$	V_{ISEN} = V_{ISEN_MIN}	4	10	16	mV
Modulation Maximum Range (Note 5)	$V_{ISEN\_JITTER\_MAX}$	V_{ISEN} = V_{ISEN_LIM}	48	58	68	mV
Modulation Period (Note 5)	T_{JITTER}		200	250	300	μs
VSEN Pin Section						
OVP Voltage Threshold	V_{VSEN_OVP}		1.4	1.5	1.6	V
Number of Consecutive VSEN OVP Enter Hiccup Mode (Note 5)	N_{VSEN_OVP}		-	4	-	
UVP Voltage Threshold (Note 5)	V_{VSEN_UVP}		0.75	0.8	0.85	V
Blanking Time for VSEN UVP (Note 5)	T_{VSEN_UVP}		49	62	78	ms
Internal Reference Voltage	V_{VSEN_REF}		1.232	1.25	1.268	V
Cable Compensation Coefficient	K3		36	50	64	μA/V
Sourcing Current Threshold for VSEN Pin Short Detection	I_{VSEN_SHORT}		65	100	135	μA
Voltage Threshold for VSEN Pin Short Detection (Note 5)	V_{VSEN_SHORT}		30	60	90	mV

Blanking Time for VSEN Pin Short Detection (Note 5)	T_{VSEN_SHORT}		85	128	152	μs
Sourcing Current Threshold for Upper Resistor Open	I_{BO}		10	18	26	μA
Number of Consecutive Upper Resistor Open Enter Hiccup Mode (Note 5)	N_{BO}		-	8	-	
Voltage Threshold for Current Cross Zero (Note 5)	V_{VSEN_CCZ}		65	100	135	mV
Voltage Threshold for Zero Zoltage Detection (Note 5)	V_{ZERO}		-70	-40	-10	mV
Turn On Delay After Zero Voltage Detection (Note 5)	T_{DELAY}		300	400	500	ns
DISABLE Pin Section						
Disable On Threshold	$V_{DISABLE\_ON}$	$V_{DISABLE}$ increasing	0.85	1	1.15	V
Disable Off Threshold	$V_{DISABLE\_OFF}$	$V_{DISABLE}$ decreasing	0.85	1	1.15	V
Gate Driver Section						
Gate Driver Voltage	V_{GATE}	V_{VIN} =V_{VIN_OFF}+0.2V	5.9	-	-	V
		V_{VIN}=16V	10.2	12	13.8	V
Maximum Source Current (Note 5)	I_{SOURCE_MAX}		-	160	-	mA
Maximum Sink Current (Note 5)	I_{SINK_MAX}		-	800	-	mA
Protection Timer Section						
Max ON Time (Note 5)	T_{ON_MAX}		19	26	33	μs
Min OFF Time1	T_{OFF_MIN1}	V_{ISEN} = V_{ISEN_MIN}	1.6	1.9	2.3	μs
Min OFF Time2	T_{OFF_MIN2}	V_{ISEN} = V_{ISEN_LIM}	2.1	2.7	3.5	μs
Max OFF Time	T_{OFF_MAX}		1.58	2.0	2.42	ms
Max OFF Time for Start Up (Note 5)	$T_{OFF\_MAX\_ST}$		24.3	36	47.6	μs
Max OFF Time for Load Transient 1 (Note 5)	$T_{OFF\_MAX\_LT1}$		90	125	160	μs
Number of Consecutive Max OFF Time for Load Transient 1 (Note 5)	$N_{OFF\_MAX\_LT1}$		-	4	-	
Max OFF Time for Load Transient 2 (Note 5)	$T_{OFF\_MAX\_LT2}$		190	250	310	μs
Working Time for Load Transient 2 (Note 5)	$T_{OFF\_MAX\_LT2}$		6.3	8.0	9.7	ms
Minimum Switching Period	T_{PERIOD_MIN}		6.9	8	9.1	μs
Thermal Section						
Thermal Shutdown Temperature (Note 5)	T_{SD}	Temperature increasing	-	150	-	°C
Thermal Shutdown Temperature Hysteresis (Note 5)	T_{SD_HYS}	Temperature decreasing	-	20	-	°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on "2 x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal via to bottom layer ground plane.

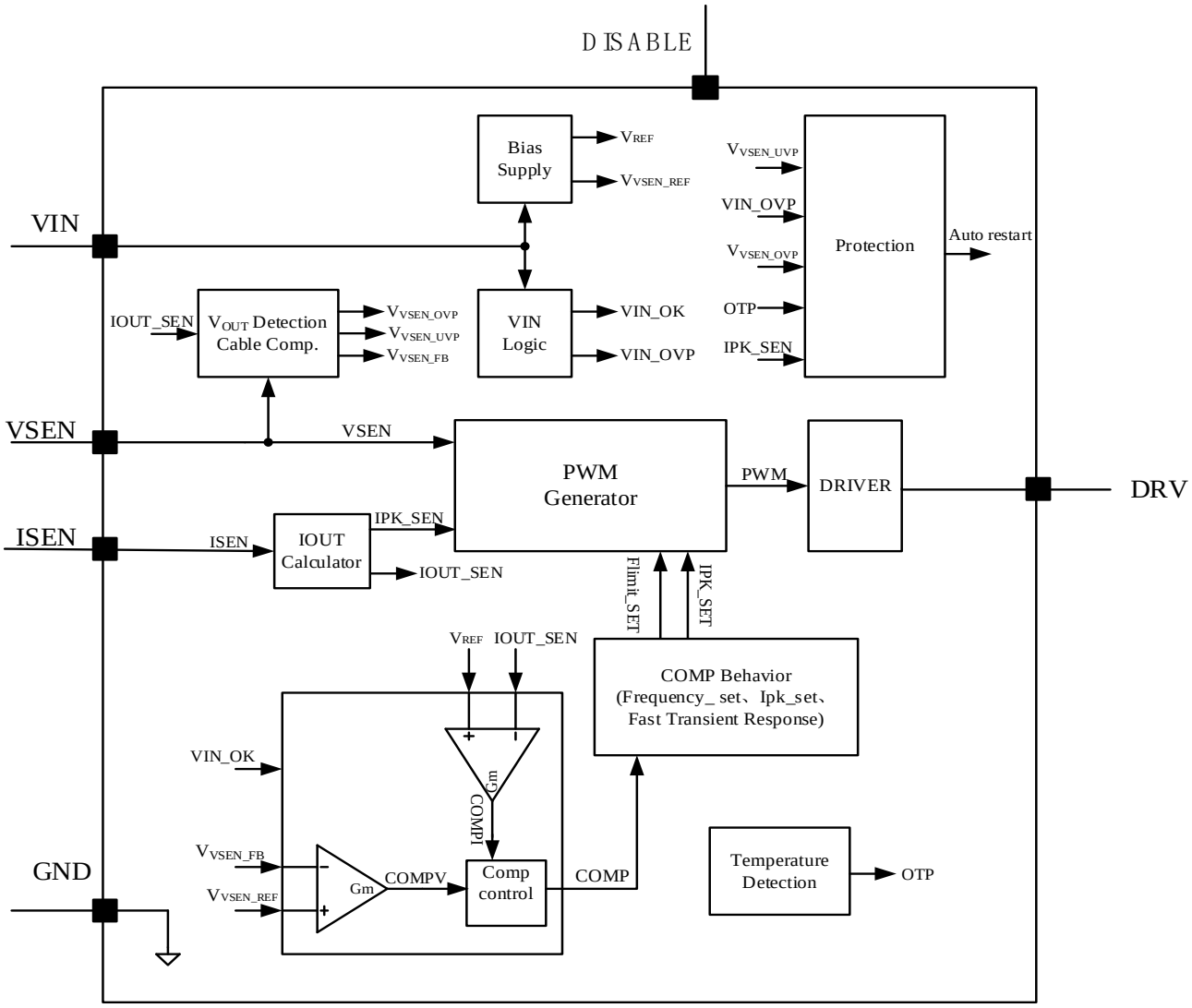
Note 3: Meets JEDEC standards NO.78D november 2014 and JS-001-2014.

Note 4: Increase VIN pin voltage gradually higher than V_{VIN_ON} voltage to start the IC first, then set VIN to 12V.

Note 5: Guarantee by design.

Note 6: Application test result.

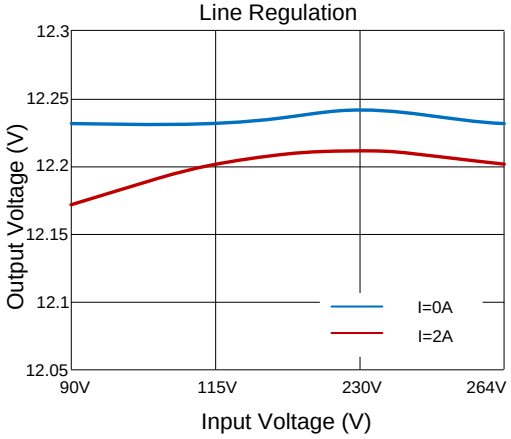
Block Diagram



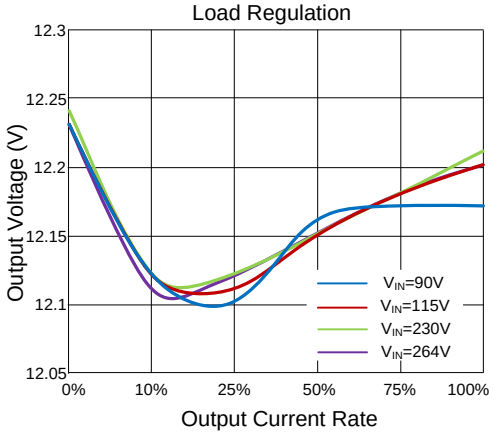
Typical Performance Characteristics

(Test condition: input voltage: 90~264Vac; output spec: 12Vdc_2A; output cable: 22AWG_1.2m; Ambient temperature: 25±5 ℃; Ambient humidity: 65±25 %.)

Line Regulation

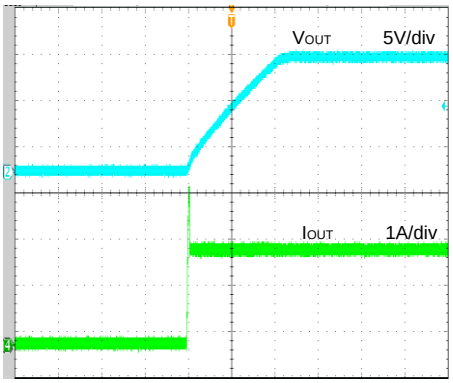


Load Regulation



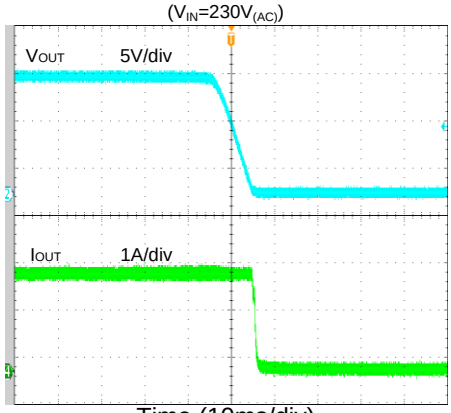
Startup

(V_{IN}=230$V_{(AC)}$)



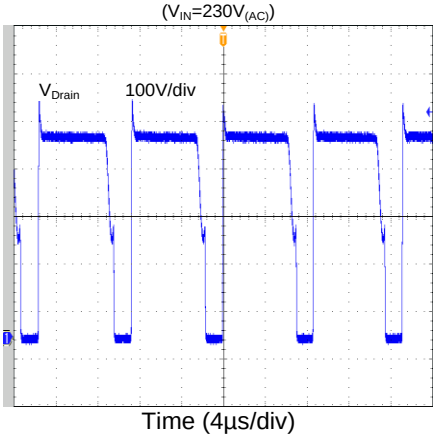
Shutdown

(V_{IN}=230$V_{(AC)}$)



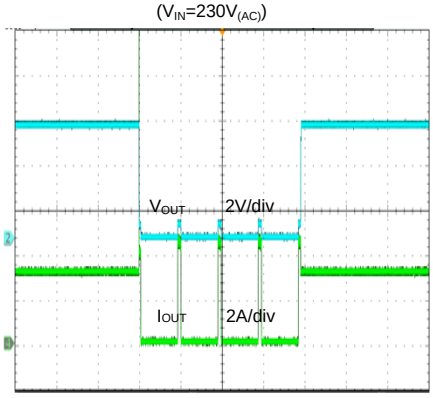
Steady States

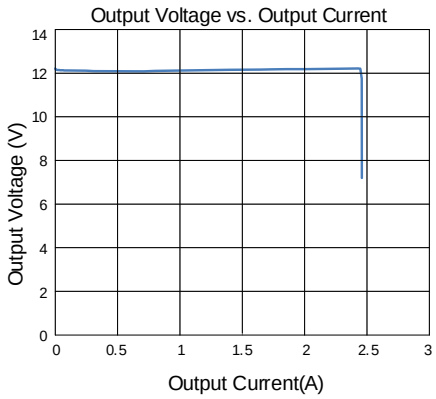
(V_{IN}=230$V_{(AC)}$)

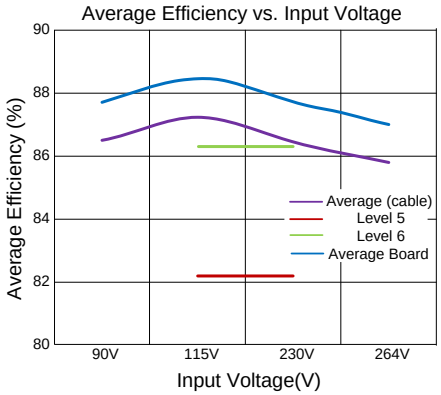


Short Circuit Protection

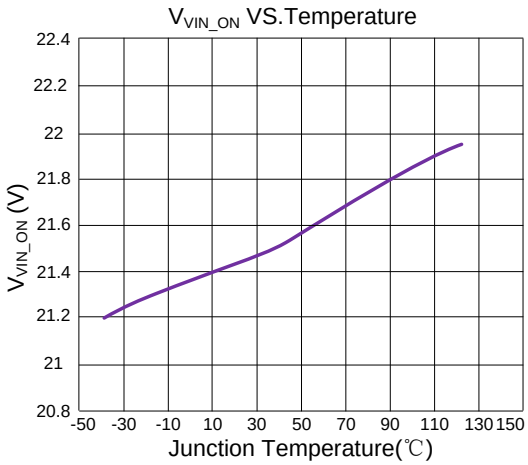
(V_{IN}=230$V_{(AC)}$)

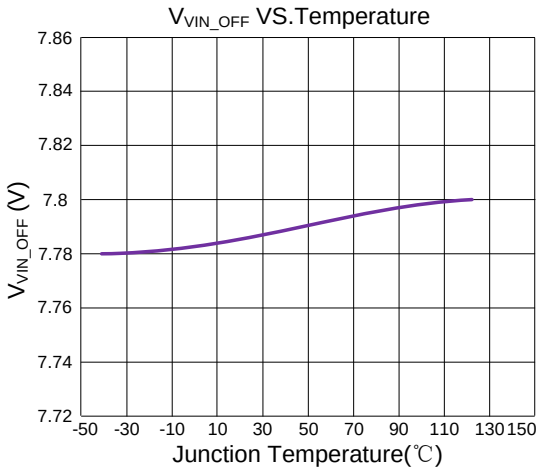


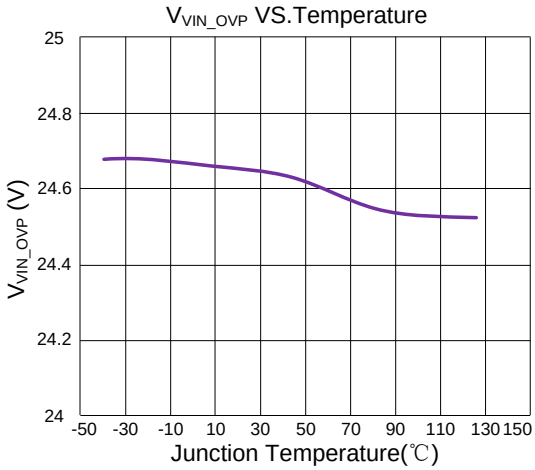


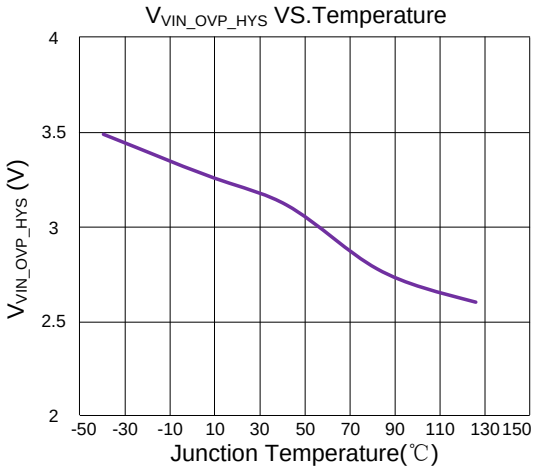


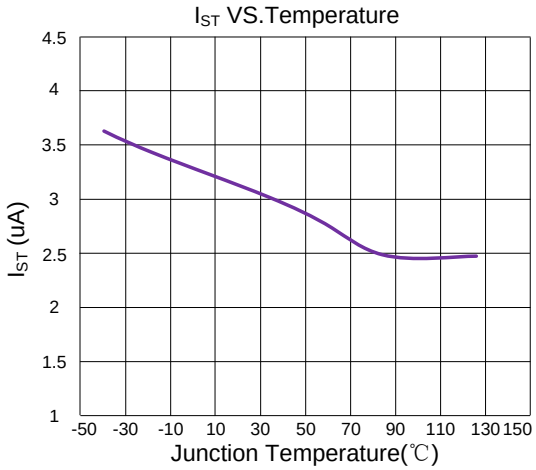
Typical Characteristics

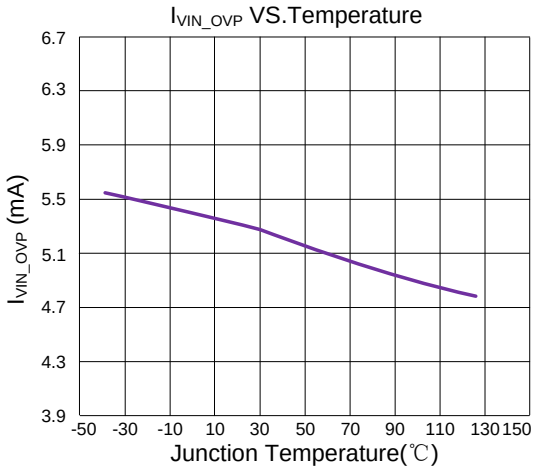


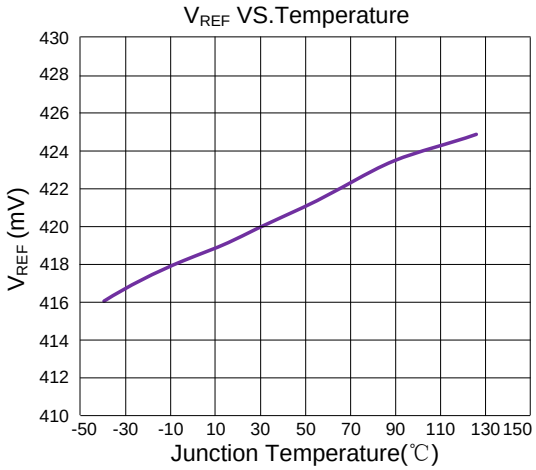


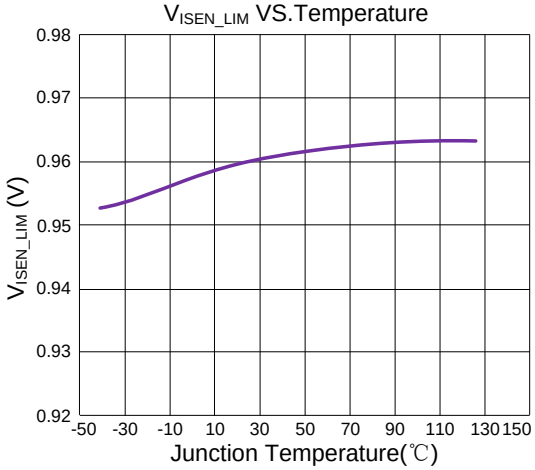


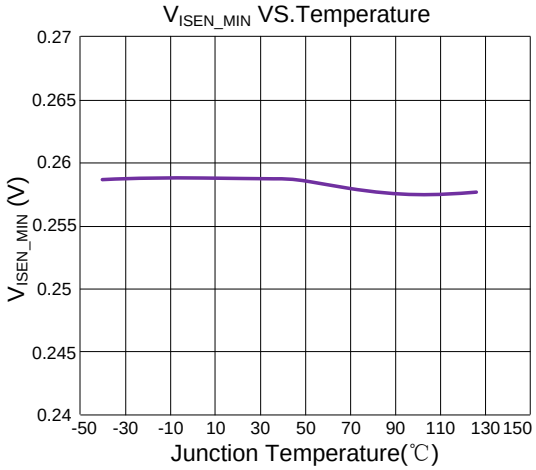


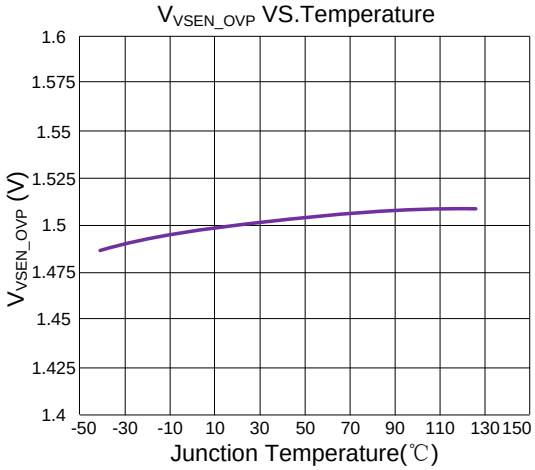




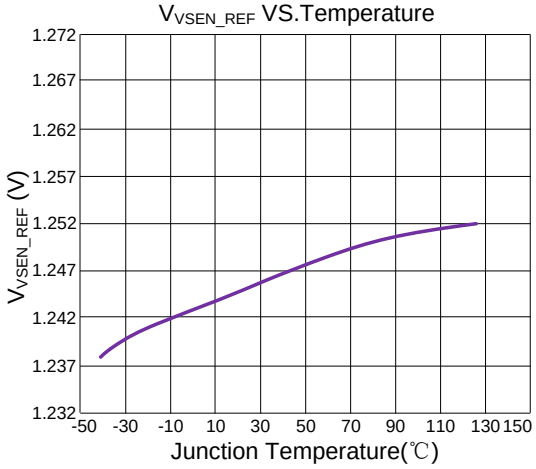




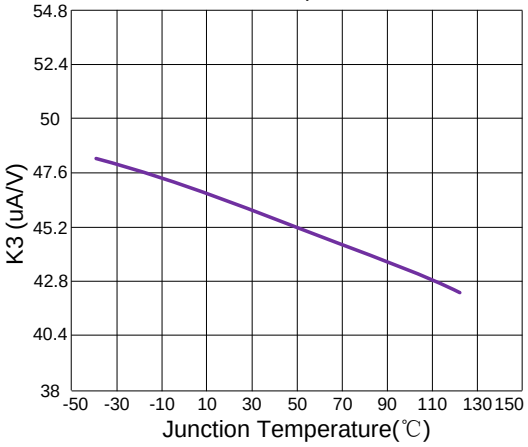




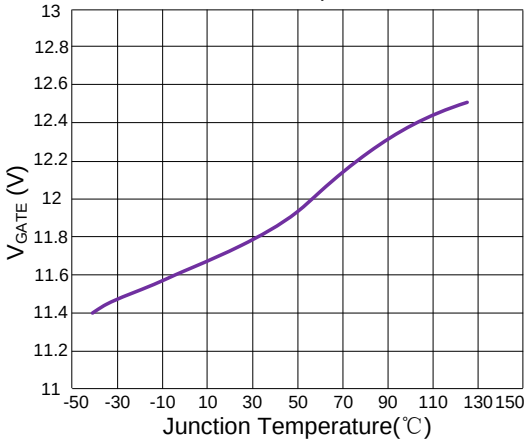
V_{VSEN_REF} VS.Temperature



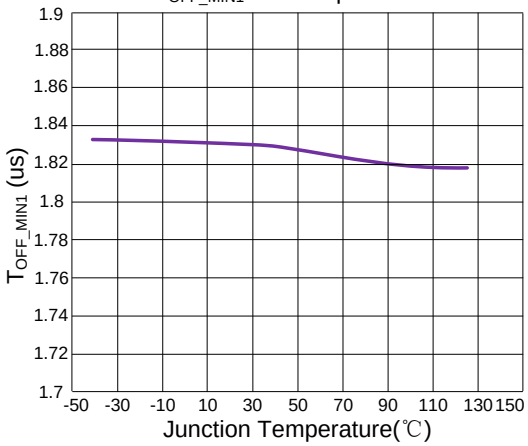
K3 VS.Temperature



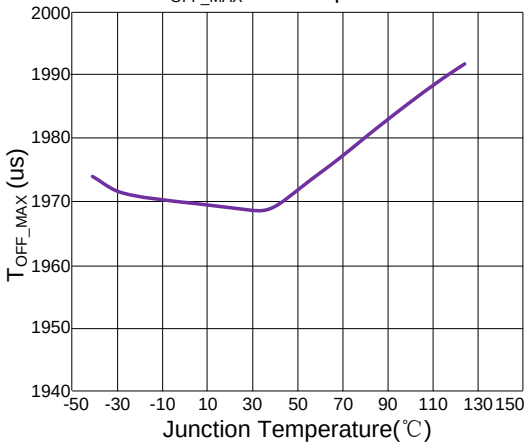
V_{GATE} VS.Temperature



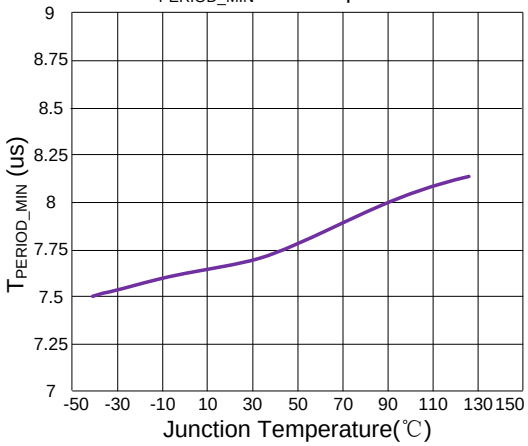
T_{OFF_MIN1} VS.Temperature



T_{OFF_MAX} VS.Temperature



T_{PERIOD_MIN} VS.Temperature



Operation Principles

Start-up Operation

After AC supply is powered on, the rectified BUS voltage ramps up. The capacitor across VIN and GND pins, C_{VIN}, is charged up by the BUS voltage through a start up resistor R_{ST}. Once V_{VIN}, the voltage on the VIN pin, rises up to V_{VIN_ON}, the internal blocks starts the operation. V_{VIN} will subsequently be pulled down by the power consumption of the circuitry until the auxiliary winding of Flyback transformer can supply sufficient energy to maintain V_{VIN} above V_{VIN_OFF}.

The start-up procedure is divided into two sections, as shown in Fig.1: t_{STC} is the C_{VIN} charged up section, and t_{STO} is the output voltage built-up section. The start up time t_{ST} composes of t_{STC} and t_{STO}, and usually t_{STO} is much smaller than t_{STC}.

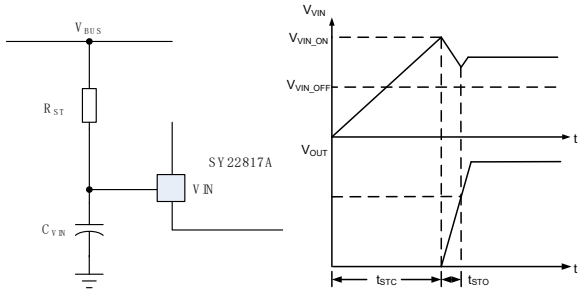


Fig.1 Start up

The start up resistor R_{ST} and C_{VIN} are designed by the following rules:

(a) Preset start-up resistor R_{ST}, make sure that the current through R_{ST} is larger than I_{ST} and smaller than I_{VIN_OVP}

$$\frac{V_{BUS\_MAX}}{I_{VIN\_OVP}} < R_{ST} < \frac{V_{BUS\_MIN}}{I_{ST}} \quad (1)$$

Where V_{BUS} is the BUS line voltage.

(b) Select C_{VIN} to obtain an ideal start-up time $t_{ST,}$ and ensure the output voltage is built up with only one try.

$$C_{VIN} = \frac{(\frac{V_{BUS\_MIN}}{R_{ST}} - I_{ST}) \times t_{ST}}{V_{VIN\_ON}} \quad (2)$$

(c) If the C_{VIN} is not big enough to build up the output voltage with one try, increase C_{VIN} and decrease R_{ST}, go back to step (a) and repeat the same design flow until the ideal start up procedure is obtained.

Shut-down Operation

After AC supply is powered off, the energy stored in the BUS capacitor will be discharged. When the auxiliary winding of Flyback transformer cannot supply enough energy to the VIN pin, V_{VIN} will decrease. Once V_{VIN} is below V_{VIN_OFF}, the IC will stop working.

Quasi-Resonant Operation (valley detection)

The Quasi-Resonant switching mode is applied, which means to turn on MOSFET at voltage valley. QR mode operation provides the low turn-on switching losses for Flyback converter.

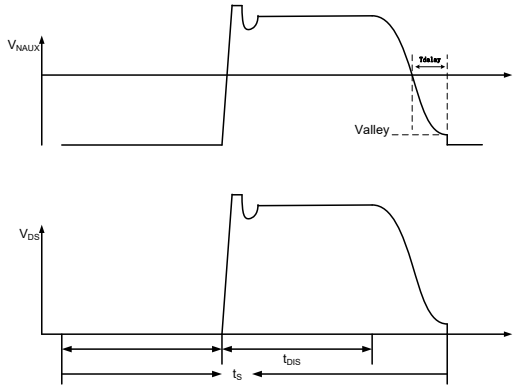


Fig.2 QR mode operation

The voltage across drains and source of the primary MOSFET is reflected to the auxiliary winding of the Flyback transformer. VSEN pin detects the voltage across the auxiliary winding by a resistor divider. As shown in Fig.2, when the voltage on VSEN pin across zero, the MOSFET would be turned on after 400ns delay.

Output voltage control (CV control)

In order to achieve primary side constant voltage control, the output voltage is sensed by the auxiliary winding.

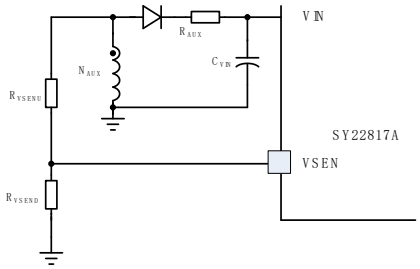


Fig.3 VSEN pin connection

As shown in Fig.4, during OFF time, the voltage across the auxiliary winding is

$$V_{AUX} = (V_{OUT} + V_{D\_F}) \times \frac{N_{AUX}}{N_S} \quad (3)$$

N_{AUX} is the turns of auxiliary winding; N_S is the turns of secondary winding; V_{D_F} is the forward voltage of the power diode.

At the current zero-crossing point, V_{D_F} is zero, so V_{OUT} is proportional to V_{AUX}. The voltage of this point is sampled by the IC as the feedback of output voltage. The resistor divider is designed by

$$\frac{V_{VSEN\_REF}}{V_{OUT}} = \frac{R_{VSEND}}{R_{VSENU} + R_{VSEND}} \times \frac{N_{AUX}}{N_S} \quad (4)$$

where R_{VSEND} and R_{VSENU} are the low side and high resistors at the VSEN pin, respectively, and V_{VSEN_REF} is the internal voltage reference at 1.25V

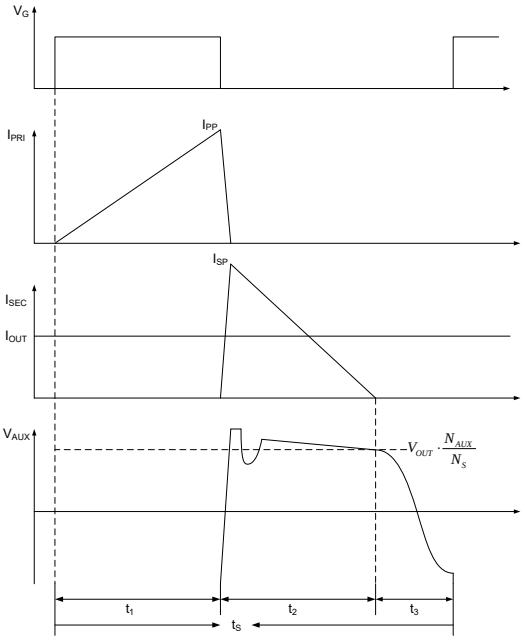


Fig.4 Auxiliary winding voltage waveforms

Output current control (CC control)

The output current is regulated by SY22817A with primary side detection technology, the maximum output current I_{OUT_LIM} can be set by

$$I_{OUT\_LIM} = \frac{k_1 \times V_{REF} \times N_{PS}}{R_S} \quad (5)$$

Where k_1 is the output current weight coefficient; V_{REF} is the internal reference voltage; R_S is the current sense resistor.

k_1 and V_{REF} are all internal constant parameters, I_{OUT_LIM} can be programmed by N_{PS} and R_S.

$$R_S = \frac{k_1 \times V_{REF} \times N_{PS}}{I_{OUT\_LIM}} \quad (6)$$

K_1 is set to 0.5

When the over current operation or short circuit operation takes place, the output current will be limited at I_{OUT_LIM}. The V-I curve is shown as Fig.5.

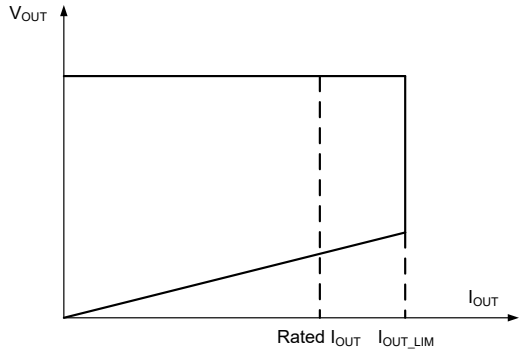


Fig.5 V-I curve

The IC provides line regulation modification function to improve line regulation performance of the output current limit.

Cable impedance compensation

SY22817A incorporates the cable impedance compensation to provide a better load regulation of output voltage at cable terminals. When the converter output load increases from no load to full load, the resulting voltage decrease on the output cables are compensated by decreasing the voltage feedback signals, which is shown by Fig. 6.

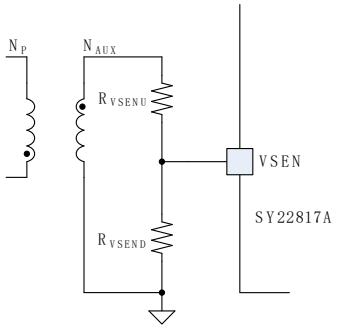


Fig. 6 Cable compensation

$$R_{VSENU} = \frac{R_{Cable}}{2k_3 \cdot R_S} \cdot \frac{N_P}{N_S} \cdot \frac{N_{AUX}}{N_S} \quad (7)$$

where k_3 is set to 50uA/V, R_S is the current sense resistor connecting to the ISEN pin.

R_{cable} is the resistance on the cable. The cable compensation effect can be adjusted by change the resistance of R_{VSENU} to achieve good load regulation of different output cables. The larger R_{VSENU}, the stronger cable compensation effect will be.

If the output current is below 10% the OCP point, the cable compensation is disabled.

Fault Protection modes

Over-temperature Protection (OTP)

SY22817A includes over-temperature protection (OTP) circuitry to prevent the overheating due to the excessive power dissipation. It will shut down the switching operation when the IC temperature exceeds the OTP threshold, about 150°C. In OTP mode, if the IC temperature decreases by approximately 20°C, the IC will resume the normal operation. For a continuous normal operation, provide an adequate cooling so that the IC temperature does not exceed the OTP threshold.

Short Circuit Protection (SCP)

When the output is shorted to ground, the output voltage is clamped to zero. The valley signal of the auxiliary winding voltage might not be detected by the VSEN pin. In this case, MOSFET cannot be turned on until maximum off time is reached. IC will shut down until VIN is below V_{VIN_OFF}, and then enter the hiccup mode.

When the output voltage is not low enough to disable the valley detection in short condition, SY22817A will operate in CC mode until VIN decreases below V_{VIN_OFF}. As shown in Fig.7, a filter resistor R_{AUX} is needed to prevent the SCP function from being affected by the voltage spikes of the auxiliary winding,

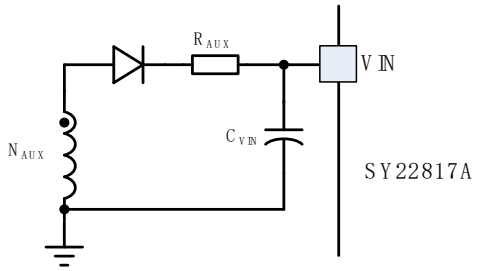


Fig. 7 Filter resistor R_{AUX}

VIN voltage OVP

When the VIN voltage exceeds V_{VIN_OVP} threshold, SY22817A will stop switching and discharge the VIN voltage. Once V_{VIN} is below V_{VIN_OFF}, the SY22817A will shut down and VIN will be charged again.

Output voltage OVP

When the VSEN pin signal exceeds V_{VSEN_OVP} threshold, reflecting an output over-voltage condition, SY22817A will stop switching and discharge the VIN voltage. Once V_{VIN} is below V_{VIN_OFF}, the IC will shut down and then enter the hiccup mode.

Output voltage UVP

When the VSEN pin signal less than V_{VSEN_UVP}, reflecting an output under-voltage condition, SY22817A will stop switching and discharge the VIN voltage.
Once V_{VIN} is below V_{VIN_OFF}, the IC will shut down and then enter the hiccup mode.

VSEN pin short protection

The SY22817A has a protection against the faults caused by shorting VSEN pin to GND. When the VSEN voltage does not reach the sense protection trigger level at the end of startup, the VSEN pin is deemed shorting to GND, and the protection is activated: the IC stops switching and discharge the VIN voltage. Once V_{VIN} decreases below V_{VIN_OFF}, the IC will shut down and then enter the hiccup mode. In order to ensure reliable detection, the pull-down resistor at VSEN pin should be larger than 2kΩ.

ISEN pin short protection

The SY22817A has a protection against the faults caused by shorting ISEN pin to GND. If ISEN short is detected at startup the IC stops switching and discharge the VIN voltage. Once V_{VIN} decreases below V_{VIN_OFF}, the IC will shut down and then enter the hiccup mode.

VSEN pin upper divider resistor disconnect protection

If the upper divider resistor disconnected lasting for 8 switching cycles, the IC will stop switching and discharge the VIN voltage. Meanwhile, limit the V_{ISEN} at V_{I_MIN}. Once V_{VIN} is below V_{VIN_OFF}, the SY22817A will shut down and VIN will be charged again.

Power Supply Design Considerations

Transformer Design Considerations (N_{PS} and L_M)

N_{PS} is limited by the electrical stress of the power MOSFET:

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - \sqrt{2} V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \quad (8)$$

where $V_{MOS\_(BR)DS}$ is the breakdown voltage of MOSFET. V_{D_F} is the forward voltage of secondary power diode; ΔV_S is the overshoot voltage clamped by RCD snubber during OFF time.

In Quasi-Resonant mode, each switching period cycle, t_S, consists of three parts: current rising time t_1, current falling time t_2 and quasi-resonant time t_3 shown in Fig.8.

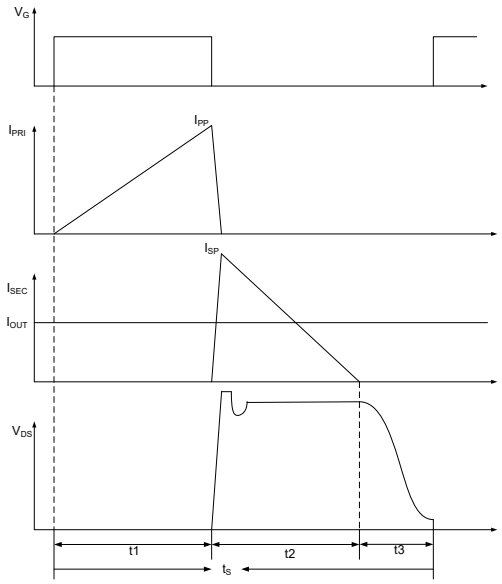


Fig.8 switching waveforms

Under the conditions of the minimum input AC RMS voltage and full load, the switching frequency is minimum while the peak current through MOSFET is maximum.

Once the minimum frequency f_{S_MIN} is set, the inductance of the transformer could be designed. The design flow is shown below:

(a) Select N_{PS}

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - \sqrt{2} V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \quad (9)$$

(b) Preset minimum frequency f_{S_MIN}

(c) Compute inductor L_M and maximum primary peak current $I_{P\_PK\_MAX}$

$$I_{P\_PK\_MAX} = \frac{2P_{OUT}}{\eta \times V_{DC\_MIN}} + \frac{2P_{OUT}}{\eta \times N_{PS} \times (V_{OUT} + V_{D\_F})} + \pi \sqrt{\frac{2P_{OUT}}{\eta} \times C_{Drain} \times f_{S\_MIN}} \quad (10)$$

$$L_M = \frac{2P_{OUT}}{\eta \times I_{P\_PK\_MAX}^2 \times f_{S\_MIN}} \quad (11)$$

where C_{Drain} is the parasitic capacitance at drain of MOSFET, η is the efficiency, and P_{OUT} is the rated full load power

(d) Compute current rising time t_1 and current falling time t_2

$$t_1 = \frac{L_M \times I_{P\_PK\_MAX}}{V_{BUS}} \quad (12)$$

$$t_2 = \frac{L_M \times I_{P\_PK\_MAX}}{N_{PS} \times (V_{OUT} + V_{D\_F})} \quad (13)$$

$$t_S = \frac{1}{f_{S\_MIN}} \quad (14)$$

(e) Compute primary maximum RMS current $I_{P\_RMS\_MAX}$ for the transformer fabrication.

$$I_{P\_RMS\_MAX} = \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \times \sqrt{\frac{t_1}{t_S}} \quad (15)$$

(f) Compute secondary maximum peak current $I_{S\_PK\_MAX}$ and RMS current $I_{S\_RMS\_MAX}$ for the transformer fabrication.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} \quad (16)$$

$$I_{S\_RMS\_MAX} = \frac{\sqrt{3}}{3} N_{PS} \times I_{P\_PK\_MAX} \times \sqrt{\frac{t_2}{t_S}} \quad (17)$$

Transformer Design Considerations

The key transformer parameters are shown below:

Necessary parameters	
Primary to Secondary Turns ratio	N_{PS}
Inductance	L_M
Primary maximum current	$I_{P\_PK\_MAX}$
Primary maximum RMS current	$I_{P\_RMS\_MAX}$
Secondary maximum RMS current	$I_{S\_RMS\_MAX}$

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area A_e.

(b) Preset the maximum magnetic flux ΔB

ΔB=0.22~0.28T

(c) Compute primary turn N_P

$$N_P = \frac{L_M \times I_{P\_PK\_MAX}}{\Delta B \times A_e} \quad (18)$$

(d) Compute secondary turn N_S

$$N_S = \frac{N_P}{N_{PS}} \quad (19)$$

(e) Compute auxiliary turn N_{AUX}

$$N_{AUX} = N_S \times \frac{V_{VIN}}{V_{OUT}} \quad (20)$$

where V_{VIN} is the working voltage of VIN pin (9V~20V is recommended).

(f) Select an appropriate wire diameter

With $I_{P\_RMS\_MAX}$ and $I_{S\_RMS\_MAX}$, select appropriate wire to achieve the current density from 4A/mm^2 to 10A/mm^2.

(g) If the window area of the core and bobbin is not enough, reselect the core style, go to **(a)** and redesign the transformer until the ideal transformer is achieved.

Mosfet Selection

Under the conditions of the maximum input voltage and full load, the voltage stress of primary power MOSFET is maximum;

$$V_{MOS\_DS\_MAX} = \sqrt{2}V_{AC\_MAX} + N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S \quad (21)$$

where V_{AC_MAX} is maximum input AC RMS voltage, N_{PS} is the primary to secondary turns ratio of the Flyback transformer and V_{OUT} is the rated output voltage.

Under the conditions of the minimum input voltage and full load, the current stress of power MOSFET is maximum.

$$I_{MOS\_PK\_MAX} = I_{P\_PK\_MAX} \quad (22)$$

$$I_{MOS\_RMS\_MAX} = I_{P\_RMS\_MAX} \quad (23)$$

Where $I_{P\_PK\_MAX}$ is maximum primary peak current.

Diode Selection

Under the conditions of the maximum input voltage and full load, the voltage stress of secondary power diode is maximum;

$$V_{D\_R\_MAX} = \frac{\sqrt{2}V_{AC\_MAX}}{N_{PS}} + V_{OUT} \quad (24)$$

where V_{AC_MAX} is maximum input AC RMS voltage, N_{PS} is the primary to secondary turns ratio of the Flyback transformer and V_{OUT} is the rated output voltage.

Under the conditions of the minimum input voltage and full load, the current stress of power diode is maximum.

$$I_{D\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} \quad (25)$$

$$I_{D\_AVG} = I_{OUT} \quad (26)$$

Where $I_{P\_PK\_MAX}$ is maximum primary peak current.

Input Capacitor C_{BUS} Selection

Generally, the input capacitor C_{BUS} is selected by

$$C_{BUS} = 2 \sim 3\mu F / W,$$

or more accurately by

$$C_{BUS} = \frac{\arcsin(1 - \frac{\Delta V_{BUS}}{\sqrt{2}V_{AC\_MIN}}) + \frac{\pi}{2}}{\pi} \times \frac{P_{OUT}}{\eta} \times \frac{1}{2f_{IN}V_{AC\_MIN}^2[1 - (1 - \frac{\Delta V_{BUS}}{\sqrt{2}V_{AC\_MIN}})^2]} \quad (27)$$

Where ΔV_{BUS} is the voltage ripple of BUS line.

RCD snubber for MOSFET selection

The power loss of the snubber P_{RCD} is evaluated as:

$$P_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{\Delta V_S} \times \frac{L_K}{L_M} \times P_{OUT} \quad (28)$$

where V_{OUT} is the output voltage, V_{D_F} is the forward voltage of the power diode, ΔV_S is the overshoot voltage clamped by RCD snubber, L_K is the leakage inductor, L_M is the inductance of the Flyback transformer and P_{OUT} is the output power.

The R_{RCD} is calculated as:

$$R_{RCD}=\frac{(N_{PS}\times(V_{OUT}+V_{D\_F})+\Delta V_S)^2}{P_{RCD}} \quad (29)$$

The C_{RCD} is calculated as:

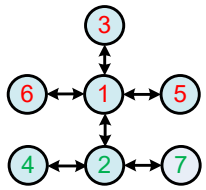
$$C_{RCD}=\frac{N_{PS}\times(V_{OUT}+V_{D\_F})+\Delta V_S}{R_{RCD}f_S\Delta V_{C\_RCD}} \quad (30)$$

Layout Considerations

A proper PCB design must follow the below guidelines:
(a) To achieve a good EMI performance and to reduce the line frequency voltage ripples, the output of the bridge rectifier should be connected to the BUS line capacitor first, then to the switching circuit.

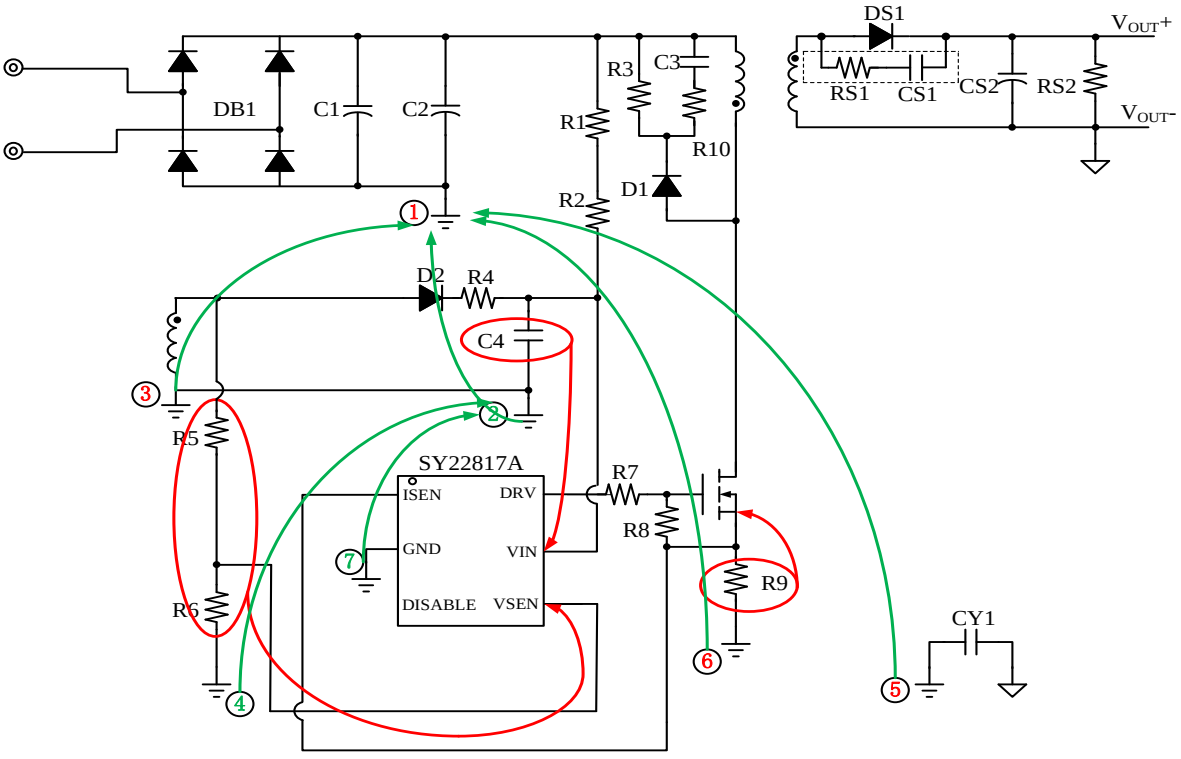
(b) The circuit loop of all switching circuit should be kept as small as possible: primary power loop, secondary loop and auxiliary power loop.

(c) The connection of primary ground is recommended as:

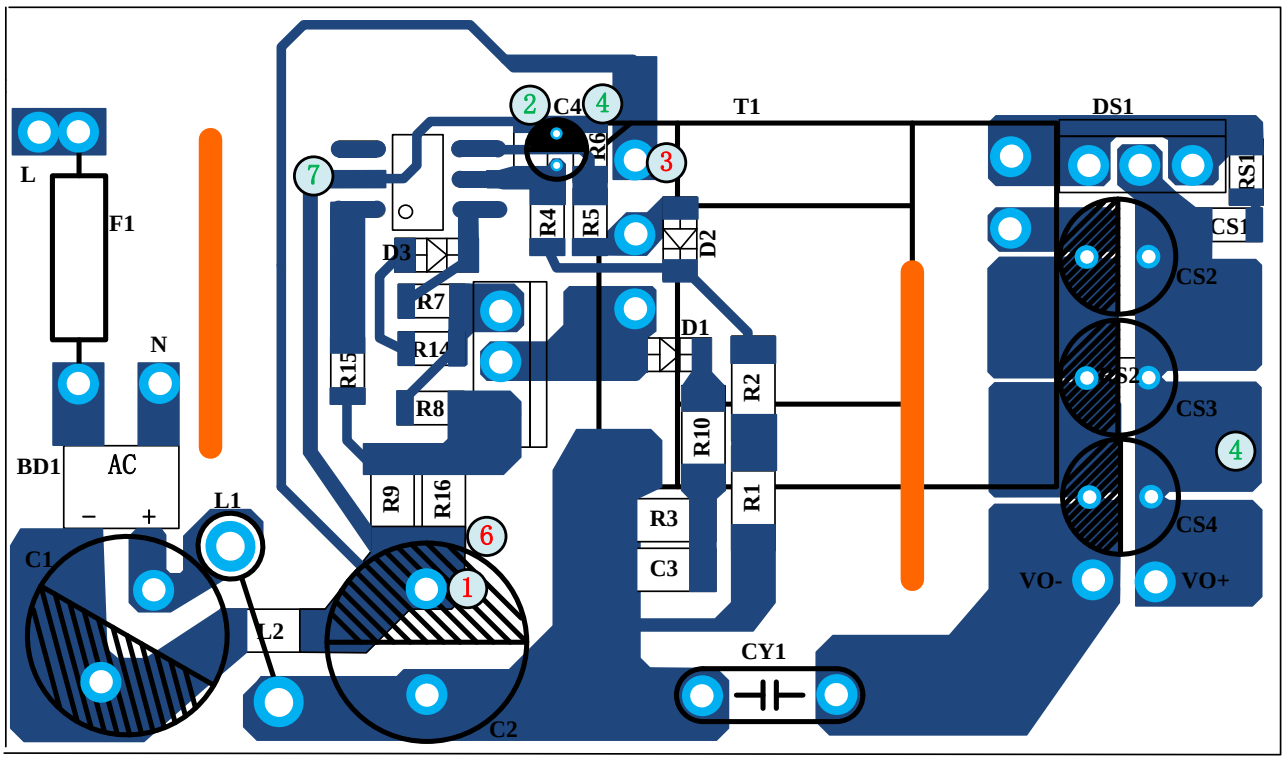


Ground ①: ground of BUS line capacitor.
Ground ②: ground of bias supply capacitor.
Ground ③: ground node of auxiliary winding.
Ground ④: ground node of divider resistor.
Ground ⑤: primary ground node of Y capacitor.
Ground ⑥: ground node of current sample resistor.
Ground ⑦: ground of IC GND.

(d) Bias supply trace should be connected to the bias supply capacitor first and then to the GND pin. The bias supply capacitor should be put right beside the IC.
(e) The loop consisting of ‘Source pin – current sense resistor – GND pin’ should be kept as small as possible.
(f) The resistor divider connected to VSEN pin is recommended to be put close to the IC.



Note：Ground node of current sample resistor must be connected to the ground of bus line capacitor



Example layout

Design Notes

1. At no load, the secondary side diode freewheeling time should be more than 2.3μs.
2. VIN voltage should be designed to higher than 11V for all conditions.
3. RCD snubber's influence:
   At no load or light load, the off-time of main switch is very long and the snubber capacitor's voltage may be discharged to a small value. When the primary switch turns on and then turns off, the primary winding current needs a longer than normal time to charge up the snubber capacitor. This might affect the feedback voltage sensing. If Imin (Imin=0.26V/Rs) is 0.1A, the snubber capacitor should be no larger than 470pF.
4. At heavy load, the peak-to-peak voltage at the Vsen pin should be less than approximately 100mVp-p after off-min time (2.1μs). This can be guaranteed by decreasing the leakage inductance and using proper RCD snubber.
5. R_{VSENU} is the upper resistor of the divider. Normally, its value is recommended between 10kΩ~65kΩ.
6. In order to ensure the CC/CV loop stability, the output capacitor should use the following formula to estimate:
   Cout= 3.7m*Iou t/Vout.
   For example, in the 5V/2A output case, Cout=3.7*2/5=1.48mF. The output capacitor can choose from 1270uF to 1680uF. On the other hand, switching frequency ripple should also be considered. If the switching frequency ripple is too large, increase the capacitance of Cout properly or use low ESR capacitor.

Design Example

A design example of typical application is shown below step by step. (Cable Test)
Note: All selected parameter (set value) need to adjust according to the practical condition.

#1. Identify design specification

Design Specification			
V_{AC}(RMS)	90V~264V	V_{OUT}	12V
I_{OUT}	2A	η	90%

#2. Transformer design (N_{PS}, L_M, N_P, N_S, N_{AUX})

(**1**)Refer to **Transformer selection (N_{PS} and L_M)**

Conditions			
V_{AC_MIN}	90V	V_{AC_MAX}	264V
ΔV_S	70V	$V_{MOS\_(BR)DS}$	600V
P_{OUT}（Max）	24W	V_{D_F}	1V
C_{Drain}	100pF	f_{S_MIN}	55kHz
ΔV_{BUS}	30% V_{BUS_MIN}		

(a) Compute turns ratio N_{PS} first

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - \sqrt{2} V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}}$$

$$= \frac{600V \times 0.9 - \sqrt{2} \times 264V - 70V}{12V + 1V}$$

$$= 7.434$$

N_{PS} is set to

$$N_{PS} = 7.25$$

(b)f_{S_MIN} is preset

$$f_{S,MIN} = 55kHz$$

(c) Compute inductor L_M and maximum primary peak current $I_{P\_PK\_MAX}$

$$I_{P\_PK\_MAX} = \frac{2P_{OUT}}{\eta \times \left(\sqrt{2} V_{AC\_MIN} - \Delta V_{BUS}\right)} + \frac{2P_{OUT}}{\eta \times N_{PS} \times (V_{OUT} + V_{D\_F})} + \pi \sqrt{\frac{2P_{OUT}}{\eta} \times C_{Drain} \times f_{S\_MIN}}$$

$$= \frac{2 \times 24W}{0.9 \times (\sqrt{2} \times 90V - 0.3 \times \sqrt{2} \times 90V)} + \frac{2 \times 24W}{0.9 \times 7.25 \times (12V + 1V)} + \pi \times \sqrt{\frac{2 \times 24W}{0.9} \times 100pF \times 55kHz}$$

$$= 1.218A$$

$$L_M = \frac{2P_{OUT}}{\eta \times I_{P\_PK\_MAX}^2 \times f_{S\_MIN}}$$
$$= \frac{2 \times 24W}{0.9 \times (1.218A)^2 \times 55kHz}$$
$$= 0.653mH$$

Set: L_M=0.65mH. (Note: the actual value generally less than the compute value)

(d) Compute current rising time t_1 and current falling time t_2

$$t_1 = \frac{L_M \times I_{P\_PK\_MAX}}{V_{BUS\_MIN}} = \frac{0.65mH \times 1.218A}{\sqrt{2} \times 90V} = 6.222\mu s$$

$$t_2 = \frac{L_M \times I_{P\_PK\_MAX}}{N_{PS} \times (V_{OUT} + V_{D\_F})} = \frac{0.65mH \times 1.218A}{7.25 \times (12V + 1V)} = 8.402\mu s$$

$$t_3 = \pi \times \sqrt{L_M \times C_{Drain}} = \pi \times \sqrt{0.65mH \times 100pF} = 0.801\mu s$$

$$t_S = t_1 + t_2 + t_3 = 6.222\mu s + 8.402\mu s + 0.801\mu s = 15.42\mu s$$

(e) Compute primary maximum RMS current $I_{P\_RMS\_MAX}$ for the transformer fabrication.

$$I_{P\_RMS\_MAX} = \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \times \sqrt{\frac{t_1}{t_S}} = \frac{\sqrt{3}}{3} \times 1.218A \times \sqrt{\frac{6.222\mu s}{15.42\mu s}} = 0.447A$$

(f) Compute secondary maximum peak current $I_{S\_PK\_MAX}$ and RMS current $I_{S\_RMS\_MAX}$ for the transformer fabrication.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} = 7.25 \times 1.218A = 8.833A$$

$$I_{S\_RMS\_MAX} = N_{PS} \times \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \times \sqrt{\frac{t_2}{t_S}} = 7.25 \times \frac{\sqrt{3}}{3} \times 1.218A \times \sqrt{\frac{8.402\mu s}{15.42\mu s}} = 3.764A$$

(2) Refer to **Transformer number of turns selection (N_P, N_S, N_{AUX})**

(a) Select the magnetic core style, identify the effective area A_e. There select EE22 thickened for compute example. Its A_e is 48.7 mm^2. The EE22 thickened can be replaced by other reasonable magnetic core style.

(b) Preset the maximum magnetic flux ΔB. Usually ΔB=0.22~0.28T .

Set: ΔB=0.28T .

(c) Compute primary turn N_P

$$N_P = \frac{L_M \times I_{P\_PK\_MAX}}{\Delta B \times A_e} = \frac{0.65*10^{-3}*1.218A}{0.28*48.7*10^{-6}} = 58.073$$

Set: N_P=58

(d) Compute secondary turn N_S

$$N_S = \frac{N_P}{N_{PS}} = \frac{58}{7.25} = 8$$

Set: N_S=8

(e) Compute auxiliary turn N_{AUX}

$$N_{AUX} = N_S \times \frac{V_{VIN}}{V_{OUT}} = 8 * \frac{15}{12} = 10$$

Set: N_{AUX}=10
Where V_{VIN} is the working voltage of VIN pin (9V~20V is recommended).

(f) Select an appropriate wire diameter

With $I_{P\_RMS\_MAX}$ and $I_{S\_RMS\_MAX}$, select appropriate wire to make sure the current density ranges from 4A/mm^2 to 10A/mm^2.

Primary wire diameter selection: current density j is set to 9 A/mm^2.

The compute primary wire cross-sectional area $S1 = \frac{I_{P\_RMS\_MAX}}{j} = \frac{0.447}{9} = 0.05\text{mm}^2$

The compute primary wire diameter $D1 = 2 * \sqrt{\frac{S1}{\pi}} = 2 * \sqrt{\frac{0.05}{\pi}} = 0.251\text{mm}$

Set: D1=0.25mm.

Secondary wire diameter selection: current density j is set to 7 A/mm^2.

The compute secondary wire cross-sectional area $S2 = \frac{I_{S\_RMS\_MAX}}{j} = \frac{3.764}{7} = 0.538\text{mm}^2$

The compute secondary wire diameter $D2\_1 = 2 * \sqrt{\frac{S2/2}{\pi}} = 2 * \sqrt{\frac{0.339/2}{\pi}} = 0.585\text{mm}$

Set: D2=D2_1*2=0.6mm*2.

Consider transformer style, the actual primary and secondary wire diameter can be adjusted for best production.

(g) If the winding area of the core and bobbin is not enough, reselect the core style, go to **(a)** and redesign the transformer until the ideal transformer is achieved.

(h) Other usually transformer inductance

	Specification	Remark
Thickened EE22 (90~264Vac,12V2A)		
Primary-Side Inductance	0.65mH±5%	40kHz,1V,25±5 ℃,Hum:65±25%
Primary-Side Leakage Inductance	50μH Maximum	Short One of Secondary Winding
N_P	58	
N_S	8	
N_A	10	
RM8 (90~264Vac,5V4A)		
Primary-Side Inductance	0.97mH±5%	40kHz,1V,25±5 ℃,Hum:65±25%
Primary-Side Leakage Inductance	50μH Maximum	Short One of Secondary Winding
N_P	64	
N_S	4	
N_A	10	

#3_1. Select primary power mos

Refer to **Mosfet selection**

Known conditions at this step			
V_{AC_MAX}	264V	N_{PS}	7.25
V_{OUT}	12V	V_{D_F}	1V
ΔV_S	70V		

Compute the voltage and the current stress of primary power mosfet

$$V_{MOS\_DS\_MAX}=\sqrt{2}V_{AC\_MAX}+N_{PS}\times(V_{OUT}+V_{D\_F})+\Delta V_S=\sqrt{2}\times 264V+7.25\times(12V+1V)+70V=537.6V$$

$$I_{MOS\_PK\_MAX}=I_{P\_K\_MAX}=1.218A$$

$$I_{MOS\_RMS\_MAX}=I_{P\_RMS\_MAX}=0.447A$$

#3_2. Select secondary power diode

Refer to **Diode selection**

Compute the voltage and the current stress of secondary power diode

$$V_{D\_R\_MAX}=\frac{\sqrt{2}V_{AC\_MAX}}{N_{PS}}+V_{OUT}=\frac{\sqrt{2}\times 264V}{7.25}+12V=63.5V$$

$$I_{D\_PK\_MAX}=N_{PS}\times I_{P\_PK\_MAX}=7.25\times 1.218A=8.833A$$

$$I_{D\_AVG}=2A$$

#4. Select the input capacitor CIN

Refer to **Input capacitor C_{BUS}**

Known conditions at this step			
V_{AC_MIN}	90V	ΔV_{BUS}	30% V_{BUS_MIN}

$$C_{BUS}=\frac{\arcsin(1-\frac{\Delta V_{BUS}}{\sqrt{2}V_{AC\_MIN}})+\frac{\pi}{2}}{\pi}\times\frac{P_{OUT}}{\eta}\times\frac{1}{2f_{IN}V_{AC\_MIN}^2[1-(1-\frac{\Delta V_{BUS}}{\sqrt{2}V_{AC\_MIN}})^2]}$$

$$=\frac{\arcsin(1-\frac{0.3\times\sqrt{2}\times 90V}{\sqrt{2}\times 90V})+\frac{\pi}{2}}{\pi}\times\frac{24W}{0.9}\times\frac{1}{2\times 50Hz\times 90V^2\times[1-(1-\frac{0.3\times\sqrt{2}\times 90V}{\sqrt{2}\times 90V})^2]}$$

$= 48.2\mu F$

Set: C_{BUS}=55 μF

Where ΔV_{BUS} is the voltage ripple of BUS line.

#5. Set VIN pin

Refer to **Start up**

Conditions			
V_{BUS_MIN}	$90V\times\sqrt{2}$	V_{BUS_MAX}	$264V\times\sqrt{2}$
I_{ST}	5μA (max)	V_{VIN_ON}	21.2V (typical)
I_{VIN_OVP}	5.2mA (typical)	t_{ST}	3s (designed by user)

(a) R_{ST} is preset

$$R_{ST}<\frac{V_{BUS\_MIN}}{I_{ST}}=\frac{90V\times\sqrt{2}}{5\mu A}=25.452M\Omega,$$

$$R_{ST}>\frac{V_{BUS\_MAX}}{I_{VIN\_OVP}}=\frac{264V\times\sqrt{2}}{5.2mA}=71.78k\Omega$$

Set R_{ST}

R_{ST}=6M

(b) Design C_{VIN}

$$C_{VIN}=\frac{(\frac{V_{BUS\_MIN}}{R_{ST}}-I_{ST})\times t_{ST}}{V_{VIN\_ON}}=\frac{(\frac{90V\times\sqrt{2}}{6M\Omega}-5\mu A)\times 3s}{21.2V}=2.24\mu F$$

Set C_{VIN}

C_{VIN} =2.2μF

#6. Set current sense resistor to achieve ideal output current

Refer to **Output current control (CC control)**

Known conditions at this step			
k_1	0.5	N_{PS}	7.25
V_{REF}	0.42V	I_{OUT_LIM}	2.4A

The current sense resistor is

$$R_S = \frac{k_1 \times V_{REF} \times N_{PS}}{I_{OUT\_LIM}} = \frac{0.5 \times 0.42V \times 7.25}{2.4A} = 0.634\Omega$$

Set R_S

Rs=0.6Ω

#7. Set VSEN pin

Refer to **Output voltage control (CV control)**

First compute R_{VSENU}

Conditions			
V_{OUT}	12V	V_{VSEN_REF}	1.25V
R_{Cable}	0.130Ω(22AWG 1.2m)	N_S	8
N_{AUX}	10	K_3	50

$$R_{VSENU} = \frac{N_P}{N_S} \cdot R_{Cable} \cdot \frac{N_{AUX}}{N_S} \cdot \frac{1}{2K_3 \cdot R_S} = 19.6k\Omega$$

Set R_{VSENU}

R_{VSENU} = 25kΩ

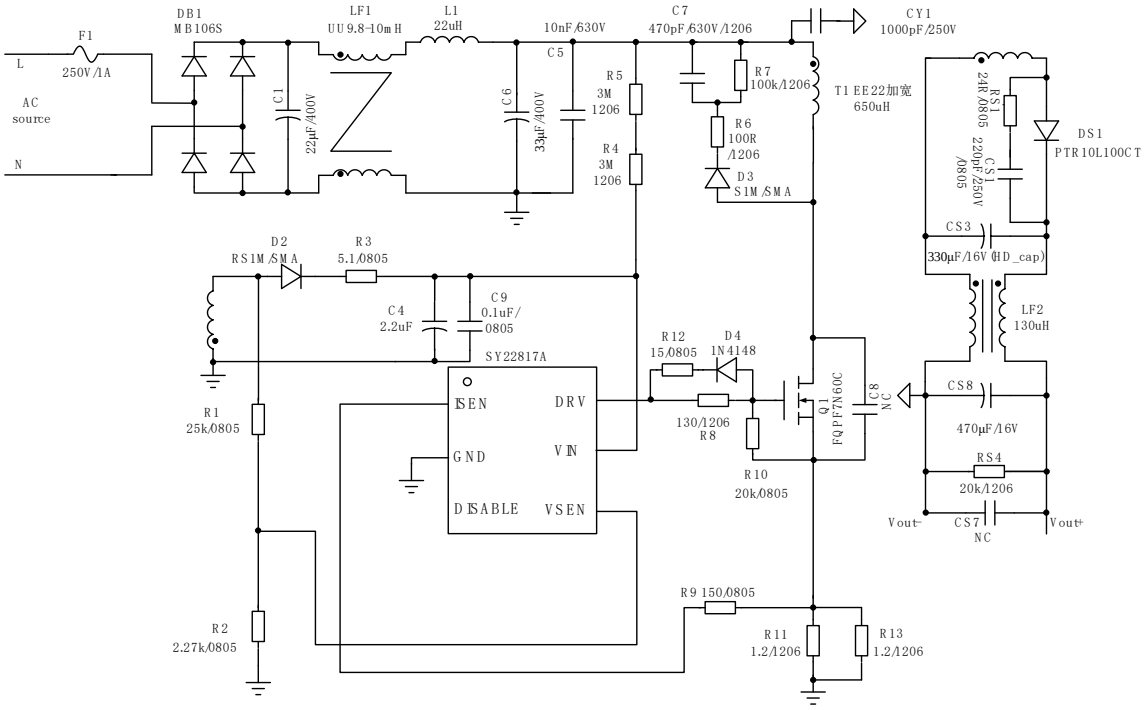
Then compute R_{VSEND}

$$R_{VSEND} = \frac{R_{VSENU}}{\frac{V_{OUT} N_{AUX}}{V_{VSEN\_REF} N_S} - 1} = \frac{25k\Omega}{(\frac{12V \times 10}{1.25V \times 8} - 1)} = 2.27k\Omega$$

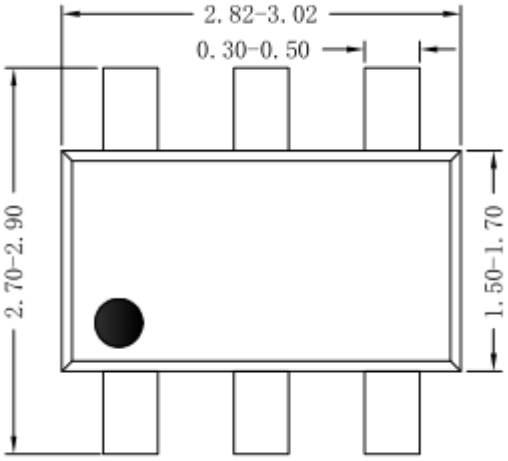
Set R_{VSEND}

R_{VSEND} = 2.27kΩ

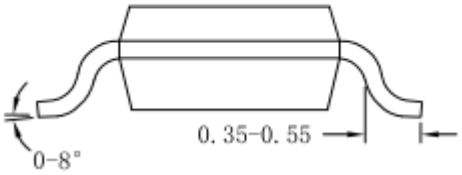
#8. Final result



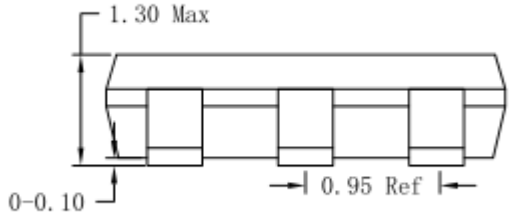
SOT23-6 Package outline & PCB layout design



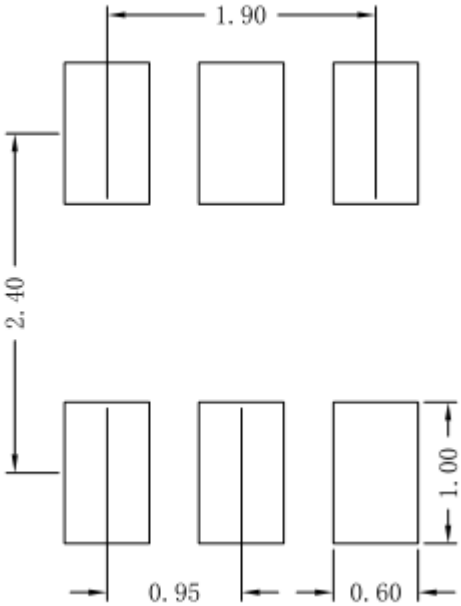
Top View



Side View



Side View

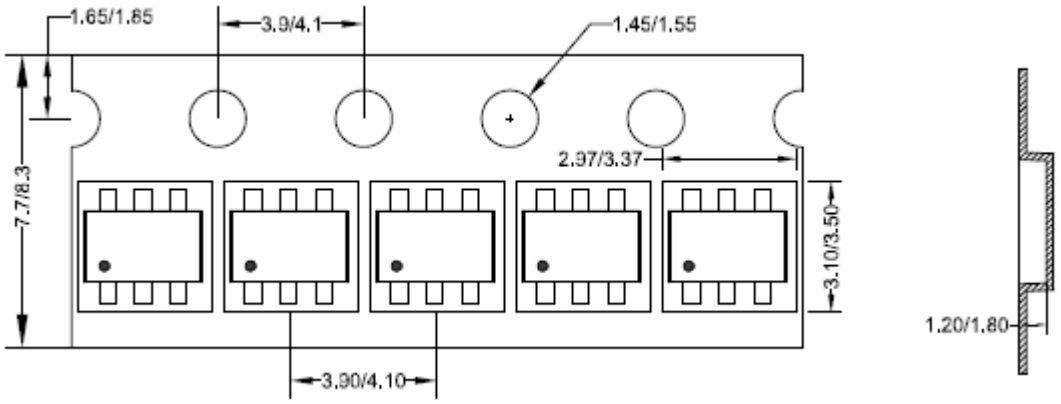


Recommended Pad Layout

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

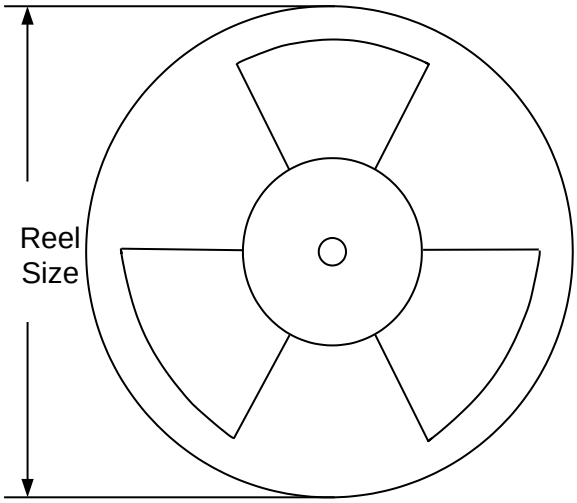
Taping & Reel Specification

1. Taping orientation for packages（SOT23-6）



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-6	8	4	7"	280	160	3000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
	Revision 0.9	Initial Release

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