SY21525B

Quad Output PMIC

General Description

The SY21525B is a high-efficiency, quad output, synchronous Buck regulator. The SY21525B features four integrated power stages and each phase has the capability to deliver up to 5A continuous output current. This flexibility allows the device to work for a wide range of applications where high-power and multi-output is needed.

The SY21525B operates over a wide input voltage range from 2.5V to 5.5V. This device adopts instant PWM control scheme to achieve fast transient response and loop stabilization. And seamless DCM/CCM transitions maximize efficiency at either heavy load or light load. During start-up and voltage change, the device controls the output slew rate to minimize output voltage overshoot and in-rush current.

The SY21525B supplies under voltage lockout, over voltage, over current and over temperature protection to ensure reliable operation of the system.

In addition to the standard interrupt, chip enable, and watchdog reset functions, the SY21525B also supports I^2C communication protocol.

The part is available in a WLCSP 2.66x3.89-54 package.

Ordering Information

SY21525 □(□□ □)

Package Code

Optional Spec Code

Ordering Number	Package type	Note
SY21525BVCS	WLCSP 2.66x3.89-54	--

Features

- 2.5V to 5.5V Wide Input Voltage Range
- Quad Output 1+1+1+1
- 5A Per Phase Output Current Capability
- Low IQ in Low Power Mode
- COT Control Achieves Fast Transient Performance
- I^2C Programmable Output Voltages from 0.45V to 2.0V
- ±0.7% System Accuracy with Remote Sensing
- Independent Dynamic Voltage Scaling (DVS) for each Output
- Support Start-up with Pre-bias Voltage
- Status Feedback with Interrupt Pin
- Reliable OTP/SCP/UVP/OVP Protection
- Compact Package: WLCSP 2.66x3.89-54

Targeted Applications

- Smart Phones, Tablets
- FPGA and ASIC Power
- Industrial MPU Power

Overview

SY21525B Typical Application

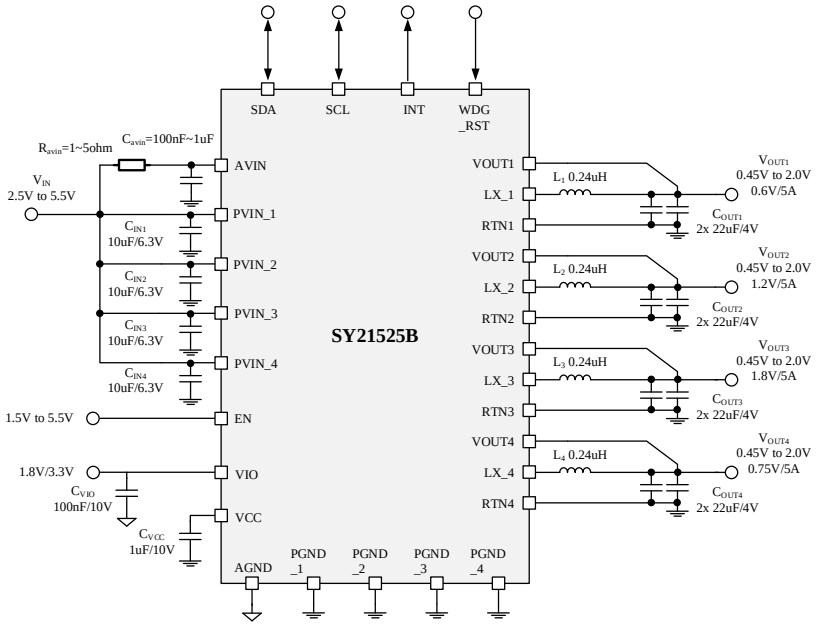


Fig.1 SY21525B: 4-phase quad output

Capacitor Selection

	Part Number	Size	Value / μF	Voltage rating / V
PVIN capacitors	GRM188D70J106MA73	0603	10	6.3
VCC capacitors	GRM155C81A105KA12	0402	1	10
VIO capacitors	GRM155R71A104MA01	0402	0.1	10
VOUT capacitors	GRM188C80G226ME15	0603	22	4

Inductor Selection

Part Number	Size	Value / nH	DCR/mΩ	ISAT / A
DFE201610E-R24M	2.0mm*1.6mm*1.2mm	240	16	6.8

Block Diagram

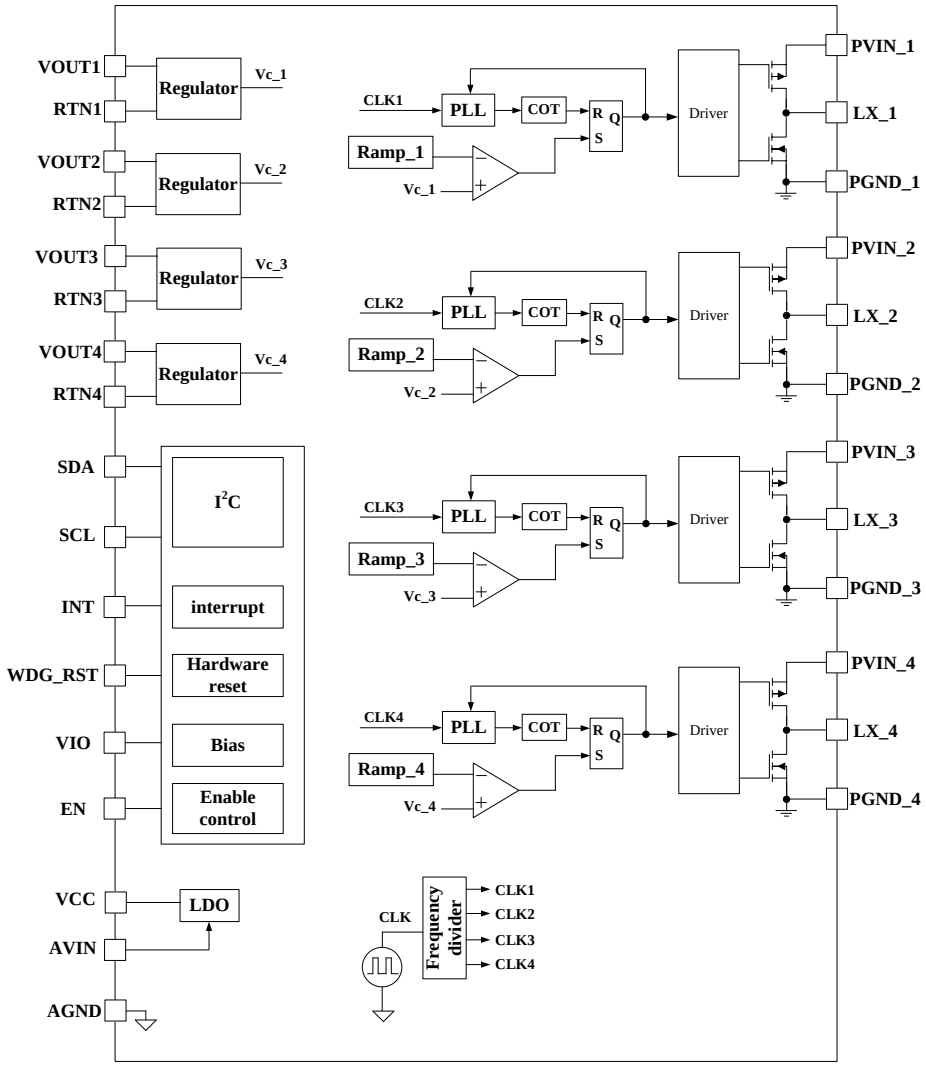


Fig.2 Block Diagram

Pin Description

Fig.3 Pin out (Top view)

Top Mark: EAM *xyz* **(**Device code: EAM, ***x=year code, y=week code, z= lot number code***)

Table. 1Pin Configuration

Pin Name	Pin Number	Type (Note 1)	Description
PVIN_3	A1, B1	PS	Power supply for BUCK3.
LX_3	A2, B2, C2	A/O	Switching node for BUCK3.
PGND_3	A3, B3, C3	G	Ground connection for BUCK3.
PGND_2	A4, B4, C4	G	Ground connection for BUCK2.

LX_2	A5, B5, C5	A/O	Switching node for BUCK2.
PVIN_2	A6, B6	PS	Power supply for BUCK2.
SCL	C1	D/I	I^2C clock.
WDG_RST	C6	D/I	Digital input, resets the bucks to default output voltage.
EN	D1	D/I	Master chip enable input.
SDA	D2	D/I/O	I^2C data.
INT	D3	D/O	Interrupt line.
NC	D4, F4, F5, F6, G6	-	Not connected.
GND	D5	G	Analog chip ground. Ensure that pin D5 has a low impedance connection to the internal ground layer.
RTN1	D6	A/I	Remote ground voltage sense for output 1.
VOUT4	E1	A/I	Remote output voltage sense for output 4.
RTN3	E2	A/I	Remote ground voltage sense for output 3.
VOUT3	E3	A/I	Remote output voltage sense for output3.
VOUT2	E4	A/I	Remote output voltage sense for output 2.
RTN2	E5	A/I	Remote ground voltage sense for output 2.
VOUT1	E6	A/I	Remote output voltage sense for output 1.
RTN4	F1	A/I	Remote ground voltage sense for output 4.
VCC	F2	A/O	Internal 2.7V LDO output, power supply for the internal analog and digital control circuits. Decouple this pin to AGND pin with at least 1μF ceramic ca-
VIO	F3	PS	IO supply voltage for digital communications. SDA/SCL should be pull up to VIO voltage with pull up resister. Normally connected to 1.8V/3.3V supply. Decouple this pin to AGND pin with at least 100nF ceramic capacitor, if VIO connect to PVIN, it is better to add RC filter to decrease input ripple voltage.
AVIN	G1	PS	Analog supply voltage, 2.5V to 5.5V. Decouple this pin to AGND pin with at least 100nF ceramic capacitor, if AVIN connect to PVIN, it is better to add RC filter to decrease input ripple voltage.
LX_4	G2, H2, J2	A/O	Switching node for BUCK4.
PGND_4	G3, H3, J3	G	Ground connection for BUCK4.
PGND_1	G4, H4, J4	G	Ground connection for BUCK1.

LX_1	G5, H5, J5	A/O	Switching node for BUCK1.
PVIN_4	H1, J1	PS	Power supply connection for BUCK4.
PVIN_1	H6, J6	PS	Power supply connection for BUCK1.

Note 1: A: Analog Pin, D: Digital Pin, G: Ground Pin, PS: Power Supply Pin, I: Input Pin, O: Output Pin

Absolute Maximum Ratings (Note 1)

PVIN, AVIN ---------- -0.3 to 6V
LX ---------- -0.3V (-2V for <40ns, -3V for <10ns) to PVIN+0.3V
VIO, EN, SCL, SDA ---------- -0.3 to AVIN+0.3V
OUT ---------- -0.3 to 3V
RTN, GND ---------- -0.3 to 0.3V
Other PINs ---------- -0.3 to 6V
Junction Temperature ---------- 150°C
Ambient Temperature ---------- -40°C to 105°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature ---------- -65°C to +150°C
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 21°C/W
θ_{JC_TOP} ---------- 2°C/W
Power Dissipation, PD @ T_A=25°C WLCSP 2.66x3.89-54 ---------- 6W
Power Dissipation, PD @ T_A=25°C WLCSP 2.66x3.89-54 ---------- 6W
Dynamic VDS for HS and LS MOSFET Tested ---------- Down to -2V<40ns
Dynamic VDS for HS and LS MOSFET Tested ---------- Down to -3V <10ns
Dynamic VDS for HS and LS MOSFET Tested ---------- Up to +7V<15ns
Dynamic VDS for HS and LS MOSFET Tested ---------- Up to +8V<5ns
ESD Rating
HBM (Human Body Model) ----------2kV
CDM (Charged Device Model) ---------- 750V
Latch-up ----------200mA

Recommended Operating Conditions (Note 3)

PVIN, AVIN ---------- 2.5V to 5.5V
VIO ---------- 1.7V to AVIN
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 105°C

Electrical Characteristics

(T_A = -40°C~125°C, AVIN/PVIN=3.7V,V_{OUT}=1V, unless otherwise specified)

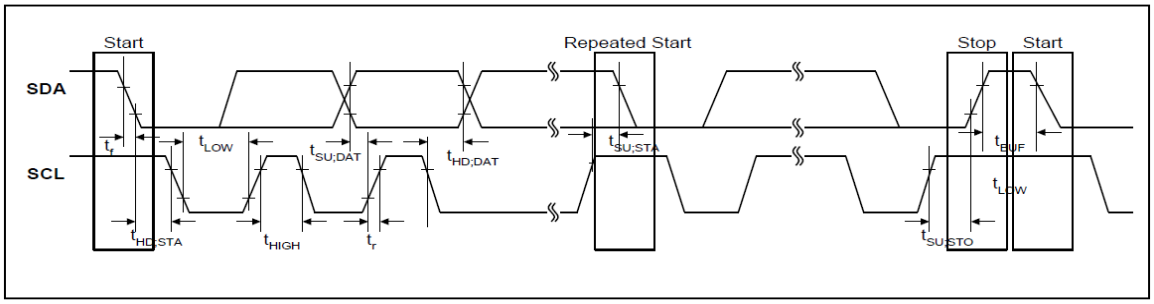
General Characteristics						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
Input Supply						
Supply Voltage	AVIN		2.5		5.5	V
Ripple Voltage	AVIN				120	mV
Ripple Voltage	VCC				12	mV
Supply Voltage	PVIN		2.5		5.5	V
AVIN Supply Current	I_Q	EN=0		1.5	2	μA
AVIN + PVIN Supply Current		EN=0		3	6	μA
AVIN + PVIN Supply Current EN=3.3V		All BUCK's EN bit=0		30		μA
		All BUCK on, no switching, DCM		290		μA
UVLO Rising Threshold	V_{UVLOR}	Rising	2.52	2.60	2.67	V
UVLO Falling Threshold	V_{UVLOF}	Falling	2.28	2.34	2.40	V
Input OVP Rising Threshold	V_{OVPR}	Rising	5.684	5.8	5.916	V
Input OVP Falling Threshold	V_{OVPF}		5.567	5.68	5.794	V
Power Stage						
VOUT Voltage Range	V_{out}		0.45		2.0	V
VOUT Step Size	V_{step}	V_{out}≤1.45V		5		mV
		V_{out}>1.45V		10		mV
VOUT Accuracy	V_{ACC}	CCM, V_{OUT}>0.6V T_A=+25℃	-0.5		0.5	%
		CCM, V_{OUT}>0.6V T_A=-10℃ to +85℃	-0.7		0.7	%
		CCM, V_{OUT}>0.6V T_A=-40℃ to +125℃	-1		1	%
		CCM,V_{OUT}<0.6V T_A=+25℃	-4		+4	mV
		CCM,V_{OUT}<0.6V T_A=-10℃ to +85℃	-5.5		+5.5	mV
		CCM,V_{OUT}<0.6V T_A=-40℃ to +125℃	-8		+8	mV
DVS Slew Rate Accuracy	V_{DVS}	Default DVS Up=16mV/μs Default DVS Down=4mV/μs	-15		15	%
Soft Start Slew Rate Accuracy	T_{SS}	Slew Rate=10mV/μs	-15		15	%
Switching Frequency	f_{sw}	T_A=25℃	1.71	1.8	1.89	MHz
		T_A=-40℃ to +125℃	1.566	1.8	2.034	MHz
Maximum Output Current (Each Phase)	I_{OUT}		5			A
Top FET Ron	$R_{ds(on)\_T}$	PVIN=3.7V		26		mΩ
Bottom FET Ron	$R_{ds(on)\_B}$	PVIN=3.7V		9		mΩ
Output Discharge Resistance	R_{DIS}	Output disabled		125		Ω

Min off time	T_{MIN_OFF}			100		ns
Output Step up Voltage when startup from 0 with nonlinear slew rate	V_{SUP}			70	120	mV
I^2C Turn on Command to output response delay time	T_{I2C_OUT}				100	μs
Protection Characteristics						
High Side Switch Current Limit	I_{PLMT}	T_A=25℃	7.7		9.3	A
		T_A=-40℃ to +125℃	6.8		10.2	A
Low Side Switch Current Limit	I_{VLMT}	T_A=25℃	5.8		7	A
		T_A=-40℃ to +125℃	4.8		8	A
Low Side Switch Negative Current Limit	I_{NLMT}	T_A=25℃	-4.8		-2.4	A
		T_A=-40℃ to +125℃	-5.4		-1.8	A
Thermal Warning Threshold	T_{WN}	Typical=+109℃	-10		10	%
Thermal Warning Hysteresis	T_{WNHYS}	Typical=+15℃	-10		10	%
Thermal Shutdown Temperature	T_{SD}	Typical=+155℃	-10		10	%
Thermal Shutdown Hysteresis	T_{SDHYS}	Typical=+15℃	-10		10	%
Output OVP Threshold	V_{TH_OVP}		116	126	136	$\%V_{SET}$
Output UVP Threshold	V_{TH_UVP}		30	40	50	$\%V_{SET}$
Output OCP Threshold	V_{TH_OCP}		70	80	90	$\%V_{SET}$
IO PINs						
EN						
Low-Level Input Voltage	V_{ENIL}				0.4	V
High-Level Input Voltage	V_{ENIH}		1.2			V
VIO PIN						
Power Supply Voltage			1.7	1.8/3.3	AVin	V
Ripple Voltage					120	mV
Supply Current					1	μA
WDG_RST						
Low-Level Input Voltage	V_{RSTIL}				0.3* VIO	V
High-Level Input Voltage	V_{RSTIH}		0.7* VIO			V
SCL, SDA						
Low-Level Input Voltage	V_{I2CIL}				0.3* VIO	V
High-Level Input Voltage	V_{I2CIH}		0.7* VIO			V
Serial Interfaces						
I^2C Frequency Capability	f_{I2C}				3.4	MHz

I^2C Timing Spec table.

Characteristics	Symbol	Units	Standard Mode		Fast Mode		High-Speed Mode	
			Min	Max	Min	Max	Min	Max

Pull-up Voltage	V_{PU}	V	1.7V to VIO					
SCL clock frequency	f_{SCL}	kHz	0 to 100kHz		0 to 400kHz		0 to 3.4MHz	
Hold time (repeated) START condition. After this period,	$t_{HD;STA}$	ms	4		0.6		0.16	
LOW period of the SCL clock	t_{LOW}	ms	4.7		1.3		0.16	
HIGH period of the SCL clock	t_{HIGH}	ms	4		0.6		0.06	
Set-up time for a repeated START condition	$t_{SU;STA}$	ms	4.7		0.6		0.16	
DATA in Hold time	$t_{HD;DI}$	ns	0	3450	0	900	0	70
DATA out Hold time	$t_{HD;DO}$	ns	12	70	12	70	12	70
Data set-up time	$t_{SU;DAT}$	ns	250		100		10	
Rise time of both SDA and SCL signals	t_r	ns		1000	5	300	5	40
Fall time of both SDA and SCL signals	t_f	ns		300	5	300	5	40
Set-up time for STOP condition	$t_{SU;STO}$	ms	4		0.6		0.16	
Bus free time between STOP and START conditions	t_{BUF}	ms	4.7		1.3			
Capacitive load for each bus line	C_b	pF		400		400		100



Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C according to JESD51-2 and PCB is built as Silergy test board. θ_{JC_TOP} is measured according to JESD51-14

Note 3: The device is not guaranteed to function outside its operating condition**.**

Feature Description

1 Output Voltage Setting and Dynamic Voltage Scaling (DVS)

1.1 Output Voltage Setting

The output voltage can be programmed by writing an 8-bit register BUCK1_DVS0CFG1. The corresponding output voltage of the DAC code is shown below. For more details, see Register “BUCK1_DVS0CFG1”.

Table. 2DAC code vs. setting Vout

DAC code	Vo/V	DAC code	Vo/V	DAC code	Vo/V	DAC code	Vo/V
0000 0000	0.45	0100 0001	0.775	1000 0010	1.1	1100 0011	1.425
0000 0001	0.455	0100 0010	0.78	1000 0011	1.105	1100 0100	1.43
0000 0010	0.46	0100 0011	0.785	1000 0100	1.11	1100 0101	1.435
0000 0011	0.465	0100 0100	0.79	1000 0101	1.115	1100 0110	1.44
0000 0100	0.47	0100 0101	0.795	1000 0110	1.12	1100 0111	1.445
0000 0101	0.475	0100 0110	0.8	1000 0111	1.125	1100 1000	1.45
0000 0110	0.48	0100 0111	0.805	1000 1000	1.13	1100 1001	1.46
0000 0111	0.485	0100 1000	0.81	1000 1001	1.135	1100 1010	1.47
0000 1000	0.49	0100 1001	0.815	1000 1010	1.14	1100 1011	1.48
0000 1001	0.495	0100 1010	0.82	1000 1011	1.145	1100 1100	1.49
0000 1010	0.5	0100 1011	0.825	1000 1100	1.15	1100 1101	1.5
0000 1011	0.505	0100 1100	0.83	1000 1101	1.155	1100 1110	1.51
0000 1100	0.51	0100 1101	0.835	1000 1110	1.16	1100 1111	1.52
0000 1101	0.515	0100 1110	0.84	1000 1111	1.165	1101 0000	1.53
0000 1110	0.52	0100 1111	0.845	1001 0000	1.17	1101 0001	1.54
0000 1111	0.525	0101 0000	0.85	1001 0001	1.175	1101 0010	1.55
0001 0000	0.53	0101 0001	0.855	1001 0010	1.18	1101 0011	1.56
0001 0001	0.535	0101 0010	0.86	1001 0011	1.185	1101 0100	1.57
0001 0010	0.54	0101 0011	0.865	1001 0100	1.19	1101 0101	1.58
0001 0011	0.545	0101 0100	0.87	1001 0101	1.195	1101 0110	1.59
0001 0100	0.55	0101 0101	0.875	1001 0110	1.2	1101 0111	1.6
0001 0101	0.555	0101 0110	0.88	1001 0111	1.205	1101 1000	1.61
0001 0110	0.56	0101 0111	0.885	1001 1000	1.21	1101 1001	1.62
0001 0111	0.565	0101 1000	0.89	1001 1001	1.215	1101 1010	1.63
0001 1000	0.57	0101 1001	0.895	1001 1010	1.22	1101 1011	1.64

0001 1001	0.575	0101 1010	0.9	1001 1011	1.225	1101 1100	1.65
0001 1010	0.58	0101 1011	0.905	1001 1100	1.23	1101 1101	1.66
0001 1011	0.585	0101 1100	0.91	1001 1101	1.235	1101 1110	1.67
0001 1100	0.59	0101 1101	0.915	1001 1110	1.24	1101 1111	1.68
0001 1101	0.595	0101 1110	0.92	1001 1111	1.245	1110 0000	1.69
0001 1110	0.6	0101 1111	0.925	1010 0000	1.25	1110 0001	1.7
0001 1111	0.605	0110 0000	0.93	1010 0001	1.255	1110 0010	1.71
0010 0000	0.61	0110 0001	0.935	1010 0010	1.26	1110 0011	1.72
0010 0001	0.615	0110 0010	0.94	1010 0011	1.265	1110 0100	1.73
0010 0010	0.62	0110 0011	0.945	1010 0100	1.27	1110 0101	1.74
0010 0011	0.625	0110 0100	0.95	1010 0101	1.275	1110 0110	1.75
0010 0100	0.63	0110 0101	0.955	1010 0110	1.28	1110 0111	1.76
0010 0101	0.635	0110 0110	0.96	1010 0111	1.285	1110 1000	1.77
0010 0110	0.64	0110 0111	0.965	1010 1000	1.29	1110 1001	1.78
0010 0111	0.645	0110 1000	0.97	1010 1001	1.295	1110 1010	1.79
0010 1000	0.65	0110 1001	0.975	1010 1010	1.3	1110 1011	1.8
0010 1001	0.655	0110 1010	0.98	1010 1011	1.305	1110 1100	1.81
0010 1010	0.66	0110 1011	0.985	1010 1100	1.31	1110 1101	1.82
0010 1011	0.665	0110 1100	0.99	1010 1101	1.315	1110 1110	1.83
0010 1100	0.67	0110 1101	0.995	1010 1110	1.32	1110 1111	1.84
0010 1101	0.675	0110 1110	1	1010 1111	1.325	1111 0000	1.85
0010 1110	0.68	0110 1111	1.005	1011 0000	1.33	1111 0001	1.86
0010 1111	0.685	0111 0000	1.01	1011 0001	1.335	1111 0010	1.87
0011 0000	0.69	0111 0001	1.015	1011 0010	1.34	1111 0011	1.88
0011 0001	0.695	0111 0010	1.02	1011 0011	1.345	1111 0100	1.89
0011 0010	0.7	0111 0011	1.025	1011 0100	1.35	1111 0101	1.9
0011 0011	0.705	0111 0100	1.03	1011 0101	1.355	1111 0110	1.91
0011 0100	0.71	0111 0101	1.035	1011 0110	1.36	1111 0111	1.92
0011 0101	0.715	0111 0110	1.04	1011 0111	1.365	1111 1000	1.93
0011 0110	0.72	0111 0111	1.045	1011 1000	1.37	1111 1001	1.94
0011 0111	0.725	0111 1000	1.05	1011 1001	1.375	1111 1010	1.95
0011 1000	0.73	0111 1001	1.055	1011 1010	1.38	1111 1011	1.96

0011 1001	0.735	0111 1010	1.06	1011 1011	1.385	1111 1100	1.97
0011 1010	0.74	0111 1011	1.065	1011 1100	1.39	1111 1101	1.98
0011 1011	0.745	0111 1100	1.07	1011 1101	1.395	1111 1110	1.99
0011 1100	0.75	0111 1101	1.075	1011 1110	1.4	1111 1111	2
0011 1101	0.755	0111 1110	1.08	1011 1111	1.405		
0011 1110	0.76	0111 1111	1.085	1100 0000	1.41		
0011 1111	0.765	1000 0000	1.09	1100 0001	1.415		
0100 0000	0.77	1000 0001	1.095	1100 0010	1.42		

1.2 DVS

The ramp up slew rate BUCKx_RSPUP[2:0] bits and the ramp down slew rate BUCKx_RSPDN[2:0] bits in the BUCKx_RSPCFG1 register set the slew rates(DVS speed) in BUCKx during normal DVS transition. For more details, see Register “BUCK1_RSPCFG”.

2 Power Sequencing

2.1 Enable Logic

There are two levels of enabling logic in SY21525B, which go down step by step:

- Global EN pin
- Software EN bit: [BUCKx_EN_DVS] in “BUCKx_DVSxCFG0” Register.

When the PVIN rise above UVLO and the global EN pin is pulled high, the I^2C is fully functional. Note that the software EN bit default value is ‘0’, each channel must be enabled by I^2C.

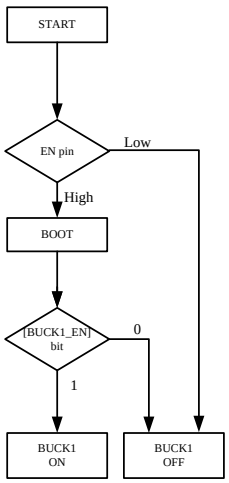


Fig.4 Enable logic (BUCK1, for example)

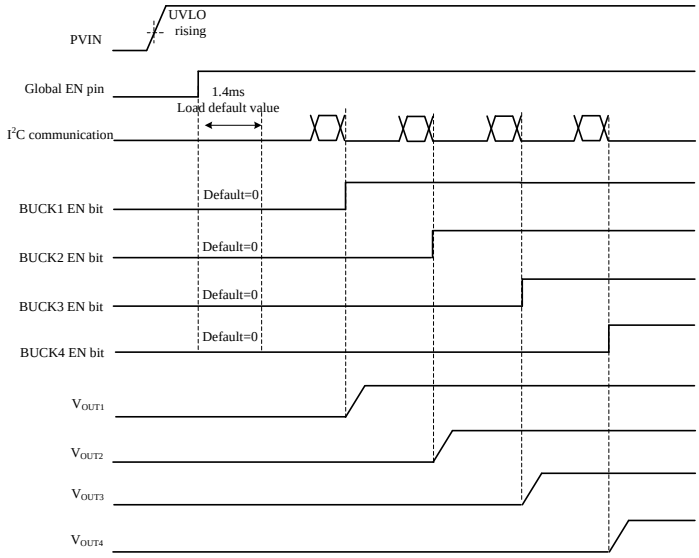


Fig.5 Power up sequencing

2.2 Power-Up Operation

When the global chip Enable (EN) pin is brought above the threshold, the device will power up its key biasing circuits, load the One-Time-Programmable (OTP) configuration registers. And when the turn-on signal is detected, the buck will enter forced CCM mode and start a power-up sequence at a specified slew rate.

The slew rate of each buck during its soft-start can be configured in Register “BUCKx_SLEWCTRL”.

2.3 Shutdown Operation

When the turn-off signal is detected, the buck will turn off the high-side switch and turn on the low side switch until the inductor current reach zero. A discharge resistor can be used to pull down the output and it can be disabled by [VOUT_DISCHARGE_EN] bit in Register “BUCKx_CFG0”.

3 PFM/PWM Operation

The converter can be either operated at forced PWM mode or automatic PFM/PWM mode through register “BUCKx_DVS0CFG0”. In forced PWM mode, the converter always operates at forced continuous conduction mode even at light load. The advantage is that the converter operates with a fixed frequency that allows simple filtering of the switching frequency for noise-sensitive applications. In this mode, the efficiency is lower compared to the PFM during light loads. In automatic PFM/PWM mode, the converter operates in regulated frequency PWM mode at moderate to heavy loads and in the PFM mode during light loads, which maintains high efficiency over a wide load current range.

4 Watchdog Debounce Time (WDOG_RST Pin)

The SY21525B implements a watchdog function which allows the output voltages to return to a safe default when communication to the processor host is lost. This is determined by monitoring the state of the WDOG_RST pin. If the falling edge is detected and the low state for a duration is greater than the debounce time (0ms typically),the output voltage setting Register (BUCKx_DVS0CFG1) and the EN bit (BUCKx_EN_DVS0)will be reset to default code. The watchdog reset function can be disabled and the debounce time is also programmable by register “IO_RSTDVS”.

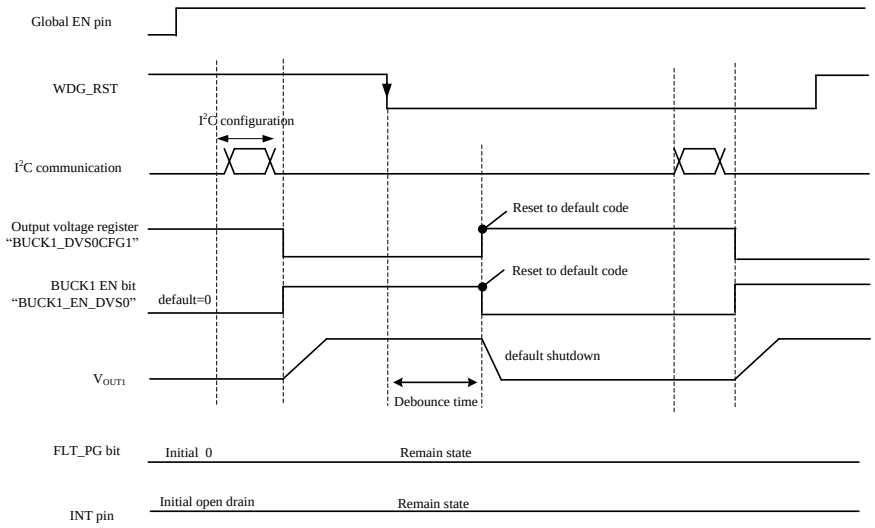


Fig.6 Watch-dog reset function

5 Protection Features

TheSY21525B has integrated over current (OC), over voltage (OV), undervoltage (UV), And over Temperature(OT) protection features.

Table. 3protection features

Protection	Threshold	Deglitch time	Operation
Thermal shut-down	Rising: 155℃ Falling: 140℃	-	Controlled by "FLT_OT_CTRL" Shutdown when temperature>155℃ Restart when temperature<140℃
Thermal warn-ing	Rising: 109℃ Falling: 94℃	-	Record to thermal warning bit.
Output OC	80%V_{set}	200μs	Hic-cup mode
Output OVP	120%V_{set}	2μs	Stop switching when VOUT>126%Vset Resume switching when VOUT<126%Vset
Output UVP	40%V_{set}	10μs	Controlled by corresponding "FLT_BUCKx_CTRL" Latch off or hiccup, default hiccup mode.
Input OVP	5.8V	4μs	Shutdown when VIN>5.8V, restart when VIN<5.68V

5.1 Over-Temperature Protection

The device provides thermal warning function and thermal shutdown protection. If the junction temperature is higher than 109℃, the thermal warning [FLT_TEMP_DIE] bit will be set to 1. The bit can be reset to 0 after I^2C read if the temperature drops below 94℃. The thermal warning function is activated once the global EN pin is pulled high.

As the temperature goes higher, the device goes into thermal shutdown when the junction temperature exceeds typically 155℃, In this mode, the HS switch and LS switch are turned off. When the junction temperature falls below typically 140℃, the buck will be re-enabled automatically.

The over-temperature protection can be disabled by Register "**FLT_OT_CTRL**".The thermal fault detection is activated once the global EN pin is pulled high.

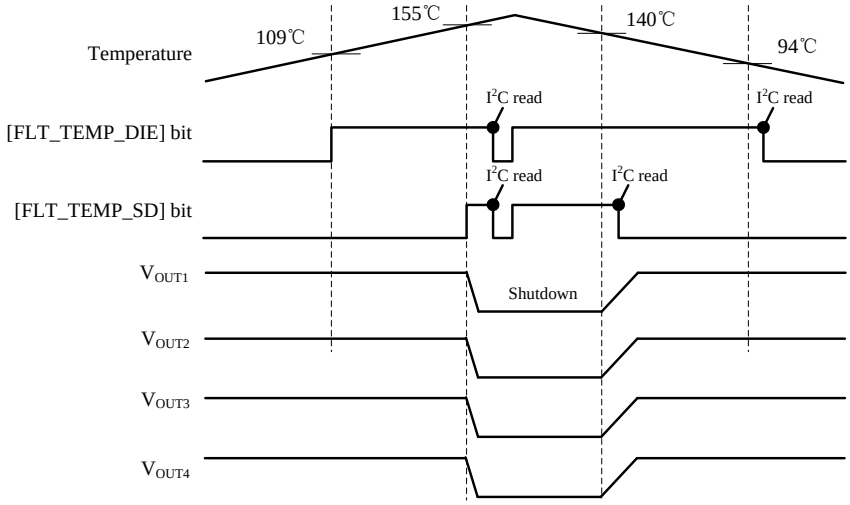


Fig.7 Thermal warning and thermal shutdown

5.2 Overcurrent Protection Mode

The device implements cycle by cycle current limit to protect the device against over current. When the current in the high side MOSFET reaches its current limit, the high side MOSFET is turned off and the low side MOSFET is turned on. The regulator continues to limit the current on a cycle-by-cycle basis. As the load current increases, the output voltage will drop. As soon as the output voltage drops below $80\%V_{SET}$ for a duration of 1ms, the buck will be turned off for 7x soft start time. The buck will then restart. If the over load condition remains the buck will be turned off for another 7x soft start time. This restart will continue until the over load condition is removed. The OC fault detection is disabled during the normal power up, shut down and DVS period.

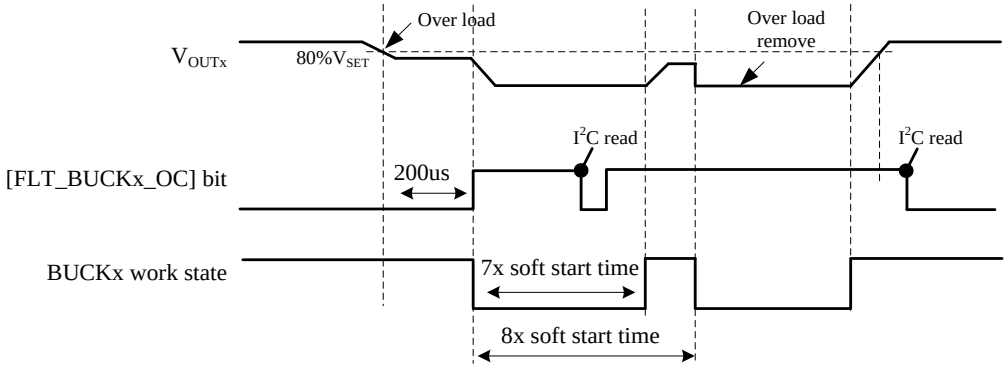


Fig.8 OCP function

5.3 Overvoltage (OV)/Undervoltage (UV) Protection

The SY21525B protects against output overvoltage and undervoltage fault conditions. When the output voltage reaches 126% V_{SET} or a duration of 10µs, the buck converter will enter no switching mode. Both high side and low side MOSFETS are turned off when zero cross is detected. The buck will resume normal operation whenthe output voltage drops below 126%V_{SET}.The OV fault detection is disabled during the normal power up, shut down and DVS period.

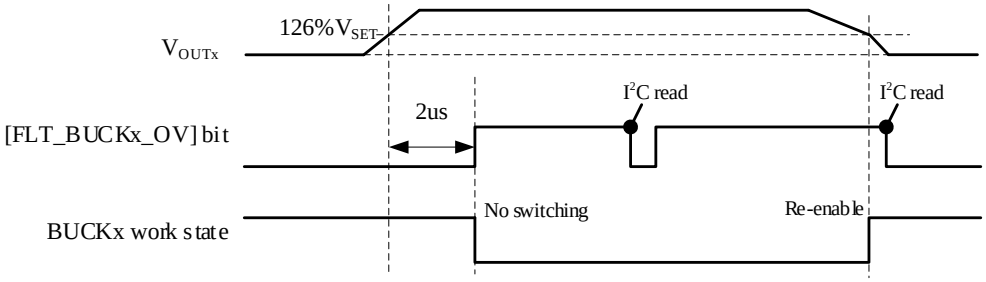
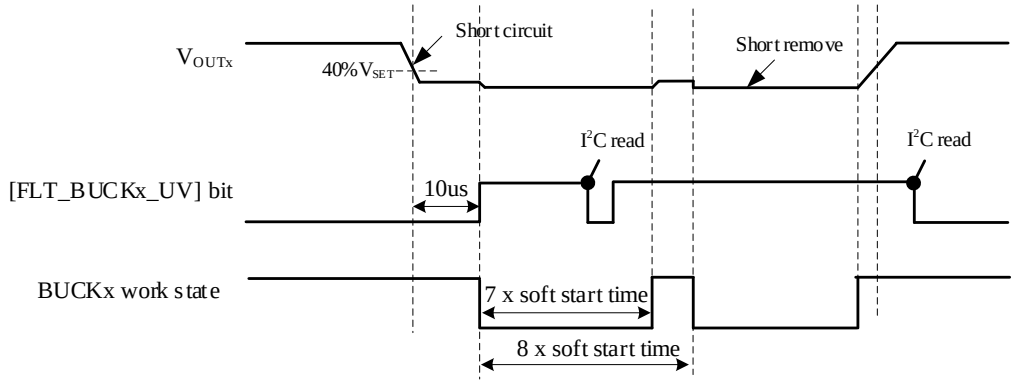
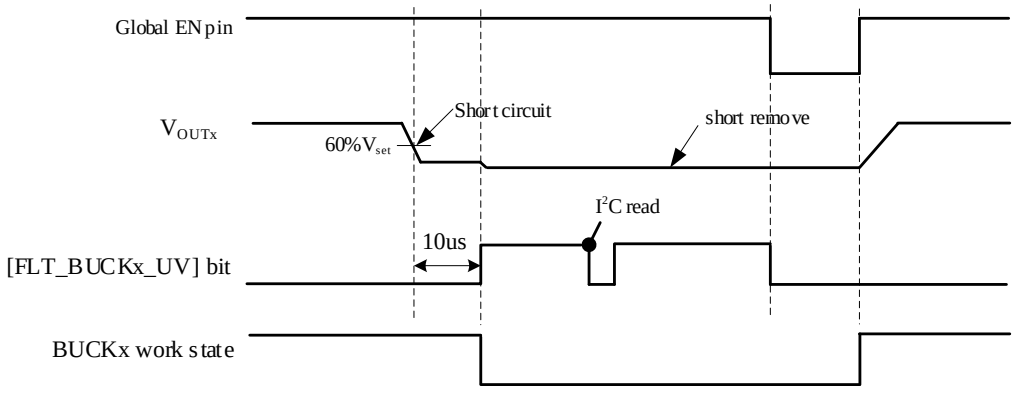


Fig.9 Output OVP function

When the output voltage drops below 60%V_{SET} for 50µs, the buck will be turned off. The device provides hiccup and latch off protection modes which is selected by register "**FLT_BUCKx_CTRL**". If latch off mode is selected, the buck will not re-enable after UV event. The state can only be cleared by recycling the PVIN/AVIN or by toggling the EN pin. When the UV hiccup mode is selected, the buck will restart after 7x soft start time off time. The UV fault detection is disabled during the normal power up, shut down and DVS period.



(a). UVP hic-cup



(b) UVP latch off

Fig.10 UVP function, hic-cup mode

5.4 Input OVP

The device provides input OVP function to protect the input from overvoltage. The input OVP detection is activated once the global EN pin is pulled high. When PVIN exceeds 5.8V, all the channels will be turned off. The OVP hysteresis is 120mV. When PVIN decreases to 5.62V, all channels will restart. The input OV fault detection is activated once the global EN pin is pulled high.

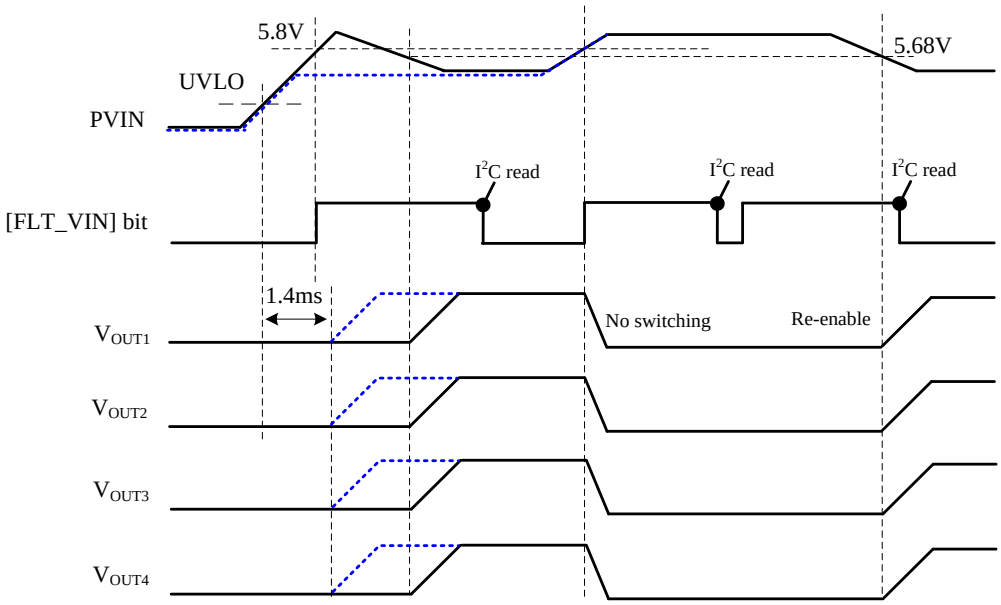


Fig.11 Input OVP

6 Interrupt Pin

The SY21525B can alert the host when a fault has occurred through an IRQ interrupt request signal with configurable masking options that is connected to a configurable interrupt (INT) pin. The interrupt pin is set as an active low, OD output internally.

When a fault occurred, the corresponding fault record bit will be set to 1 until the fault is cleared. When the fault is cleared, the corresponding fault record bit will be set to 0 after read.

When a fault occurred and the corresponding fault record is not masked, the INT pin will be pulled down to low level. And when all the fault record is cleared, the INT pin will be released to high level. Fig. shows the interrupt tree structure.

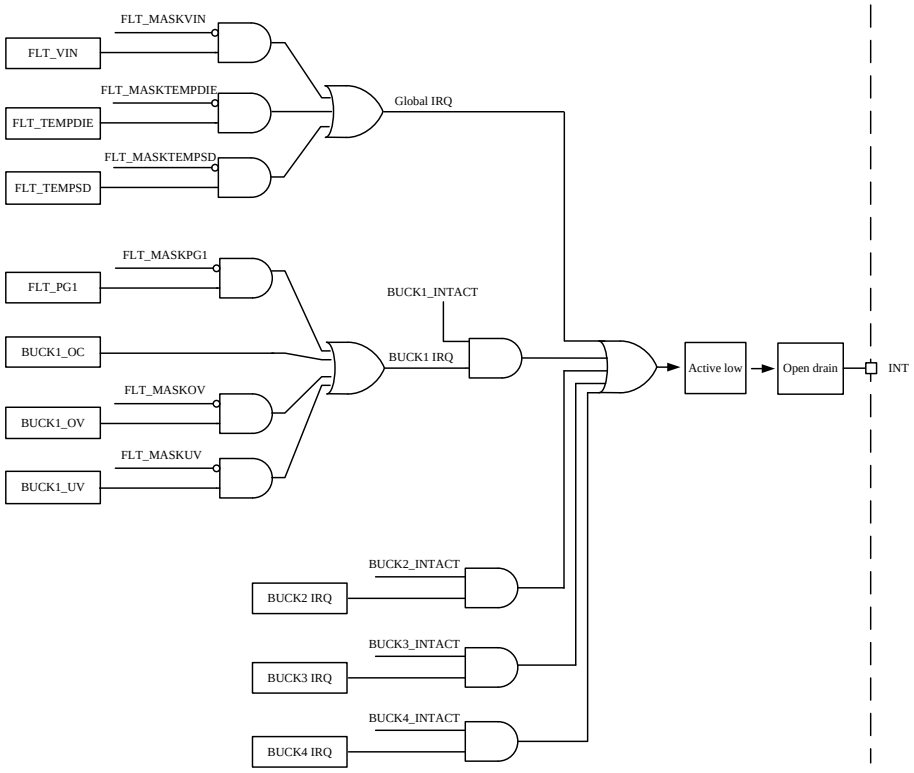


Fig.12 Interrupt tree

6.1 Input OVP Interrupt

The device provide a [FLT_VIN] bit in Register "FLT_RECORDTEMP" to indicate input OVP fault. If the input voltage is larger than OVP threshold, the bit will set to 1 and pull INT pin to low level. The bit can be reset to 0 after read if the OVP state is clear. This interrupt can be masked by [FLT_MASKVIN] bit in Register "FLT_MASKTEMP".

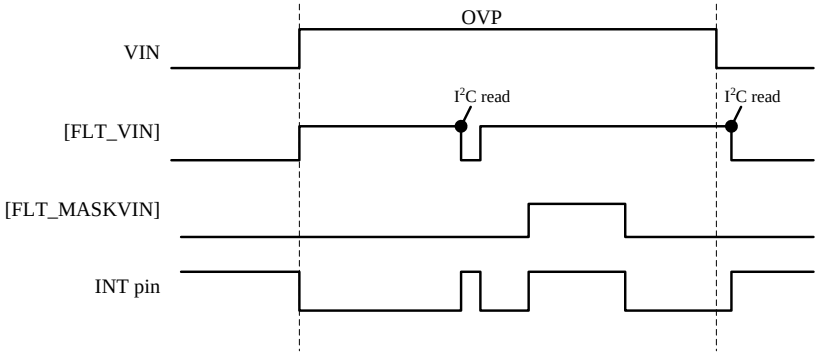


Fig.13 Input OVP interrupt function

6.2 Temperature Interrupt

The device provide a [FLT_TEMP_DIE] bit in Register "FLT_RECORDTEMP" for the warning of over-heating. If the temperature of the device is higher than 109℃, the bit will set to 1 and pull INT pin to low level. The bit can be reset to 0 after read if the temperature drops below 94℃. This interrupt can be masked by [FLT_MASKTEMP_DIE] bit in Register "FLT_MASKTEMP".

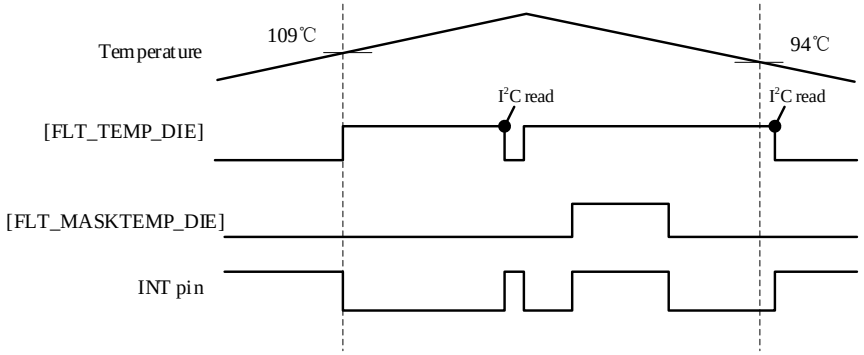


Fig.14 Thermal warning interrupt function

The device also provide a [FLT_TEMP_SD] bit in Register "FLT_RECORDTEMP" for over temperature protection. If the temperature of the device is higher than 155℃, the bit will set to 1 and pull INT pin to low level. The bit can be reset to 0 after read if the temperature drops below 140℃. This interrupt can be masked by[FLT_MASKTEMP_SD] bit in Register "FLT_MASKTEMP".

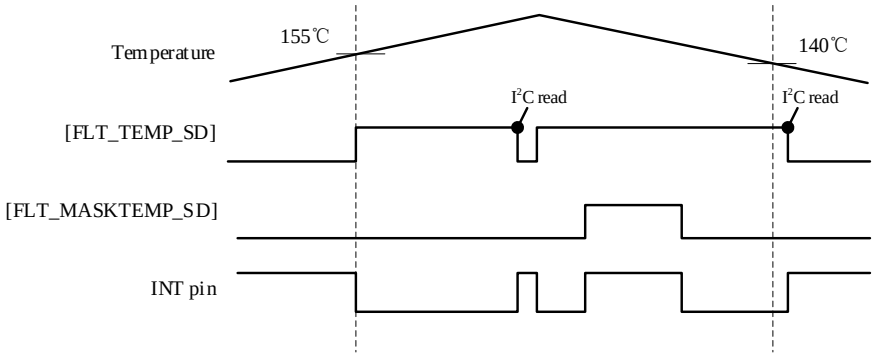


Fig.15 Thermal shutdown interrupt function

6.3 Fault Power Good Interrupt

The device provide a [FLT_PGx] bit in Register "FLT_RECORDBUCKx" to indicate power good state for each buck. If the output voltage is detected between 90%Vset and 110%Vset, the bit will set to 0, and if the output voltage is out of range, the bit will set to 1. The bit can be reset to 0 after read if the not power good state is clear. This interrupt can be masked by [FLT_MASKPGx] bit in Register "FLT_MASKBUCKx". The power good fault detection is disabled during the normal power up, shut down and DVS period.

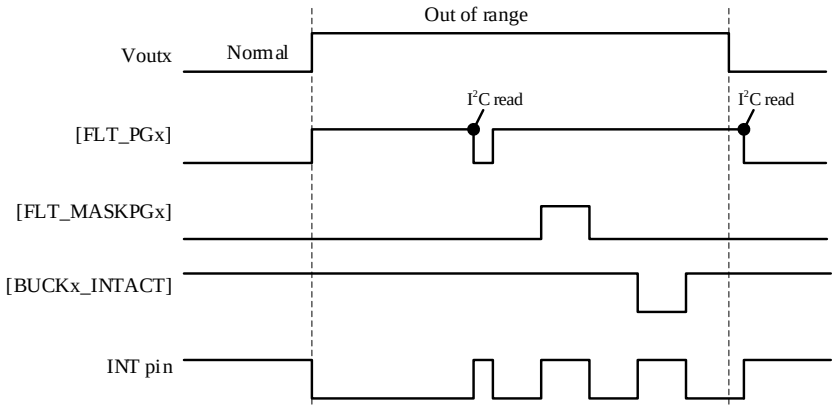


Fig.16 Fault power good interrupt function

6.4 Over Current Interrupt

The device provide a [FLT_BUCK1_OC] bit in Register “FLT_RECORDBUCKx” to indicate over current state. If the over current state is detected, the bit will set to 1. The bit can be reset to 0 after read if the fault state is clear. This interrupt can only be masked by [BUCKx_INTACT] bit in Register “FLT_MASKBUCKx”.

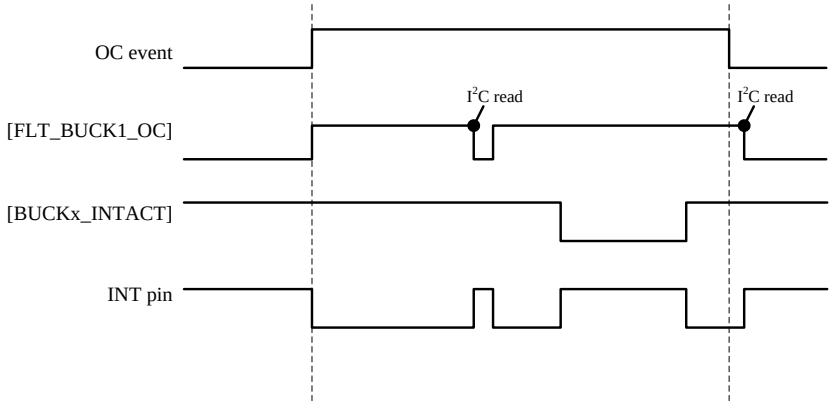


Fig.17 Input OCP interrupt function

6.5 Over Voltage Interrupt

The device provide a [FLT_BUCKx_OV] bit in Register “FLT_RECORDBUCKx” to indicate over voltage state. If the over voltage state is detected, the bit will set to 1. The bit can be reset to 0 after read if the fault state is clear. This interrupt can be masked by [FLT_BUCKx_MASKOV] bit and [BUCKx_INTACT] bit in Register “FLT_MASKBUCKx”.

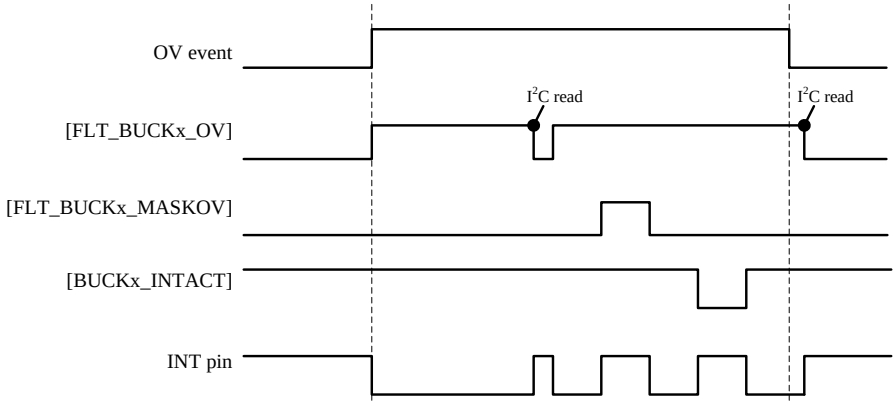


Fig.18 Input OVP interrupt function

6.6 Under Voltage Interrupt

The device provide a [FLT_BUCKx_UV] bit in Register “FLT_RECORDBUCKx” to indicate under voltage state. If the under voltage state is detected, the bit will set to 1. The bit can be reset to 0 after read if the fault state is clear. This interrupt can be masked by [FLT_BUCKx_MASKUV] bit and [BUCKx_INTACT] bit in Register “FLT_MASK-BUCKx”.

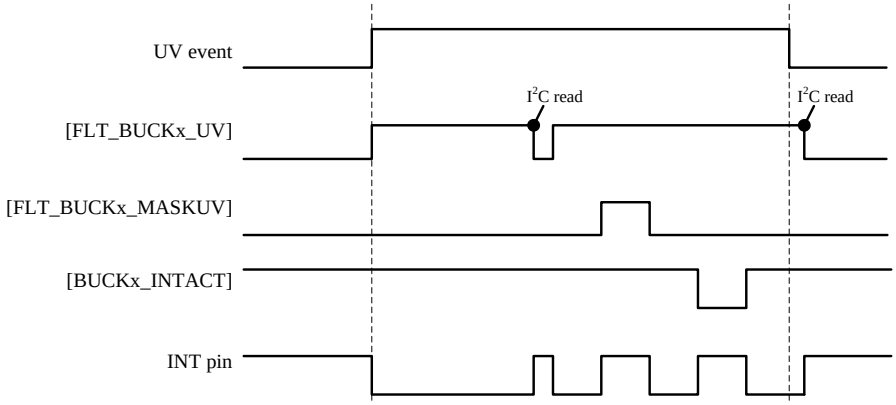


Fig.19 Input UVP interrupt function

6.7 Interrupt Condition During Power Sequencing

As The global fault detection (input OVP, thermal warning, thermal shutdown) is activated once the global EN pin is pull high. The buck fault (PG, OC, OV, UV) detection is blocked during the normal power up, shut down and DVS period.

When the buck is shut down by toggling global EN pin, the fault record Registers “FLT_RECORDTEMP” and “FLT_RECORDBUCKx” will be reset to default value.

Shutdown the buck by software EN bit will not change the fault record Registers “FLT_RECORDTEMP” and “FLT_RECORDBUCKx”.

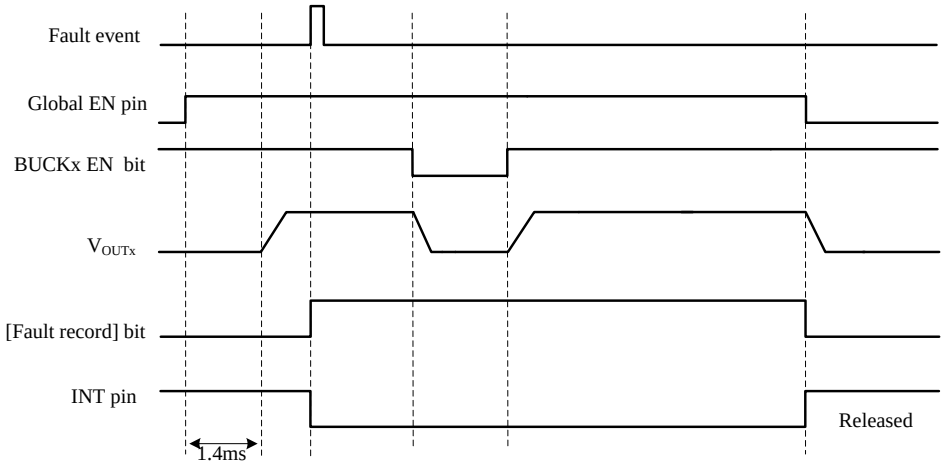


Fig.20 interrupt function during power sequencing

7 Component Selection Guide

Assume that buck work in CCM and ignore capacitor’s ESL, component selection guide is shown below.

7.1 Inductor Selection

The inductor is necessary to supply constant current to the output load while being driven by the switched input volage.

Instant-PWM operates well over a wide range of inductor values. This flexibility allows for optimization to find the best trade-off of efficiency, cost and size for a particular application. Selecting a low inductor value will help reduce size and

cost and enhance transient response, but increase peak inductor ripple current, reducing efficiency and increasing output voltage ripple. The low DC resistance (DCR) of these low value inductors may help reduce DC losses and increase efficiency. On the other hand, higher inductor values tend to have higher DCR and will slow transient response.

A reasonable compromise between size, efficiency, and transient response can be determined by selecting a ripple current (Δi_L) about 20% ~ 50% of the desired full output load current. Start calculating the approximate inductor value by selecting the input and output voltages, the operating frequency (f_S), the maximum output current (I_{omax}) and estimating Δi_L as some percentage of that current.

$$\Delta_{iL} = \frac{Vo}{f_s \cdot L} \cdot (1 - D) = \frac{Vin}{f_s \cdot L} \cdot D \cdot (1 - D)$$

$$iL_{peak} = Io + 0.5\Delta_{iL}$$

Where $D = \frac{Vo}{Vin}$.

The worst case condition is Vout=0.5V_{IN}, and $\Delta_{iL} = \frac{Vin}{4f_S \cdot L}$, $iL_{peak} = I_{omax} + \frac{Vin}{8f_S \cdot L}$.

Select an inductor with a saturation current and thermal rating in excess of iL_{peak}

If FCCM light load operation is selected, make sure the inductor value is high enough to avoid reverse current limit is been triggered just under steady state if the load current is zero.

For highest efficiency, select an inductor with a low DCR that meets the inductance, size and cost targets. Low loss ferrite materials should be considered.

7.2 Inductor Design Example

Consider a typical design for a device providing 1.65V_O at 5A from 3.3V_{IN}, operating at 2MHz and using target inductor ripple current (ΔI_L) of 40% or 2A.

$$\Delta_{iL} = \frac{1.65V}{2MHz \cdot L} \cdot \left(1 - \frac{1.65V}{3.3V}\right) < 2A$$

Conclude from above equation, L>0.206uH.

For the inductor, 0.24uH low ESR inductor is suggested.

$$\Delta_{iL} = \frac{1.65V}{2MHz \cdot 0.24uH} \cdot \left(1 - \frac{1.65V}{3.3V}\right) = 1.72A$$

$$iL_{peak} = 5A + 0.5 \times 1.72A = 5.29A$$

The resulting 1.72A ripple current is 1.72A/5A is about 34.4%, well within the 20% ~ 50% target.

Finally, select an available inductor with a saturation current higher than the resulting iL_{peak} of 5.29A.

7.3 Input Capacitor Selection

Input filter capacitors are needed to reduce the ripple voltage on the input, to filter the switched current drawn from the input supply and to reduce potential EMI. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating above the system requirements. X5R or X7R series ceramic capacitors are most often selected due to their small size, low cost, surge current capability and high RMS current ratings over a wide temperature and voltage range. However, systems that are powered by a wall adapter or other long and therefore inductive cabling may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{RMS} \approx Io \cdot \sqrt{D \cdot (1 - D)}$$

$$\Delta_{Vin} = \frac{Io}{f_s \cdot Cin} \cdot D \cdot (1 - D) + iL_{max} \cdot ESR$$

The worst case condition is Vout=0.5V_{IN}, and $\Delta_{Vin} = \frac{0.25Io}{f_s \cdot Cin}$, $I_{RMS} = 0.5Io$.

The capacitance value is less important than the RMS current rating. Take care to locate the ceramic input capacitor as close to the device IN and GND pin as possible.

For the input capacitor, one 10μF low ESR ceramic capacitors are suggested.

7.4 AVIN RC Filter Parameter Selection

The current of V_{IN} capacitor for buck is un-continuous which will generate large ripple voltage. The heavier the load, the larger the ripple voltage. So, it is necessary to add RC filter to decrease AVIN ripple voltage if AVIN connect to PVIN, especially when buck with heavy load. Proper RC filter is good for the stability of PMIC.

R/C parameter should satisfy

$$f_{cutoff} = \frac{1}{2\pi RC} < f_s$$

Generally, a R with 1~5 ohm and C with 0.1uF~1uF MLCC cap is suggested. The heavier of load, the larger of RC.

7.5 Output Capacitor Selection

Instant-PWM provides excellent performance with a wide variety of output capacitor types. Ceramic and POS types are most often selected due to their small size and low cost. Total capacitance is determined by the transient response and output voltage ripple requirements of the system.

$$\Delta_{Vo} = \Delta_{iL}(ESR + \frac{1}{8f_s \cdot C_o})$$

For the output capacitor, two 22μF low ESR ceramic capacitors are suggested.

Consider a typical application with Δ_{iL} = 1.72A using two 22μF ceramic capacitors, each with an ESR of 6mΩ for parallel total of 44μF and 3mΩ ESR, capacitor DC rating 29% at 1.65V.

$$\Delta_{Vo} = 1.72A \times \left(3m\Omega + \frac{1}{8 \times 2MHz \times 44uF \times 71\%}\right) = 8.6mV$$

7.6 Output Transient Undershoot/Overshoot

If very fast load transient must be supported, consider the effect of the output capacitor on the output transient undershoot and overshoot. Instant-PWM responds quickly to changing load conditions, however, some considerations must be needed, especially when using small ceramic capacitors which have low capacitance at low output voltages which results in insufficient stored energy for load transient. Output transient undershoot and overshoot have two causes: voltage changes caused by the ESR of the output capacitor and voltage changes caused by the output capacitance and inductor current slew rate.

ESR undershoot or overshoot may be calculated as V_{ESR}=ΔI_O×ESR. Using the ceramic capacitor example above and a fast load transient of ±4A, V_{ESR} = ±4A × 3mΩ = ±12mV.

Capacitive undershoot (load increasing) is a function of the output capacitance, the load step, the inductor value and the input-output voltage difference and the maximum duty factor. During a fast load transient, the maximum duty factor of instant-PWM is a function of t_{on} and the minimum t_{off} as the control scheme is designed to rapidly ramp the inductor current by grouping together many t_{on} pulses in this case. The maximum duty factor D_{max} may be calculated by

$$D_{max} = \frac{t_{on}}{t_{on}+t_{off,min}}$$

Given this, the capacitive undershoot may be calculated by

$$V_{undershoot} = -\frac{L \cdot \Delta I_O^2}{2C_O \cdot (V_{in,min} \cdot D_{max} - V_O)}$$

Consider a 4A load increase using the ceramic capacitor case when V_{IN} = 3.3V. At V_O = 1.65V, the result is t_{on} = 400ns, $t_{off,min}$ = 100ns, D_{max} = 400 / (400 + 100) =0.8 and capacitor DC rating 29% at 1.65V.

$$V_{undershoot} = -\frac{0.24uH \times (4A)^2}{2 \times 71\% \times 44uF \cdot (3V \times 0.8 - 1.65V)} = 82mV$$

In fact， t_{on} can be extended to longer and D_{max} larger, the load transient performance will be better than the calculated value.

Capacitive overshoot (load decreasing) is a function of the output capacitance, the inductor value and the output voltage.

$$V_{overshoot} = \frac{L \cdot \Delta I_O^2}{2C_O \cdot V_O}$$

Consider a 4A load decrease using the ceramic capacitor case above. At V_O = 1.65V the result is

$$V_{overshoot} = \frac{0.24uH \times (4A)^2}{2 \times 71\% \times 44uF \times 1.65V} = 37.2mV$$

Combine the ESR and capacitive undershoot and overshoot to calculate the total overshoot and undershoot for a given application.

8 PCB Layout Design

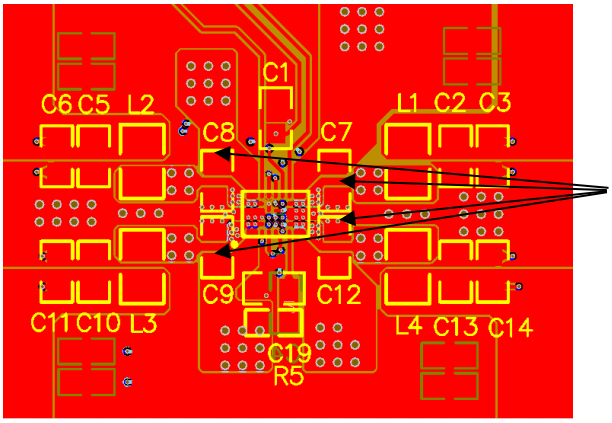
The PK77B is a high switching frequency and high current regulators and the proper PCB layout is a very important design practice to ensure a satisfactory performance. The power loop is composed of the input capacitor C_{IN}, the output inductor L, the output capacitor C_{OUT}. It is important to place power devices as close as possible to make small power loop and the connecting traces among them should be short and wide.

Place input capacitors as close as possible to the PVIN(s) and PGND(s) pins. This reduces the parasitic PCB inductance, which can adversely affect operation. The use of small low ESL capacitors at the input will improve noise immunity. The ground of the input and output capacitors should be connected as close as possible as well. In addition, a solid ground plane is helpful for a good EMI performance.

Inductor placement should also be as close to the LX(s) pins as possible. Using wide traces and reducing the length helps to improve the overall efficiency and reduce the amount of radiated EMI. It is recommended to only descend at least one layer to reduce the effective path to the inductor.

The V_{OUT}(s) and RTN lines are used to sense the output voltage and should be routed directly to the load. Keep the V_{OUT}(s) and RTN traces away from switching nodes or high-speed digital signals.

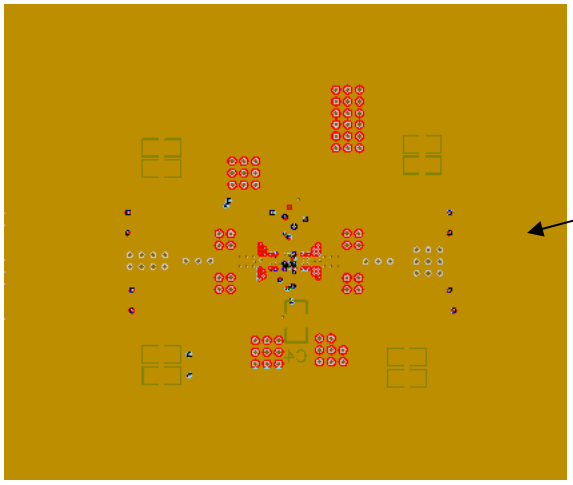
Place an AVIN filter capacitor as close as possible to the AVIN_FILT pin but away from noise sources. Always reference the GND pad of the decoupling capacitor to a quiet GND plane. And the same design practice for VCC capacitor.



Place input capacitors C7, C8, C9, and C12 as close as possible to the PVIN and PGND pins, each channel required at least a 10μF capacitor.

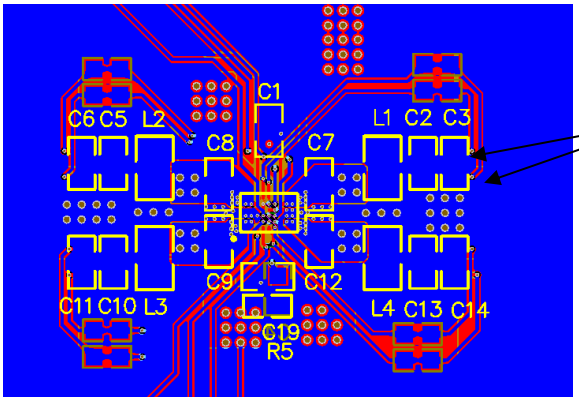
The ground of the input and output capacitors should be connected as close as possible as well.

Fig.21 Recommended PCB Layout Top Layer



Provide a solid ground plane for a low impedance path to support high current flow, which is helpful for a good EMI performance.

Fig.22 Recommended PCB Layout Ground Layer



Feedback lines are used to sense the output voltage and should be routed directly to the load. So keep the VOUT(s) and RTN traces away from switching nodes or high-speed digital signals.

Fig.23 Recommended PCB Layout Bottom Layer

I²C Communication Interface

I²C interface is a simple, bidirectional 2-wire bus protocol, consisting of the Serial Clock Control (SCL) and the Serial Data Signal (SDA). The SY21525B hosts a slave I²C interface that supports data speeds up to 3.4Mbps. SCL is an input to the SY21525B and is supplied by the controller, whereas SDA is bidirectional. The SY21525B has an open-drain output to transmit data on SDA. An external pull-up resistor must be placed on the serial data line to pull the drain output high during data transmission.

The default address of the SY21525B is set to0x1E(0011110x) by internal MTP.

1 START and STOP Conditions

The device is controlled via an I²C compatible interface. The START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition. The I²C master always generates the START and STOP conditions.

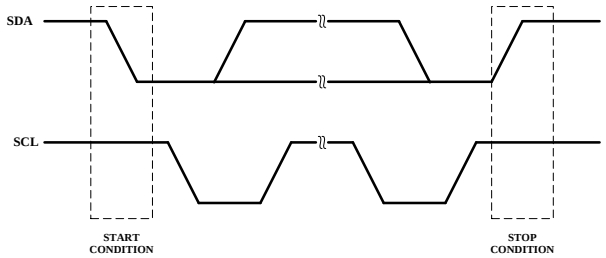


Fig.24

2 Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

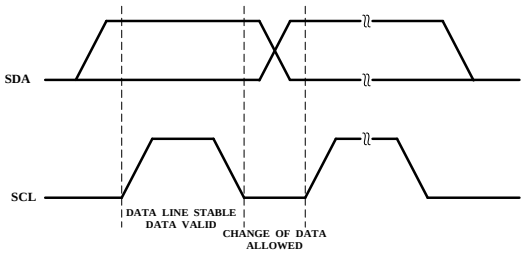


Fig.25

3 Acknowledge

Each address and data transmission uses 9-clock pulses. The ninth pulse is the acknowledge bit (ACK). After the START condition, the master sends 7-slave address bits and an $R/\overline{W}$ bit during the next 8-clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge. The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data.

4 Data Transactions

All transactions start with a control byte sent from the I^2C master device. The control byte begins with a START condition, followed by 7-bits of slave address (0011110x) for the Device, this address can be changed if necessary) followed by the 8th bit, $R/\overline{W}$ bit. The $R/\overline{W}$ bit is 0 for a write or 1 for a read. If any slave devices on the I^2C bus recognize their address, they will acknowledge by pulling the SDA line low for the last clock cycle in the control byte. If no slaves exist at that address or are not ready to communicate, the data line will be 1, indicating a Not Acknowledge condition. Once the control byte is sent, and the device acknowledges it, the 2nd byte sent by the master must be a register address byte. The register address byte tells the device which registers the master will write or read. Once the device receives a register address byte it responds with an acknowledge.

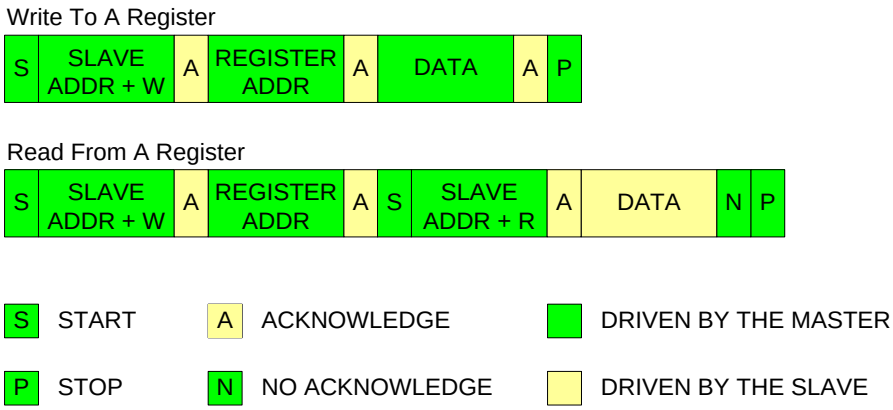


Fig.25

Register Map

1 Register Address Map

No.	Address	Register	No.	Address	Register
1	0x01	IO_CHIPNAME			
2	0x02	IO_CHIPVERSION			
3	0x0F	IO_SOFTRESET			
4	0x13	FLT_RECORDTEMP			
5	0x14	FLT_RECORDBUCK1			
6	0x15	FLT_RECORDBUCK3			
7	0x16	FLT_RECORDBUCK2			
8	0x17	FLT_RECORDBUCK4			
9	0x22	IO_I2CCFG	27	0x5B	BUCK3_RAMP
10	0x25	IO_RSTDVS	28	0x5F	BUCK3_CFG0
11	0x30	FLT_OT_CTRL	29	0x62	BUCK3_DVS0CFG1
12	0x32	FLT_MASKTEMP	30	0x63	BUCK3_DVS0CFG0
13	0x33	FLT_MASKBUCK1	31	0x6E	BUCK3_RSPCFG
14	0x34	FLT_MASKBUCK3	32	0x6F	BUCK3_SLEWCTRL
15	0x35	FLT_MASKBUCK2	33	0x75	BUCK2_RAMP
16	0x36	FLT_MASKBUCK4	34	0x79	BUCK2_CFG0
17	0x37	FLT_BUCK1_CTRL	35	0x7C	BUCK2_DVS0CFG1
18	0x38	FLT_BUCK3_CTRL	36	0x7D	BUCK2_DVS0CFG0
19	0x39	FLT_BUCK2_CTRL	37	0x88	BUCK2_RSPCFG
20	0x3A	FLT_BUCK4_CTRL	38	0x89	BUCK2_SLEWCTRL
21	0x3E	BUCK1_RAMP	39	0x8F	BUCK4_RAMP
22	0x42	BUCK1_CFG0	40	0x93	BUCK4_CFG0
23	0x48	BUCK1_DVS0CFG1	41	0x96	BUCK4_DVS0CFG1
24	0x49	BUCK1_DVS0CFG0	42	0x97	BUCK4_DVS0CFG0
25	0X54	BUCK1_RSPCFG	43	0xA2	BUCK4_RSPCFG
26	0X55	BUCK1_SLEWCTRL	44	0xA3	BUCK4_SLEWCTRL

2 Register Description

IO_CHIPNAME				
Register Address:		0x01		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:0	11111111	CHIPNAME	R	Manufacturer Identification

IO_CHIPVERSION				
Register Address:		0x02		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:0	00000000	CHIPVERSION	R	Version Number Identification

IO_SOFTRESET				
Register Address:		0x0F		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:1	0000 000	-	-	-
0	0	SOFTRESET	R/W	Reset All Registers and Reload from OTP: 0: Do nothing 1: Reset and bit cleared

FLT_RECORDTEMP				
Register Address:		0x13		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	FLT_VIN	R/W	VIN OVP Occurred Record (cleared when read) 0: No fault, less than threshold. 1: Fault, greater than threshold, send interrupt request
6:3	0000	-	-	-
2	0	FLT_TEMP_DIE	R/W	Over-Temperature Record For Die (109℃) (cleared when read) 0: No fault, less than threshold. 1: Fault, greater than threshold, send interrupt request
1	0	FLT_TEMP_SD	R/W	Over-Temperature Shutdown Record (150℃) (cleared when read) 0: No fault, less than threshold.

				1: Fault, greater than threshold, send interrupt request
0	0	-	-	-

FLT_RECORDBUCK1				
Register Address:		0x14		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	FLT_PG1	R/W	Output Power Good for BUCK1 0: 110% V_{set}> VOUT1 > 90% V_{set}. 1: VOUT1 is out of range, send interrupt request
6	0	FLT_BUCK1_OC	R/W	Overcurrent for BUCK1 (cleared when read) 0: No fault, less than threshold. 1: Fault, greater than threshold, send interrupt request
5	0	FLT_BUCK1_OV	R/W	Overvoltage for BUCK1 (cleared when read) 0: No fault, less than threshold. 1: Fault, greater than threshold, send interrupt request
4	0	FLT_BUCK1_UV	R/W	Under Voltage for BUCK1 (cleared when read) 0: No fault, less than threshold. 1: Fault, greater than threshold, send interrupt request
3-0	0000	-	-	-

FLT_RECORDBUCK3				
Register Address:		0x15		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	FLT_PG3	R/W	Refer to FLT_RECORDBUCK1
6	0	FLT_BUCK3_OC	R/W	
5	0	FLT_BUCK3_OV	R/W	
4	0	FLT_BUCK3_UV	R/W	
3-0	0000	-	-	

FLT_RECORDBUCK2				
Register Address:		0x16		

Bits	Default	Signal Name	R/W	Description
7	0	FLT_PG2	R/W	Refer to FLT_RECORDBUCK1
6	0	FLT_BUCK2_OC	R/W	
5	0	FLT_BUCK2_OV	R/W	
4	0	FLT_BUCK2_UV	R/W	
3-0	0000	-	-	

FLT_RECORDBUCK4				
Register Address:		0x17		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	FLT_PG4	R/W	Refer to FLT_RECORDBUCK1
6	0	FLT_BUCK4_OC	R/W	
5	0	FLT_BUCK4_OV	R/W	
4	0	FLT_BUCK4_UV	R/W	
3-0	0000	-	-	

IO_I2CCFG				
Register Address:		0x22		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	Reserved	R/W	
6:0	001 1110	I2C_ADDRESS	R/W	I^2C device address setting, programmed by factory.

IO_RSTDVS				
Register Address:		0x25		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	1	IO_RSTDVS _CTRL	R/W	Enable/disable Buck4 watchdog reset function 0: Disable 1: Enable
6	1		R/W	Enable/disable Buck2 watchdog reset function 0: Disable 1: Enable
5	1		R/W	Enable/disable Buck3 watchdog reset function 0: Disable 1: Enable

4	1		R/W	Enable/disable Buck1 watchdog reset function 0: Disable 1: Enable
3	0	-	R/W	
2:0	000	IO_DEBOUNCETIME	R/W	Delay before start reset DVS when WDG_RST pin is asserted 000: 0 (default) 001: 1.56 010: 3.125 011: 6.25 100: 12.5 101: 9 110: 15.25 111: 14.5

FLT_OT_CTRL				
Register Address:		0x30		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:4	0000	-	-	-
3	0	FLT_OT_CTRL	R/W	Over Temperature Shutdown Mode 0: Shutdown and auto recover 1: Do nothing
2:0	000	-	-	-

FLT_MASKTEMP				
Register Address:		0x32		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	FLT_MASKVIN	R/W	Mask IRQ for VIN OVP 0: Pass IRQ to INT pin. 1: Mask IRQ.
6:3	000	-	-	-
2	0	FLT_MASKTEMP_DIE	R/W	Mask IRQ for hot die 0: Pass IRQ to INT pin. 1: Mask IRQ
1	0	FLT_MASKTEMP_SD	R/W	Mask IRQ for thermal shutdown 0: Pass IRQ to INT pin. 1: Mask IRQ.
0	0	-	-	-

FLT_MASKBUCK1				
Register Address:		0x33		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	FLT_BUCK1_MASKPG	R/W	Mask IRQ for FLT_PG1 0: Pass IRQ to INT pin. 1: Mask IRQ.
6	0	BUCK1_INTACT	R/W	Enable or disable Buck1 INT function 0: Disable 1: Enable

				Metal change available for the default value
5	0	FLT_BUCK1 _MASKOV	R/W	Mask IRQ for FLT_BUCK1_OV 0: Pass IRQ to INT pin. 1: Mask IRQ
4	0	FLT_BUCK1 _MASKUV	R/W	Mask IRQ for FLT_BUCK1_UV 0: Pass IRQ to INT pin. 1: Mask IRQ.
3:0	0000	-	-	-

FLT_MASKBUCK3				
Register Address:		0x34		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	FLT_BUCK3 _MASKPG	R/W	Refer to FLT_MASKBUCK1
6	0	BUCK3_INTACT	R/W	
5	0	FLT_BUCK3 _MASKOV	R/W	
4	0	FLT_BUCK3 _MASKUV	R/W	
3:0	0000	-	-	

FLT_MASKBUCK2				
Register Address:		0x35		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	FLT_BUCK2 _MASKPG	R/W	Refer to FLT_MASKBUCK1
6	0	BUCK2_INTACT	R/W	
5	0	FLT_BUCK2 _MASKOV	R/W	
4	0	FLT_BUCK2 _MASKUV	R/W	
3:0	0000	-	-	

FLT_MASKBUCK4				
Register Address:		0x36		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	FLT_BUCK4_MA SKPG	R/W	Refer to FLT_MASKBUCK1
6	0	BUCK4_INTACT	R/W	
5	0	FLT_BUCK4_MA SKOV	R/W	
4	0	FLT_BUCK4_MA SKUV	R/W	
3:0	0000	-	-	

FLT_BUCK1_CTRL				
Register Address:		0x37		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:4	0000	-	-	-
3	1	FLT_BUCK1_CT RL	R/W	Protection Mode For UV 0: UV Shutdown and latch off 1: UV Hic-cup

2:0	000	-	-	-

FLT_BUCK3_CTRL				
Register Address:		0x38		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:4	0000	-	-	Refer to FLT_BUCK1_CTRL
3	1	FLT_BUCK3_CTRL	R/W	
2:0	000	-	-	

FLT_BUCK2_CTRL				
Register Address:		0x39		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:4	0000	-	-	Refer to FLT_BUCK1_CTRL
3	1	FLT_BUCK2_CTRL	R/W	
2:0	000	-	-	

FLT_BUCK4_CTRL				
Register Address:		0x3A		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:4	0000	-	-	Refer to FLT_BUCK1_CTRL
3	1	FLT_BUCK4_CTRL	R/W	
2:0	000	-	-	

BUCK1_RAMP				
Register Address:		0x3E		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	-	-	-
6	1	FCCM_DVS_UP	R/W	Work mode when DVS up 0: Controlled by WORK_MODE bit 1: Forced PWM
5:3	00 0	-	-	-
2	1	FCCM_DVS_DN	R/W	Work mode when DVS down 0: Controlled by WORK_MODE bit 1: Forced PWM
1:0	00	-	-	-

BUCK1_CFG0				
Register Address:		0x42		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:1	0000 000	-	-	-
0	1	VOUT_DISCHARGE_EN	R/W	Enable Discharge Resistor When Shut Down 0:.Disable 1: Enable

BUCK1_DVS0CFG1				
Register Address:		0x48		
Bits	**Default**	**Signal Name**	**R/W**	**Description**

7:0	0x1E	BUCK1_DVS0	R/W	8-bit DAC[7:0] value to generate VOUT for DVS Configuration 0.

DAC	Vo/V	DAC	Vo/V
00000000	0.450	1100 1001	1.46
00000001	0.455	1100 1010	1.47
…	…	…	…
11000111	1.445	1111 1110	1.99
11001000	1.450	11111111	2.00

BUCK1_DVS0CFG0				
Register Address:		0x49		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:6	00	-	-	-
5	1	WORK_MODE	R/W	BUCK1 work mode 0: Automatic PFM/PWM 1:Forced PWM
4:1	0000	-	-	-
0	0	BUCK1_EN_DVS	R/W	Enable Buck1 0: Disable, V_{OUT1}=0 1: Enable

BUCK1_RSPCFG				
Register Address:		0x54		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	-	-	-
6:4	001	BUCK1_RSPUP	R/W	

	Ramp up speed mV/μs
001	16
011	8
100	4
101	2
110	1
111	0.5

3	0	-	-	-
2:0	100	BUCK1_RSPDN	R/W	

	Ramp down speed mV/μs
001	16
011	8
100	4
101	2
110	1
111	0.5

BUCK1_SLEWCTRL				
Register Address:		0x55		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:6	00	-	-	-
5:4	00	BUCK1_POWERUP	R/W	

	Power up speed mV/μs
00	10
01	5
10	2.5
11	1.25

3:0	0000	-	-	-

BUCK3_RAMP				
Register Address:		0x5B		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	-	-	-
6	1	FCCM_DVS_UP	R/W	Work mode when DVS up 0: Controlled by WORK_MODE bit 1: Forced PWM
5:3	00 0	-	-	-
2	1	FCCM_DVS_DN	R/W	Work mode when DVS down 0: Controlled by WORK_MODE bit 1: Forced PWM
1:0	00	-	-	-

BUCK3_CFG0				
Register Address:		0x5F		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:1	0000 000	-	-	-
0	1	VOUT_DISCHARGE_EN	R/W	Enable Discharge Resistor When Shut Down 0:.Disable 1: Enable

BUCK3_DVS0CFG1				
Register Address:		0x62		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:0	0xEB	BUCK3_DVS0	R/W	8-bit DAC[7:0] value to generate VOUT for DVS Configuration 0.

DAC	Vo/V	DAC	Vo/V
00000000	0.450	1100 1001	1.46
00000001	0.455	1100 1010	1.47
…	…	…	…
11000111	1.445	1111 1110	1.99
11001000	1.450	11111111	2.00

BUCK3_DVS0CFG0				
Register Address:		0x63		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:6	00	-	-	-
5	1	WORK_MODE	R/W	Buck3work mode 0: Automatic PFM/PWM 1: Forced PWM
4:1	0000	-	-	-
0	0	BUCK3_EN_DVS	R/W	Enable Buck3 0: Disable 1: Enable

BUCK3_RSPCFG				
Register Address:		0x6E		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	-	-	-
6:4	001	BUCK3_RSPUP	R/W	Ramp up speed mV/μs

				001 16 011 8 100 4 101 2 110 1 111 0.5
3	0	-	-	-
2:0	100	BUCK3_RSPDN	R/W	Ramp down speed mV/μs 001 16 011 8 100 4 101 2 110 1 111 0.5

BUCK3_SLEWCTRL				
Register Address:		0x6F		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:6	00	-	-	-
5:4	00	BUCK3_POWERUP	R/W	Power up speed mV/μs 00 10 01 5 10 2.5 11 1.25
3:0	0000	-	-	-

BUCK2_RAMP				
Register Address:		0x75		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	-	-	-
6	1	FCCM_DVS_UP	R/W	Work mode when DVS up 0: Controlled by WORK_MODE bit 1: Forced PWM
5:3	00 0	-	-	-
2	1	FCCM_DVS_DN	R/W	Work mode when DVS down 0: Controlled by WORK_MODE bit 1: Forced PWM
1:0	00	-	-	-

BUCK2_CFG0				
Register Address:		0x79		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:1	0000 000	-	-	-
0	1	VOUT_DISCHARGE_EN	R/W	Enable Discharge Resistor When Shut Down 0:.Disable 1: Enable

BUCK2_DVS0CFG1				
Register Address:		0x7C		
Bits	**Default**	**Signal Name**	**R/W**	**Description**

<table>
<tr><td>7:0</td><td>0x96</td><td>BUCK2_DVS0</td><td>R/W</td><td>8-bit DAC[7:0] value to generate VOUT forDVS Configuration 0.
<table>
<tr><td>DAC</td><td>Vo/V</td><td>DAC</td><td>Vo/V</td></tr>
<tr><td>00000000</td><td>0.450</td><td>1100 1001</td><td>1.46</td></tr>
<tr><td>00000001</td><td>0.455</td><td>1100 1010</td><td>1.47</td></tr>
<tr><td>…</td><td>…</td><td>…</td><td>…</td></tr>
<tr><td>11000111</td><td>1.445</td><td>1111 1110</td><td>1.99</td></tr>
<tr><td>11001000</td><td>1.450</td><td>11111111</td><td>2.00</td></tr>
</table></td></tr>
</table>

BUCK2_DVS0CFG0				
Register Address:		0x7D		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:6	00	-	-	-
5	1	WORK_MODE	R/W	Buck2 work mode 0: Automatic PFM/PWM 1: Forced PWM
4:1	0000	-	-	-
0	0	BUCK2_EN_DVS	R/W	Enable Buck2 0: Disable 1: Enable

BUCK2_RSPCFG				
Register Address:		0x88		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	-	-	-
6:4	001	BUCK2_RSPUP	R/W	001: 16 011: 8 100: 4 101: 2 110: 1 111: 0.5
3	0	-	-	-
2:0	100	BUCK2_RSPDN	R/W	001: 16 011: 8 100: 4 101: 2 110: 1 111: 0.5

BUCK2_SLEWCTRL				
Register Address:		0x89		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:6	00	-	-	-
5:4	00	BUCK2_POWERUP	R/W	00: 10 01: 5 10: 2.5 11: 1.25
3:0	0000	-	-	-

BUCK4_RAMP				
Register Address:		0x8F		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	-	-	-
6	1	FCCM_DVS_UP	R/W	Work mode when DVS up 0: Controlled by WORK_MODE bit 1: Forced PWM
5:3	00 0	-	-	-
2	1	FCCM_DVS_DN	R/W	Work mode when DVS down 0: Controlled by WORK_MODE bit 1: Forced PWM
1:0	00	-	-	-

BUCK4_CFG0				
Register Address:		0x93		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:1	0000 000	-	-	-
0	1	VOUT_DISCHARGE_EN	R/W	Enable Discharge Resistor When Shut Down 0: Disable 1: Enable

BUCK4_DVS0CFG1				
Register Address:		0x96		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:0	0x3C	BUCK4_DVS0	R/W	8-bit DAC [7:0] value to generate VOUT for DVS Configuration 0.

DAC	Vo/V	DAC	Vo/V
00000000	0.450	1100 1001	1.46
00000001	0.455	1100 1010	1.47
…	…	…	…
11000111	1.445	1111 1110	1.99
11001000	1.450	11111111	2.00

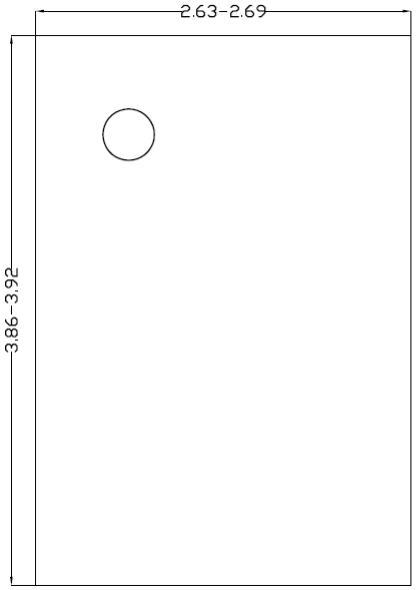
BUCK4_DVS0CFG0				
Register Address:		0x97		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:6	00	-	-	-
5	1	WORK_MODE	R/W	Buck4 work mode 0: Automatic PFM/PWM 1: Forced PWM
4:1	0000	-	-	-
0	0	BUCK4_EN_DVS	R/W	Enable Buck4 0: Disable 1: Enable

BUCK4_RSPCFG				
Register Address:		0xA2		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	-	-	-

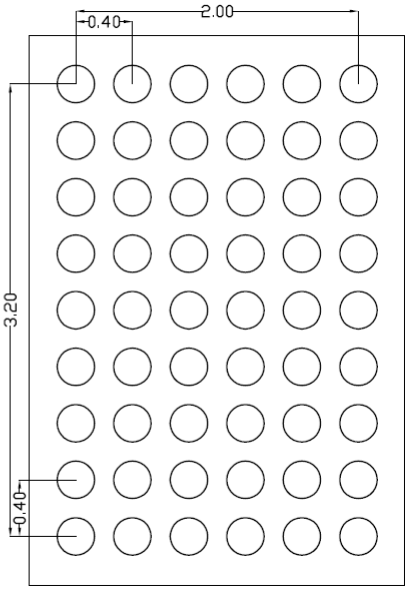
6:4	001	BUCK4_RSPUP	R/W		DVS up speed mV/μs
				001	16
				011	8
				100	4
				101	2
				110	1
				111	0.5
3	0	-	-	-	
2:0	100	BUCK4_RSPDN	R/W		DVS down speed mV/μs
				001	16
				011	8
				100	4
				101	2
				110	1
				111	0.5

BUCK4_SLEWCTRL				
Register Address:		0xA3		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:6	00	-	-	-
5:4	00	BUCK4_POWERUP	R/W	Power up slew rate
				00 10 mV/μs
				01 5 mV/μs
				10 2.5 mV/μs
				11 1.25 mV/μs
3:0	0000	-	-	-

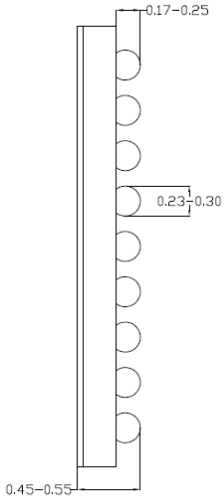
CSP2.66x3.89-54 Package Outline Drawing



Top view



Bottom view



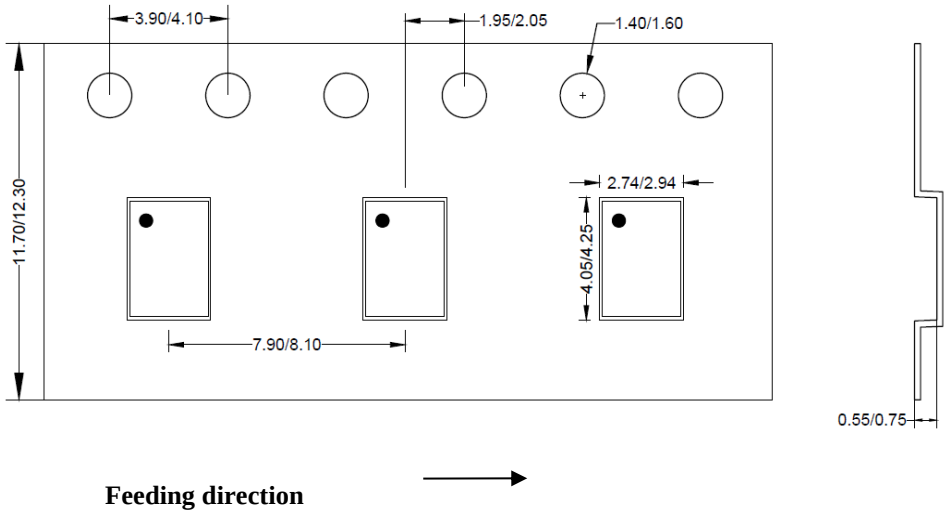
Side view

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

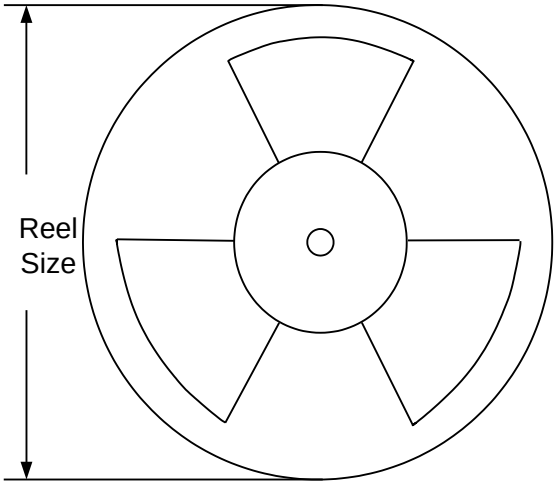
Taping & Reel Specification

1. Taping orientation

CSP2.66x3.89



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
CSP2.66x3.89	12	8	13"	400	400	5000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Mar. 16, 2023	Revision 0.9	Initial Release.
Apr. 10, 2023	Revision 0.9A	1. Add support start-up with pre-bias voltage. 2. Data out hold time min 12ns. 3. Add the description about AVIN RC filter. 4. Add the LC selection guide. 5. Add both 1.8V and 3.3V can be connected to VIO.
Jul. 17, 2025	Revision 1.0	Production release, no change.

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