SY2A29117

High Efficiency, 15A Synchronous Boost Regulator

General Description

The SY2A29117 develops a high efficiency, high power density synchronous Boost regulator. The device operates over a wide input voltage range from 1.2V to 16V with 15A switch current capability. The SY2A29117 adopts adaptive constant off time peak current control. The switching frequency is 400kHz.

The SY2A29117 has low shutdown current to extend the battery life time. Other features include programmable peak current limitation, programmable soft-start, output over voltage protection etc.

The SY2A29117 is available in compact QFN3x4-15 package.

Ordering Information

SY2A29117□(□□□)

Package Code

Optional Spec Code

Ordering Number	Package type	Note
SY2A29117VPA	QFN3x4-15	----

Features

- Wide Input Range:
  - 2.7V to 16V Start-up Voltage
  - 1.2V to 16V Operation Voltage
- 400kHz Pseudo-constant Frequency
- True Shutdown Function
- Low $R_{DS(ON)}$ Internal Switch
  - Main FET: 10mΩ
  - Rectifier FET: 20mΩ
  - Disconnect FET: 30 mΩ
- External Loop Compensation
- Programmable Peak Current Limit Threshold
- Battery Voltage Monitoring
- Programmable Soft-Start Limits the Inrush Current
- Input Voltage UVLO
- Over Temperature Protection
- Output Over Voltage Protection
- RoHS Compliant and Halogen Free
- Compact Package: QFN3x4-15
- Automotive AEC- Q100 Grade 1 Certified

Applications

- Backup Battery
- Automotive Boost

Typical Applications

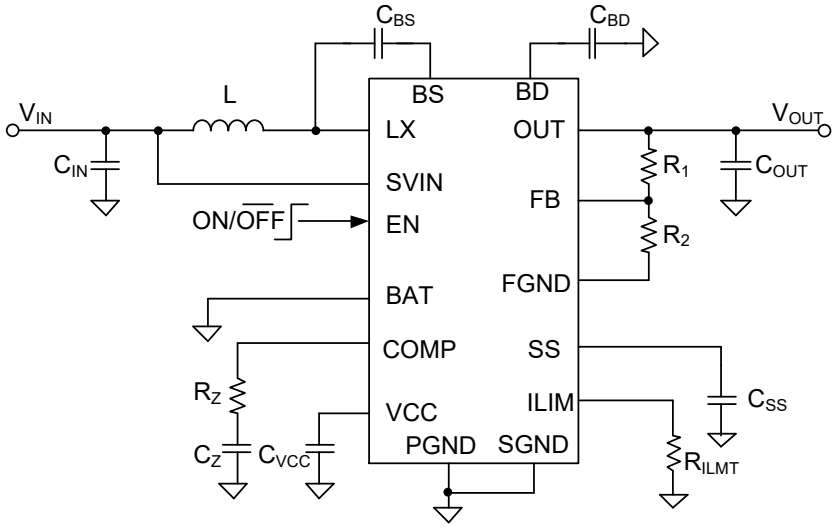
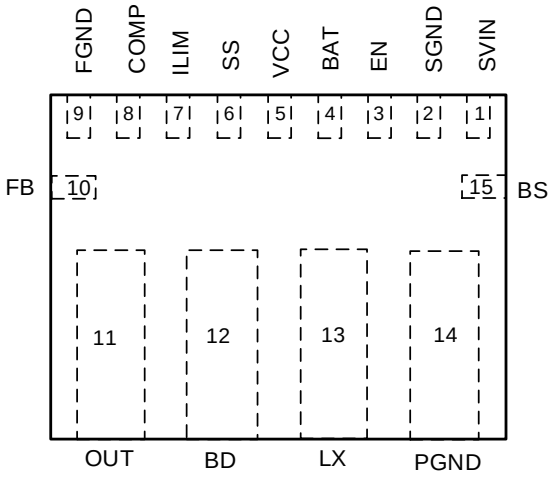


Figure 1. Schematic Diagram

Pinout (top view)



(QFN3x4-15)

Top mark: **CUU*xyz*** (Device code: CUU, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
SVIN	1	IC power supply pin. Decouple this pin to the SGND pin with a 1μF ceramic capacitor.
SGND	2	Signal ground pin
EN	3	Enable control. Pull this pin high to enable the IC, pull this pin low to disable the IC. Do not leave it floating.
BAT	4	Battery voltage monitor input pin. The Boost regulator is in active mode when the voltage on this pin is lower than BAT falling threshold. The Boost regulator is in standby mode when the voltage on this pin is higher than BAT rising threshold.
VCC	5	Internal 3.3V LDO output. Decouple this pin to SGND with a 1μF ceramic capacitor. VCC is powered by the higher voltage of either SVIN or BD.
SS	6	COMP voltage soft-start programming pin. Connect a capacitor from this pin to SGND to program the soft-start time. $t_{SS}(ms)=C_{SS}(nF)\times 1V/6\mu A$
ILIM	7	Peak current limit program pin. Connect a resistor R_{ILIM} from this pin to SGND to program peak current limitation threshold. $I_{LIM}(A)=1200/ R_{ILIM}(k\Omega)$
COMP	8	Loop compensation pin. Connect a RC network across this pin and ground to stabilize the control loop.
FGND	9	Feedback ground pin. This pin integrates a N-FET to SGND. The N-FET is turn off when the IC is disable.
FB	10	Feedback pin. Connect to the center of resistor voltage divider to program the output voltage: $V_{OUT}=1V\times(R_1/R_2+1)$
OUT	11	The output of disconnect FET
BD	12	The output of the Boost regulator and the input of disconnect FET. Bypass at least a 10μF ceramic capacitor to PGND.
LX	13	Inductor node. Connect an inductor from power input to the LX pin.
PGND	14	Power ground pin
BS	15	Boot-strap pin. Supply Rectified FET's gate driver. Connect a 0.1μF ceramic capacitor between the BS pin and the LX pin. Do not connect a resistor in series with the capacitor.

Block Diagram

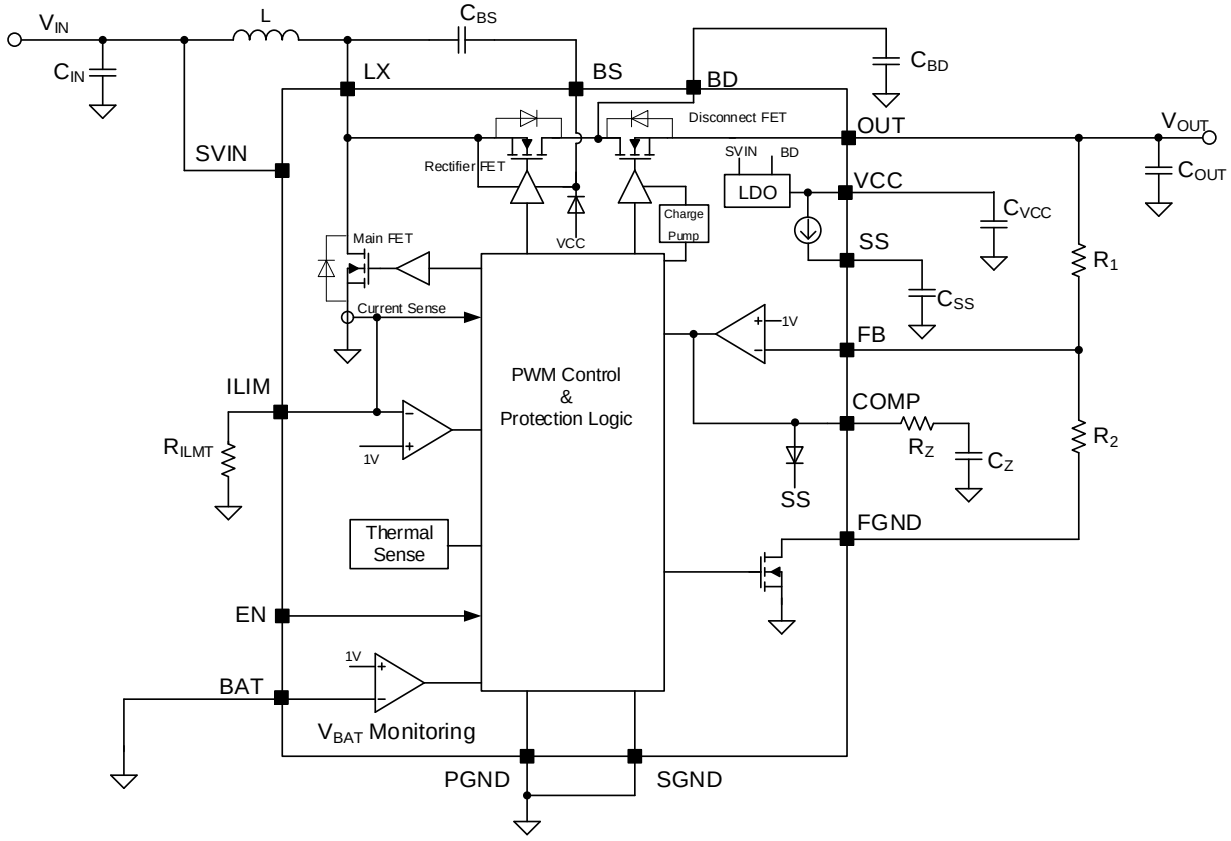


Figure 2. Block Diagram

Absolute Maximum Ratings (Note 1)

SVIN, OUT, EN, BAT, FB, FGND, BD ---------- -0.3V to 28V
LX ---------- -0.3V to 18V
VCC, COMP, ILIM, SS ---------- -0.3V to 4V
BS-LX ---------- -0.3V to 4V
Power Dissipation, P_D @ T_A = 25°C QFN3x4-15----------3.1W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 32°C/W
θ_{JC} ----------14°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

Start-up Input Voltage---------- 2.7V to 16V
Operating Input Voltage---------- 1.2V to 16V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 125°C

Electrical Characteristics

(V_{IN} =3.3V, V_{OUT}=12V, T_J = -40°C to 125°C. Typical values are at T_J=25°C, unless otherwise specified. The values are guaranteed by test, design or statistical correlation.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Input Voltage	V_{IN}		1.2		16	V
Start-up Input Voltage	V_{SVIN}				2.7	V
		V_{BD}≥4V			1.2	V
Quiescent Current	$I_{Q,IN}$	FB=1.1V, SVIN=EN=3V, VOUT=12V, no switching, measured on V_{IN}			5	μA
	$I_{Q,OUT}$	FB=1.1V, SVIN=EN=3V, VOUT=12V, no switching, measured on V_{OUT}		300	380	μA
Shutdown Current	I_{SHDN}	EN=0, T_J = -40℃ to 125℃		2.2	10	μA
Standby Current	I_{STBY}	EN=1, BAT=3V		25		μA
OUT Pin Leakage Current	$I_{OUT,LK}$	EN=0, SVIN=3.3V, VOUT=12V, T_J = -40℃ to 125℃		2.2	7	μA
VCC UVLO Rising Threshold	$V_{VCC,UVLO}$		2.2	2.4	2.6	V
VCC UVLO Hysteresis	$V_{VCC,HYS}$			0.2		V
Main N-FET RON	$R_{DS(ON),M}$			10		mΩ
Rectifier N-FET RON	$R_{DS(ON),R}$			20		mΩ
Disconnect N-FET RON	$R_{DS(ON),D}$			30		mΩ
FGND N-FET RON	$R_{DS(ON),F}$			10		Ω
Feedback Reference Voltage	V_{REF}	T_J =25°C.	0.99	1	1.01	V
		T_J = -40°C to 125°C	0.985	1	1.015	V
FB Input Current	I_{FB}	V_{FB}=3V	-50		50	nA
Output Voltage OVP	$V_{OUT,OVP}$		15.5	17	18	V
	$V_{FB,OVP}$			1.15		V
Main N-FET Current Limit Program Range	$I_{LMT,RNG}$		3		15	A
Current Limit Setting Accuracy	I_{LMT}	R_{ILMT}=120kΩ	8	10	12	A
Peak Current Limit Reference Voltage	V_{ILIM}			1		V
Output Current Limit	$I_{LMT,OUT}$	V_{OUT}>V_{IN}	3	3.3		A
Linear Current Limit	I_{CHARGE}	V_O<V_{IN}		1.5		A
Error Amplifier Trans-conductance	G_M			120		μA
Current Sense Gain	R_I			75		mΩ
EN Input Voltage High	$V_{EN,H}$		0.9			V
EN Input Voltage Low	$V_{EN,L}$				0.4	V
EN Turn-on Delay	t_d	EN ON to LX switching, C_{VCC}=1μF T_J = -40°C to 125°C		100	250	μs
BAT Rising Threshold	$V_{BAT,R}$		1.1	1.2	1.3	V
BAT Falling Threshold	$V_{BAT,F}$		0.9	1	1.1	V
Switching Frequency	f_{SW}		320	400	480	kHz
Soft-start Charging Current	I_{SS}		3	6	9	μA
Minimum ON Time	$t_{ON,MIN}$			100		ns
Minimum OFF Time	$t_{OFF,MIN}$			80		ns
Maximum ON Time	$t_{ON,MAX}$		3.6	4.8	6	μs
Thermal Shutdown Temperature	T_{SD}			150		°C

Thermal Shutdown Hysteresis	T_{HYS}			15		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

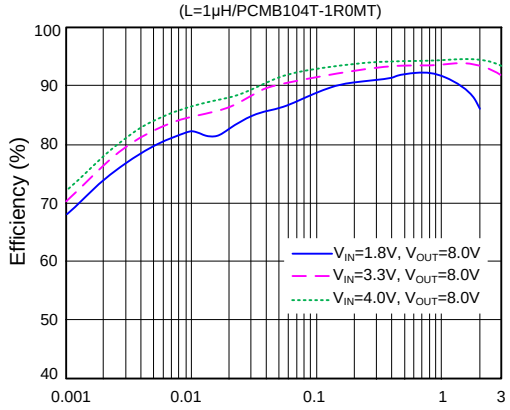
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a four-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

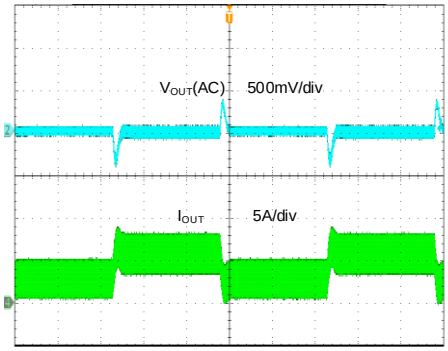
Efficiency vs. Load Current

(L=1μH/PCMB104T-1R0MT)



Load Transient

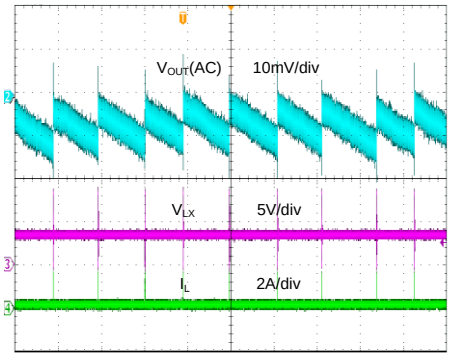
(V_{IN}=3.3V, V_{OUT}=8V, I_O=1 ~ 2A)



Time (400μs/div)

Output Ripple

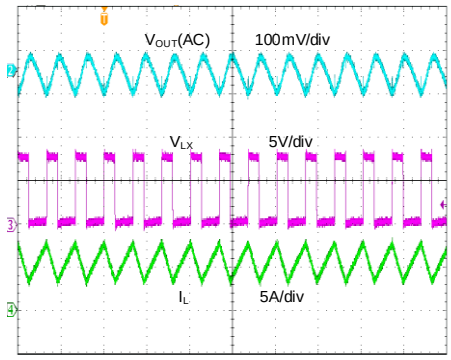
(V_{IN}=3.3V, V_{OUT}=8V, I_O=0A)



Time (400μs/div)

Output Ripple

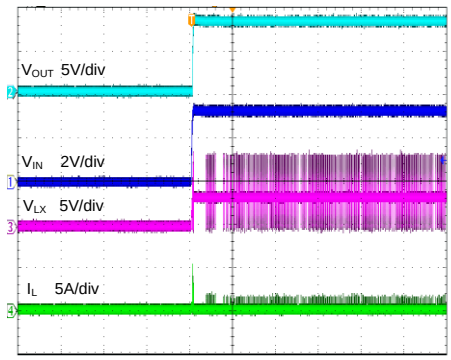
(V_{IN}=3.3V, V_{OUT}=8V, I_O=2A)



Time (4μs/div)

Startup from V_{IN}

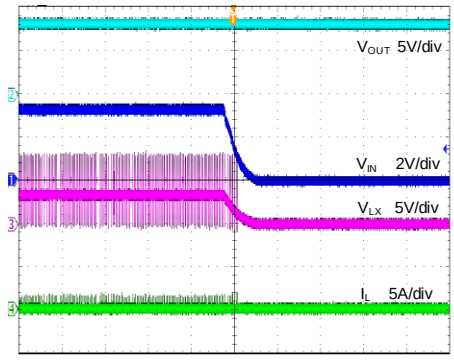
(V_{IN}=3.3V, V_{OUT}=8V, I_O=0A)



Time (20ms/div)

Shutdown from V_{IN}

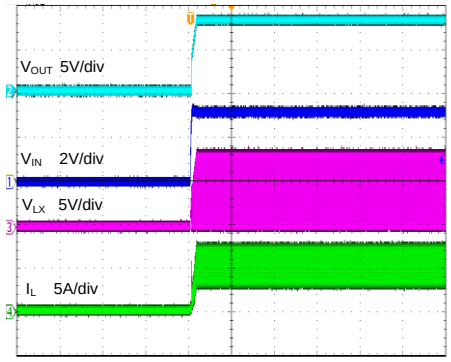
(V_{IN}=3.3V, V_{OUT}=8V, I_O=0A)



Time (20ms/div)

Startup from V_{IN}

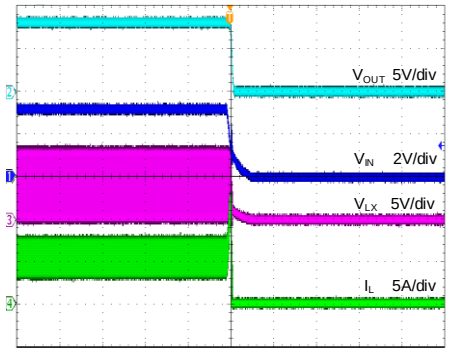
(V_{IN}=3.3V, V_{OUT}=8V, I_O=2A)



Time (20ms/div)

Shutdown from V_{IN}

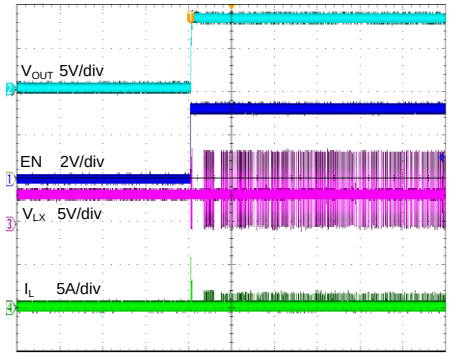
(V_{IN}=3.3V, V_{OUT}=8V, I_O=2A)



Time (20ms/div)

Startup from Enable

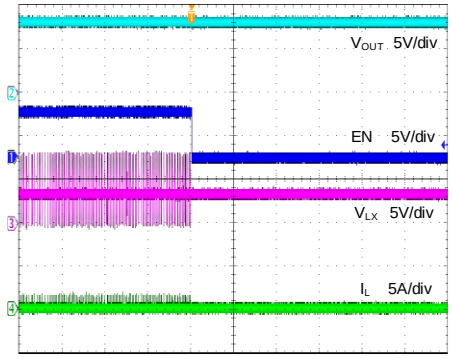
(V_{IN}=3.3V, V_{OUT}=8V, I_O=0A)



Time (20ms/div)

Shutdown from Enable

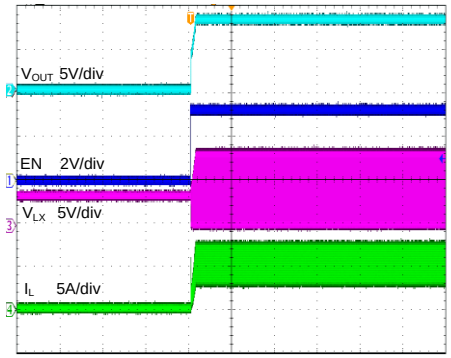
(V_{IN}=3.3V, V_{OUT}=8V, I_O=0A)



Time (20ms/div)

Startup from Enable

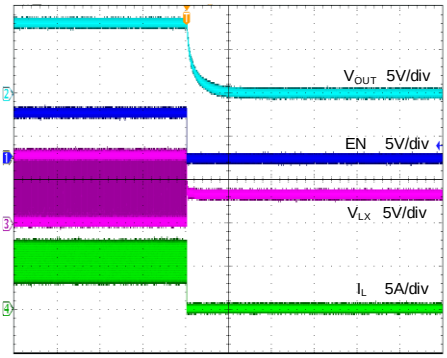
(V_{IN}=3.3V, V_{OUT}=8V, I_O=2A)



Time (20ms/div)

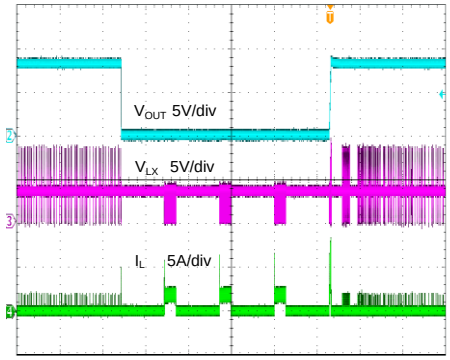
Shutdown from Enable

(V_{IN}=3.3V, V_{OUT}=8V, I_O=2A)



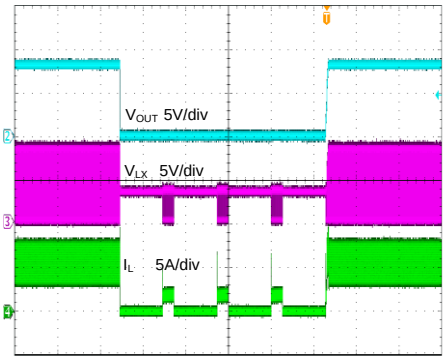
Time (800µs/div)

Short Circuit Protection
(V_{IN}=3.3V, V_{OUT}=8V, I_O=0A)



Time (20ms/div)

Short Circuit Protection
(V_{IN}=3.3V, V_{OUT}=8V, I_O=2A)



Time (20ms/div)

Applications Information

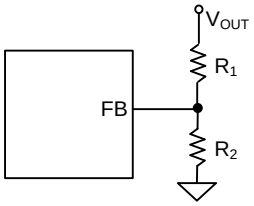
The SY2A29117 develops a high efficiency synchronous Boost regulator with programmable peak current limit. The device adopts adaptive constant off time and current mode control. The integrated low $R_{DS(ON)}$ switches minimize the conduction loss.

The SY2A29117 features cycle-by-cycle peak current limit, output short circuit protection and true shutdown. Low output voltage ripple and small external inductor and capacitor size are achieved with 400kHz pseudo-constant frequency.

Feedback Resistor divider R_1 and R_2

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light load, it is desirable to choose large resistance values for both R_1 and R_2. A value between 10k and 1M is recommended for both resistors. If R_1=200k is chosen, then R_2 can be calculated to be:

$$R_2 = \frac{R_1}{V_{OUT} - 1}(\Omega)$$



Input Capacitor C_{IN}

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2\sqrt{3} \times L \times f_{SW} \times V_{OUT}}(A)$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the VIN and PGND pin. Care should be taken to minimize the loop area formed by C_{IN}, VIN, and the PGND pin. In this case a 10µF low ESR ceramic capacitor is recommended.

The SVIN capacitor must be close to the SVIN and SGND pins to minimize the potential noise problem. Care should be taken to minimize the loop area formed by C_{IN}, and SVIN/SGND pins. In this case a 2.2µF low ESR ceramic is recommended.

Boost Output Capacitor C_{BD} and Disconnection FET Output Capacitor C_{OUT}

The Boost Output capacitor C_{BD} and disconnection FET Output capacitor C_{OUT} are selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into account when selecting these capacitors. For the best performance, it is recommended to use X5R or better grade ceramic capacitor with 25V rating and more than 44µF capacitors.

Boost Inductor L

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum average input current. The inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{f_{SW} \times I_{OUT\_MAX} \times 40\%}(H)$$

Where f_{SW} is the switching frequency and I_{OUT_MAX} is the maximum load current.

The SY2A29117 regulator is less sensitive to the ripple current variations. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of an inductor must be selected to guarantee an adequate margin to the peak inductor current under full load conditions.

$$I_{SAT,\,MIN} > \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT,\,MAX} + \frac{V_{IN}(V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<10mΩ to achieve a good overall efficiency.

Enable Operation

Pulling the EN pin low (<0.4V) will shut down the device. During shutdown mode. Driving the EN pin high (>0.8V) will turn on the IC again.

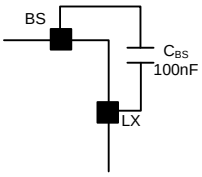
Soft-start

The SY2A29117 provides programmable COMP voltage soft-start time to limits the inrush current during start up. Connect a capacitor across the SS pin and SGND to lengthen the soft-start time.

$$tss(ms) = Css(nF) \times \frac{1(V)}{6(\mu A)}$$

External Bootstrap Capacitor

This capacitor provides the gate driver voltage for internal rectifier. A 100nF low ESR ceramic capacitor connected between the BS pin and the LX pin is recommended. Do not connect a resistor in series with the capacitor.



Peak Current Limit Setting

The peak current limit can be programmed with a resistor R_{ILIM} connecting from the ILIM pin to ground:

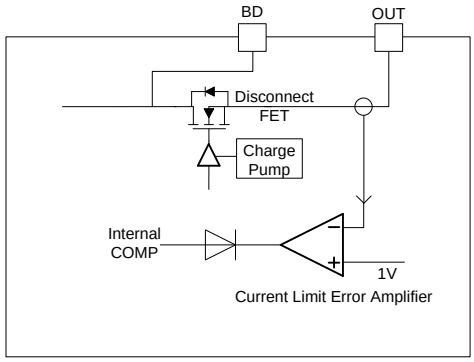
$I_{LIM}(A)=1200/ R_{ILIM}(k\Omega)$.

Short-circuit Protection

The SY2A29117 integrates hic-cup mode short circuit protection function. If the device is operated in current limit continuously and V_{OUT} drops below V_{IN}, the short-circuit protection mode will be initiated. The device will shut down for approximately 20ms, and then restart with a complete soft-start cycle that is approximately 5ms. If the short circuit condition remains another 'hiccup' cycle of shutdown and restart will continue indefinitely.

Output Current Limit

The SY2A29117 senses the Disconnect FET current, this current sense voltage is fed to the negative input of the current-limit error amplifier. The current-limit amplifier output clamps VCOMP if the output current signal is higher than the current limit threshold. As a result, the output current is limited by the internal COMP signal, and the output voltage decreases.

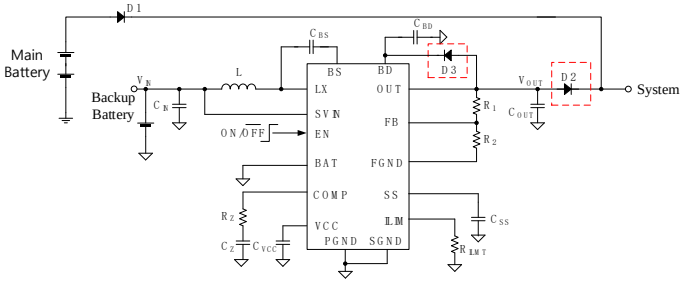


Over-temperature Protection (OTP)

The SY2A29117 includes over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will shut down switching operation when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 15°C the IC will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the OTP threshold.

Application for Automotive Backup Battery System

For applications where the system power supply voltage (V_{SYS}) may change greatly or the BD pin may be shorted to GND, excessive large current will flow through the body diode of the disconnection MOSFET, and that may cause the IC damage. A Schottky diode D2 is recommended to block current from V_{SYS} to the BD when V_{SYS} changes greatly, and Schottky diode D3 can be used for shunting current through the body diode of disconnection MOSFET when the BD is shorted to GND.



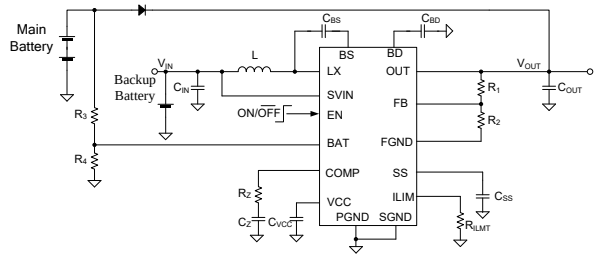
Battery Voltage Monitor Function

The battery voltage monitor function is used for monitoring main battery voltage when SY2A29117 is used as backup power supply and make the SY2A29117 in standby mode when the main battery voltage overtops a user-set threshold voltage.

The function can greatly reduce the standby current form 300μA to 25μA and improve the standby power supply start up speed.

During normal operation, the Boost regulator is in active mode when the voltage on the BAT pin is lower than BAT falling threshold(1V). The Boost regulator is in standby mode when the voltage on the BAT pin is higher than BAT rising threshold (1.2V).

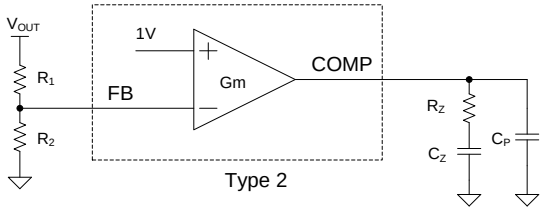
Monitor main battery voltage, can be programmed with a resistive divider connected to the BAT pin. If the Battery voltage monitor function is not used, the BAT pin should be connected to GND. Do not leave the BAT pin floating.

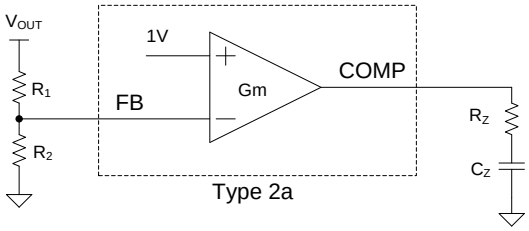


Loop Compensation

The SY2A29117 incorporates constant off time current mode control scheme. The current mode control scheme has two feedback loops. The inner loop, current loop, does not require any external compensation component. The outer loop, voltage loop, is compensated with external components.

In most applications, a Type 2 or Type 2a compensation network shown below can be used to stabilize the voltage loop. The Type 2 is the most widely used and works fine for power stages lagging down to -90˚ and where the boost brought by the output capacitor ESR must be canceled. Type 2a is used where the output capacitor ESR effect can be neglected.





Follow the steps below to calculate the value of external components for voltage loop compensation.

1. Select the crossover frequency fc of the closed loop. It is recommending that the crossover frequency is chosen to be the minimum value of 1/5 of right half plane zero (f_{RHPZ}) and 1/10 of switching frequency for the tradeoff of stability and transient response of the system. The system has faster response at higher crossover frequency.

$$f_{RHPZ} = \frac{(1-D_{MAX})^2 \times V_{OUT}}{2\pi \times L \times I_{OUT}}$$

2. Select a Rz value of the R-C series combination connected to the COMP pin.

$$R_Z = \frac{V_{OUT}}{g_m \times G_{fc} \times V_{REF}}$$

Where g_m is the error amplifier trans-conductance, which is typically 120uS; G_{fc} is gain of the power stage at crossover frequency.

$$G_{fc} = \frac{(1-D_{MAX})}{2\pi \times fc \times C_{OUT} \times R_i}$$

Where R_i is the current sense gain, which is typically 75mΩ.

3. Select a Cz value of the R-C series combination connected to the COMP pin. The compensation zero decides phase margin at the crossover frequency. Place a compensation zero at or before the dominant pole of R_L and C_O. R_L is the load resistance, which equals to V_{OUT}/I_{OUT}.

$$C_Z = \frac{V_{OUT} \times C_{OUT}}{I_{OUT} \times R_Z}$$

4. A high frequency pole is recommended to attenuate the high frequency noise. Place this pole to cancel the ESR zero of C_{OUT}

$$C_P = \frac{R_{ESR} \times C_O}{R_Z}$$

Layout Design

The layout design of the SY2A29117 regulator is highly simplified. To achieve a higher efficiency and better noise immunity, the following components should be placed close to the IC: C_{SVIN}, C_{BD}, C_{OUT}, C_{VCC}, L, R_1 and R_2.

1) It is desirable to maximize the PCB copper area connecting to the PGND pin to achieve a better thermal performance and noise immunity. If the board space allowed, a designated ground plane layer is highly recommended.

2) C_{SVIN} must be close to the SVIN and the SGND pins. The loop area formed by C_{SVIN}, the SVIN and the SGND pins must be minimized.

3) C_{BD} must be close to the BD and the PGND pins. The loop area formed by C_{BD}, BD and the PGND pins must be minimized.

4) The PCB copper area associated with the LX pin must be minimized to improve the noise immunity.

5) The components R_1 and R_2 and the trace connecting to the FB pin must NOT be adjacent to the LX node on the PCB layout to minimize the noise coupling to FB pin.

6) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the SVIN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull-down 1MΩ resistor across the EN and the SGND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

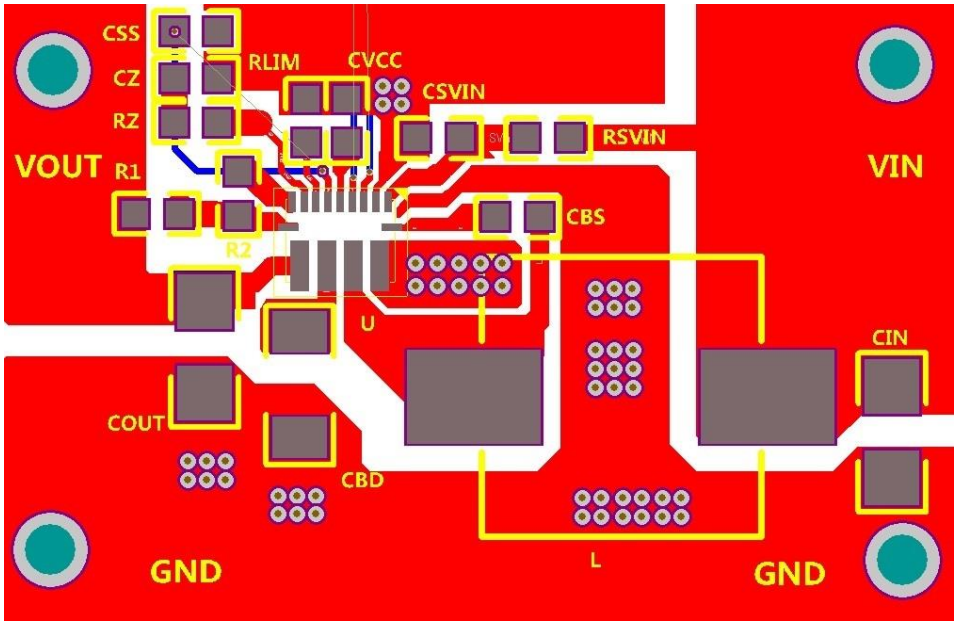
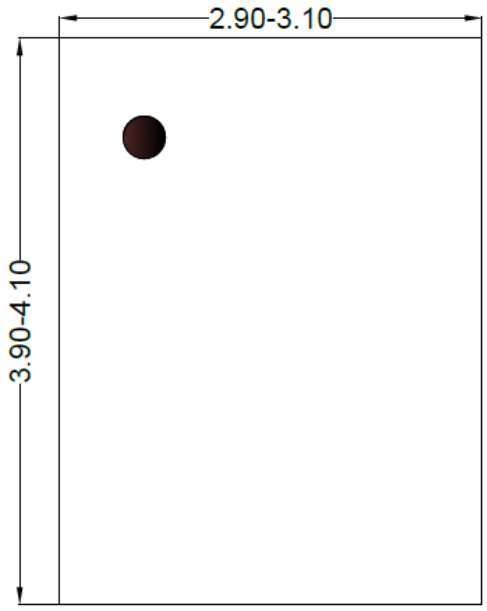
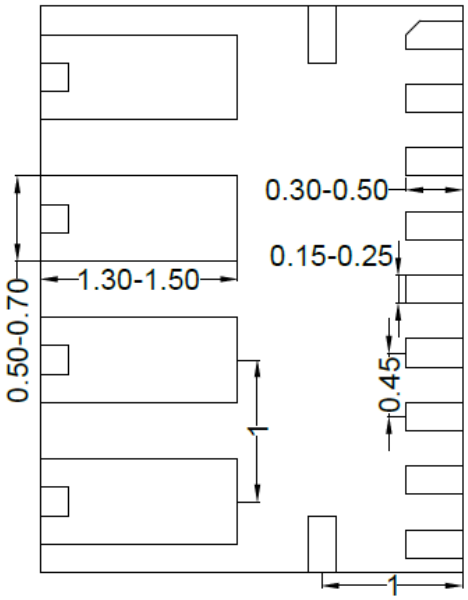


Figure 3. PCB Layout Suggestion

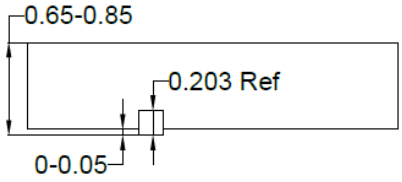
QFN3x4-15 Package Outline Drawing



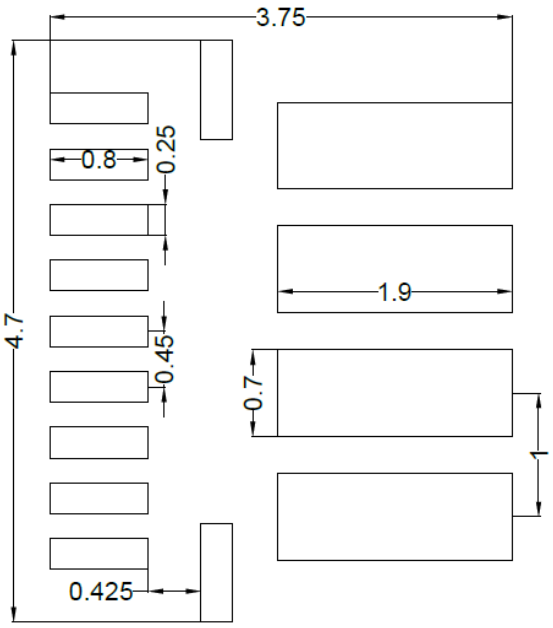
Top View



Bottom View



Front View

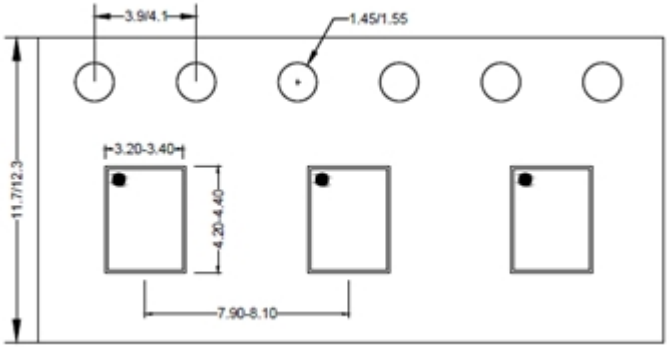


Recommended PCB Layout
(only for reference)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

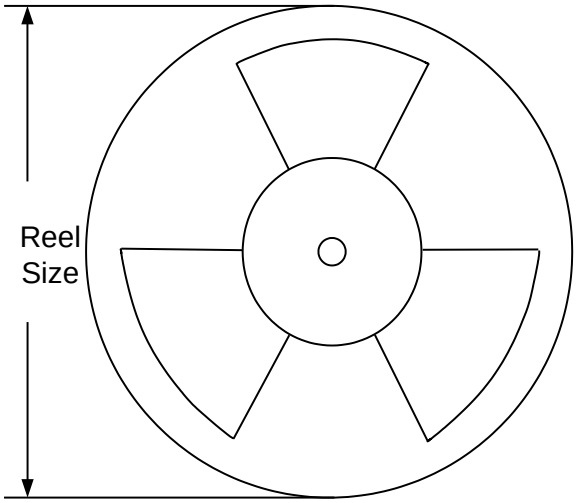
Taping & Reel Specification

1. Taping orientation for packages



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3x4	12	8	13"	400	400	5000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
June 12, 2025	Revision 1.0A	Add the following description to the BS pin description (Page2) and the **External Bootstrap Capacitor** application information (page 10): ---- Do not connect a resistor in series with the capacitor.
Jun. 09, 2024	Revision 1.0	Initial Production Release
Jun. 09, 2023	Revision 0.9	Initial Release.

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