SY23496

High Frequency QR Flyback Converter with Valley Lockout and E-mode GaN Integrated

General Description

SY23496 is a high frequency QR Flyback converter targeting at PD adaptors and fast charges. SY23496 integrates enhancement GaN FET (650V 0.165Ohm). It is suitable for wide output voltage range application, with maximum 140W output power. Maximum switching frequency can be up to 500kHz, so size of transformer and capacitors can be reduced.

In normal QR Flyback solutions, valley number always jumps between 1-2 or 3-5, which will increase Vo ripple and bring audio niose. SY23496 can lock valley with proprietary circuit and valley number can be 1 to 6th. System state is more stable than normal QR solutions.

SY23496 works under peak current mode. It adopts QR mode and GaN FET can be turned on at valley point to reduce switching loss, especially under high input voltage. If load decreases more, SY23496 will enter DCM to reduce switching frequency for higher efficiency. If load is very light, SY23496 will enter burst mode to reduce power loss.

SY23496 also provides comprehensive and reliable functions including HV startup, X-cap discharge, brown out protection, output OVP and UVP, OLP, VCC OVP, internal and external OTP, etc.

SY5239 is recommended to be used as secondary side SR controller in conjunction with SY23496. Then ZVS operation can be achieved for higher efficiency.
SY23496 is available with QFN 5×7-18.

Features

- DCM+QR Combined Operating Mode
- Adaptive OCP (LPS, Limited Power Source)
- Integrated GaN (650V 0.165Ohm_typ)
- New Package for Excellent Heat Sink.
- Programmable Gate Driver Current
- 140V LDO in VCCH Pin
- Switching Frequency Range: 25kHz~500kHz
- Valley Lockout from 1 to 6th
- Low Frequency Burst (1kHz)
- Frequency Modulation to Reduce EMI Noise
- Internal Soft Start
- Integrated 700V HV Start up
- Brown In/Out Protection
- X-cap Discharge Protection
- Programmable Output OVP&UVP
- Current Sense Resistor Short Protection
- Internal & External OTP
- Compact Package: QFN 5×7-18

Applications

- AC-DC Adaptors
- PD Adaptors
- Quick Chargers

Ordering Information

SY23496□(□□□)

- Package Code
- Optional Spec Code

Ordering Number	Package Type	Note
SY23496XDQ	QFN 5×7-18	--------

Typical Applications

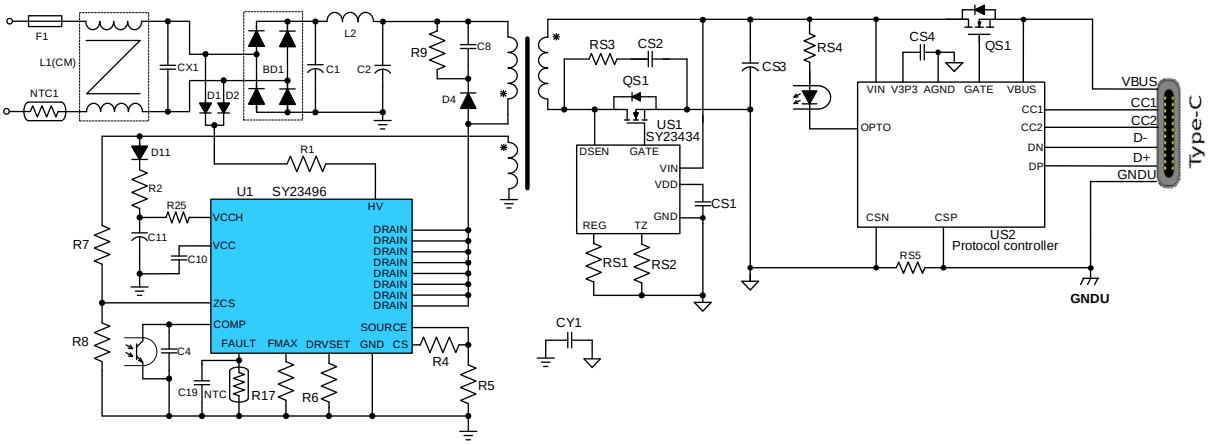
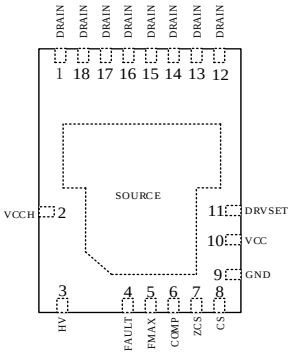


Figure 1. Typical Application Circuit

Pinout (top view)



QFN 5×7-18 (Top view)

Top Mark: FMR***xyz*** **(**Device code: FMR; ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Description
Drain	Drain of internal GaN FET
Source	Source of internal GaN FET (Exposed PAD)
FAULT	External OTP and Vout OVP pin.
FMAX	Maximum switching frequency set.
COMP	Compensation voltage of secondary side, connected to an opto-coupler.
ZCS	Output voltage, input voltage and QR valley detection pin.
CS	Inductor current sensing pin.
GND	Ground pin.
DRVSET	Programmable GaN FET gate drive pin.
VCC	Power supply pin.
VCCH	High voltage power supply pin.
HV	HV startup, Brown in/out, X-cap discharge detection pin.

Absolute Maximum Ratings (Note 1)

Drain ---------- -0.3V to 650V
Drain pulsed voltage (Intended for repetitive pulse, T_{PULSE} < 100 ns) ---------- -0.3V to 750V
HV ---------- -0.3V to 700V
VCC ---------- -0.3V to 30V
VCCH ---------- -0.3V to 140V
DRVSET ---------- -0.3V to 8V
CS, COMP, FAULT, FMAX ---------- -0.3V to 4V
ZCS ---------- -1V(Note1) to 7V
Power Dissipation at T_A = 25°C QFN 5×7-18---------- 4.8W
Package Thermal Resistance (Note 2)
Θ_{JA} QFN 5×7-18---------- 26°C/W
Θ_{JC} QFN 5×7-18---------- 9°C/W
Junction Temperature Range ---------- -40℃ to 150℃
Lead Temperature (Soldering, 10 sec.) ---------- 260℃
Storage Temperature Range ---------- -60℃ to 150℃
Note1, Dynamic ZCS negative voltage in 50us Duration ---------- -1V
Note1, Dynamic ZCS negative current in 50us Duration ---------- -2mA

Recommended Operating Conditions

HV ---------- -0.3V to 700V
VCC ---------- 8V to 25V
VCCH ---------- 9V to 140V
DRVSET ---------- 4V to 6V
CS ---------- -0.3V to 0.5V
ZCS ---------- -0.3V to 3.0V
COMP ---------- -0.3V to 2.5V
FAULT ---------- -0.3V to 3.0V
Junction Temperature Range ---------- -40℃ to 125℃
Case Temperature Range ---------- -40℃ to 105℃

Block Diagram

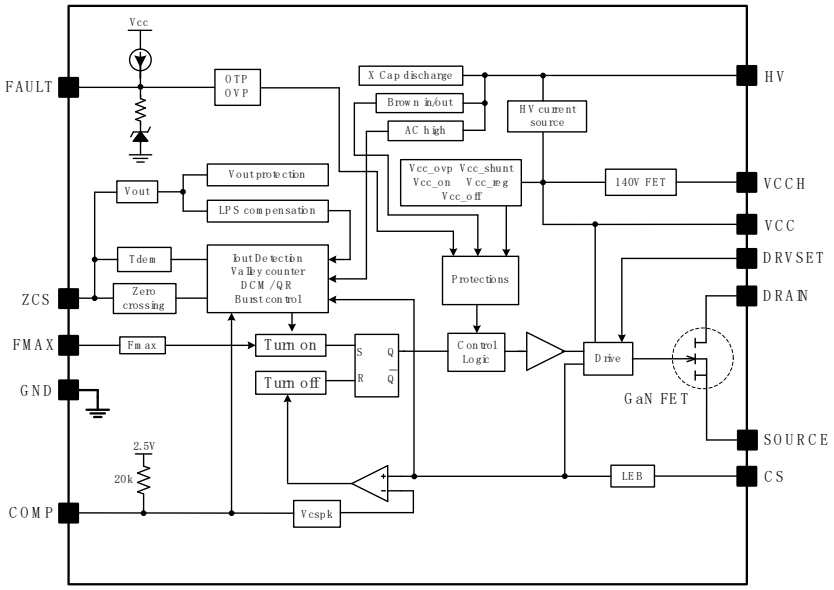


Fig.2 Block Diagram

Electrical Characteristics

(V_{CC} = 13V (Note 3), T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Integrated GaN FET						
Break down voltage	V_{DS_BR}	V_{GS}=0V, I_D=20uA	650			V
ON resistance	R_{DSON}	V_{GS}=6V, I_D=3A		165	260	mΩ
HV Pin Section						
HV Current to Charge VCC	$I_{HV\_CHARGE1}$	V_{HV} =100V_{DC}, V_{CC}=0V	0.15	0.3	0.55	mA
		V_{HV} =100V_{DC}, V_{CC}=3V	2.6	4.0	5.4	mA
Current to Discharge X Cap	I_{HV_XCAP} (Note 6)			2.0		mA
High or Low Voltage Detection	HV_{th_AChigh}		200	218	236	V
AC Low Debounce Time	T_{AClow_DBC}			20		ms
Debounce Time to Detect AC Unplug	T_{UNPLUG_DBC} (Note 6)			100		ms
BO Threshold	HV_{th_BO}		89	95	103	V
BI Threshold	HV_{th_BI}			105		V
BO Debounce Time	T_{BO_DBC}			100		ms
BI Debounce Time	T_{BI_DBC}			200		µs
VCC Pin Section						
VCC Turn-on Threshold	V_{CC_ON}	V_{CC} rising	18	20	22	V
VCC Turn-off Threshold	V_{CC_OFF}	V_{CC} falling	6.5	7.0	7.5	V
VCC Short Threshold	$V_{CCSHORT\_TH}$		0.5	0.7	0.8	V
VCCH Regulation Threshold	V_{CC_REG}		10	11.0	12	V
VCCH Regulation Hysteresis	V_{CC_REGHYS}			1.0		V
Protection Timer after Error Trigger	T_{ERROR}			1.0		s
VCC OVP Threshold	V_{CC_OVP}	V_{VCC} rising	26.4	28.0	29.6	V
VCC OVP Debounce Cycles	N_{VCCOVP_DBC}			4		
VCC Shunt Threshold	V_{CC_SHUNT}		25	27.0	29	V
VCC Shunt Current Capability	I_{VCC_SHUNT}	Vcc>$V_{CC,\ SHUNT}$		10		mA
Normal Operation Current Consumption	$I_{CC\_OPERATING}$	C_L=open, Fsw=50kHz		1.2		mA
Standby Current Consumption	$I_{CC\_STANDBY}$	V_{COMP}<$V_{TH\_SLEEP\_IN}$	280	400	520	µA
VCCH Pin Section						
Maximum Voltage	$VCCH_{BV}$		140			V
CS Pin Section						
Maximum Peak Current Limit Threshold if Secondary Side Short	V_{CS_MAX}		685	720	755	mV
Leading Edge Blanking for Vcs_max	T_{CS_LEB1}			150		ns
Delay Time from Vcs_max to PWM off	T_{CSMAX_DELAY}			30		ns
Vcs_max Debounce Cycles	N_{VCSMAX_DBC}			4		
Vcs Limit	V_{CS_limit}		475	500	525	mV
OCP Threshold for Normal Option (Note 4)	$V_{REF\_OCPNORMAL}$		530	555	580	mV
OCP High Threshold for LPS Option (Note 5)	$V_{REF\_OCPLPSH}$	V_{ZCS}<V_{ZCSLPS_LOW}	730	770	810	mV

OCP Low Threshold for LPS Option (Note 5)	$V_{REF\_OCPLPSL}$	$V_{ZCS}>V_{ZCSLPS\_HIGH}$	425	450	480	mV
Leading Edge Blanking Time for Vpk Control and Vcs_limit	T_{CS_LEB2}			250		ns
Delay Time from Vcs_limit to DRV Falling	T_{CS_DELAY2}			30		ns
Delay time from Vpk control to DRV Falling	T_{CS_DELAY3}			30		ns
Vcs Min in DCM Mode	V_{CSMIN_DCM}		65	80	95	mV
Debounce Time of I_{OUT} OCP	$T_{IOUTOCP\_DBC}$			200		ms
Soft Start Time	T_{SST}			10		ms
Frequency of Modulation in QR Mode	$F_{MODULATION\_QR}$			4		kHz
Vcspk Modulation Amplitude in QR Mode	$V_{QR\_MODULATION1}$	Valley=1~3		20		mV
		Valley=4~6		30		mV
CS Short Circuit Protection	V_{CS_SHORT}	Ton=4μs		60		mV
ZCS Pin Section						
OVP Threshold Voltage	V_{ZCS_OVP}		2.36	2.50	2.64	V
OVP Threshold Voltage Debounce Cycles	N_{ZCSOVP_DBC}			4		
UVP Threshold Voltage of Vout	V_{ZCS_UVP}			150		mV
UVP Threshold Voltage Debounce Time	$T_{VOUTUVP\_DBC}$			20		ms
Maximum Value of off Blanking Time	T_{ZCSLEB_MAX}		1.3	1.80	2.3	μs
Minimum Value of off Blanking Time	T_{ZCSLEB_MIN}		0.5	0.7	1.0	μs
Maximum off Time	T_{OFF_MAX}		90	120	150	μs
Zero Cross Point Detect	V_{ZCS_ZERO}			0		mV
QR Turn on Delay Time	$T_{ZCS\_ONDELAY}$			100		ns
LPS Compensation High Point	V_{ZCSLPS_HIGH}		1.74	1.90	1.98	V
LPS Compensation Low Point	V_{ZCSLPS_LOW}		1.06	1.12	1.24	V
Fault Pin Section						
Current Source for OTP Detection	I_{OTP}		46.5	49	51.5	μA
OTP Threshold	V_{OTP_TH}		0.37	0.4	0.43	V
OTP Exit Threshold	$V_{OTPEXIT\_TH}$			0.9		V
Clamp Diode for OVP	$V_{OVPDIODE}$		1.45	1.7	1.95	V
Capability of Clamp Diode for OVP	$I_{RFAULTOVP}$			1		mA
OVP Threshold	V_{OVP_TH}			2.5		V
Debounce Time to Trigger OTP/OVP	$T_{FAULTOTP/OVP\_DBC}$	$V_{FAULT}<V_{OTP\_TH}$ $V_{FAULT}>V_{OVP\_TH}$		100		μs
Fmax Pin Section						
Frequency Set	F_{MAX}	R>260kΩ		100		kHz
		R=100kΩ		260		kHz
		R<52kΩ or floating	470	500	530	kHz
COMP pin section						
Internal Pull up Voltage Source	V_{COMP_PULLUP}			2.5		V
Internal Pull up Resister	R_{COMP_PULLUP}			20		kΩ
Vcs_limit Point	V_{COMP_LIMIT}			1.9		V
QR Mode to DCM Change Threshold	V_{COMPTH_DCM}			1.0		V
Hysteresis of QR Mode to DCM	V_{COMPTH_DCMHYS}			0.1		V

Minimum Switching Frequency Threshold	V_{COMP_FMIN}		0.55	0.7	0.85	V
Enter Burst Mode Threshold	$V_{COMP\_BURSTIN}$	V_{COMP} falling	0.19	0.25	0.31	V
Exit Burst Mode Threshold	$V_{COMP\_BURSTOUT}$	V_{COMP} increasing		0.45		V
Start PWM Threshold in Burst Mode	$V_{COMP\_BURSTSTART}$	V_{COMP} increasing		0.35		V
Burst Frequency	$V_{COMP\_BURSTFREQ}$			1		kHz
OLP Threshold	V_{COMP_OLP}	V_{COMP} rising	1.95	2.2	2.45	V
OLP Debounce Time	T_{OLP_DBC}	V_{COMP}> V_{TH_OLP}		50		ms
DRVSET Pin Section						
High Voltage Clamp	V_{DRV-CS_CLAMP}		5.5	5.8	6.1	V
Programmable Driver Current	I_{DRV}	DVR-GND: 43kohm		5		mA
		DVR-GND: 22kohm		10		mA
		DVR-GND: 10kohm	14	20	26	mA
		DVR-GND: <2kohm		Error		
Ton_max	T_{ON_MAX}		14	20	26	μs
Frequency Limit in DCM Mode.	F_{LIMIT_DCM}			75		kHz
Frequency Min in DCM Mode	F_{MIN_DCM}		20	25	32	kHz
Frequency of Modulation in DCM Mode	$F_{MODULATION\_DCM}$			250		Hz
Minimum Valley Number in QR Mode	$VALLEY_{NUMBER}$	HV<218V	1			
		HV>218V	2			
Internal OTP						
OTP Threshold	$T_{OVP\_SHUNTDOWN}$			150		℃
Recovery Threshold	$T_{OVP\_RECOVERY}$			130		℃

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θJA is measured in the natural convection at TA = 25℃ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on "2 x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal via to bottom layer ground plane.

Note 3: Increase VCC pin voltage gradually higher than VCC_ON voltage then turn down to 13V.

Note 4: Normal OCP option is selected by ZCS pin resistor.

Note 5: LPS OCP option is selected by ZCS pin resistor.

Note 6: Selection of ZCS resistors is as follows.

ZCS pull down	Xcap function	Iout_ocp
25-27kOhm ±1%	Disabled.	Normal Option
13.0kOhm ±1%	Enabled.	Normal Option
7.5kOhm ±1%	Disabled.	LPS Option
3.0-3.6kOhm ±1%	Enabled.	LPS Option

ZCS_ovp threshold is 2.50V. When pull down resistor is determined, pull up resistor can be calculated according to Vout_ovp and Na/Ns. Then CS pin's in series resistor should be adjusted too. If Iout_ocp increases according to Vac's rising, value of CS pin's in series resistor should be increased for more compensation.

Operation Principles

HV start up and power supply

HV pin charges Vcc capacitor at AC power on. When Vcc voltage rises to start up threshold and HV will stop charging. Internal circuit of HV pin will be turned off for lower standby loss.

At start up, HV will charge Vcc pin and VCCH pin together at AC power on. VCCH's capacitor may be 10uF and Vcc's capacitor can be as less as 1uF, which is convenient to PCB layout.

In protection mode, SY23496 will stop PWM for $T_{ERROR.}$ During $T_{ERROR,}$ SY23496 has current consumption and Vcc(VCCH) capacitor cannot hold for so long time. When Vcc falls to Vcc_reg, HV will charge Vcc(VCCH) again until Vcc>(Vcc_reg + Vcc_reghys). After T_{ERROR}, internal logic will be reset for restart.

QR mode (Valley number is 1-6)

In QR mode, PWM turns on at valley point of GaN FET's drain voltage. So, EMI is improved and efficiency is higher too. Vcspk is controlled by Vcomp and valley number is controlled by output load. When Vcomp is higher than (V_{COMP_THDCM}+V_{COMPTH_DCMHYS}), QR mode is enabled and valley number is 6^{th}. As load increases, valley number decreases one by one until to the minimum value. When HV is lower than HV_{th_AChigh} and lasts for debounce time, AC low is declared and minimum valley number is 1^{th}. When HV is higher than HV_{th_AChigh}, AC high is declared and minimum valley number is 2^{th}, which is helpful to efficiency for lower switching loss at high input voltage.

Valley detect

Following waveform shows the method of valley detection. When falling edge of zero crossing voltage appears at ZCS pin, SY23496 will turn on GaN FET after some delay time.

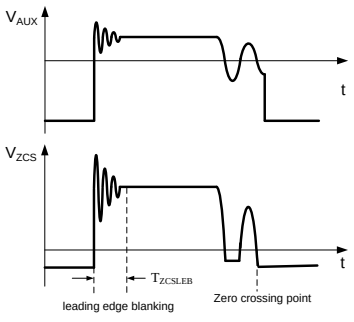


Fig.3 Valley detection

There is noise at ZCS pin when GaN FET turns off. The noise may affect valley detection. SY23496 uses blanking time to avoid the noise, which will be described in the **Output OVP & UVP** section.

DCM mode

When Vcomp is lower than V_{COMPTH_DCM}, DCM mode is enabled. In DCM mode, Vcspk and switching frequency are all controlled by Vcomp. PWM turns on at Fsw instant and won't wait for valley point. As load decreases, frequency firstly decreases from $F_{LIMIT,\ DCM}$ to $F_{MIN,\ DCM}$, which is known as PFM mode. Light load efficiency is optimized for lower switching loss. When frequency has decreased to $F_{MIN,\ DCM}$ and load goes on decreasing, Vcspk begins decreasing to keep constant voltage on output load.

Burst mode

When frequency and Vcspk have all decreased to minimum value, if output load keeps on decreasing, Vcomp will be lower than $V_{COMP\_BURSTIN}$. Then Burst mode is enabled. PWM will start when Vcomp is higher than $V_{COMP\_BURSTSTART.}$ PWM number is controlled by Tburst in order to keep burst frequency lower than certain value. PWM won't stop until the number has been complete. Then PWM stops and wait for next rising edge of $V_{COMP\_BURSTSTART}$. With this method, burst frequency is low and audible noise is optimized.

When Vcomp is higher than $V_{COMP\_BURSTOUT}$, SY23496 will enter DCM mode.

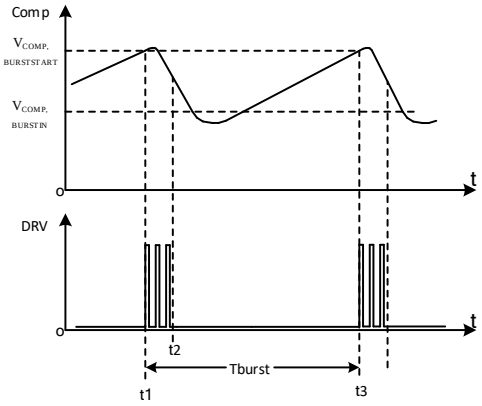


Fig.4 Quiet Burst

VCCH power supply

In order to simplify outside circuit, SY23496 contains VCCH pin. Maximum voltage of VCCH can be up to 140V. When Vcc is lower than V_{CC_REG}, VCCH will charge Vcc capacitor by inner circuit. When Vcc is higher than (V_{CC_REG} + V_{CC_REGHYS}), VCCH will stop charging.

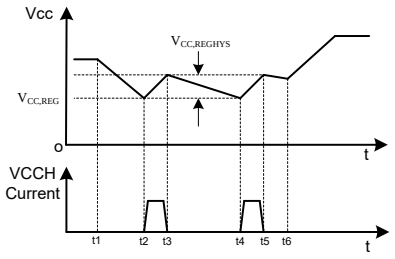


Fig.5 VCCH Charge Function

If efficiency is important and BOM cost is ok, two windings can used to reduce Vcc loss. In Fig.6, if Vout is low, Na3 voltage is too low and VCCH charges Vcc. If Vout is high, Na3 voltage is high enough and VCCH will be floating. A resistor and zener beside C11 are recommended, which can clamp high voltage coming from Na1's leakage inductance. R25 can be 1kOhm. D25's clamp voltage should be higher than Na1 voltage and be lower than C11's rating voltage.

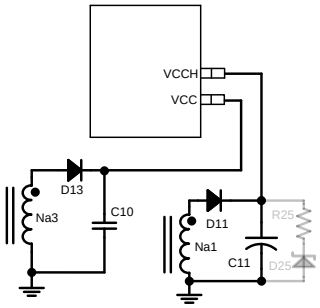


Fig.6 Typical Circuit for high efficiency application

Fig.7 shows one wingding application. C10 can be as low as 1uF SMT capacitor. Resistor and zener diode beside C11 are not needed any more.

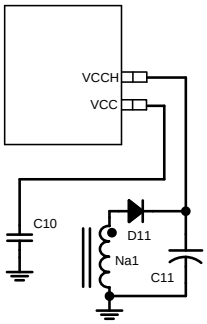


Fig.7 Typical Circuit for one winding application

During Xcap discharge process, voltage of C10 may be charged to Vcc_shunt. Then 35V capacitor is recommended.

Output over current protection (Iout_ocp)

SY23496 detects output current at primary side. At PWM turn off instant, CS pin samples voltage on Rcs. When current of Ns winding falls to zero, ZCS pin records demagnetization time. With these two signals, SY23496 calculates output current and the result is compared with Vref_ocp. When the result is higher than Vref_ocp for $T_{IOUTOCP\_DBC}$, PWM stops and timer begins. After T_{ERROR}, logic will be reset and HV will charge Vcc to V_{CC_ON} for restart.

Iout_ocp can be set by Rcs with following formula. Vref_ocp is inner voltage of SY23496. Nps is Np/Ns of transformer. Rcs is R5 in following circuit.

$$Iout\_ocp = 0.93 * \frac{Vref\_ocp * Nps}{6 * Rcs}$$

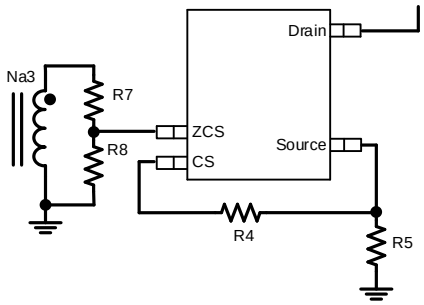


Fig.8 Rcs(R5) set for Iout_ocp

SY23496 samples voltage on Rcs before PWM's falling edge. After a very short time, PWM turns off. Then M1 usually has turn off delay. So, sampled voltage is not real peak current of transformer. When input voltage becomes higher, the error will be greater too. SY23496 uses R4 to compensate the error. If Iout_ocp becomes higher according to input voltage's increase, R4 should be added. If Iout_ocp falls according to input voltage's increase, which means compensation is too much, R4 should be reduced.

R4 range may be 50ohm to 500ohm.

In quick charging applications, Vout range is usually very wide, such as 3.3V to 21V. Iout range is very wide too. SY23496 has two OCP options to adapt different applications.

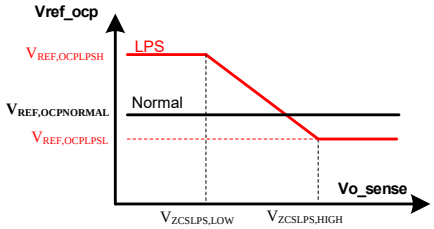


Fig.9 Two OCP options

The first example is as follows. Output includes 5V/3A, 9V/3A, 12V/3A, 15V/3A, 20V/3.25A, 3.3V-21V/3A.

Normal OCP option is suitable. $V_{REF\_OCPNORMAL}$ is changeless according to different output voltages.

The second example is different. Output includes 5V/3A, 9V/3A, 10V/6.5A, 12V/5A, 15V/4A, 20V/3.25A, 5V-12V/5A. If normal OCP option is adopted, OCP value should be higher than 6.5A and may be set to 7.0A. When Vout is changed to 20V, Iout_ocp is still 7.0A and maximum output power will be 140W. This is forbidden in UL60950.

SY23496's LPS option is suitable for the second example. V_{REF_OCPLPS} is related to Vout. Iout_ocp can be set by Rcs when Vout is highest. When Vout is lower and V_{REF_OCPLPS} becomes higher. At Vout=10V, Iout_ocp is higher than 6.5A and 10V 6.5A won't trigger OCP.

LPS and Xcap selection by ZCS resistor

SY5020 has two options about output OCP. One is Normal option and the other is LPS option, which have been described in Iout_ocp section. Two options can be selected by ZCS resistor.
Meanwhile, X cap discharge function can be selected by ZCS resistor too. When Xcap is enabled, HV should be connected to AC side via two diodes. When Xcap is disabled, HV can be connected to Vbus to save BOM cost of the diodes.
Selection of ZCS resistors is as follows.

ZCS pull down (R8)	Xcap function	Iout_ocp
25-27kOhm ±1%	Disabled.	Normal Option
13.0kOhm ±1%	Enabled.	Normal Option
7.5kOhm ±1%	Disabled.	LPS Option
3.0-3.6kOhm ±1%	Enabled.	LPS Option

ZCS_ovp threshold is 2.50V. When R8 is determined, R7 can be calculated according to Vout_ovp and Na/Ns. Then CS in series resistor R4 should be adjusted too. If Iout_ocp increases according to Vac's rising, value of R4 should be increased for more compensation.

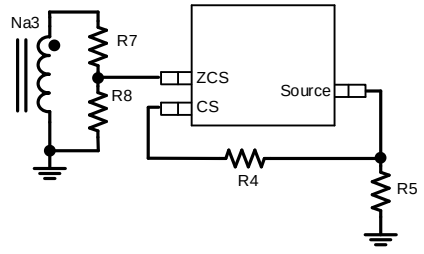


Fig.10 LPS and Xcap selection by ZCS resistor

Programmable drive current

At turn on instant, SY23496 uses constant current to charge Cgs of M1 and EMI performance is improved. At turn off instant, DRVSET pin will be fast pulled down to reduce turn off loss.

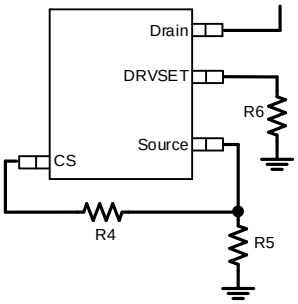


Fig.11 Drive circuit of GaN FET

At turn on instant, constant current value can be selected by R6. When current is lower, GaN's turn on speed will be slower and EMI performance will be better. Table is as follows. At SY23496's startup, R6 is detected and current is fixed until startup again.

R6	Constant current
10kohm	20mA
22kohm	10mA
43kohm	5mA
<2kohm	No PWM

Fig.12 Drive current table

Frequency limitation

To QR mode operation, when load decreases, switching frequency will increase and switching loss will increase too. Fmax pin can be used to limit maximum frequency. Relationship between frequency limitation and Fmax pin resistor is shown as follows.

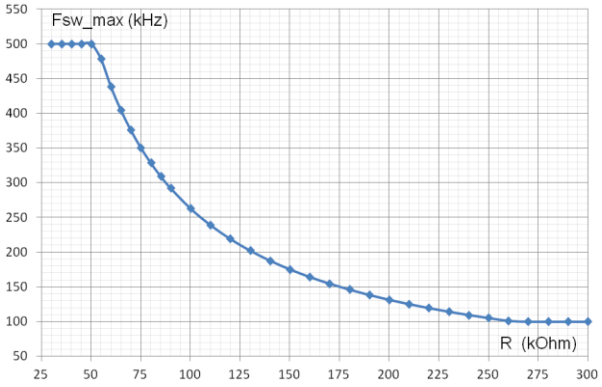


Fig.13 Frequency limitation

When Fmax pin is floating, frequency limitation is 500kHz. In the package without Fmax pin, frequency limitation is also 500kHz. If the resistor is lower than 30kOhm, frequency limitation is 500kHz too. When frequency limitation is triggered, PWM will turn on at the valley after limitation.

Frequency Modulation

In QR mode, SY23496 adds triangle voltage on Vcs for frequency modulation. If Ring is 1-3, modulation amplitude is 20mV. If Ring is 4-6, modulation amplitude is 30mV in order to obtain effective range of frequency modulation.

Soft start

At start up, when Vcomp rises to $V_{COMP\_BURSTSTART}$, PWM starts and Vcs increases from minimum value linearly. Under heavy load or Vout short conditions, soft start will terminate after T_{SST}. Under light load or no-load conditions, when Vcs value determined by Vcomp is lower than the value determined by soft start, soft start will terminate and Vcomp will control Vcs.

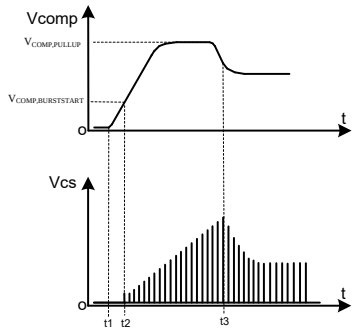


Fig.14 Soft start process

Under start up or Vout short conditions, Vout is very low and ZCS is the same. If ZCS cannot detect effective valley signal, Toff_max will be enabled. This is helpful to reduce deep CCM switching and voltage stress of SR MOS's Vds is optimized.

Vcs_limit

After T_{CS_LEB2} in every cycle, when Vcs is higher than Vcs_limit, PWM will turn off immediately. It is cycle by cycle and won't affect next cycle's PWM On.

Vcs_max

Under normal working state, Vcs_limit can limit peak current of GaN and provide enough protection. When transformer's winding or secondary diode is short circuit, current slope is very high and transformer will enter saturation state. The current can rise to much higher level in T_{CS_LEB2}.

SY23496 can detect Vcs after T_{CS_LEB1}, which is shorter than T_{CS_LEB2}. If Vcs is higher than V_{CS_MAX} in 4 continuous cyles, PWM stops and timer begins. After T_{ERROR}, logic will be reset and HV will charge Vcc to V_{CC_ON} for restart.

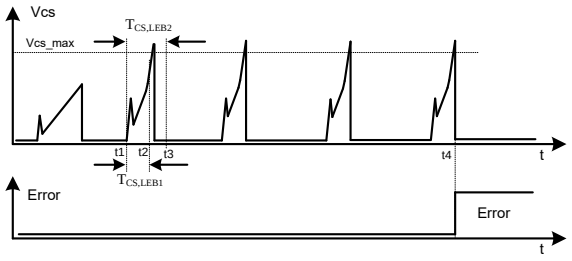


Fig.15 Vcs_max process

Brown out

When input voltage is lower than AC90V, current stress of transformer and primary GaN FET is very high. Heat stress is very high too. SY23496 has Brown out (BO) protection to protect power supply from broken down.

- BO: HV is lower than $HVth_{,BO}$ and last for $T_{BO,DBC}$.
- BI: HV is higher than $HVth_{,BI}$ and last for $T_{BI,DBC}$.

After BO, PWM stops and timer begins. After T_{ERROR}, logic will be reset and HV will charge Vcc to V_{CC_ON} for restart.

X-cap discharge

Under light load, when charger is unplugged from AC socket, there may be remaining high voltage on input terminal, which is dangerous to be touched.

SY23496 uses HV to discharge X-cap. HV pin is connected to AC side through R1, D1 and D3. R1 is recommended to be 5k – 10kOhm, which can provide more reliability against surge voltage on AC line.

If HV hasn't rising edge for continuous T_{UNPLUG_DBC}, AC unplug is detected. PWM stops and timer begins. HV sinks current of I_{HV_XCAP} to Vcc pin. Vcc rises to V_{CC_SHUNT} and HV falls linearly. When HV can't supply Vcc and Vcc is lower than V_{CC_OFF}, discharge will stop.

Voltage rating of Vcc capacitor should be higher than Vcc_shunt. Then 35V capacitor is recommended.

During X-cap discharge, once HV detects rising edge, which means AC re-plug happens, the discharge will be terminated immediately. Timer of T_{ERROR} will go on. During T_{ERROR}, HV will keep Vcc between V_{CC_REG} and (V_{CC_REG}+V_{CC_REGHYS}). After T_{ERROR}, logic will be reset and HV will charge Vcc to V_{CC_ON} for restart.

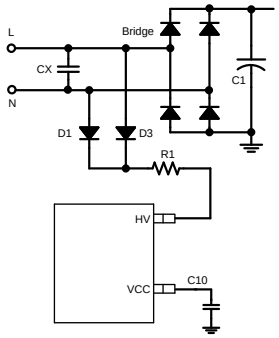


Fig.16 X-cap discharge circuit

Following waves show the process.

At t1, AC unplug happens.

At t2, AC unplug is confirmed. PWM stops and HV sinks current to Vcc.

At t3, Vcc rises to V_{CC_SHUNT}.

At t4, X-cap discharge current is lower than Vcc's dissipation and Vcc begins falling.

At t5, Vcc is lower than V_{CC_OFF} and discharge is reset.

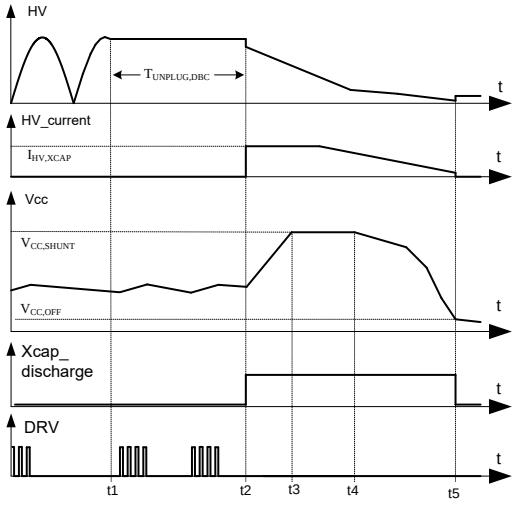


Fig.17 X-cap discharge waveforms

Output OVP & UVP

SY23496 detects output voltage through ZCS pin. When primary GaN FET turns off, there is a parasitic resonance on AUX winding. To avoid false trigger, blanking time is adopted, which is shown as follows. Blanking time is adaptive according to Vcspk. When Vcspk is 200mV, primary current is small and energy stored in leakage inductance is small too. Parasitic resonance on auxiliary winding will be shorter and blanking time can be shorter too. Blanking time rises to the maximum value along with Vcspk rising to 500mV.

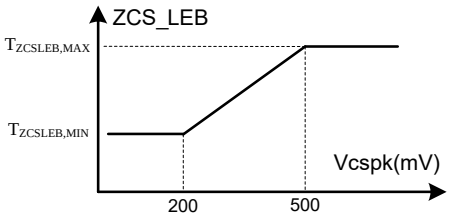


Fig.18 ZCS blanking time

When ZCS is higher than V_{ZCS_OVP} in continuous N_{ZCSOVP_DBC} cycles, ZCS_OVP is triggered. PWM stops and timer begins. After T_{ERROR}, logic will be reset and HV will charge Vcc to V_{CC_ON} for restart.

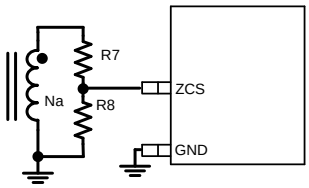


Fig.19 ZCS OVP setting

Output OVP threshold is calculated as below:

$$Vout\_ovp = Vzcs.ovp * \frac{R7 + R8}{R8} * \frac{Ns}{Na}$$

When ZCS is lower than V_{ZCS_UVP} in continuous time of $T_{VOUTUVP\_DBC}$, ZCS_UVP is triggered. PWM stops and timer begins. After T_{ERROR}, logic will be reset and HV will charge Vcc to V_{CC_ON} for restart.

Note: Pull down resistor R8 should be determined firstly by LPS and Xcap selection. Then R7 is calculated according to above equation. UVP is used to avoid continuous working under Vout short circuit and is not necessary to be designed.

Vcc OVP

Vcc_ovp can prevent IC from damage due to abnormal high voltage when feedback loop is open or number of Na winding is wrong. When Vcc rises to V_{CC_SHUNT} and outside power's current ability is higher than shunt ability, Vcc can go on rising.

Vcc is detected all the time. If Vcc is higher than V_{CC_OVP} in continuous 4 cycles, Vcc_ovp is triggered. PWM stops and timer begins. After T_{ERROR}, logic will be reset and HV will charge Vcc to V_{CC_ON} for restart.

If the error condition still exists after restart, IC will work in hiccup mode.

Open Loop Protection

If output is short circuit, or opto-coupler open circuit, or load increase too much, Vcomp will be pulled up. When Vcomp is higher than V_{COMP_OLP} and last for

T_{OLP_DBC}, OLP is triggered. PWM stops and timer begins. After T_{ERROR}, logic will be reset and HV will charge Vcc to V_{CC_ON} for restart.

Fault OTP & OVP

Fault pin can be used as OVP and OTP functions. Outside circuit is as follows. At normal state, current of Iotp is clamped by D12. D12's clamp voltage is between OTP threshold and OVP threshold. So, both protections won't be triggered.

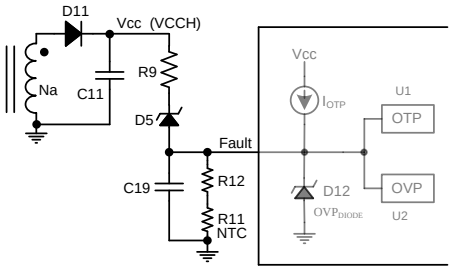


Fig.20 Fault OTP & OVP

Under error conditions, Vcc or VCCH will rise. D5 may be broken down. If pull up current is higher than D12's clamp ability, Fault voltage will be pulled up. When Fault pin is higher than V_{OVP_TH} and last for $T_{FAULTOTP/OVP\_DBC}$, Fault_ovp is triggered. PWM stops and timer begins. After T_{ERROR}, logic will be reset and HV will charge Vcc to V_{CC_ON} for restart.

R11 is NTC resistor. As temperature's rising, R11's resistance falls. When R11 is small enough, there will be no current flowing into D12 and all the current of Iotp will flow into R11. As Iotp is changeless, Fault voltage will fall along with R11's resistance. When Fault voltage is lower than V_{OTP_TH}, Fault_otp is triggered. PWM stops and timer begins. After T_{ERROR}, logic will be reset and HV will charge Vcc to V_{CC_ON} for restart. After restart, Fault pin is detected. PWM won't begin until Fault is higher than $V_{OTPEXIT\_TH}$.

R9 is used to limit the current flowing into Fault pin. OVP threshold is mainly decided by D5's breakdown voltage. R12 is used to adjust OTP threshold conveniently. C19 is used to filter various noise and recommended value is 100pF.

CS pin short circuit

In Ton of every PWM, Vcs is detected at 4us and compared with V_{CS_SHORT}. If Vcs<V_{CS_SHORT}, short circuit protection is triggered. PWM stops and timer begins. After T_{ERROR}, logic will be reset and HV will charge Vcc to V_{CC_ON} for restart.

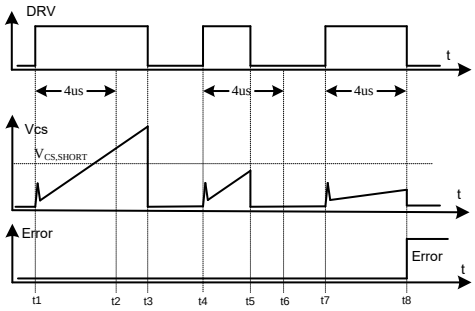


Fig.21 CS short protection

Above waveforms show the logic.

At t2, Vcs is higher than V_{CS_SHORT}. No protection.

At t5, Timer of 4us hasn't arrived.

No compare and no protection.

At t8, Vcs is lower than V_{CS_SHORT} at 4us.

Protection is triggered.

Internal OTP

SY23496 monitors die temperature under normal operating mode. Once die temperature rises above internal OTP threshold, PWM stops and timer begins. After T_{ERROR}, logic will be reset and HV will charge Vcc to V_{CC_ON} for restart.

Power Supply Design Guide

BUS capacitor calculation

Generally, bulk capacitor CBUS is selected according to the following rules.

- No PF: 1.5-1.8uF per watt (Output power).
- With PF: 0.5-0.8uF per watt (Output power).

Minimum BUS voltage calculation

Minimum BUS voltage appears when input voltage Vac is lowest and output current reaches rated value. When there isn't PF circuit before Flyback, minimum BUS voltage is calculated as:

$$V_{BUS\_MIN} = \sqrt{2V_{IN\_MIN}^2 - \frac{P_O(1-K_{CH})}{\eta C_{BUS} f_o}} \qquad \text{Formula (1)}$$

KCH is BUS capacitor charge coefficient (generally KCH is set to 0.2~0.3). η is conversion efficiency and f_o is frequency of AC input.

Following examples are helpful to fast selection. AL Cap's actual capacitance is only 85-90% of its nominal

value and capacitance has deviation in mass production. Following information is for reference only.

To 30W solution, there isn't Boost PFC circuit. Bus nominal capacitance is 27+27uF. Vbus_min is as follows.

Output Power	30W	35W	40W	45W
AC90V 50Hz	86V	80V	75V	68V
AC90V 60Hz	93V	87V	83V	78V

For better performance, Vbus_min should be higher than 80V.

To 66W solution, there isn't Boost PFC circuit. Under full load 20V3.3A, Vbus_min is as follows.

Bus nominal capacitance	82+22uF	82+10uF	82uF	68uF
AC90V 50Hz	82V	78V	72V	60V

For better performance, Vbus_min should be higher than 80V.

To 140W solution, topology is Boost + Flyback. Output is 28V 5A. Bus nominal capacitance is 39+39uF.

At AC90V 50Hz, Boost PFC outputs DC240V. Vbus is 222V(min) to 253V(max). Ripple is 31V.

At AC176V 50Hz, Boost PFC outputs DC350V. Vbus is 338V(min) to 362V(max). Ripple is 24V.

Transformer parameter calculation

1) Primary/secondary turns ratio: NPS

NPS is limited by voltage stress of primary GaN FET:

$$N_{PS} \le \frac{V_{MOS\_BR} K_{DR} - \sqrt{2} V_{IN\_MAX} - \Delta V_{SN}}{V_O + V_{D\_F}} \quad \text{Formula (2)}$$

VMOS_BR is the breakdown voltage of primary GaN FET;

KDR is VDS de-rating factor of power MOS;

$V_{IN,MAX}$ is always AC264V;

VD_F is forward voltage of secondary rectification diode; If SR is adopted at secondary side, VD_F is equal to 0.

ΔVSN is voltage spike at primary GaN turn off. Starting value can be 50V.

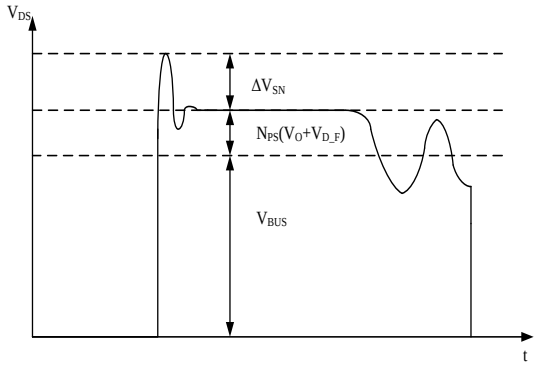


Fig.22 Primary Vds waveform

When Nps is determined, reflect voltage can be calculated as follows.

$$V_{OR} = N_{PS} * (V_O + V_{D\_F})$$

2) Primary inductance: LP

SY23496 has QR/DCM mode and CCM is not available. Transformer primary inductance is mainly related with switching frequency. When Vbus is the minimum value, Lp can be calculated by following formula.

$$L_P = \frac{1}{2 * F_{SW\ MIN} * V_O * I_O} * \left(\frac{V_{BUS\_MIN} * V_{OR}}{V_{BUS\ MIN} + V_{OR}}\right)^2 \quad \text{Formula (3)}$$

Vo: Output voltage and unit is V.

Nps: Primary/secondary turns ratio without unit.

Vbus_min: Minimum voltage after bridge and unit is V.

Fsw_min: Frequency at Vbus_min and unit is kHz.

Io: Output current and unit is A.

Lp: Primary inductance and unit is mH.

In the parameters, Vo, Nps, Vbus_min and Io have been determined. Only Fsw_min needs to be selected. When Fsw_min is higher, Lp will be smaller. The frequency at AC230V will be higher too.

To typical application, Fsw_min is about 100-130kHz, which is at Vbus_min (usually 80-90V). Then frequency at Vbus_max (370V) is about 160-220kHz.

3) Turns of primary winding: NP

(a) Select the magnetic core, confirm the effective AE

(b) Preset Bmax of magnetic core (0.32T~0.36T)

(c) Calculate primary Rcs

$$Rcs = 0.93 * \frac{Vref\_ocp * Nps}{6 * Iout\_ocp} \quad \text{Formula (4)}$$

In normal option, Vref_ocp is $V_{REF\_OCPNORMAL}$.

In LPS option, Vref_ocp is $V_{REF\_OCPLPSL}$.

(d) Calculate maximum primary peak current

$$I_{PPK\_MAX} = \frac{V_{CS.LIMIT}}{R_{CS}}$$ Formula (5)

(e) Calculate primary turns: NP

$$N_P = \frac{L_P * I_{PPK\_MAX}}{B_{MAX} * A_E}$$ Formula (6)

4) Turns of secondary winding: NS

$$N_S = \frac{N_P}{N_{PS}}$$

In actual design, Fsw_min is difficult to be determined. If a random value is selected, later calculation may be hard and this may be unsuitable to the bobbin of transformer. So design procedure is always as follows, which is inverse to traditional method.

Select transformer and AE ->

Determine winding width of bobbin ->

Select Ns wire -> Determine Ns ->

Determine Vor and Nps -> Calculate Np ->

Calculate Rcs according to Formula (4)

Calculate Ippk_max according to Formula (5)

Determine Bmax (0.32-0.36T)

Calculate Lp at last according to Formula (6)

With this procedure, Fsw_min is not an input parameter. When Lp is calculated, switching frequency Fsw is determined too. This will always lead to a satisfactory design and efficiency will always be close to highest value for certain transformer. It is not needed to try again and again.

5) Turns of auxiliary winding: NA

To fast charge application, Vout range is wide. Turns of AUX winding should take Vout_max andVout_min into consideration.

If efficiency is important and BOM cost is ok, two AUX windings are recommended.

- AUXL can supply Vcc at Vout_max.

$$18V < \frac{V_{OUT\_MAX}}{N_S} * N_{AUXL} < 22V$$

- AUXH can supply Vcc at Vout_min.

$$10V < \frac{V_{OUT\_MIN}}{N_S} * N_{AUXH} < 14V$$

If BOM cost is important, one winding is enough, which is AUXH. Turns of AUXH wingding is the same as N_{AUXH} in above formula.

Secondary MOSFET Selection

Under the conditions of Vbus_max and Vout_ovp, the reverse voltage of secondary rectification MOSFET will reach maximum level. The maximum voltage (ignore voltage spike when primary MOS is turned on) is calculated as follows.

$$V_{D\_R\_MAX} = \frac{\sqrt{2}V_{IN\_MAX}}{N_{PS}} + V_{O\_OVP}$$

Maximum instantaneous forward current is calculated as equation below:

$$I_{SPK\ MAX} = I_{PPK\ MAX} * N_{PS}$$

To a 66W (20V 3.3A) solution, BSC098N10NS5 is recommended, which is 100V 8.2mOhm (Vgs=10V).

To a 90W (20V 4.5A) solution, BSC0805LS is recommended, which is 100V 6.0mOhm (Vgs=10V).

To a 120W (20V 6.0A) solution, two MOSFETs in parallel is recommended, which is mainly for heat sink consideration. BSC098N10NS5 is ok, which is 100V 8.2mOhm (Vgs=10V).

MOS selection is related to heat dissipation design. Place refer to actual temperature test.

Layout Considerations

Following rules is recommended for normal working and EMI considerations.

(a) Switching node: Primary Drain/AUX/Core;
Secondary Drain/AUX/Core.

(b) Important signal node (easy to be disturbed):
Primary: Vcs, Fault, Comp, ZCS and Fmax etc.
Secondary: REG, TZ and Feedback loop etc.

(c) In order to guarantee normal working, important signal node should be far away from switching node. If PCB routing is hard, static node should be used as shielding between switching and signal node. Static node can be Vbus, GND, Vcc, VCCH and Vout, SGND etc.

(d) In order to realize good EMI performance, switching node on PCB layout should be as small as possible. Switching node should not be selected as heat sink method, such as GaN's drain.

(e) In order to realize good EMI performance, main current loop should be as small as possible.
- Current in Ton: Bus cap -> transformer -> GaN -> Rcs -> GND -> Bus cap.
- Current in Toff: Transformer -> SR_MOS

-> Cout -> GND -> Transformer.

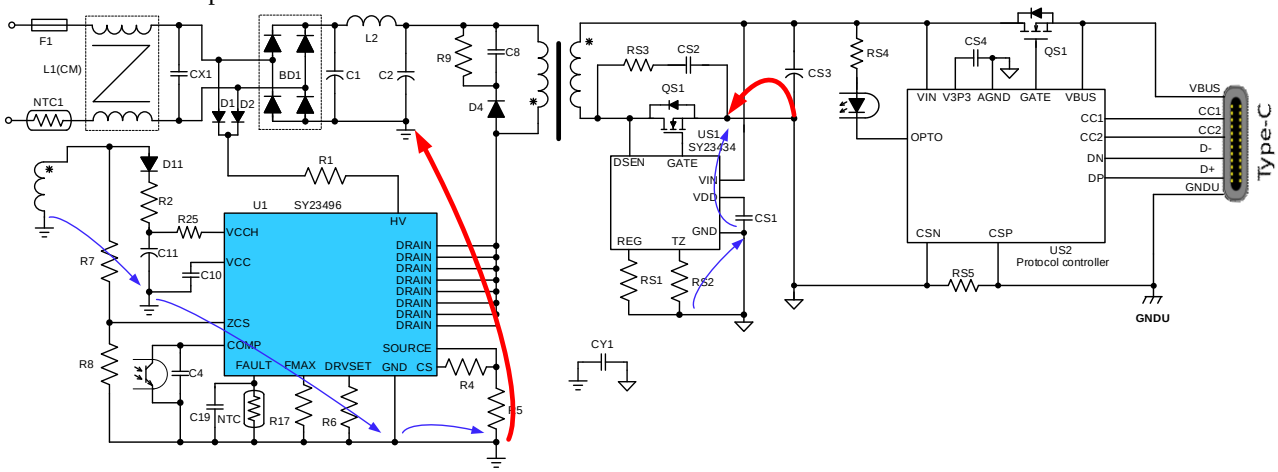
- Current in leakage inductance and snuber circuit.
- Drive loop of primary and secondary MOS.

(f) These components should be closed to SY23496. Fault capacitor, Comp Capacitor, Fmax resistor, CS resistor (in series), Vcc capacitor.

ZCS pull up resistor should be placed at AUX pin of transformer and pull-down resister should be closed to ZCS pin.

(g) These components should be closed to SY5238. REG resistor, TZ resistor, Vdd capacitor and Vin capacitor.

(h) GND routing is as follows.
SY23496's GND should be connected to Rcs-GND in order to get accurate Vcs signal.



As Vgs(th) of GaN FET is as low as 1.2V, it is easy to be falsely triggered by noise.

- **IC_GND should be connected to Rcs_GND directly.**
- **Drive loop should be as small as possible.**

Design Example

A design example of typical application is shown below step by step.

Input/output specification

Parameter	Symbol	Value
Input voltage range	V_{IN}	90V~264V
Rated output power	P_O	66W
Rated output voltage	V_O	5V - 20V
Output OVP level	$V_{O,OVP}$	24V
Rated output current	I_O	3.3A
OCP	I_{OCP}	3.68A
Efficiency	η	93%

Preset parameter

Parameter	Symbol	Value
Break down voltage of power FET	$V_{MOS,BR}$	650V
V_{DS} de-rating factor of power FET	K_{DR}	90%
Spike on V_{DS} at power FET turn off	ΔV_{SN}	70V
BUS capacitor charge coefficient	K_{CH}	0.2
Secondary diode forward voltage drop	$V_{D,R}$	0V
Transformer effective Ae (RM8)	A_E	62 mm^2

1) BUS capacitor selection

Select BUS capacitor: C_{BUS}=104uF (1.57uF/W)

2) Minimum BUS voltage calculation

BUS capacitor charge coefficient: K_{CH}=0.2

$$V_{BUS\_MIN}=\sqrt{2V_{IN\_MIN}^2-\frac{P_O(1-K_{CH})}{\eta C_{BUS}f_o}}=\sqrt{2\times 90^2-\frac{66\times(1-0.2)}{93\%\times 104u\times 60}}=84V$$

3) Transformer design

(a) Calculate primary/secondary turns ratio: N_{PS}

$$N_{PS}\le\frac{V_{MOS\_BR}K_{DR}-\sqrt{2}V_{IN\_MAX}-\Delta V_{SN}}{V_O+V_{D\_F}}=\frac{650\times 0.9-\sqrt{2}\times 264-70}{20+0}=7.1$$

N_{PS} is selected to: N_{PS}=6.25, Reflect voltage Vor=6.25*20V=125V.

(b) Calculate Lp of transformer: Select Fsw_min=110kHz

$$L_p=\frac{1}{2*F_{SW\ MIN}*V_O*I_O*}*\left(\frac{V_{BUS\_MIN}*V_{OR}}{V_{BUS\ MIN}+V_{OR}}\right)^2=\frac{1}{2*110kHz*20V*3.3A}*\left(\frac{84*125}{84+125}\right)^2=0.174mH$$

(c) Calculate Rcs: In normal option, Vref_ocp=0.555V.

$$R_{CS}=\frac{093*V_{REF\_OCP}*N_{PS}}{6*I_{OUT\ OCP}}=\frac{0.93*0.555*6.25}{6*3.68}=0.146Ohm$$

(d) Calculate maximum primary peak current:

$$I_{PPK\_MAX}=\frac{V_{CS.LIMITL}}{R_{CS}}=\frac{0.50}{0.146}=3.42A$$

(e) Calculate primary winding turns N_P: B_{MAX}=0.27T

$$N_p=\frac{L_p*I_{PPK\_MAX}}{B_{MAX}*A_E}=\frac{170uH*3.42A}{0.37T*62mm^2}=25.3ts$$

(f) Calculate secondary winding turns: N_S

$$N_S = \frac{N_P}{N_{PS}} = \frac{25}{6.25} = 4$$

(g) Calculate auxiliary winding turns N_{AUXL}=4ts: Vout_max=20V

$$18V < \frac{V_{OUT\_MAX}}{N_S} * N_{AUXL} < 22V, \quad So, \quad 3.6 < N_{AUXL} < 4.4$$

Calculate auxiliary winding turns N_{AUXH}=10ts: Vout_min=5V

$$10V < \frac{V_{OUT\_MIN}}{N_S} * N_{AUXL} < 14V, \quad So, \quad 8 < N_{AUXH} < 11.2$$

5) Secondary diode selection

(a)Maximum reverse voltage calculation:

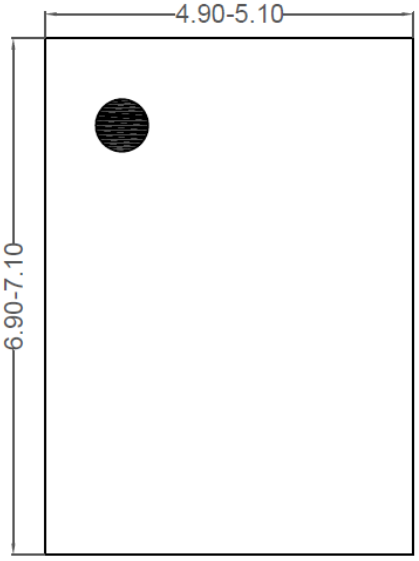
$$V_{D\_R\_MAX} = \frac{\sqrt{2}V_{IN\_MAX}}{N_{PS}} + V_{O\_OVP} = \frac{\sqrt{2}\times 264}{6.25} + 24 = 84V$$

Considering the voltage spike, reverse voltage rating is recommended to be 100V~120V.

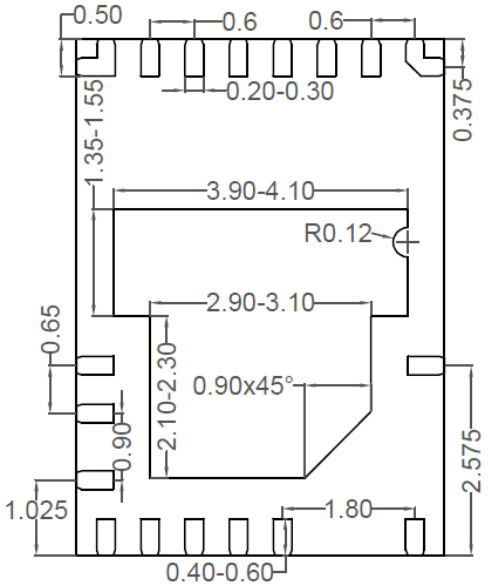
(b) Maximum instantaneous forward current:

$$I_{SPK\ MAX} = I_{PPK\ MAX} * N_{PS} = 3.42A * 6.25 = 21.4A$$

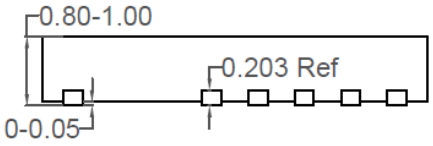
QFN5x7-18 Package Outline Drawing



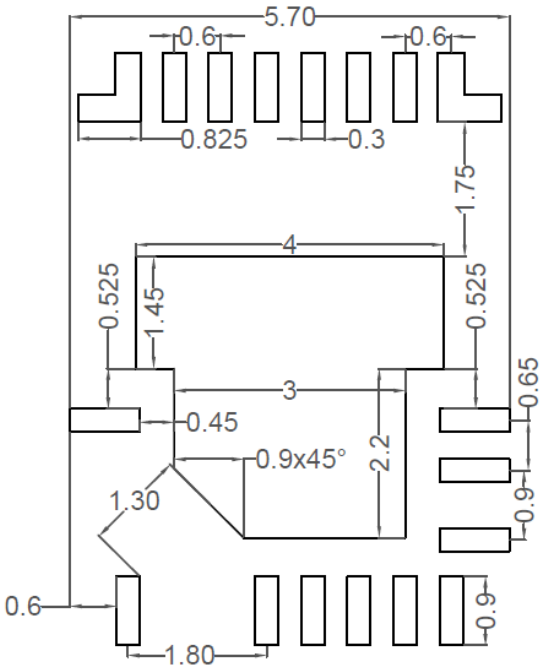
Top View



Bottom view



Front View



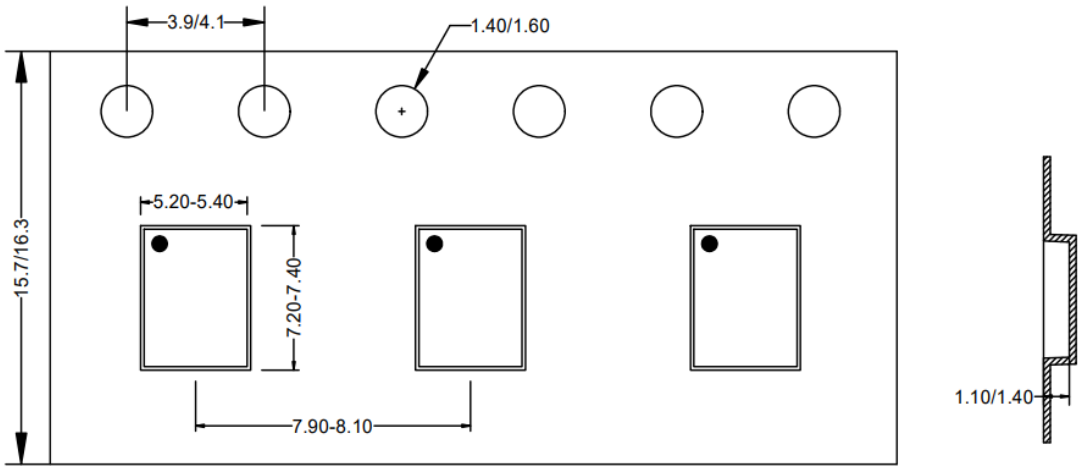
Recommended PCB layout
(Only for reference)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

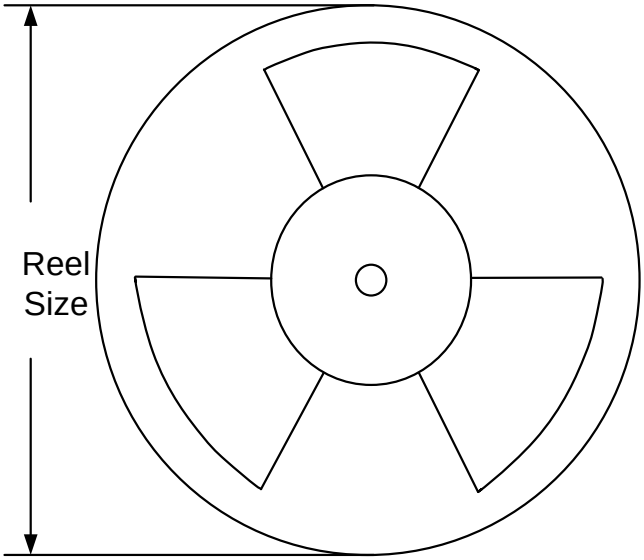
1. Taping Orientation

QFN5x7-18



Feeding Direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
QFN5x7-18	16	8	13"	400	400	3000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
May 25, 2023	Revision 0.9	Initial Release

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