SY20776D

Multi-Cell Synchronous Buck-Boost Battery Charger Controller with NVDC Power Path Management

1 General Description

The SY20776D is a switching mode battery charger controller. It can drive 4-switch synchronous Buck-Boost converter to support the wide input range and multi-cell Li-ion and Li-polymer batteries. The IC includes full protections during charging process for safety.

The SY20776D can operate in Narrow-VDC(NVDC) mode. With this feature, the system voltage will not drop below setting minimum system voltage even though the battery is depleted or removed. Charge current will reduce to pre-charge level during NVDC mode. The IC also features Dynamic Power Management (DPM) to avoid AC adapter overloading. Besides charging the battery, SY20776D can realize USB On-The-Go (OTG) function. Battery can reversely offer energy to the input port.

Ordering Information

SY20776 □(□□ □)

Package Code

Optional Spec Code

Ordering Number	Package type	Note
SY20776DQFQ	QFN4×4-32	

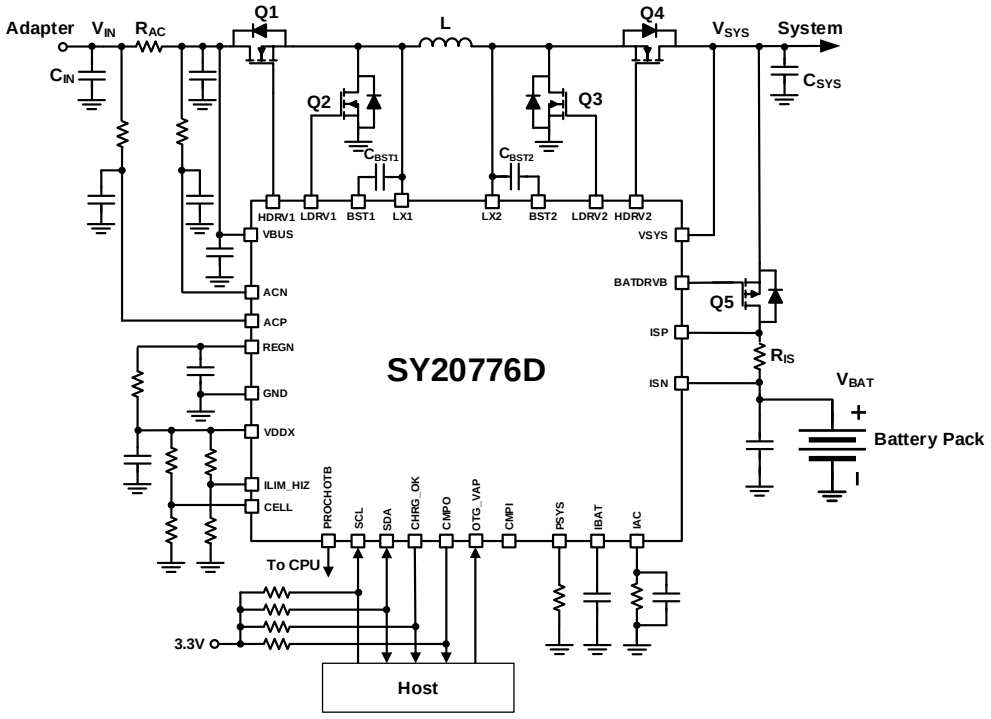
2 Features

- 3.5V to 25V Input Operating Voltage
- Charge 1s to 4s Battery from Wide Range of Input Source
- Drive Bi-Direction 4-switch Buck-Boost with Single Inductor
- 800kHz or 1.2MHz Programmable Switching Frequency
- I^2C Controls
  - -- Battery Charge Voltage (1.024V - 19.2V)
  - -- Minimum System Voltage (1.024V - 16.128V)
  - -- OTG Output Voltage (3V - 20.8V)
  - -- Battery Charge Current (64mA - 8.128A)
  - -- Input Voltage Limit for DPM (3.2V - 19.52V)
  - -- Input Current Limit for DPM (50mA - 6.4A)
  - -- OTG Output Current Limit (50mA - 6.35A)
- High Accuracy for Voltage/Current Regulation
- Accurate Power/Current Monitor and Comprehensive PROCHOT for CPU Throttling
- ILIM_HIZ Pin to Set Input Current Limit
- NVDC Power Path Management
  - -- Battery Supplements System when Adapter is Fully-Loaded
  - -- Battery MOSFET (BATFET) Ideal Diode Operation in Supplement Mode
- Pass Through Mode (PTM) for System Power Efficiency Improvement
- When System is Powered by Battery Only, Vmin Active Protection (VAP) Mode Supplements System from Input Capacitors during System Peak Power Spike
- Support Battery LEARN Function
- Adaptive Input Current Limit (AICL) to Extract Max Input Power
- Host Control Interface for Flexible System Configuration
- Integrated ADC to Monitor Voltage, Current and Power
- Thermal Shutdown Protection
- Input, System, Battery Overvoltage Protection
- Input, MOSFET, Inductor Overcurrent Protection
- Compact Package: QFN4x4-32

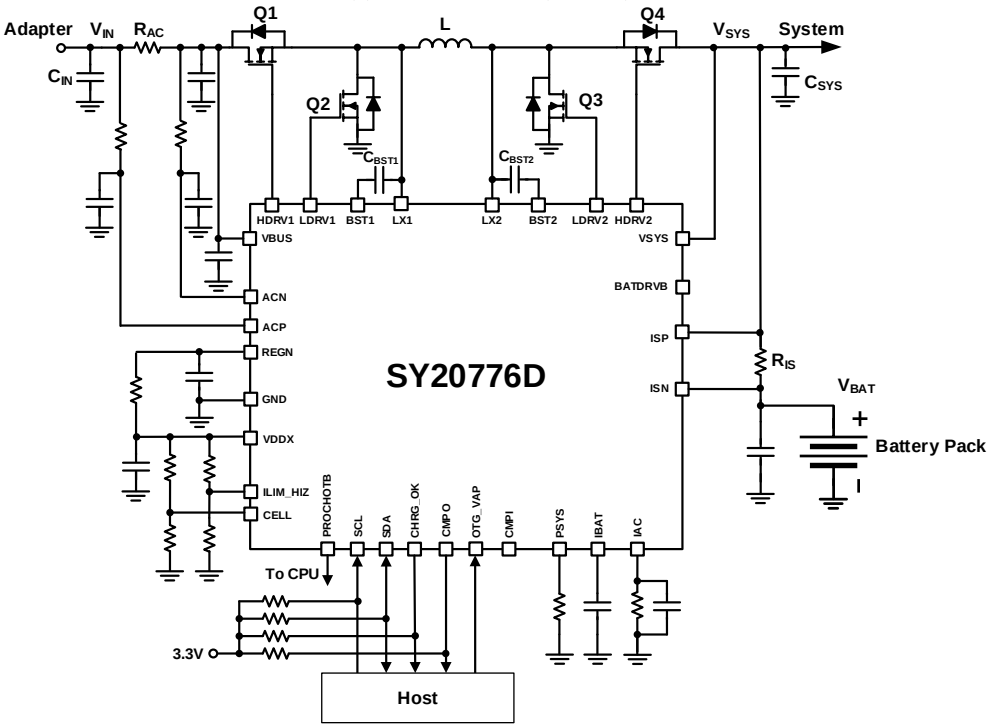
3 Applications

- Notebook, Ultra-Book, Tablet PC
- Industrial and Medical Equipment
- Portable Equipment with Rechargeable Batteries

4 Typical Application Schematic



(a) With BATFET (Default)



(b) Without BATFET

Figure 4-1. Schematice Diagram

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5 Pin Configuration and Functions

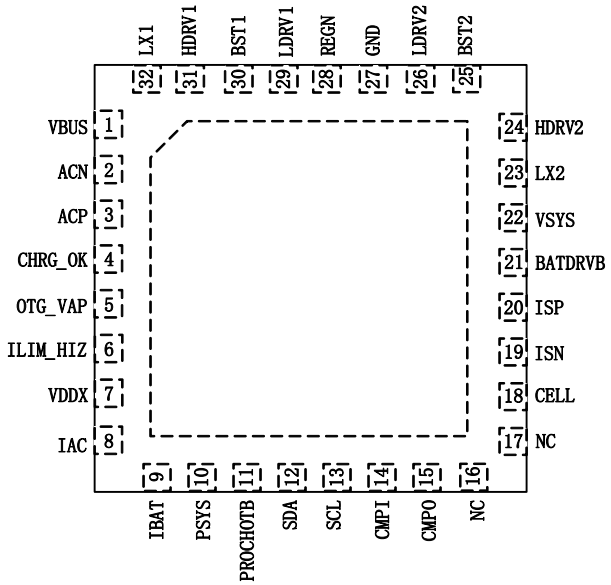


Figure 5-1. QFN 4×4-32 in top view

Top Mark: AAAB***xyz*** **(**Device code: AAAB, ***x=year code, y=week code, z= lot number code***)

Table 5-1. Pin Description

Name	Pin	Description
VBUS	1	IC power supply input. 1Ω resistor and 0.47μF capacitor is recommended to filter the input inrush current and high frequency noise.
ACN	2	Input current sense negative input in forward charging mode or output current sense positive input in reversed OTG mode. The leakage current on ACP and ACN are matched. A R-C low-pass filter is required to be placed between the sense resistor R_{AC} and the ACN pin to suppress high frequency noise in the current sense signal. Refer to application section for ACP/ACN filter design.
ACP	3	Input current sense positive input in forward charging mode or output current sense negative input in reversed OTG mode. The leakage current on ACP and ACN are matched. A R-C low-pass filter is required to be placed between the sense resistor R_{AC} and the ACN pin to suppress high frequency noise in the current sense signal. Refer to application section for ACP/ACN filter design.
CHRG_OK	4	Open drain active HIGH indicator. Connect a 10kΩ pull-up resistor to power rail. CHRG_OK HIGH logic indicates VBUS is in the range of 3.5V to 25V without fault.
OTG_VAP	5	Active HIGH to enable OTG or VAP modes. When REG0x34[5]=1, pulling OTG_VAP pin HIGH and setting REG0x35[4]=1 can enable OTG mode. When REG0x34[5]=0, pulling OTG_VAP pin HIGH can enable VAP mode.
ILIM_HIZ	6	External input current limit setting and HIZ control pin. Program ILIM_HIZ voltage by connecting a resistor divider from pull-up rail to ILIM_HIZ pin to ground. The ILIM_HIZ voltage is calculated as $V_{ILIM\_HIZ}=1V+40\times I_{DPM}\times R_{AC}$, in which I_{DPM} is the target input regulation current. When REG0x32[7]=1, the lower setting of ILIM_HIZ voltage and REG0x0F/0E() sets input current regulation limit. ILIM_HIZ pin can be disabled by setting REG0x32[7]=0 or pulling the ILIM_HIZ above 4V. When the pin voltage is below 0.4V, the device enters HIZ mode with low quiescent current. When the pin voltage is above 0.8V, the device is out of HIZ mode.

VDDX	7	Internal reference bias pin. Connect a 10Ω resistor from REGN to VDDX and a 1μF ceramic capacitor from VDDX to power ground.
IAC	8	Buffered AC current output. A resistor from the IAC pin to ground indicates the inductance in use. For a 2.2μH inductance, the resistor is 137kΩ. Place a 100pF or less ceramic decoupling capacitor from IAC pin to ground. IAC output voltage is clamped below 3.3V. This pin can be floating if not in use.
IBAT	9	Buffered charge/discharge current output. Place a 100pF or less ceramic decoupling capacitor from IBAT pin to ground. IBAT output voltage is clamped below 3.3V. This pin can be floating if not in use.
PSYS	10	Buffered total system power monitor. The output current is proportional to the total power from the adapter and the battery. The gain is selectable through I^2C.
PROCHOTB	11	Open drain active LOW output of processor hot indicator. It monitors adapter input current, battery discharging current and system voltage. If any event in the PROCHOT profile is triggered, a LOW pulse is asserted.
SDA	12	I^2C data I/O. Open drain output. Connect a 10kΩ pull-up resistor according to I^2C specification.
SCL	13	I^2C clock input. Connect a 10kΩ pull-up resistor according to I^2C specification.
CMPI	14	Input of independent comparator. Internal reference, output polarity and deglitch time is selectable by I^2C. With polarity HIGH (REG0x30[6]=1), place a resistor between CMPI and CMPO to program hysteresis. With polarity LOW (REG0x30[6]=0), the internal hysteresis is 100mV. This pin needs to be connected to ground if not in use.
CMPO	15	Open drain output of independent comparator. Place a 10kΩ pull-up resistor to power rail. Internal reference, output polarity and deglitch time are selectable by I^2C. This pin can be floating if not in use.
NC	16,17	Not connected.
CELL	18	Battery cell selection pin for 1-4 cell battery setting. CELL pin is biased from VDDX with a resistor divider. CELL pin also sets SYSOVP threshold to 5V for 1 cell, 12V for 2 cells, and 19.5V for 3 cells or 4 cells.
ISN	19	Battery charging current sense negative input in forward charging mode or discharging current sense positive input in reversed OTG or battery only mode.The leakage current on ISP and ISN are matched.
ISP	20	Battery charging current sense positive input in forward charging mode or discharging current sense negative input in reversed OTG or battery only mode.The leakage current on ISP and ISN are matched.
BATDRVB	21	The P-channel battery MOSFET (BATFET) gate driver output. It is shorted to VSYS to fully turn off the BATFET. It goes 10 V maximun below VSYS to fully turn on BATFET. BATFET is in linear mode to regulate VSYS at minimum system voltage when battery is depleted. BATFET is fully on during fast charge and works as an ideal diode in supplement mode.
VSYS	22	Charger system voltage sensing pin. The system voltage regulation limit is programmed in REG0x05/04() and REG0x0D/0C().
LX2	23	Inductor connecting point 2.
HDRV2	24	High side power MOSFET(Q4) driver output 2.
BST2	25	High side power MOSFET driver power supply 2. Connect a 47nF ceramic capacitor between BST2 and LX2 for bootstrap capacitor.
LDRV2	26	Low side power MOSFET(Q3) driver output 2.
GND	27	Power ground.
REGN	28	LDO output for power stage gate driver. Connect a 2.2μF ceramic capacitor from REGN to GND.
LDRV1	29	Low side power MOSFET(Q2) driver output 1.

BST1	30	High side power MOSFET driver power supply 1. Connect a 47nF ceramic capacitor between BST1 and LX1 for bootstrap capacitor.
HDRV1	31	High side power MOSFET(Q1) driver output 1.
LX1	32	Inductor connecting point 1.
Thermal pad	-	Exposed pad beneath the IC. Always solder thermal pad to the board, and have vias on the thermal pad plane connecting to power ground planes. It serves as a thermal pad to dissipate the heat.

6 Specifications

6.1 Absolute Maximum Ratings (Note 1)

ISN, ISP, ACN, ACP, VBUS, VSYS, LX1, LX2 ---------- -0.3V to 30V
BST1, BST2, HDRV1, HDRV2 ---------- -0.3V to 36V
SDA, SCL, REGN, PSYS, CHRG_OK, OTG_VAP, CELL, ILIM_HIZ, LDRV1, LDRV2, VDDX, CMPI, CMPO, PROCHOTB, IAC, IBAT ---------- -0.3V to 6V
BST1-LX1, BST2-LX2, HDRV1-LX1, HDRV2-LX2 ---------- -0.3V to 6V
ISP-ISN, ACP-ACN ---------- -0.5V to 0.5V
BATDRVB-VSYS ---------- -15V to 0.3V
Package Thermal Resistance (Note 2)
QFN4x4-32, θ_{JA} ---------- 33.3 °C/W
QFN4x4-32, θ_{JC} ---------- 29.7 °C/W
Junction Temperature Range ---------- -40°C to 150°C
Operating Temperature Range ---------- -40°C to 100°C
Storage Temperature ---------- -65°C to 150°C
Lead Temperature (Soldering, 10s) ---------- 260°C

6.2 ESD Susceptibility

HBM (Human Body Mode) ---------- ±2kV
CDM (Charged Device Mode) ---------- ±750V

6.3 Recommended Operating Conditions (Note 3)

ISN, ISP, ACN, ACP, VBUS, VSYS, LX1, LX2 ---------- -0.3V to 25V
BST1, BTST2, HDRV1, HDRV2 ---------- -0.3V to 30V
SDA, SCL, REGN, PSYS, CHRG_OK, OTG_VAP, CELL, ILIM_HIZ, LDRV1, LDRV2, VDDX, CMPI, CMPO, PROCHOTB, IAC, IBAT ---------- -0.3V to 5.5V
ACP-ACN, ISP-ISN ---------- -0.35V to 0.35V
BATDRVB-VSYS ---------- -12V to 0.3V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

6.4 Electrical Characteristics

(T_J = -40°C to 125°C, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IN_OP}	VBUS, input voltage operating range		3.5		25	V
Charge Voltage Regulation						
V_{BAT_RNG}	Charge voltage regulation range	Voltage on ISN pin	1.024		19.2	V
$V_{BAT\_REG\_ACC}$	Charge voltage regulation accuracy (0°C to 85°C)	REG0x05/04() = 0x41A0		16.8		V
			-0.48%		0.52%	
		REG0x05/04() = 0x3138		12.6		V
			-0.5%		0.5%	
		REG0x05/04() = 0x20D0		8.4		V
			-0.56%		-0.64%	
		REG0x05/04() = 0x1068		4.2		V
			-0.7%		0.8%	
Charge Current Regulation						
V_{ICHG_RNG}	Charge current regulation differential voltage range	V_{ISP} –V_{ISN}, 10mΩ sense resistor	0		81.28	mV
$I_{CHG\_REG\_ACC}$	Charge current regulation accuracy with 10mΩ sense resistor (0°C to 85°C)	REG0x03/02() = 0x1000		4096		mA
			-2%		2.5%	
		REG0x03/02() = 0x0800		2048		mA
			-2%		3%	
		REG0x03/02() = 0x0400		1024		mA
			-5%		5%	
		REG0x03/02() = 0x0200		512		mA
			-10%		10%	
Pre-Charge Current Regulation						
I_{PRECHG_CLAMP}	Pre-charge current clamp	2s-4s		384		mA
		1s, V_{ISN} < 3V		384		mA
		1s, 3V < V_{ISN} < V_{SYSMIN}		2		A
$I_{PRECHG\_REG\_ACC}$	Pre-charge current regulation accuracy with 10mΩ sense resistor (0°C to 85°C)	REG0x03/02() = 0x0180		384		mA
			-15%		15%	
		REG0x03/02() = 0x0100		256		mA
			-20%		20%	
		REG0x03/02() = 0x00C0		192		mA
			-25%		25%	
		REG0x03/02() = 0x0080		128		mA
		2s-4s	-30%		30%	
$I_{LEAK\_ISP\_ISN}$	ISP,ISN leakage current mismatch (0°C to 85°C)		-16.5		12.5	μA

Input Current Regulation						
$V_{IINDPM\_REG\_RNG}$	Adapter current regulation differential voltage range	V_{ACP} –V_{ACN}, 10mΩ sense resistor	0.5		64	mV
$I_{INDPM\_REG\_ACC}$	Adapter current regulation accuracy (-40°C to 105°C) with 10mΩ ACP/ACN series resistor	REG0x0F/0E() = 0x4FFF	3800	3900	4000	mA
		REG0x0F/0E() = 0x3BFF	2800	2900	3000	mA
		REG0x0F/0E() = 0x1DFF	1300	1400	1500	mA
		REG0x0F/0E() = 0x09FF	300	400	500	mA
$I_{LEAK\_ACP\_ACN}$	ACP,ACN leakage current mismatch (0°C to 85°C)		-15		14.5	μA
V_{IINDPM_LIM}	Voltage range for input current regulation (ILIM_HIZ Pin)		1		4	V
$I_{INDPM\_REG\_ACC\_LIM}$	Adapter current limit accuracy on ILIM_HIZ Pin, V_{ILIM_HIZ}= 1V+ 40×I_{DPM}×R_{AC}, with 10mΩ ACP/ACN series resistor	V_{ILIM_HIZ}=2.6V	3900	4000	4150	mA
		V_{ILIM_HIZ}=2.2V	2900	3000	3150	mA
		V_{ILIM_HIZ}=1.6V	1400	1500	1600	mA
		V_{ILIM_HIZ}=1.2V	350	500	700	mA
I_{LEAK_ILIM}	ILIM_HIZ pin leakage current		-1		1	μA
Input Voltage Regulation						
V_{INDPM_RNG}	Input voltage regulation range	Voltage on VBUS pin	3.2		19.52	V
$V_{INDPM\_REG\_ACC}$	Input voltage regulation accuracy	REG0x0B/0A() = 0x3C80		18688		mV
			-1.8%		1.5%	
		REG0x0B/0A() = 0x1E00		10880		mV
			-2%		2%	
		REG0x0B/0A() = 0x0500		4480		mV
			-3.5%		3%	
Minimum System Voltage Regulation						
V_{SYSMIN_RNG}	Minimum system voltage range	Voltage on VSYS pin	1.024		16.128	V
$V_{SYSMIN\_REG\_ACC}$	Minimum system voltage regulation accuracy (V_{BAT} below REG0x0D/0C() setting)	REG0x0D/0C() = 0x3000		12.288		V
			-2%		1.5%	
		REG0x0D/0C() = 0x2400		9.216		V
			-2%		1.5%	
		REG0x0D/0C() = 0x1800		6.144		V
			-2.5%		2%	
		REG0x0D/0C() = 0x0E00		3.584		V
			-2.5%		3.5%	
Maximum System Voltage Regulation						
V_{SYSMAX_RNG}	System voltage range (charge disabled)		1.024		19.2	V
V_{SYSMAX_ACC}	System voltage regulation accuracy(charge disabled)	REG0x05/04() = 0x41A0		V_{ISN}+ 200mV		
			-2%		2%	
		REG0x05/04() = 0x3138		V_{ISN}+ 200mV		

			-2%		2%	
		REG0x05/04() = 0x20D0		V_{ISN}+ 200mV		
			-2%		2%	
		REG0x05/04() = 0x1068		V_{ISN}+ 200mV		
			-2.5%		2.5%	
OTG Voltage Regulation						
$V_{OTG\_REG\_RNG}$	OTG voltage regulation range	Voltage on VBUS pin	3		20.8	V
$V_{OTG\_REG\_ACC}$	OTG voltage regulation accuracy	REG0x07/06()=0x23F8; 0x34[2]=0		20		V
			-2%		2%	
		REG0x07/06()=0x1710; 0x34[2]=1		12		V
			-2%		2%	
		REG0x07/06()=0x099C; 0x34[2]=1		5		V
			-3%		3%	
OTG Current Limit						
$V_{IOTG\_REG\_RNG}$	OTG output current regulation differential voltage range	V_{ACN} –V_{ACP}, 10mΩ sense resistor	0		81.28	mV
I_{OTG_ACC}	OTG current limit accuracy	REG0x09/08()=0x3C00	2900	3000	3100	mA
		REG0x09/08()=0x1E00	1400	1500	1600	mA
		REG0x09/08()=0x0A00	400	500	600	mA
REGN REGULATOR						
V_{REGN}	REGN LDO voltage	VBUS=10V	4.9	5.2	5.5	V
I_{REGN_LIM}	REGN current limit	VBUS=10V, V_{REGN}=4.5V	50	85		mA
$V_{DROPOUT}$	REGN voltage in drop out mode	VBUS=5V, I_{Load}=20mA	4	4.5	4.8	V
C_{REGN}	REGN output capacitor required for stability	Load current 100μA to 50mA	2.2			μF
C_{VDDX}	VDDX output capacitor required for stability	Load current 100μA to 50mA	1			μF
Current Sense Amplifier						
V_{IAC_CLAMP}	IAC output clamp voltage		3.1	3.2	3.3	V
A_{IAC}	Adapter current sense amplifier gain	Input current sense amplifier gain (REG0x00[4] = 0)		20		V/V
		Input current sense amplifier gain (REG0x00[4] = 1)		40		V/V
I_{IAC}	IAC output clamp current			1.8		mA
V_{IBAT_CLAMP}	IBAT output clamp voltage		3.1	3.2	3.3	V
A_{IBAT}	BAT current sense amplifier gain	Discharge current sense amplifier gain (REG0x00[3] = 0)		8		V/V
		Discharge current sense amplifier gain (REG0x00[3] = 1)		16		V/V
I_{IBAT}	IBAT output clamp current			2.1		mA
V_{ACP/ACN_OP}	Input common mode range	Voltage on ACP/CAN pin	3.5		26	V
V_{ISP/ISN_OP}	Battery common mode range	Voltage on ISP/ISN pin	2.5		18	V

V_{IAC_ACC}	Input current monitor accuracy, T_A= 0°C to 85°C	V_{ACP}-V_{ACN} =40.96mV	-2%		2%	
		V_{ACP}-V_{ACN} =20.48mV	-3%		3%	
		V_{ACP}-V_{ACN} =10.24mV	-6%		6%	
		V_{ACP}-V_{ACN} =5.12mV	-11%		11%	
V_{IBAT_ACC}	Charge and discharge current monitor accuracy, T_A= 0°C to 85°C	V_{ISN}-V_{ISP} =40.96mV	-2.5%		2.5%	
		V_{ISN}-V_{ISP} =20.48mV	-4%		4%	
		V_{ISN}-V_{ISP} =10.24mV	-6%		6%	
		V_{ISN}-V_{ISP} =5.12mV	-15%		15%	
System Power Sense Amplifier						
V_{PSYS}	PSYS output voltage range		0		3.3	V
I_{PSYS}	PSYS output clamp current			300		μA
A_{PSYS}	System power Sense amplifier gain	V_{PSYS}/[(P_{IN}+P_{BAT})xR_{PSYS}] (REG0x31[1] = 1)		1		μA/W
V_{PSYS_ACC}	PSYS gain accuracy, (REG0x31[1] = 1)	Adapter only with system power=19.5V/45W, T_A= 0°C to 85°C	-5%		5%	
		Battery only with system power=11V/44W, T_A= 0°C to 85°C	-3.5%		3%	
V_{PSYS_CLAMP}	PSYS clamp voltage		3		3.3	V
VBUS UVLO Comparator						
V_{VBUS_UVLOZ}	VBUS under voltage rising threshold	VBUS rising threshold	2.30	2.55	2.80	V
V_{VBUS_UVLO}	VBUS under voltage falling threshold	VBUS falling threshold	2.18	2.40	2.62	V
$V_{VBUS\_UVLO\_HYS}$	VBUS under voltage hysteresis			150		mV
V_{VBUS_CONVEN}	VBUS enable switching rising threshold	VBUS rising threshold	3.2	3.5	3.9	V
$V_{VBUS\_CONVENZ}$	VBUS enable switching falling threshold	VBUS falling threshold	2.9	3.2	3.5	V
$V_{VBUS\_CONVEN\_HYS}$	VBUS enable switching hysteresis			300		mV
BAT UVLO Comparator						
V_{VBAT_UVLOZ}	VBAT UVLO rising threshold	V_{ISN} rising threshold	2.35	2.55	2.75	V
V_{VBAT_UVLO}	VBAT UVLO falling threshold	V_{ISN} falling threshold	2.2	2.4	2.6	V
$V_{VBAT\_UVLO\_HYS}$	VBAT UVLO hysteresis			150		mV
V_{VBAT_OTGEN}	VBAT OTG enable switching rising threshold	V_{ISN} rising threshold	3.25	3.6	3.85	V
V_{VBAT_OTGENZ}	VBAT OTG enable switching falling threshold	V_{ISN} falling threshold	2.2	2.4	2.6	V
$V_{VBAT\_OTGEN\_HYS}$	VBAT OTG enable switching hysteresis			1.2		V
VBUS Under Voltage(UV) Comparator (OTG mode)						
$V_{VBUS\_OTG\_UV}$	VBUS UV falling threshold	As percentage of REG0x07/06()		85%		
$t_{VBUS\_OTG\_UV}$	VBUS UV deglitch time			7		ms

VBUS Over Voltage(OV) Comparator (OTG mode)						
$V_{VBUS\_OTG\_OV}$	VBUS OV rising threshold	As percentage of REG0x07/06()		110%		
$t_{VBUS\_OTG\_OV}$	VBUS OV deglitch time			10		ms
Pre-charge to Fast Charge/ Fast Charge to Pre-charge Transition Comparator						
$V_{BAT\_SYSMIN\_RISE}$	Pre-charge to fast charge threshold	V_{ISN} rising, as percentage of REG0x0D/0C()	98%	100%	102%	
$V_{BAT\_SYSMIN\_FALL}$	Fast charge to pre-charge threshold	V_{ISN} falling, as percentage of REG0x0D/0C()		97.5%		
$V_{BAT\_SYSMIN\_HYS}$	Fast charge mode to pre-charge mode hysteresis	As percentage of REG0x0D/0C()		2.5%		
BATLOWV Comparator (Pre-charge to Fast Charge Threshold for 1s)						
V_{BATLV_FALL}	BATLOWV falling threshold			2.8		V
V_{BATLV_RISE}	BATLOWV rising threshold			3		V
V_{BATLV_HYS}	BATLOWV hysteresis			200		mV
ACOV Comparator						
V_{ACOV_RISE}	VBUS OV rising threshold	VBUS rising	25	26	27	V
$t_{ACOV\_RISE\_DEG}$	VBUS OV deglitch time	VBUS rising to stop switching		1		µs
V_{ACOV_FALL}	VBUS OV falling threshold	VBUS falling	23.5	24.5	25.5	V
$t_{ACOV\_FALL\_DEG}$	VBUS OV deglitch time	VBUS falling to restart switching		1		ms
V_{ACOV_HYS}	VBUS OV hysteresis			1.5		V
ACOC Comparator						
V_{ACOC}	Input current rising threshold for throttling as 200% of ILIM2 (REG0x37[7:3])	REG0x32[2] = 1	180%	200%	220%	
V_{ACOC_FLOOR}	V_{ACP}-V_{ACN} during ACOC	Set IDPM to minimum	44	50	56	mV
$V_{ACOC\_CEILING}$		Set IDPM to maximum	172	180	188	mV
$t_{ACOC\_DEG\_RISE}$	Rising deglitch time	Deglitch time to trigger ACOC		250		µs
t_{ACOC_RELAX}	Relax time	Relax time before converter starts again		250		ms
System Over-Voltage Comparator (SYSOVP)						
V_{SYSOVP_RISE}	System overvoltage rising threshold to turn off converter	1s	4.75	5	5.15	V
		2s	11.6	12	12.2	V
		3s, 4s	18.8	19.5	20	V
V_{SYSOVP_FALL}	System overvoltage falling threshold	1s	4.6	4.8	4.9	V
		2s	11	11.5	12	V
		3s, 4s	18.4	19	19.6	V
I_{SYSOVP}	Discharge current during SYSOVP	on VSYS pin		18		mA
BAT Over-Voltage Comparator (BATOVP)						
V_{BATOVP_RISE}	Overvoltage rising threshold as percentage of V_{BAT_REG} in REG0x05/04()	1s, 4.2V	102%	104%	106%	
		2s - 4s	102%	104%	105%	
V_{BATOVP_FALL}	Overvoltage falling threshold as percentage of V_{BAT_REG} in REG0x05/04()		100%	102%	104%	

V_{BATOVP_HYS}	Overvoltage hysteresis as percentage of V_{BAT_REG} in REG0x05/04()			2%		
I_{BATOVP}	Discharge current during BATOVP	on VSYS pin		15		mA
t_{BATOVP_RISE}	Overvoltage rising deglitch time to disable charge			1		µs
Converter Over-Current Comparator (Q2)						
V_{OCP_Q2}	Converter overcurrent limit	REG0x32[5]=1		170		mV
		REG0x32[5]=0		240		mV
$V_{OCP\_SYSSHORT\_Q2}$	System short	REG0x32[5]=1		50		mV
		REG0x32[5]=0		70		mV
Converter Over-Current Comparator (ACX)						
V_{OCP_ACX}	Converter overcurrent limit	REG0x32[4]=1		150		mV
		REG0x32[4]=0		280		mV
$V_{OCP\_SYSSHORT\_ACX}$	System short	REG0x32[4]=1		90		mV
		REG0x32[4]=0		150		mV
Thermal Shutdown Comparator						
T_{TSD_RISE}	Thermal shutdown rising temperature threshold	Temperature increasing		155		℃
T_{TSD_FALL}	Thermal shutdown falling temperature threshold	Temperature falling		135		℃
T_{TSD_HYS}	Thermal shutdown temperature hysteresis			20		℃
T_{TSD_RDEG}	Thermal shutdown rising deglitch time			100		µs
T_{TSD_FDEG}	Thermal shutdown falling deglitch time			12		ms
VSYS PROCHOT Comparator						
V_{SYS_TH1}	VSYS_TH1 comparator falling threshold	REG0x36[7:4] = 0111, 2-4s		6.6		V
		REG0x36[7:4] = 0100, 1s		3.5		V
V_{SYS_TH2}	VSYS_TH2 comparator falling threshold	REG0x36[3:2] = 10, 2-4s		6.5		V
		REG0x36[3:2] = 10, 1s		3.5		V
$t_{SYS\_PRO\_falling\_DEG}$	V_{SYS} falling deglitch time for throttling			4		µs
ICRIT PROCHOT Comparator						
V_{ICRIT_PRO}	Input current rising threshold for throttling as 10% above ILIM2 (REG0x37[7:3])	Only when ILIM2 setting is higher than 2A	105%	110%	117%	
INOM PROCHOT Comparator						
V_{INOM_PRO}	INOM rising threshold as 10% above IDPM (REG0x0F/0E())		105%	110%	116%	
IDCHG PROCHOT Comparator						
V_{IDCHG_PRO}	IDCHG threshold for throttling for IDCHG of 6 A	REG0x39[7:2] = 001100		6272		mA
			95%		105%	

INDEPENDENT Comparator						
V_{INDEP_CMP}	Independent comparator threshold	REG0x30[7] = 1, CMPI falling	1.165	1.2	1.24	V
		REG0x30[7] = 0, CMPI falling	2.245	2.3	2.345	V
$V_{INDEP\_CMP\_HYS}$	Independent comparator hysteresis	REG0x30[7] = 0, CMPI falling		100		mV
PWM Oscillator						
F_{sw}	PWM switching frequency	REG0x01[1] = 0	990	1200	1360	kHz
		REG0x01[1] = 1	660	800	925	kHz
BATFET Gate Driver (BATDRVB)						
V_{BATDRV_ON}	Gate drive clamp voltage on BATFET	V_{SYS}-$V_{BATDRVB}$	8.5	10	11.5	V
V_{BATDRV_DIODE}	Drain-source voltage on BATFET during ideal diode operation			35		mV
R_{BATDRV_ON}	Measured by sourcing 10μA current to BATDRVB		5	8	11	kΩ
R_{BATDRV_OFF}	Measured by sinking 10μA current to BATDRVB			5.8		kΩ
PWM High Side Driver (HDRV1 Q1)						
$R_{DS\_HI\_ON\_Q1}$	High side driver turn on resistance	V_{BST1} - V_{LX1} = 5 V		8		Ω
$R_{DS\_HI\_OFF\_Q1}$	High side driver turn off resistance	V_{BST1} - V_{LX1} = 5 V		3		Ω
$V_{BTST1\_REFRESH}$	Bootstrap refresh comparator falling threshold voltage	V_{BST1} - V_{LX1} when low side refresh pulse is requested		2.9		V
PWM High Side Driver (HDRV2 Q4)						
$R_{DS\_HI\_ON\_Q4}$	High side driver turn on resistance	V_{BST2} - V_{LX2} = 5 V		8		Ω
$R_{DS\_HI\_OFF\_Q4}$	High side driver turn off resistance	V_{BST2} - V_{LX2} = 5 V		3		Ω
$V_{BTST2\_REFRESH}$	Bootstrap refresh comparator falling threshold voltage	V_{BST2} - V_{LX2} when low side refresh pulse is requested		2.9		V
PWM Low Side Driver (LDRV1 Q2)						
$R_{DS\_LO\_ON\_Q2}$	Low side driver turn on resistance			7		Ω
$R_{DS\_LO\_OFF\_Q2}$	Low side driver turn off resistance			2.5		Ω
PWM Low Side Driver (LDRV2 Q3)						
$R_{DS\_LO\_ON\_Q3}$	Low side driver turn on resistance			8.5		Ω
$R_{DS\_LO\_OFF\_Q3}$	Low side driver turn off resistance			3.3		Ω
Internal Soft Start During Charge Enable						
I_{STEP}	Soft start step size			64		mA
t_{STEP}	Soft start step time			8		μs
Logic Input (SCL, SDA, OTG_VAP)						
V_{IN_LO}	Input low threshold				0.4	V
V_{IN_HI}	Input high threshold		1.3			V

Logic Output Open Drain (CHRG_OK, SDA, CMPO)						
V_{OUT_LO}	Output saturation voltage	5 mA drain current			0.4	V
Logic Output Open Drain (PROCHOTB)						
$V_{OUT\_LO\_PROCHOT}$	V_{OUT_LO}, output saturation voltage	5 mA drain current			0.3	V
Analog Input (ILIM_HIZ)						
V_{HIZ_LO}	Voltage to get out of HIZ mode	ILIM_HIZ pin rising	0.8			V
V_{HIZ_HIGH}	Voltage to enable HIZ mode	ILIM_HIZ pin falling			0.4	V
Analog Input (CELL)						
V_{CELL_4S}	4s	VDDX = 5V, as percentage of VDDX	68.4%	75%		
V_{CELL_3S}	3s		51.7%	55%	65%	
V_{CELL_2S}	2s		35%	40%	49.1%	
V_{CELL_1S}	1s		18.4%	25%	31.6%	
V_{CELL_RISE}	Battery is present	V_{CELL} rising, as percentage of VDDX	18%			
V_{CELL_FALL}	Battery is removed	V_{CELL} falling, as percentage of VDDX			15%	
Quiescent Current						
$I_{BAT\_BATFET\_ON}$	Battery supply current	V_{BAT} = 18V, REG0x01[7] = 1, in low power mode		24	45	μA
		V_{BAT} = 18V, REG0x01[7] = 1, in low power mode, REG0x31[5] = 1, REGN off		60	160	μA
		V_{BAT} = 18 V, REG0x01[7] = 0, in performance mode, REG0x31[4] = 0, REGN on, disable PSYS		880	1150	μA
		V_{BAT} = 18 V, REG0x01[7] = 0, in performance mode, REG0x31[4] = 1, REGN on, enable PSYS		980	1250	μA
I_{AC_SW}	Adapter supply current (system is no load and charging is disabled)	V_{IN} = 20 V, V_{BAT} = 12.6 V, 3s, REG0x01[2] = 0, F_{SW}=800kHz, MOSFET Qg = 6.8 nC		3.2		mA
		V_{IN} = 5 V, V_{BAT} = 8.4 V, 2s, REG0x01[2] = 0, F_{SW}=800kHz MOSFET Qg = 6.8 nC		6		mA
		V_{IN} = 12 V, V_{BAT} = 12 V, REG0x01[2] = 0, F_{SW}=800kHz MOSFET Qg = 6.8 nC		3		mA
I_{BAT_SW}	Battery supply current in OTG mode (system and OTG output are both no load)	V_{BAT} = 8.4 V, VBUS = 5 V, F_{SW}=800kHz, MOSFET Qg = 6.8nC		3.1		mA
		V_{BAT} = 8.4 V, VBUS = 12 V, F_{SW}=800kHz, MOSFET Qg = 6.8nC		6.3		mA
		V_{BAT} = 8.4 V, VBUS = 20 V, F_{SW}=800kHz, MOSFET Qg = 6.8nC		9		mA

6.5 Timing Requirements

Parameter	Test Conditions	Min	Typ	Max	Unit
$F_{S(CLK)}$	Clock frequency	10		100	kHz
t_{RISE}	SCL/SDA rise time			1	μs
t_{FALL}	SCL/SDA fall time			300	ns
$t_{W(HIGH)}$	SCL pulse width HIGH	4		50	μs
$t_{W(LOW)}$	SCL pulse width LOW	4.7			μs
$t_{SET(START)}$	Setup time for START condition	4.7			μs
$t_{HOLD(START)}$	START condition hold time after which first clock pulse is generated	4			μs
$t_{SET(DAT)}$	Data setup time	250			ns
$t_{HOLD(DAT)}$	Data hold time	300			ns
$t_{SET(STOP)}$	Setup time for STOP condition	4			μs
$t_{FREE(BUS)}$	Bus free time between START and STOP condition	4.7			μs
$t_{timeout}$	I^2C bus release timeout		30		ms
t_{Deg_WD}	Deglitch for watchdog reset signal	10			ms
t_{WD}	Watchdog timeout period, REG0x01[6:5] = 01	4	5.5	7	s
	Watchdog timeout period, REG0x01[6:5] = 10	70	88	105	s
	Watchdog timeout period, REG0x01[6:5] = 11	140	175	210	s

Note 1: Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

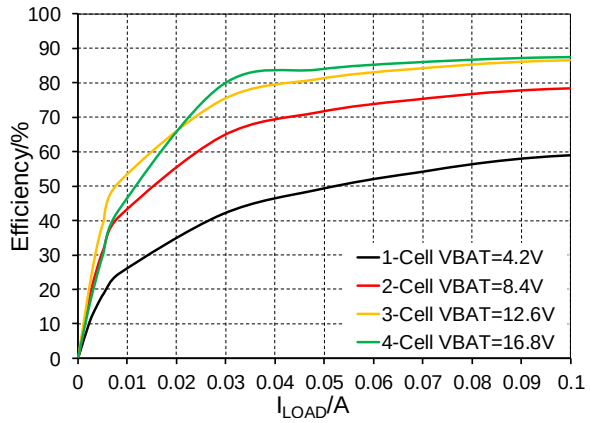
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective four layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

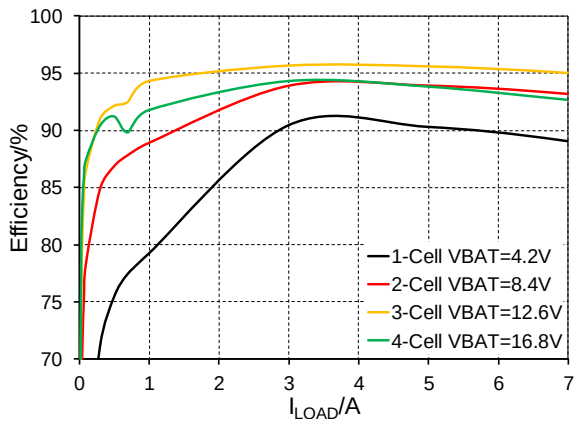
6.6 Typical Characteristics

T_A=25°C, VBUS=20V. Charge is disabled. Enable OOA. L=2.2μH(SPM6530T-2R2M), Q1~Q4:SIR472DP, Q5:BSC080P03LS, R_{AC}=10mΩ, R_{IS}=10mΩ, F_{sw}=800kHz.

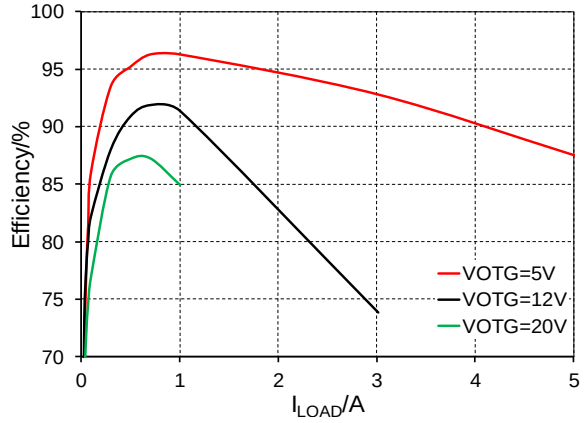
Light Load Efficiency



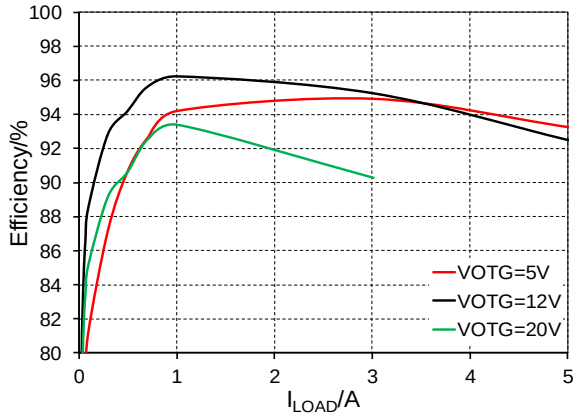
System Efficiency



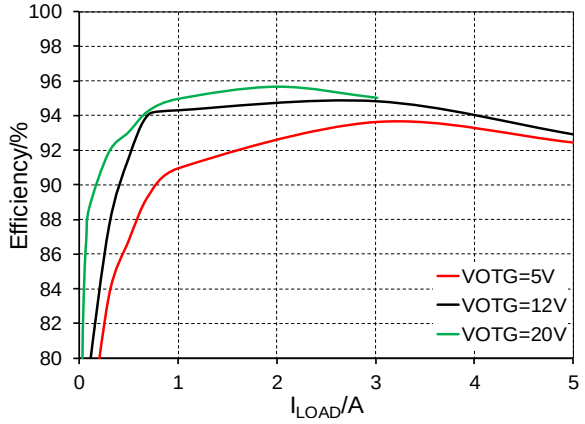
OTG Efficiency with 1-Cell VBAT=4.2V



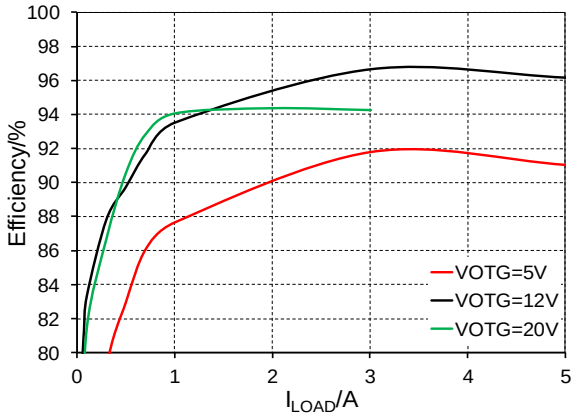
OTG Efficiency with 2-Cell VBAT=8.4V



OTG Efficiency with 3-Cell VBAT=12V

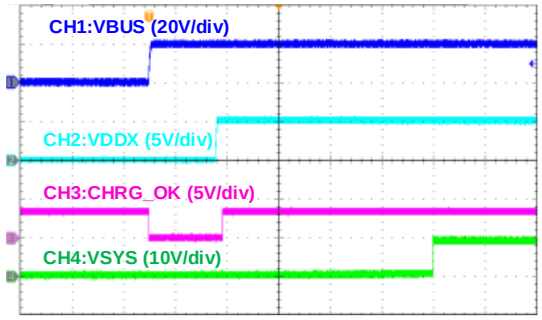


OTG Efficiency with 4-Cell VBAT=16.8V



Power Up from 20V VBUS

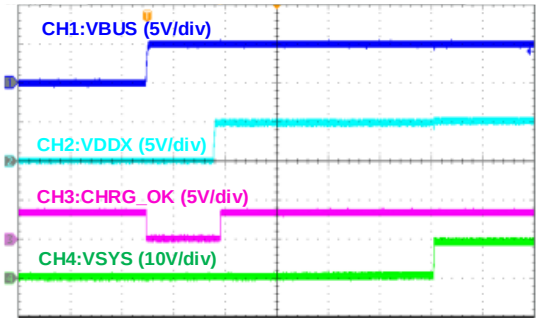
3-cell without battery



Time (40ms/div)

Power Up from 5V VBUS

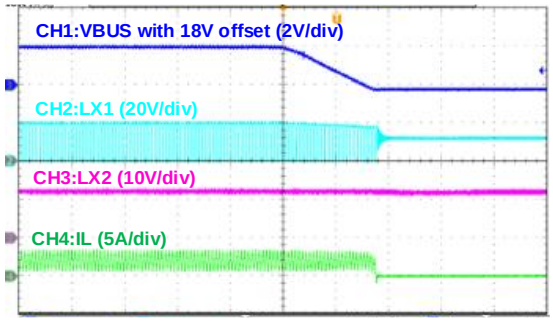
3-cell without battery



Time (40ms/div)

Power Off from 20V VBUS

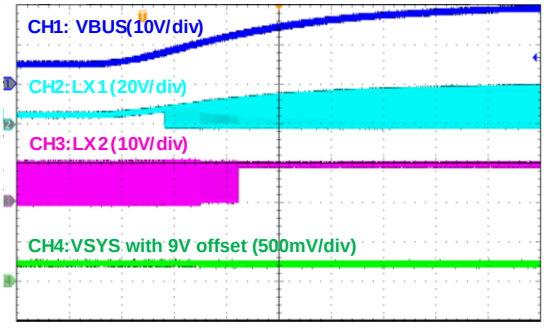
3-cell, VBAT=12V



Time (20μs/div)

System Regulation

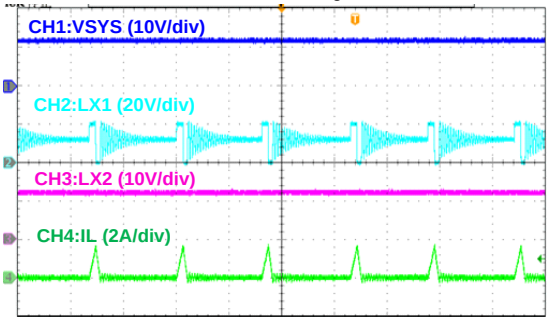
3-cell without battery, VBUS=5V->20V



Time (10ms/div)

PFM Operation

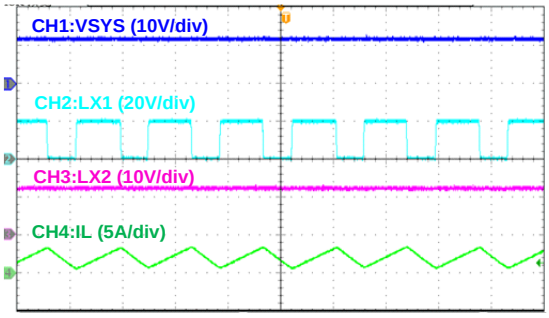
3-cell battery, VBUS=20V, VSYS=12V, ISYS=0.1A, disable charge



Time (4μs/div)

PFM Operation

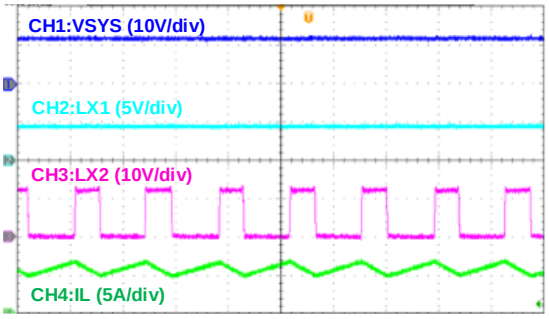
3-cell battery, VBUS=20V, VSYS=12V, ISYS=2A, disable charge



Time (1μs/div)

PFM Operation

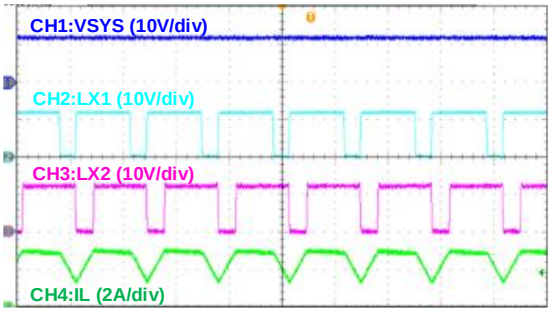
3-cell battery, VBUS=5V, VSYS=12V, ISYS=2A, disable charge



Time (1μs/div)

PFM Operation

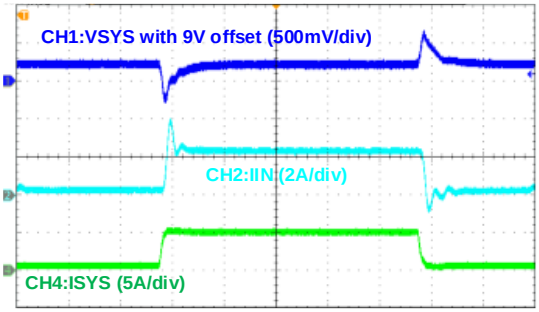
3-cell battery, VBUS=12V, VSYS=12V, ISYS=2A, disable charge



Time (1μs/div)

System Regulation in Buck Mode

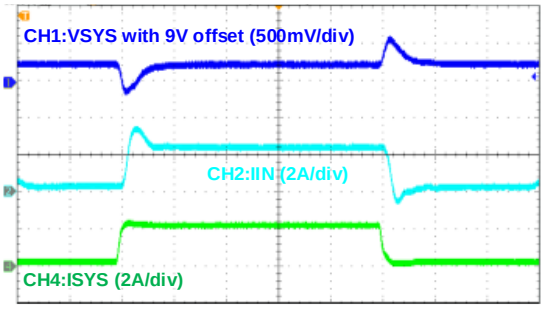
VBUS=20V/3.3A, VSYS=9.216V without battery
ISYS=0.5A->5A->0.5A



Time (100μs/div)

System Regulation in Buckboost Mode

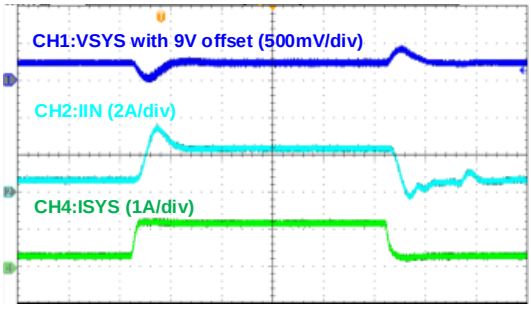
VBUS=9V/3.3A, VSYS=9.216V without battery
ISYS=0.2A->2.2A->0.2A



Time (100μs/div)

System Regulation in Boost Mode

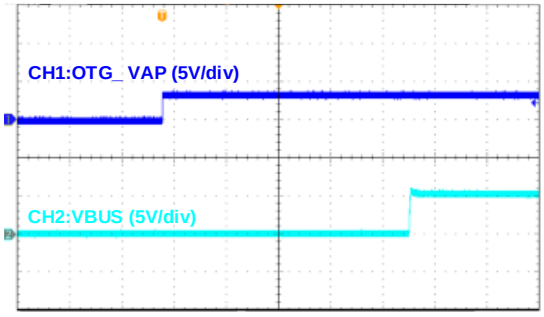
VBUS=5V/3.3A, VSYS=9.216V, ISYS=0.3A->1.2A->0.3A



Time (100μs/div)

OTG Power Up from 12V VBAT

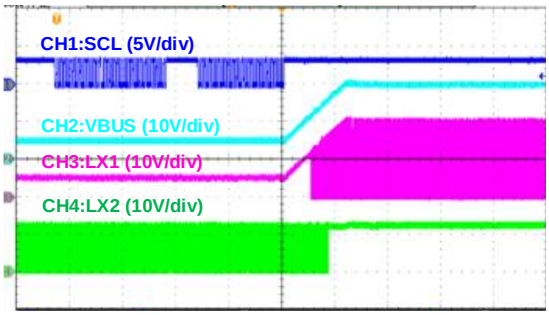
VBUS=5V



Time (4ms/div)

OTG Voltage Ramp Up

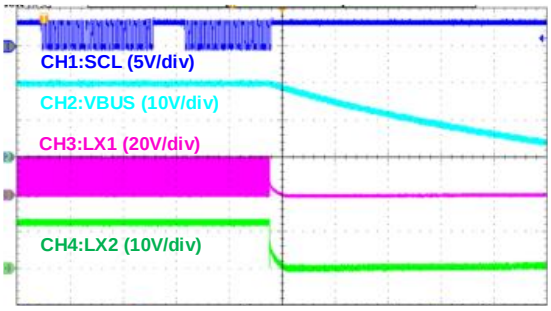
3-cell battery, VBAT=12V, VBUS=5V->20V, IOTG=0.5A



Time (200μs/div)

OTG Power Off

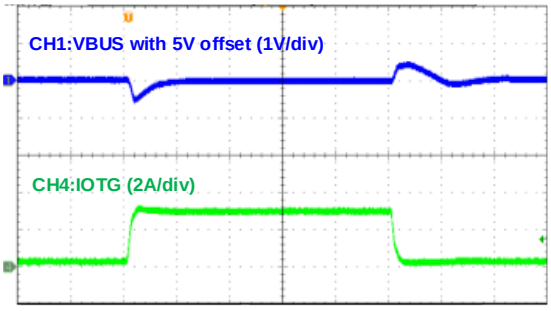
3-cell battery, VBAT=12V, VBUS=20V, IOTG=0.5A



Time (200μs/div)

OTG Load Transient in Buck Mode

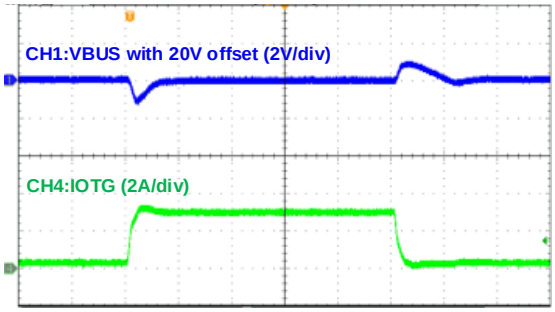
3-cell battery, VBAT=12V, VBUS=5V, IOTG=0.3A->3A->0.3A



Time (100μs/div)

OTG Load Transient in Boost Mode

3-cell battery, VBAT=12V, VBUS=20V, IOTG=0.3A->3A->0.3A



Time (100μs/div)

7 Function Description

The SY20776D is a Narrow VDC Buck-Boost charger controller for portable electronics. It supports wide range of power sources from 3.5 V to 25 V, and charges 1-4 cell battery. In the absence of input source, SY20776D supports OTG output from 1-4 cell battery to generate adjustable 3 V to 20.8 V at USB port with 8mV resolution.

When only the battery powers the system and no external load is connected to the USB OTG port, SY20776D provides the Vmin Active Protection (VAP) feature. The VAP is designed to absorb system power peaks during the periods of high demand to improve the system turbo performance.

The SY20776D features Dynamic Power Management (DPM) to limit the input voltage fall/input current rise, avoid AC adapter overloading.

The I^2C controls input current, input voltage, charge current and charge voltage registers with high resolution, high accuracy regulation.

The SY20776D also includes PSYS function to monitor the total platform power from adapter and battery. It also sets the PROCHOT timing and threshold profile to meet system requirements.

7.1 Functional Block Diagram

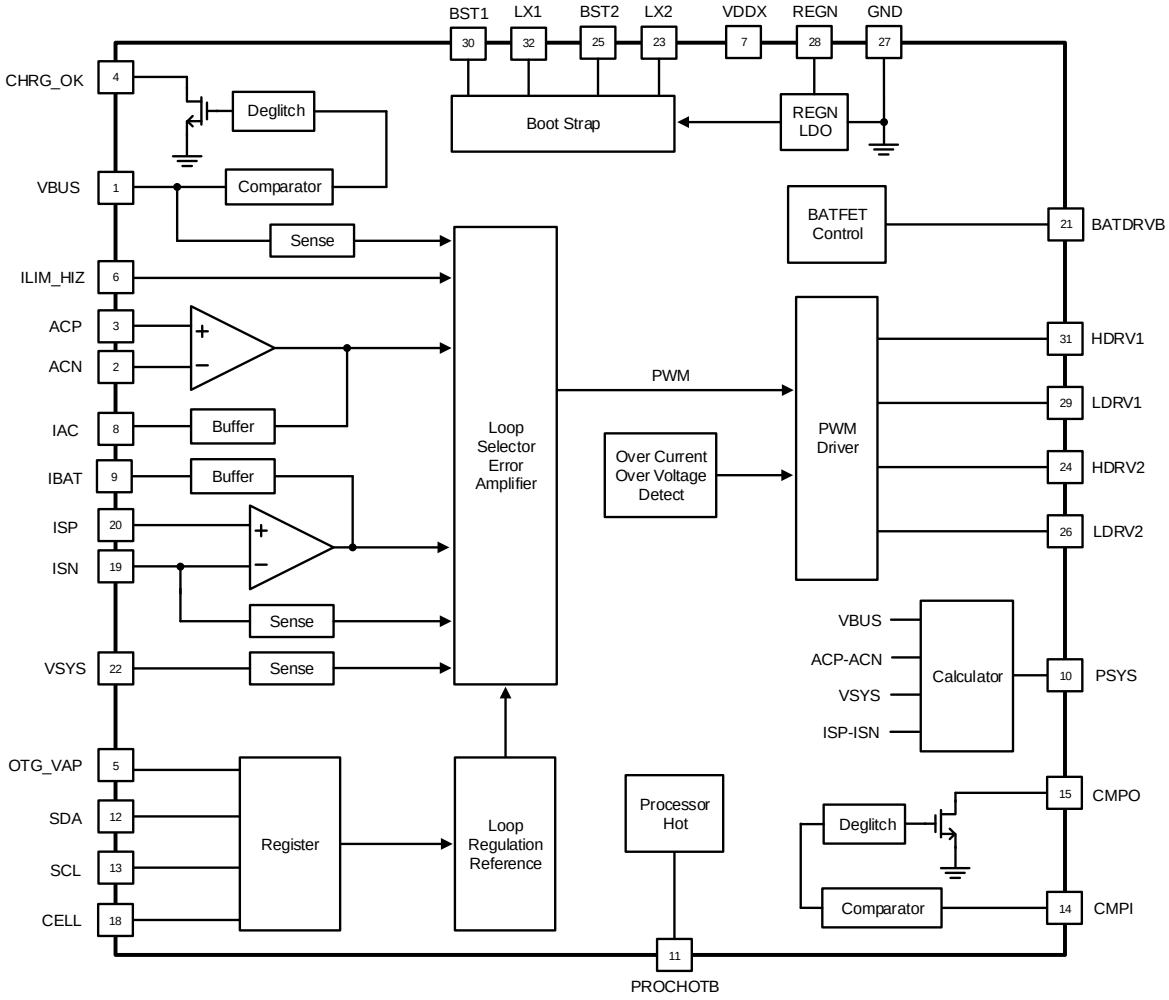


Figure 7-1. Functional Block Diagram

7.2 Power up

7.2.1 Power Up from Battery Only

When battery is present and adapter is absent, and the battery voltage is above V_{VBAT_UVLOZ}, the BATFET turns on to supply system.
By default, the charger is in low power mode(REG0x01[7]=1) with lowest quiescent current. The REGN LDO is always off. By setting REG0x31[5]=1, the independent comparator can be enabled to monitor the system voltage to assert PROCHOTB if the system power is too high.
When the charger enters performance mode (REG0x01[7]=0), the host can enable IBAT buffer through I^2C to monitor discharge current. The PSYS, PROCHOTB or independent comparator also can be enabled by the host through I^2C. In performance mode, the REGN LDO is always on to provide accurate reference and bias.

7.2.2 Power Up from DC Source

When an input source (such as an adapter) plugs in, the charger checks the input source voltage to turn on REGN LDO and all the bias circuits. It sets the input voltage/current limit before the converter starts. The power-up sequence from input source is as follows:

1. 50 ms after VBUS above V_{VBUS_CONVEN} and below V_{ACOV}, enable REGN LDO and CHRG_OK goes HIGH
2. Input voltage and current limit setup
3. Battery CELL configuration, charging voltage and minimum system voltage setup
4. 150 ms after CHRG_OK goes HIGH, converter powers up

7.2.3 Battery Cell Configuration

CELL pin is biased with a resistor divider from VDDX to CELL(refer to Figure 8-1). After VDDX is activated, the device detects the battery configuration through CELL pin bias voltage. Refer to Table 7-1 for cell setting thresholds.

Table 7-1. Battery Cell Configuration

Cell Count	Cell Voltage Refer to VDDX	Default Battery Charge Voltage	Default Minimum System Voltage	Fixed SYSOVP Threshold
4s	75%	16.800V	12.288V	19.5V
3s	55%	12.600V	9.216V	19.5V
2s	40%	8.400V	6.144V	12V
1s	25%	4.200V	3.584V	5V
Battery removal	15%			

7.2.4 Inductance Detection through IAC Pin

Before the converter starts up, the charger identifies the inductance value through the resistance tied to IAC pin. The recommended resistance is 93kΩ/137kΩ/169kΩ for 1μH/2.2μH/3.3μH inductor respectively.

Table 7-2. Inductance Detection through IAC Pin Resistor

Inductor In Use	Resistor on IAC Pin
1μH	93kΩ
2.2μH	137kΩ
3.3μH	169kΩ

7.2.5 Device HIZ State

If V_{ILIM_HIZ} < 0.4V (or REG0x35[7] = 1) and REG0x31[0]= 0, the device enters into HIZ mode.
During HIZ mode, the input source is present, and the charger is in the low quiescent current mode with REGN enabled.

7.3 Narrow VDC Architecture (NVDC) Power Path Management

SY20776D employs Narrow VDC architecture (NVDC) with BATFET separating system from battery. P-channel MOSFET is used for BATFET.

7.3.1 System Voltage Regulation

The minimum system voltage is set by MinSystemVoltage() register. Even with a deeply depleted battery, the system is regulated at the minimum system voltage.

When the charger is enabled, if $V_{BAT}<V_{SYSMIN}$, the system voltage is regulated at the higher between V_{SYSMIN} and V_{BAT}+200mV.The BATFET works at LDO mode with 384mA charging current clamp (maximum 2A with 1 cell battery setting). If $V_{BAT}> V_{SYSMIN}$, the BATFET is fully on when charging or in supplement mode, the voltage difference between the system and battery is voltage drop of BATFET and charging current sense resistor R_{IS}.

When the charger is disabled, the BATFET is always turned off. If $V_{BAT}< V_{SYSMIN}$, the system voltage is regulated at the higher between V_{SYSMIN} and V_{BAT}+200mV. If $V_{BAT}> V_{SYSMIN}$, the system voltage is regulated at V_{BAT}+200mV.

7.3.2 Dynamic Power Management (DPM)

The charger supports Dynamic Power Management (DPM). When the input current exceeds the input current setting, or the input voltage falls below the input voltage setting, the charger decreases the charge current to provide priority to the system load. Refer to section 7.13.8 and 7.13.9.

After CHRG_OK goes HIGH, the charger sets default input current limit(IDPM) and input voltage limit(VDPM).
The charger provides both external and internal input current limit setting. The actual input current limit is set by the lower setting of IIN_HOST (REG0x0F/0E) and ILIM_HIZ pin.
The device detects ILIM_HIZ pin voltage before the converter startup. The input current being adopted by ILIM_HIZ pin voltage is as follow:

$$V_{ILIM\_HIZ}= 1\ V + 40 \times I_{DPM} \times R_{AC}$$

When ILIM_HIZ pin voltage is below 0.4V, the device enters HIZ mode with low quiescent current. When ILIM_HIZ pin is above 0.8V, the device is out of HIZ mode. External ILIM_HIZ pin can be disabled by set REG0x32[7] =0 or pull the ILIM_HIZ pin above 4V.
The charger detects VBUS voltage under no load before the converter startup. The input voltage limit is set as follow:

$$V_{DPM}= VBUS - 1.28V$$

The input voltage limit is loaded to REG0x0B/0A() and the VDPM voltage can be revised by host through REG0x0B/0A().

7.3.3 Supplement Mode

When input source such as adapter is overloaded and the system voltage falls below the battery voltage, the battery supplies system by regulating BATFET at ideal diode mode. The BATFET gate driver (the voltage signal between VSYS and BATDRVB) is regulated so that the voltage difference between drain and source of BATFET stays around 35 mV. When the battery discharge current is low, BATFET ideal diode mode could prevent oscillation from entering and exiting the supplement mode.

7.4 Charging Mode

SY20776D supports 1-4 cell battery charging. Charging could be disabled by setting ChargeCurrent() to 0 or REG0x00[0]=1.

7.4.1 Auto Wakeup Charge

When the battery voltage is below the minimum system voltage if adapter plugs in, the device will automatically charge the battery with 128mA current for 30 minutes. Device will exit auto wakeup mode with only one of below events:

1. Set REG0x30[0]=0(AUTO_WAKEUP_EN) to disable auto wakeup
2. Write value command to ChargeCurrent() register
3. Battery voltage is charged up above V_{SYSMIN}

4. 30 minutes auto wakeup time out

When above condition occurs, the AUTO_WAKEUP_EN bit is reset to 0 automatically.

7.4.2 Pre-charge Mode

When battery voltage is lower than V_{SYSMIN}, the device runs in the pre-charge mode.

The BATFET is regulated at LDO mode by default and pre-charge current is clamped, the system voltage is regulated at minimum system voltage in REG0x0D/0C().For 1 cell battery, if battery voltage is below 3V, pre-charge current is clamped to 384mA. If battery voltage is between 3V and V_{SYSMIN}, charge current is clamped to 2A.For 2-4 cell battery, if battery voltage is below V_{SYSMIN}, pre-charge current is always clamped to 384mA.

When BATFET is removed, the system node VSYS is shorted to ISP, LDO disable mode should be enabled without BATFET (refer to Figure 4-1(b)). Before the converter starts operation, LDO mode needs to be disabled. The following sequence is required to configure without BATFET.

1. Before adapter plugs in, put the charger into HIZ mode(pull ILIM_HIZ pin to ground, or set REG0x35[7]=1)
2. Set REG0x00[2]=0 to disable LDO mode
3. Set REG0x30[0]=0 to disable auto wakeup mode
4. Set REG0x00[6]=1 to disable the hiccup mode during system short protection
5. Check if battery voltage is properly programmed (REG0x05/04())
6. Set pre-charge/charge current (REG0x03/02())
7. Put the device out of HIZ mode (Release ILIM_HIZ from ground and set REG0x35[7]=0)

No current clamp is applied in LDO disable mode. Thus, to ensure safety of battery charging, the charge current should be set properly by host when battery voltage is below V_{SYSMIN} voltage.

7.4.3 Fast Charge Mode

When battery voltage is above V_{SYSMIN}, the device enters fast charge mode. BATFET is fully on in fast charge mode. The charge current is regulated at the setting ChargeCurrent() register value. The charge current register is reset to 0, when following events occur:

1. Adapter is removed
2. Cell pin is pulled LOW
3. Write ChargeVoltage() register to 0

The charger fault will not reset ChargeCurrent() register.

7.4.4 Constant Voltage Charge

When battery voltage is close to maximum charge voltage setting, charge current is reduced under MaxCharge Voltage loop regulation automatically. By default, the device is without termination and BATFET is fully on. Though the charging path is still on, battery voltage is not be overcharged due to the MaxCharge Voltage loop. The host could terminate charging by setting the ChargeCurrent() register to 0 or REG0x00[0] =1 to inhibit charging. Maximum charge voltage is set by MaxCharge Voltage register(REG0x05/04()). Writing REG0x05/04() to 0 will set REG0x05/04() to the default value based on CELL pin, and force REG0x03/02() to 0 to disable charge.

7.5 USB On-The-Go (OTG)

The device supports USB OTG operation to deliver power from the battery to other portable devices through USB port. Below conditions need to meet to enter into the OTG mode:

OTG output voltage range (set by REG0x07/06()) is from 3V to 20.8V and OTG output current range (set by REG0x09/08()) is from 50mA to 6350mA.

1. Setting OTG voltage in REG0x07/06(). If REG0x34[2] = 0, the OTG output voltage is offset by 1.28V to achieve higher range from 4.28V~20.8V, if REG0x34[2] = 1, the OTG output voltage is from 3V to 19.52V
2. Setting OTG output current in REG0x09/08()
3. Setting REG0x35[4] = 1 and REG0x34[5] = 1. Pull EN_OTG pin HIGH
4. VBUS is below $V_{VBUS\_CONVENZ}$
5. 10 ms deglitch time after all conditions are valid, the converter starts and VBUS ramps up to target voltage. CHRG_OK pin goes HIGH if REG0x01[3] = 1

In OTG mode, if OTG output voltage V_{VBUS} is 10% higher than the setting OTG voltage and the deglitch time reaches, OTG over voltage protection is triggered. If OTG output voltage V_{VBUS} is 15% lower than setting OTG voltage and the deglitch time reaches, OTG under voltage protection is triggered. OTG over and under voltage both cause the device exits from OTG mode and reset the EN_OTG bit to 0.

If SYSOVP, BATOC, FORCE_LATCHOFF and thermal shutdown protection is triggered, the converter stops switching, but the EN_OTG bit is not reset to 0. Once above fault disappears, the OTG operation resumes.

7.6 Vmin Active Protection (VAP) when Battery only Mode

In VAP mode operation, the buck-boost charger delivers the energy from the battery to charge the voltage of the input decoupling capacitors as high as possible. With 1 or 2 cell battery only, VAP mode could absorb power peaks during periods of high demand. It could sustain the system voltage from drooping below the minimum system voltage and causing the system to crash.

Below conditions need to meet to enter into the VAP mode:

1. Set the voltage limit to charge VBUS in REG0x07/06()
2. Set the current limit to charge VBUS in REG0x09/08() and REG0x39[7:2]
3. Set the system voltage regulation point in REG0x0D[5:0], when the input capacitor supplements battery, the V_{SYSMIN} regulation loop will maintain VSYS at this regulation point
4. Set the VSYS_TH1 threshold to trigger the VAP discharging VBUS in REG0x36[7:4]
5. Set the VSYS_TH2 threshold to assert PROCHOTB active LOW signal to throttle SoC in REG0x36[3:2]
6. Enable the VAP mode by setting REG0x34[5] = 0, REG0x35[4] = 0, and pull the OTG_VAP pin HIGH

To exit VAP mode, the host should write either REG0x34[5] = 1 or pull the OTG_VAP pin LOW.

If SYSOVP, BATOC, FORCE_LATCHOFF and thermal shutdown protection is triggered will reset REG0x34[5] = 1, and the charger will exit VAP mode automatically.

7.7 Current and Power Monitor

7.7.1 High-Accuracy Current Sense Amplifier (IAC and IBAT)

The charger provides two high-accuracy current sense amplifiers to monitor the input current and the charge/discharge current (IBAT).

V_{IAC} = 20 or 40 × (V_{ACP} – V_{ACN}) during forward mode, 20 or 40 × (V_{ACN} – V_{ACP}) during reverse OTG mode.

V_{IBAT} = 8 or 16 × (V_{ISP} – V_{ISN}) during forward mode, 8 or 16 × (V_{ISN} – V_{ISP}) during forward supplement mode, or reverse OTG mode.

The gain of IAC can be programmed with 20 when REG0x00[4]=0 by default, and 40 when REG0x00[4]=1.

The gain of IBAT can be programmed with 16 when REG0x00[3]=1 by default, and 8 when REG0x00[3]=0.The IBAT pin monitors battery discharging current when REG0x32[6]=0 by default,and battery charging current when REG0x32[6]=1.The IBAT functionality can be enabled when REG0x31[7]=1 or disabled when REG0x31[7]=0.

7.7.2 High-Accuracy Power Sense Amplifier (PSYS)

The charger monitors total system power. During forward mode, the input adapter powers system and battery charging. During reverse OTG mode, the battery powers the system and VBUS output. The input and charge sense resistors (R_{AC} and R_{IS}) are selected in REG0x31[3:2]. PSYS pin outputs a current source and the power information is converted to voltage by resistor R_{PSYS}. The PSYS voltage can be calculated as:

$$V_{PSYS} = R_{PSYS} \times A_{PSYS} \times (V_{BUS} \times I_{IN} + V_{SYS} \times I_{BAT})$$

I_{IN} is the adapter current, I_{IN}>0 in the forward charging mode and I_{IN}<0 in reverse discharging mode. I_{BAT} is the battery current, I_{BAT}<0 in the forward charging mode and I_{BAT}>0 in reverse discharging mode. R_{PSYS} is the resistor connected with PSYS pin to GND.A_{PSYS} is the ratio of PSYS output current coefficient, it can be programmed with 1μA/W when REG0x31[1]=1 by default, and 0.25μA/W when REG0x31[1]=0.

During reverse OTG mode, the system power PSYS is the battery discharging power minus OTG output power when REG0x34[0]=0 by default. PSYS is the battery discharging power only when REG0x34[0]=1.

7.8 Two-Level Adapter Current Limit (Peak Power Mode)

Usually adapter can supply current higher than DC rating for a few milliseconds. The charger employs two-level input current limit (peak power mode) to fully utilize the overloading capability of adapter and minimize battery discharge during CPU peak power event.

1. Set peak power mode in REG0x33[5:4].
2. Set the converter input current limit same as adapter input current limit, or I_{LIM1} in REG0x0F/0E()
3. Set the overloading current, or I_{LIM2} in REG0x37[7:3], as a percentage of I_{LIM1}

When battery discharge or system voltage starts to drop, the peak power mode is triggered. The current limit switches between I_{LIM1} and I_{LIM2} as system load changes. The charger will first apply I_{LIM2} for T_{OVLD} in REG0x33[7:6], then apply I_{LIM1} for up to $T_{MAX} - T_{OVLD}$ time, T_{MAX} is programmed in REG0x33[1:0].

After T_{MAX}, if the load is still high, another peak power cycle starts. If T_{OVLD} is programmed to be equal to T_{MAX}, then peak power mode is always on. The peak power mode is illustrated as below figure.

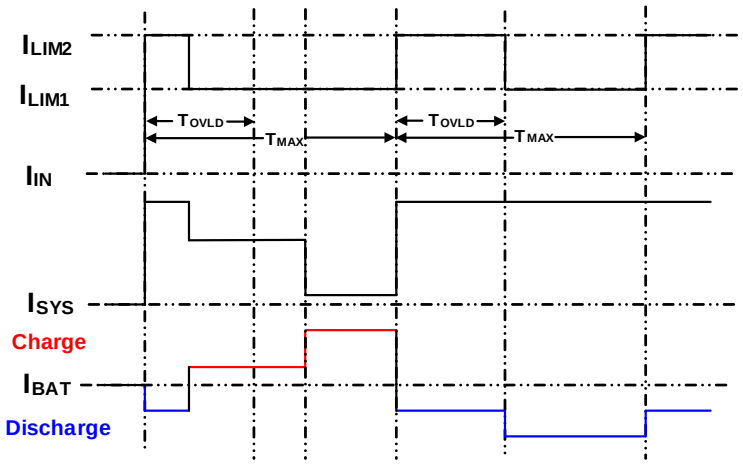


Figure 7-2. Two-Level Adapter Current Limit Timing Diagram

7.9 Processor Hot Indication

When CPU is running turbo mode, the system peak power may exceed available power from adapter and battery together. The adapter current and battery discharge peak current, or system voltage drop is an indication that system power is too high. The charger processor hot function monitors these events, and PROCHOTB pulse is asserted if the system power is too high. Once CPU receives PROCHOTB pulse from charger, it slows down to reduce system power. The events monitored by the processor hot function includes:

• ICRIT: adapter peak current, as 110% of I_{LIM2}

• INOM: adapter average current, as 110% of input current limit(I_{LIM1})

• IDCHG: battery discharge current in REG0x39[7:2]

• VSYS: system voltage on VSYS in REG0x36[3:2]

• Adapter Removal: upon adapter removal (CHRG_OK pin HIGH to LOW)

• Battery Removal: upon battery removal (CELL pin goes LOW)

• CMPO: Independent comparator output (CMPO pin HIGH to LOW)

• VDPM: VBUS lower than 80%/90%/100% of VINDPM threshold

• EXIT_VAP: Every time when the charger exits VAP mode

The threshold of ICRIT, IDCHG, VSYS or VDPM, and the deglitch time of ICRIT, INOM, IDCHG or CMPO are programmable through I^2C. Except the PROCHOT_EXIT_VAP is always enabled, the other triggering events can be individually enabled in REG0x38[7:0]. When any enabled event in PROCHOT profile is triggered, PROCHOTB is asserted low for a single pulse with minimal width programmable in REG0x23[5:4]. At the end of the single pulse, if the PROCHOT event is still active, the pulse gets extended until the event is removed.

If the PROCHOT pulse extension mode is enabled by setting REG0x23[6] = 1, the PROCHOTB pin will be kept as low until host writes REG0x23[3]= 0, even if the triggering event has been removed.

If the PROCHOT_VDPM or PROCHOT_EXIT_VAP is triggered, PROCHOTB pin will always stay low until the host clears it, no matter the PROCHOT is in one pulse mode or in extended mode.

7.9.1 PROCHOT During Low Power Mode

During low power mode (REG0x01[7] = 1), the charger offers a low power PROCHOT function with very low quiescent current consumption, which uses the independent comparator to monitor the system voltage, and assert PROCHOTB to CPU if the system power is too high.

Below lists the register setting to enable PROCHOT monitoring system voltage in low power mode.

• REG0x01[7] = 1 to enable low power mode

• REG0x38[7:0] = 00 to disable PROCHOT function

• REG0x30[6:4] = 100 to select CMP_POL=1 and disable independent comparator

Independent comparator threshold is always 1.2 V.

When REG0x31[6:5]= 01, charger monitors system voltage. Connect CMPI to voltage proportional to system. The PROCHOTB pin triggers from HIGH to LOW when CMPI voltage falls below 1.2 V.

7.9.2 PROCHOT Status

REG0x22[7:0] and REG0x23[0] reports which event in the profile triggers PROCHOTB if the corresponding bit is set to 1. The status bit can be reset back to 0 after it is read by host, when the current PROCHOT event is not active any more.

7.10 Pass Through Mode (PTM)

When the system is in the sleep mode or light load condition, the charger can be operated in the pass through mode (PTM) to improve the light load efficiency.
In PTM, the Buck and Boost high side MOSFETs Q_1 and Q_4 are both turned on, while the Buck and Boost low side MOSFETs Q_2 and Q_3 are both turned off. The input power is directly passed through the charger to the system. The switching losses of MOSFETs and the inductor core loss are saved.

Device will be transition from normal operation to PTM operation by:
1. Set REG0x32[7] = 0 to disable the EN_EXITILIM
2. Set REG0x31[0] = 1 to configure ILIM_HIZ pin as PTM enable pin when pull LOW ILIM_HIZ pin
3. Set REG0x30[2] = 1 to enable PTM
4. Pull ILIM_HIZ pin to ground

Device will transition out of PTM with only one of below events:
1. Set REG0x30[2] = 0 to disable PTM
2. Set REG0x31[0] = 0 to configure ILIM_HIZ pin as HIZ enable pin when pull LOW ILIM_HIZ pin, REG0x30[2] will be reset to 0
3. Pull ILIM_HIZ pin to HIGH
4. Device exits PTM to buck-boost operation if tripping VDPM, REG0x30[2] will be reset to 0
5. Device exits PTM to buck-boost operation under fault conditions such as ACOV, BATOC, ACOC, SYS SHORT, FORCE_LATCHOFF, BATOV, Thermal Shutdown

7.11 Device Protection

7.11.1 Watchdog Timer

The charger includes watchdog timer to terminate charging if the charger does not receive a write MaxChargeVoltage() or write ChargeCurrent() command within 175s by default (adjustable by REG0x01[6:5]). When watchdog timeout occurs, all register values are kept unchanged except ChargeCurrent() resets to 0. Battery charging

is suspended. A write to ChargeCurrent() register(higher than zero) could be reset watchdog timer and resume charging. Writing REG0x01[6:5] = 00 to disable watchdog timer also resumes charging.

7.11.2 Input Overvoltage Protection (ACOV)

When VBUS pin voltage is higher than ACOV rising threshold (V_{VBUS}>V_{ACOV_RISE}), adapter is considered as input over voltage. CHRG_OK pin will be pulled LOW, and converter stops switching. As system falls below battery voltage, BATFET will be turned on to supply system from battery. When VBUS pin voltage falls below ACOV falling threshold (V_{VBUS}<V_{ACOV_FALL}), adapter is considered as input voltage returns back to normal voltage. CHRG_OK is pulled HIGH by external pull up resistor. The converter resumes switching if enable conditions are valid.

7.11.3 Input Overcurrent Protection (ACOC)

If input overcurrent (133% or 200% of ILIM2_VTH, setting by REG0x32[2] and REG0x37[7:3] separately) is detected, ACOC protection is triggered. Converter stops switching and ACOC fault(REG0x20[5]=1) is reported to host. After relax time (t_{ACOC_RELAX}, 250 ms typical), converter starts switching again. ACOC function can be disabled by writing REG0x32[3] =0.

7.11.4 System Overvoltage Protection (SYSOVP)

After cell detection is finished, the charger sets SYSOVP threshold (5 V for 1 cell, 12 V for 2 cells, 19.5 V for 3 cells or 4 cells). When VSYS pin voltage is higher than SYSOVP rising threshold (V_{SYS}> V_{SYSOVP_RISE}), SYSOVP is triggered. The device latches off the converter and SYSOVP fault (SYSOVP_STAT bit, REG0x20[4]=1) is reported to host. After the SYSOVP is removed, the user can clear latch-off fault by either writing 0 to the SYSOVP_STAT bit or unplug and plug adapter again. After latch-off fault is cleared, the converter starts again if there is without any other faults.

7.11.5 Battery Overvoltage Protection (BATOVP)

Battery over-voltage may happen when battery is removed during charging or the user plugs in a wrong battery. The BATOVP threshold is 104% of regulation voltage set in REG0x05/04().

7.11.6 Battery Short

If the battery voltage sensed by ISN pin falls below minimum system voltage setting(V_{SYSMIN}) during charging, the maximum charging current is limited to 384 mA(2s to 4s) or 2A(1s).

7.11.7 System Short Hiccup Mode

The system voltage is sense by VSYS pin, when VSYS is lower than 2.4V, after 10ms deglitch time, the charger will be shut down for 500ms. The charger will restart for 10ms and measure VSYS again, if it is still lower than 2.4V, the charger will be shut down again. This hiccup mode will be tried continuously, if the charger restart is failed for 7 times in 90 seconds, the charger will be latched off. REG0x20[3] will be set to 1 to report a system short fault. The charger only can be enabled again once the host writes REG0x20[3]=0.The charger system short hiccup mode can be disabled by setting REG0x00[6]=1.

7.11.8 Thermal Shutdown (TSD)

When the junction temperature exceeds the 155℃, the charger stops switching and stays off. When the junction temperature falls below 135℃, the charger resumes switching with soft start. During thermal shutdown protection, the REGN LDO current limit is reduced to 16 mA and REGN LDO stays on.

7.12 I²C Interface

SY20776D uses I²C compatible interface for flexible charging parameter programming and instantaneous device status reporting. Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slave when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address 6BH, receiving control inputs from the master device like micro controller or a digital signal processor. The I²C interface supports both standard mode (up to 100kbits), and fast mode

(up to 400kbits).
Both SDA and SCL are bi-directional lines, connecting to the positive supply voltage by a current source or pull- up resistor. When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain.

7.12.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

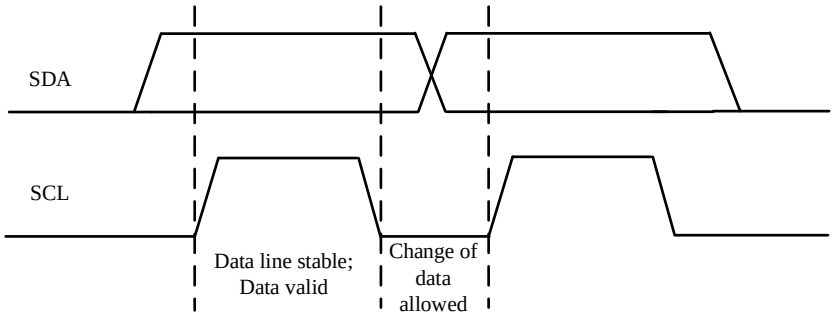


Figure 7-3. Bit Transfer over I²C

7.12.2 START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.
START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

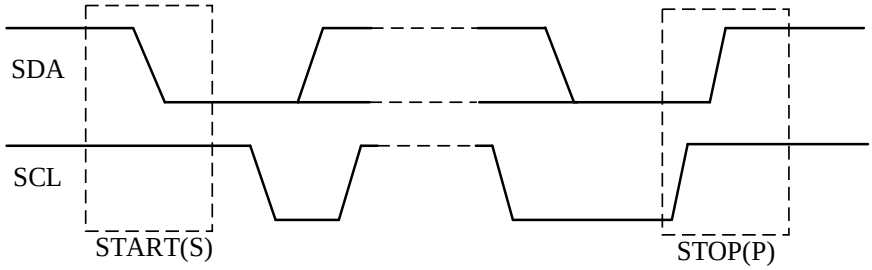


Figure 7-4. START and STOP Conditions

7.12.3 Byte Format

Every byte on the SDA line must be 8 bits long. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

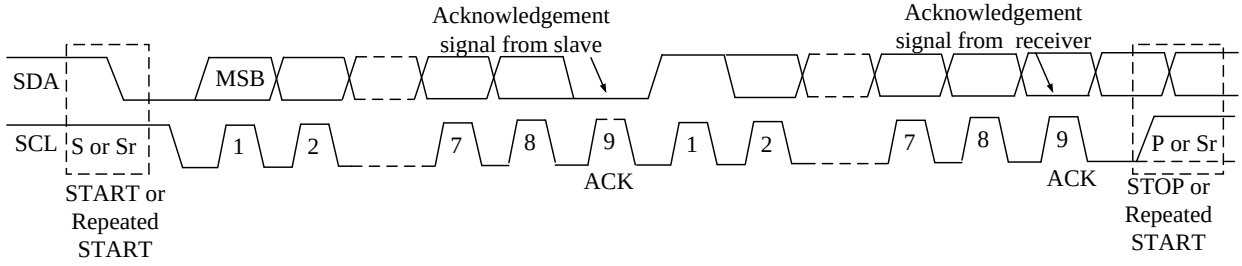


Figure 7-5. Data Transfer over I²C

7.12.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the 9th clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

7.12.5 Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

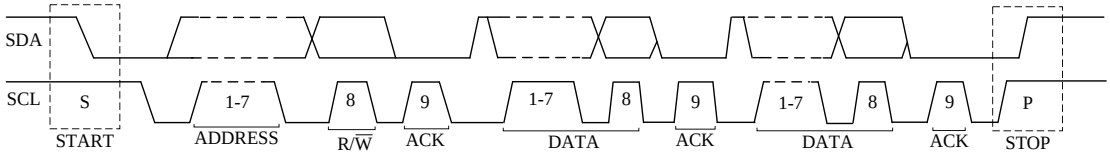


Figure 7-6. Complete Data Transfer

7.12.6 Single Read and Write

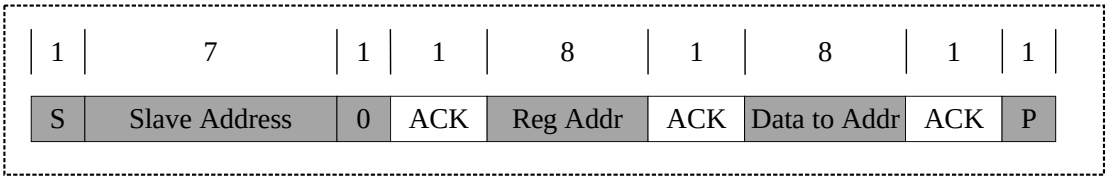


Figure 7-7. Single Write

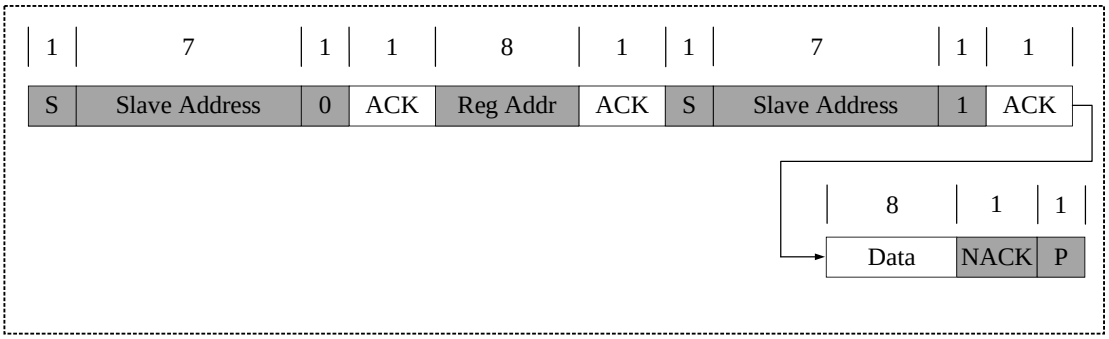


Figure 7-8. Single Read

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

7.12.7 Multi-Read and Multi-Write

The charger device supports multi-read and multi-write.

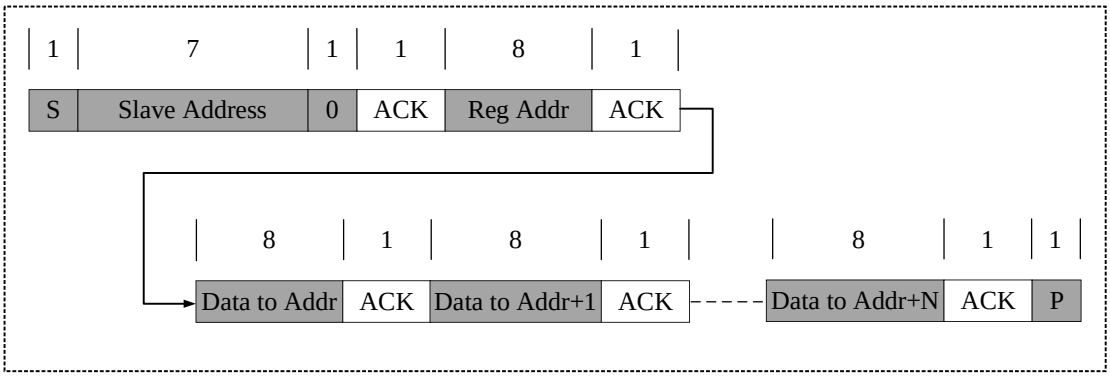


Figure 7-9. Multi-Write

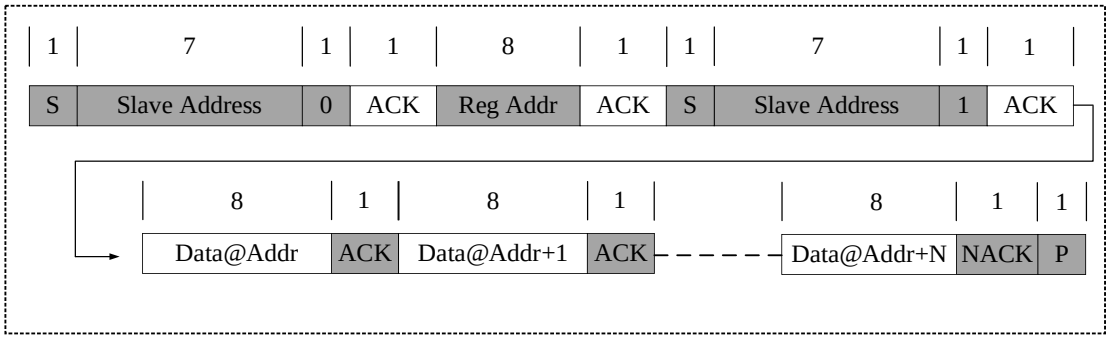


Figure 7-10. Multi-Read

7.12.8 Write 2-Byte I²C Commands

A few I²C commands combine two 8-bit registers together to form a complete value. These commands include:

- ChargeCurrent()
- MaxChargeVoltage()
- IIN_HOST()
- OTGVoltage()
- InputVoltage()

Host has to write LSB command followed by MSB command. No other command can be inserted in between these two writes. The charger waits for the complete write to the two registers to decide whether to accept or ignore the new value.

After the completion of LSB and MSB bytes, the two bytes will be updated at the same time. If host writes MSB byte first, the command will be ignored. If the time between write of LSB and MSB bytes exceeds watchdog timer, both the LSB and MSB commands will be ignored.

7.13 Register Map

The device supports 23 charger registers that use either Write-Word or Read-Word protocols, as summarized in Table 7-3. ManufacturerID and DeviceID are “read only” registers and can be used to identify the SY20776D.

Table 7-3. Register Summary

Register Address	Register Name	R/W	Description	Comment
01/00h	ChargeOption0	R/W	Charge Option Control 0	
03/02h	ChargeCurrent	R/W	7-Bit charge current setting	Default:0mA Range: 64mA-8.128A, LSB:64mA
05/04h	MaxChargeVoltage	R/W	12-Bit charge voltage setting	Default: 1s-4.2V, 2s-8.4V, 3s-12.6V, 4s-16.8V Range: 1.024V-19.2V, LSB:8mV
31/30h	ChargeOption1	R/W	Charge Option Control 1	
33/32h	ChargeOption2	R/W	Charge Option Control 2	
35/34h	ChargeOption3	R/W	Charge Option Control 3	
37/36h	PROCHOTOption0	R/W	PROCHOT Option 0	
39/38h	PROCHOTOption1	R/W	PROCHOT Option 1	
3B/3Ah	ADCOption	R/W	ADC option	
21/20h	ChargerStatus	R	Charger status	
23/22h	PROCHOTStatus	R	PROCHOT status	
25/24h	IIN_DPM	R	7-bit input current limit in use	Range: 50mA-6.4A, LSB:50mA
27/26h	ADCVBUS/PSYS	R	ADC output of input voltage, ADC output of system power	PSYS full range: 3.06V, LSB: 12mV VBUS full range: 3.2V-19.52 V, LSB: 64mV
29/28h	ADCIBAT	R	ADC output of battery charge current, ADC output of battery discharge current	ICHG full range: 8.128A, LSB: 64mA IDCHG full range: 32.512A, LSB: 256mA
2B/2Ah	ADCIIN/CMPI	R	ADC output of input current, ADC output of CMPI voltage	IIN full range: 12.75A, LSB: 50mA CMPI full range 3.06V, LSB: 12mV
2D/2Ch	ADCVSYS/VBAT	R	ADC output of system voltage, ADC output of battery voltage	VSYS full range: 2.88V-19.2V, LSB: 64mV VBAT full range : 2.88V-19.2V, LSB: 64mV
07/06h	OTGVoltage	R/W	12-bit OTG voltage setting	Range: 3V-20.8V, LSB: 8mV
09/08h	OTGCurrent	R/W	7-bit OTG output current setting	Range: 50mA-6.35A, LSB: 50mA
0B/0Ah	InputVoltage	R/W	8-bit input voltage setting	Range: 3.2V-19.52V, LSB: 64mV
0D/0Ch	MinSystemVoltage	R/W	6-bit minimum system voltage setting	Range: 1.024V-16.128V, LSB: 256mV Default: 1s-3.584V, 2s-6.144V, 3s-9.216V, 4s-12.288V
0F/0Eh	IIN_HOST	R/W	7-bit input current limit set by host	Range: 50mA-6.4A, LSB: 50mA
2Eh	ManufactureID	R	Manufacture ID	0xB6H@POR
2Fh	DeviceID	R	Device ID	0x77H@POR

7.13.1 Setting Charger Options

Table 7-4a. ChargeOption0 (Register 01h) [reset = E7h]

Bit	Bit Name	Type	POR	Description
7	EN_LWPWR	R/W	1b	Low Power Mode Enable 0b: Disable Low Power Mode. Device in performance mode with battery only. The PROCHOT, current/power monitor buffer and comparator follow register setting. 1b: Enable Low Power Mode. Device in low power mode with battery only for lowest quiescent current. The LDO is off. The PROCHOT, discharge current monitor buffer, power monitor buffer and independent comparator are disabled. ADC is not available in Low Power Mode. Independent comparator can be enabled by setting REG0x31[5] to 1. < default at POR >
6-5	WD TMR_ADJ	R/W	11b	WATCHDOG Timer Adjust Set maximum delay between consecutive I^2C write of charge voltage or charge current command. If device does not receive a write on the REG0x05/04() or the REG0x03/02() within the watchdog time period, the charger will be suspended by setting the REG0x03/02() to 0mA. After expiration, the timer will resume upon the write of REG0x03/02(), REG0x05/04() or REG0x01[6:5]. The charger will resume if the values are valid. 00b: Disable Watchdog Timer 01b: Enabled, 5 sec 10b: Enabled, 88 sec 11b: Enable Watchdog Timer, 175 sec <default at POR>
4	IDPM_AUTO_DISABLE	R/W	0b	IDPM Auto Disable When CELL pin is LOW, the charger automatically disables the IDPM function by setting EN_IDPM (REG0x00[1]) to 0. The host can enable IDPM function later by writing EN_IDPM bit (REG0x00[1]) to 1. 0b: Disable this function. IDPM is not disabled when CELL goes LOW. <default at POR> 1b: Enable this function. IDPM is disabled when CELL goes LOW.
3	OTG_ON_CHRGOK	R/W	0b	Add OTG to CHRG_OK Drive CHRG_OK to HIGH when the device is in OTG mode. 0b: Disable <default at POR> 1b: Enable
2	EN_OOA	R/W	1b	Out-of-Audio Enable 0b: No limit of PFM burst frequency 1b: Set minimum PFM burst frequency to above 25 kHz to avoid audio noise<default at POR>
1	PWM_FREQ	R/W	1b	Switching Frequency Two converter switching frequencies. One for small inductor and the other for big inductor. Recommend 800 kHz with 2.2 µH or 3.3 µH, and 1.2 MHz with 1 µH or 1.5 µH. Host has to set the right PWM frequency after device POR. 0b: 1200 kHz 1b: 800 kHz <default at POR>
0	Reserved	R/W	1b	Reserved

Table 7-4b. ChargeOption0 (Register 00h) [reset = 0Eh]

Bit	Bit Name	Type	POR	Description
7	Reserved	R/W	0b	Reserved
6	SYS_SHORT_DISABLE	R/W	0b	To disable the hiccup mode during the system short protection. 0b: When VSYS is short to lower than 2.4V, the charger enters hiccup mode <default at POR> 1b: The charger hiccup mode is disabled during system short fault
5	EN_LEARN	R/W	0b	LEARN function allows the battery to discharge while the adapter is present. It calibrates the battery gas gauge over a complete discharge/charge cycle. When the battery voltage is below battery depletion threshold, the system switches back to adapter input by the host. When CELL pin goes LOW, the device exits LEARN mode and this bit is set back to 0. 0b: Disable LEARN Mode <default at POR> 1b: Enable LEARN Mode
4	IAC_GAIN	R/W	0b	IAC Amplifier Ratio The ratio of voltage on IAC and voltage across ACP and ACN. 0b: 20× <default at POR> 1b: 40×
3	IBAT_GAIN	R/W	1b	IBAT Amplifier Ratio The ratio of voltage on IBAT and voltage across ISP and ISN 0b: 8× 1b: 16× <default at POR>
2	EN_LDO	R/W	1b	LDO Mode Enable When battery voltage is below minimum system voltage (REG0x0D/0C()), the charger is in pre-charge with LDO mode enabled. 0b: Disable LDO mode, BATFET fully ON. Precharge current is set by battery pack internal resistor (If REG0x03/02()=0000H， the IC couldn't enter into Disable LDO mode). The system is regulated by the MaxChargeVoltage register. 1b: Enable LDO mode, Precharge current is set by the ChargeCurrent register and clamped below 384 mA (2 cell – 4 cell) or 2A (1 cell). The system is regulated by the MinSystemVoltage register. <default at POR>
1	EN_IDPM	R/W	1b	IDPM Enable Host writes this bit to enable IDPM regulation loop. When the IDPM is disabled by the charger (refer to IDPM_AUTO_DISABLE), this bit goes LOW. 0b: IDPM disabled 1b: IDPM enabled <default at POR>
0	CHRG_INHIBIT	R/W	0b	Charge Inhibit When this bit is 0, battery charging will start with valid values in the MaxChargeVoltage register and the ChargeCurrent register. 0b: Enable Charge <default at POR> 1b: Inhibit Charge

Table 7-5a. ChargeOption1 (Register 31h) [reset = 02h]

Bit	Bit Name	Type	POR	Description
7	EN_IBAT	R/W	0b	IBAT Enable Enable the IBAT output buffer. In low power mode (REG0x01[7] = 1), IBAT buffer is always disabled regardless of this bit value. 0b: Turn off IBAT buffer to minimize Iq <default at POR> 1b: Turn on IBAT buffer
6	Reserved	R	0b	Reserved
5	EN_PROCHOT_LPWR	R/W	0b	Enable PROCHOTB during battery only low power mode With battery only, enable VSYS in PROCHOTB with low power consumption. Do not enable this function with adapter present. 0b: Disable low power PROCHOT <default at POR> 1b: Enable VSYS low power PROCHOT
4	EN_PSYS	R/W	0b	PSYS Enable Enable PSYS sensing circuit and output buffer (whole PSYS circuit). In low power mode (REG0x01[7] = 1), PSYS sensing and buffer are always disabled regardless of this bit value. 0b: Turn off PSYS buffer to minimize Iq <default at POR> 1b: Turn on PSYS buffer
3	RSNS_RAC	R/W	0b	Input sense resistor R_{AC} 0b: 10mΩ <default at POR> 1b: 20mΩ
2	RSNS_RIS	R/W	0b	Charge sense resistor R_{IS} 0b: 10mΩ <default at POR> 1b: 20mΩ
1	PSYS_RATIO	R/W	1b	PSYS Gain Ratio of PSYS output current vs total input and battery power with 10mΩ sense resistor. 0b: 0.25μA/W 1b: 1μA/W <default at POR>
0	PTM_PINSEL	R/W	0b	Select the ILIM_HIZ pin function 0b: charger enters HIZ mode when pull LOW the ILIM_HIZ pin. <default at POR> 1b: charger enters PTM when pull LOW the ILIM_HIZ pin.

Table 7-5b. ChargeOption1 (Register 30h) [reset = 11h]

Bit	Bit Name	Type	POR	Description
7	CMP_REF	R/W	0b	Independent Comparator Internal Reference. 0b: 2.3 V <default at POR> 1b: 1.2 V
6	CMP_POL	R/W	0b	Independent Comparator Output Polarity 0b: When CMPI is above internal threshold, CMPO is LOW (internal hysteresis) <default at POR> 1b: When CMPI is below internal threshold, CMPO is LOW (external hysteresis)
5-4	CMP_DEG	R/W	01b	Independent Comparator Deglitch Time, only applied to the falling edge of CMPO (HIGH → LOW). 00b: Independent comparator is disabled 01b: Independent comparator is enabled with output deglitch time 1μs <default at POR> 10b: Independent comparator is enabled with output deglitch time of 2ms 11b: Independent comparator is enabled with output deglitch time of

				5sec
3	FORCE_LATCHOFF	R/W	0b	Force Power Path Off When independent comparator triggers, charger turns off Q1 and Q4 (same as disable converter) so that the system is disconnected from the input source. At the same time, CHRG_OK signal goes to LOW to notify the system. 0b: Disable this function <default at POR> 1b: Enable this function
2	EN_PTM	R/W	0b	PTM enable register bit 0b: disable PTM. <default at POR> 1b: enable PTM.
1	EN_SHIP_DCHG	R/W	0b	Discharge ISN for Shipping Mode When this bit is 1, discharge ISN pin down below 3.8 V in 140ms. When 140ms is over, this bit is reset to 0. 0b: Disable shipping mode <default at POR> 1b: Enable shipping mode
0	AUTO_WAKEUP_EN	R/W	1b	Auto Wakeup Enable When this bit is HIGH, if the battery is below minimum system voltage (REG0x0D/0C()), the device will automatically enable 128mA charging current for 30mins. When the battery is charged up above minimum system voltage, charge will terminate. When the battery is above minimum system voltage + 0.25*cell, and the bit is reset to 0. 0b: Disable 1b: Enable <default at POR>

Table 7-6a. ChargeOption2 (Register 33h) [reset = 02h]

Bit	Bit Name	Type	POR	Description
7-6	PKPWR_TOVLD_DEG	R/W	00b	Input Overload time in Peak Power Mode 00b: 1 ms <default at POR> 01b: 2 ms 10b: 10 ms 11b: 20 ms
5	EN_PKPWR_IDPM	R/W	0b	Enable Peak Power Mode triggered by battery discharge current If REG0x33[5:4] are 00b, peak power mode is disabled. Upon adapter removal, the bits are not reset to 00b. 0b: Disable peak power mode triggered by input current overshoot<default at POR> 1b: Enable peak power mode triggered by input current overshoot.
4	EN_PKPWR_VSYS	R/W	0b	Enable Peak Power Mode triggered by system voltage under-shoot If REG0x33[5:4] are 00b, peak power mode is disabled. Upon adapter removal, the bits are not reset to 00b. 0b: Disable peak power mode triggered by system voltage under-shoot <default at POR> 1b: Enable peak power mode triggered by system voltage under-shoot.
3	PKPWR_OVLD_STAT	R/W	0b	Indicator that the device is in overloading cycle. Write 0 to get out of overloading cycle. 0b: Not in peak power mode. <default at POR> 1b: In peak power mode.
2	PKPWR_RELAX_STAT	R/W	0b	Indicator that the device is in relaxation cycle. Write 0 to get out of relaxation cycle. 0b: Not in relaxation cycle. <default at POR> 1b: In relaxation mode.

1-0	PKPWR_TMAX	R/W	10b	Peak power mode overload and relax cycle time. When REG0x33[7:6] is programmed longer than REG0x33[1:0], there is no relax time. 00b: 5 ms 01b: 10 ms 10b: 20 ms <default at POR> 11b: 40 ms

Table 7-6b. ChargeOption2 (Register 32h) [reset = B7h]

Bit	Bit Name	Type	POR	Description
7	EN_EXTILIM	R/W	1b	Enable ILIM_HIZ pin to set input current limit 0b: Input current limit is set by REG0x0F/0E(). 1b: Input current limit is set by the lower value of ILIM_HIZ pin and REG0x0F/0E(). <default at POR>
6	EN_ICHG_IDCHG	R/W	0b	0b: IBAT pin as discharge current. <default at POR> 1b: IBAT pin as charge current.
5	Q2_OCP	R/W	1b	Q2 OCP threshold by sensing Q2 VDS 0b: 210 mV 1b: 150 mV <default at POR>
4	ACX_OCP	R/W	1b	Input current OCP threshold by sensing ACP-ACN. 0b: 280 mV 1b: 150 mV <default at POR>
3	EN_ACOC	R/W	0b	ACOC Enable Input overcurrent (ACOC) protection by sensing the voltage across ACP and ACN. Upon ACOC (after 100-µs blank-out time), converter is disabled. 0b: Disable ACOC <default at POR> 1b: ACOC threshold 133% or 200% ILIM2
2	ACOC_VTH	R/W	1b	ACOC Limit Set ACOC threshold as percentage of IDPM with current sensed from R_{AC}. 0b: 133% of ILIM2 1b: 200% of ILIM2 <default at POR>
1	EN_BATOC	R/W	1b	BATOC Enable Battery discharge overcurrent (BATOC) protection by sensing the voltage across ISN and ISP. Upon BATOC, converter is disabled. 0b: Disable BATOC 1b: BATOC threshold 133% or 200% PROCHOT IDCHG <default at POR>
0	BATOC_VTH	R/W	1b	Set battery discharge overcurrent threshold as percentage of PROCHOT battery discharge current limit. 0b: 133% of PROCHOT IDCHG 1b: 200% of PROCHOT IDCHG <default at POR>

Table 7-7a. ChargeOption3 (Register 35h) [reset = 00h]

Bit	Bit Name	Type	POR	Description
7	EN_HIZ	R/W	0b	Device HIZ Mode Enable When the charger is in HIZ mode, the device draws minimal quiescent current. With VBUS above UVLO. REGN LDO stays on, and system powers from battery. 0b: Device not in HIZ mode <default at POR> 1b: Device in HIZ mode
6	RESET_REG	R/W	0b	Reset Registers All the registers go back to the default setting except the VINDPM register. V_{SYSMIN} will always goes back to 1S default setting (3.584V), and the charging voltage goes back to the default values according to the cell pin setting(POR value, not value now) 0b: Idle <default at POR> 1b: Reset all the registers to default values. After reset, this bit goes back to 0. When the battery voltage is lower than minimal system voltage, or the battery is removed, it is not recommended to use this bit to reset the registers to default values.
5	RESET_VINDPM	R/W	0b	Reset VINDPM Threshold 0b: Idle 1b: Converter is disabled to measure VINDPM threshold. After VINDPM measurement is done, this bit goes back to 0 and converter starts.
4	EN_OTG	R/W	0b	OTG Mode Enable Enable device in OTG mode when EN_OTG pin is HIGH. 0b: Disable OTG <default at POR> 1b: Enable OTG mode to supply VBUS from battery.
3	EN_AICL_MODE	R/W	0b	Enable AICL Algorithm 0b: Disable AICL algorithm. <default at POR> 1b: Enable AICL algorithm.
2-0	Reserved	R/W	000b	Reserved

Table 7-7b. ChargeOption3 (Register 34h) [reset = 30h]

Bit	Bit Name	Type	POR	Description
7-6	Reserved	R/W	00b	Reserved
5	OTG_VAP_MODE	R/W	1b	The selection of the external OTG_VAP pin control. 0b: the external OTG_VAP pin controls the EN/DIS VAP mode 1b: the external OTG_VAP pin controls the EN/DIS OTG mode <default at POR>
4-3	IL_AVG	R/W	10b	4 levels inductor average current clamp. 00b: 6A 01b: 10A 10b: 15A <default at POR> 11b: Disabled
2	OTG_RANGE_LOW	R/W	0b	Selection of the different OTG output voltage range. 0b: VOTG high range 4.28 V-20.8 V <default at POR> 1b: VOTG low range 3 V-19.52 V
1	BATFETOFF_HIZ	R/W	0b	Control BATFET during HIZ mode. 0b: BATFET on during HIZ <default at POR> 1b: BATFET off during HIZ

0	PSYS_OTG_IDCHG	R/W	0b	PSYS function during OTG mode. 0b: PSYS as battery discharge power minus OTG output power <default at POR> 1b: PSYS as battery discharge power only

7.13.2 Setting Prochot Options

Table 7-8a. ProchotOption0 (Register 37h) [reset = 4Ah]

Bit	Bit Name	Type	POR	Description
7-3	ILIM2_VTH	R/W	01001b	I_{LIM2} Threshold 5 bits, percentage of IDPM in REG0x0F/0E(). Measure current between ACP and ACN. Trigger when the current is above this threshold: 00001b-11001b: 110%-230%, step 5% 11010b-11110b: 250%-450%, step 50% 11111b: Out of Range (Ignored) Default 150%, or 01001
2-1	ICRIT_DEG	R/W	01b	ICRIT Deglitch time ICRIT is set to be 110% of I_{LIM2}. Typical ICRIT deglitch time to trigger PROCHOTB. 00b: 15µs 01b: 100µs <default at POR> 10b: 400µs (max 500µs) 11b: 800µs (max 1ms)
0	PROCHOT_VDPM_80_90	R/W	0b	Lower threshold of the PROCHOT_VDPM comparator When REG0x36[0]=1, the threshold of the PROCHOT_VDPM comparator is determined by this bit setting. 0b: 80% of VinDPM threshold <default at POR>. 1b: 90% of VinDPM threshold

Table 7-8b. ProchotOption0 (Register 36h) [reset = 65h]

Bit	Bit Name	Type	POR	Description
7-4	VSYS_TH1	R/W	0110b	VSYS Threshold to trigger discharging VBUS in VAP mode. Measure on VSYS with fixed 5-µs deglitch time. Trigger when SYS pin voltage is below the thresholds. 2S - 4S battery 0000b-1111b: 5.9 V-7.4V with 0.1 V step size. 1S battery 0000b-0111b: 3.1 V-3.8 V with 0.1 V step size. 1000b-1111b: 3.1 V-3.8 V with 0.1 V step size.
3-2	VSYS_TH2	R/W	01b	VSYS Threshold to assert PROCHOT_VSYS. Measure on VSYS with fixed 5-µs deglitch time. Trigger when SYS pin voltage is below the thresholds. 2S-4S battery 00b: 5.9V; 01b: 6.2V <default at POR>; 10b: 6.5V; 11b: 6.8V. 1S battery 00b: 3.1V; 01b: 3.3V <default at POR>; 10b: 3.5V; 11b: 3.7V.
1	INOM_DEG	R/W	0b	INOM Deglitch Time INOM is always 10% above IDPM in REG0x0F/0E(). Measure current between ACP and ACN. Trigger when the current is above this threshold. 0b: 1 ms (must be max) <default at POR> 1b: 50 ms (max 60 ms)

0	LOWER_PROCHOT_VDPM	R/W	1b	Enable the lower threshold of the PROCHOT_VDPM comparator 0b: the threshold of the PROCHOT_VDPM comparator follows the same VinDPM REG0x0B/0A() setting. 1b: the threshold of the PROCHOT_VDPM comparator is lower and determined by REG0x37[0] setting. <default at POR>

Table 7-9a. ProchotOption1 (Register 39h) [reset = 81h]

Bit	Bit Name	Type	POR	Description
7-2	IDCHG_VTH	R/W	100000b	IDCHG Threshold 6 bit, range 0 A to 32256 mA, step 512 mA. There is a 128 mA offset. Measure current between ISN and ISP. Trigger when the discharge current is above the threshold. If the value is programmed to 000000b, PROCHOTB is always triggered. Default: 16384mA or 100000b
1-0	IDCHG_DEG	R/W	01b	IDCHG Deglitch Time 00b: 1.6ms 01b: 100μs <default at POR> 10b: 6ms 11b: 12ms

Table 7-9b. ProchotOption1 (Register 38h) [reset = A0h]

Bit	Bit Name	Type	POR	Description
7	PROCHOT_PROFILE_VDPM	R/W	1b	PROCHOT Profile When all the REG0x38[7:0] bits are 0, PROCHOT function is disabled. Bit7 PP_VDPM detects VBUS voltage 0b: disable 1b: enable <default at POR>
6	PROCHOT_PROFILE_CMPOUT	R/W	0b	0b: disable <default at POR> 1b: enable
5	PROCHOT_PROFILE_ICRIT	R/W	1b	0b: disable 1b: enable <default at POR>
4	PROCHOT_PROFILE_INOM	R/W	0b	0b: disable <default at POR> 1b: enable
3	PROCHOT_PROFILE_IDCHG	R/W	0b	0b: disable <default at POR> 1b: enable
2	PROCHOT_PROFILE_VSYS	R/W	0b	0b: disable <default at POR> 1b: enable
1	PROCHOT_PROFILE_BATPRES	R/W	0b	0b: disable <default at POR> 1b: enable (one-shot falling edge triggered) If BATPRES is enabled in PROCHOT after the battery is removed, it will immediately send out one-shot PROCHOTB pulse.
0	PROCHOT_PROFILE_ACOK	R/W	0b	0b: disable <default at POR> 1b: enable REG0x01[7] = 0 to assert PROCHOTB pulse after adapter removal. If PROCHOT_PROFILE_ACOK is enabled in PROCHOT after the adapter is removed, it will be pulled low in one-shot PROCHOTB pulse.

When the REG0x38[7:0] are set to be disabled, the PROCHOT event associated with that bit will not be reported in the PROCHOT status register REG0x22[7:0] any more, and the PROCHOTB pin will not be pulled low any more if the event happens.

7.13.3 Setting ADC Option

Table 7-10a. ADCOption (Register 3Bh) [reset = 20h]

Bit	Bit Name	Type	POR	Description
7	ADC_CONV	R/W	0b	Typical ADC conversion time is 10ms. 0b: One-shot update. Do one set of conversion updates to registers REG0x27/26(), REG0x29/28(), REG0x2B/2A(), and REG0x2D /2C() after ADC_START = 1. 1b: Continuous update. Do a set of conversion updates to registers REG0x27/26(), REG0x29/28(), REG0x2B/2A(), and REG0x2D /2C() every 1sec.
6	ADC_START	R/W	0b	0b: No ADC conversion 1b: Start ADC conversion. After the one-shot update is complete, this bit automatically resets to zero
5	ADC_FULLSCALE	R/W	1b	ADC input voltage range. When input voltage is below 5 V, or battery is 1S, full scale 2.04 V is recommended. 0b: 2.04 V 1b: 3.06 V <default at POR>
4-0	Reserved	R/W	00000b	Reserved

Table 7-10b. ADCOption (Register 3Ah) [reset = 00h]

Bit	Bit Name	Type	POR	Description
7	EN_ADC_CMPI	R/W	0b	0b: Disable <default at POR> 1b: Enable
6	EN_ADC_VBUS	R/W	0b	0b: Disable <default at POR> 1b: Enable
5	EN_ADC_PSYS	R/W	0b	0b: Disable <default at POR> 1b: Enable
4	EN_ADC_IIN	R/W	0b	0b: Disable <default at POR> 1b: Enable
3	EN_ADC_IDCHG	R/W	0b	0b: Disable <default at POR> 1b: Enable
2	EN_ADC_ICHG	R/W	0b	0b: Disable <default at POR> 1b: Enable
1	EN_ADC_VSYS	R/W	0b	0b: Disable <default at POR> 1b: Enable
0	EN_ADC_VBAT	R/W	0b	0b: Disable <default at POR> 1b: Enable

7.13.4 Charge and Prochot Status

Table 7-11a. ChargerStatus (Register 21h) [reset = 00h]

Bit	Bit Name	Type	POR	Description
7	AC_STAT	R	0b	Input source status. 0b: Input not present 1b: Input is present
6	AICL_DONE	R	0b	After the AICL routine is successfully executed, the bit goes 1. 0b: AICL is not complete 1b: AICL is complete
5	IN_VAP	R	0b	0b: Charger is not operated in VAP mode 1b: Charger is operated in VAP mode
4	IN_VINDPM	R	0b	0b: Charger is not in VINDPM during forward mode, or voltage regulation during OTG mode 1b: Charger is in VINDPM during forward mode, or voltage regulation during OTG mode
3	IN_IINDPM	R	0b	0b: Charger is not in IINDPM 1b: Charger is in IINDPM
2	IN_FCHRG	R	0b	0b: Charger is not in fast charge 1b: Charger is in fast charger
1	IN_PCHRG	R	0b	0b: Charger is not in pre-charge 1b: Charger is in pre-charge
0	IN_OTG	R	0b	0b: Charger is not in OTG 1b: Charge is in OTG

Table 7-11b. ChargerStatus (Register 20h) [reset = 00h]

Bit	Bit Name	Type	POR	Description
7	Fault ACOV	R	0b	The faults are latched until a read from host. 0b: No fault 1b: ACOV
6	Fault BATOC	R	0b	The faults are latched until a read from host. 0b: No fault 1b: BATOC
5	Fault ACOC	R	0b	The faults are latched until a read from host. 0b: No fault 1b: ACOC
4	SYSOVP_STAT	R/W	0b	SYSOVP Status and Clear When the SYSOVP occurs, this bit is HIGH. During the SYSOVP, the converter is disabled. After the SYSOVP is removed, the user must write a 0 to this bit or unplug the adapter to clear the SYSOVP condition to enable the converter again. 0b: Not in SYSOVP <default at POR> 1b: In SYSOVP. When SYSOVP is removed, write 0 to clear the SYSOVP latch.
3	Fault SYS_SHORT	R/W	0b	The fault is latched until a clear from host by writing this bit to 0. 0b: No fault <default at POR> 1b: When SYS is lower than 2.4V, then 7 times restart tries are failed.
2	Fault Latchoff	R	0b	The faults are latched until a read from host. 0b: No fault 1b: Latch off (REG0x30[3])

1	Fault_OTG_OVP	R	0b	The faults are latched until a read from host. 0b: No fault 1b: OTG OVP
0	Fault_OTG_UVP	R	0b	The faults are latched until a read from host. 0b: No fault 1b: OTG UVP

Table 7-12a. ProchotStatus (Register 23h) [reset = 28h]

Bit	Bit Name	Type	POR	Description
7	Reserved	R	0b	Reserved
6	EN_PROCHOT _EXIT	R/W	0b	PROCHOTB Pulse Extension Enable. When pulse extension is enabled, keep the PROCHOTB pin voltage LOW until host writes REG0x23[3] = 0. 0b: Disable pulse extension <default at POR> 1b: Enable pulse extension
5-4	PROCHOT _WIDTH	R/W	10b	PROCHOTB Pulse Width Setting Minimum PROCHOT pulse width when REG0x23[6] = 0 00b: 100μs 01b: 1ms 10b: 10ms <default at POR> 11b: 5s
3	PROCHOT _CLEAR	R/W	1b	PROCHOTB Pulse Clear. Clear PROCHOTB pulse when REG0x23[6] = 1. 0b: Clear PROCHOTB pulse and drive PROCHOTB pin HIGH 1b: Idle <default at POR>
2	PROCHOT _THERMAL SHUTDOWN	R	0b	0b: Not triggered<default at POR> 1b: Triggered
1	STAT_VAP_FAIL	R/W	0b	This status bit reports a failure to load VBUS 7 consecutive times in VAP mode, which indicates the battery voltage might be not high enough to enter VAP mode, or the VAP loading current settings are too high. 0b: Not in VAP failure <default at POR> 1b: In VAP failure, the charger exits VAP mode, and latches off until the host writes this bit to 0.
0	STAT_EXIT_VAP	R/W	0b	When the charger is operated in VAP mode, it can exit VAP by either being disabled through host, or there is any charger fault. 0b: PROCHOT_EXIT_VAP is not active <default at POR> 1b: PROCHOT_EXIT_VAP is active, PROCHOTB pin is low until host writes this status bit to 0.

Table 7-12b. ProchotStatus (Register 22h) [reset = 00h]

Bit	Bit Name	Type	POR	Description
7	STAT_VDPM	R/W	0b	0b: Not triggered 1b: Triggered
6	STAT_COMP	R	0b	0b: Not triggered 1b: Triggered
5	STAT_ICRIT	R	0b	0b: Not triggered 1b: Triggered
4	STAT_INOM	R	0b	0b: Not triggered 1b: Triggered
3	STAT_IDCHG	R	0b	0b: Not triggered 1b: Triggered

2	STAT_VSYS	R	0b	0b: Not triggered 1b: Triggered
1	STAT_Battery_Removal	R	0b	0b: Not triggered 1b: Triggered
0	STAT_Adapter_Removal	R	0b	0b: Not triggered 1b: Triggered

7.13.5 ChargeCurrent Register

SY20776D has a 16-bit ChargeCurrent register(REG0x03/02()) that sets the battery charging current,using the data format listed in Table 7-13.

SY20776D controls the charge current by controlling the ISP-ISN voltage. With a 10mΩ charge current R_{IS} resistor, the charger provides charge current range of 64mA to 8.128A with a 64mA step resolution. Resistors of other values can also be used. For a larger sense resistor, a larger sense voltage means a higher regulation accuracy; but, at the expense of higher conduction loss. A current sensing resistor value no more than 20mΩ is suggested.

Upon POR, when auto wakeup is not active, ChargeCurrent() register is 0.CELL pin going LOW (battery removal) will reset the ChargeCurrent() register to 0. To stop charging, set ChargeCurrent register to 0. To start the charging, write valid numbers to the ChargeCurrent() register. All numbers requesting charge current above 8.128A will be ignored.

Charge current is not reset in ACOC, TSD, power path latch off (REG0x30[1]), and SYSOVP.

During pre-charge, BATFET works in linear mode (LDO mode) (default REG0x00[2] = 1). For 2-4 cell battery, the system is regulated at minimum system voltage in REG0x0D/0C() and the pre-charge current is clamped at 384 mA. For 1 cell battery, the pre-charge to fast charge battery voltage threshold is 3 V, and the pre-charge current is clamped at 384 mA. However, the BATFET stays in LDO mode operation till battery voltage is above minimum system voltage. During battery voltage from 3 V to V_{SYSMIN}, the fast charge current is clamped at 2 A.

Table 7-13a. Charge Current with 10mΩ R_{IS} (Register 03h) [reset = 00h]

Bit	Bit Name	Type	POR	Description
7-5	Reserved	R/W	000b	Not used. 1 = invalid write.
4	Charge Current, bit 6	R/W	0b	0 = Adds 0mA of charger current. 1 = Adds 4096mA of charger current.
3	Charge Current, bit 5	R/W	0b	0 = Adds 0mA of charger current. 1 = Adds 2048mA of charger current.
2	Charge Current, bit 4	R/W	0b	0 = Adds 0mA of charger current. 1 = Adds 1024mA of charger current.
1	Charge Current, bit 3	R/W	0b	0 = Adds 0mA of charger current. 1 = Adds 512mA of charger current.
0	Charge Current, bit 2	R/W	0b	0 = Adds 0mA of charger current. 1 = Adds 256mA of charger current.

Table 7-13b. Charge Current with 10mΩ R_{IS} (Register 02h) [reset = 00h]

Bit	Bit Name	Type	POR	Description
7	Charge Current, bit 1	R/W	0b	0 = Adds 0mA of charger current. 1 = Adds 128mA of charger current.
6	Charge Current, bit 0	R/W	0b	0 = Adds 0mA of charger current. 1 = Adds 64mA of charger current.
5-0	Reserved	R/W	000000b	Not used. Value Ignored.

7.13.6 MaxChargeVoltage Register

SY20776D has a 16-bit ChargeVoltage register (REG0x05/04()) that sets the battery charging voltage, using the data format listed in Table 7-14. The valid charge voltage range is 1.024V to 19.200V with 8 mV step resolution. All numbers requesting charge voltage below 1.024V or above 19.2V will be ignored.

Upon POR, REG0x05/04() is by default set as 4.2V for 1s, 8.4V for 2s, 12.6V for 3s or 16.8V for 4s according to CELL pin setting. After CHRG_OK goes high, the charge will start when the host writes the charging current to REG0x03/02(), the default charging voltage is used if REG0x05/04() is not programmed. If the battery is different from 4.2 V/cell, the host has to write to REG0x05/04() before REG0x03/02() for battery voltage setting. Writing REG0x05/04() to 0 will set REG0x05/04() to the default value according to CELL pin setting, and force REG0x03/02() to 0 to disable charge.

Table 7-14a. MaxChargeVoltage (Register 05h)

Bit	Bit Name	Type	POR	Description
7	Reserved	R/W	0b	Not used. 1 = invalid write.
6	Max Charge Voltage, bit 11	R/W	0b	0 = Adds 0mV of charger voltage. 1 = Adds 16384mV of charger voltage.
5	Max Charge Voltage, bit 10	R/W	0b	0 = Adds 0mV of charger voltage. 1 = Adds 8192mV of charger voltage.
4	Max Charge Voltage, bit 9	R/W	0b	0 = Adds 0mV of charger voltage. 1 = Adds 4096mV of charger voltage.
3	Max Charge Voltage, bit 8	R/W	0b	0 = Adds 0mV of charger voltage. 1 = Adds 2048mV of charger voltage.
2	Max Charge Voltage, bit 7	R/W	0b	0 = Adds 0mV of charger voltage. 1 = Adds 1024mV of charger voltage.
1	Max Charge Voltage, bit 6	R/W	0b	0 = Adds 0mV of charger voltage. 1 = Adds 512mV of charger voltage.
0	Max Charge Voltage, bit 5	R/W	0b	0 = Adds 0mV of charger voltage. 1 = Adds 256mV of charger voltage.

Table 7-14b. MaxChargeVoltage (Register 04h)

Bit	Bit Name	Type	POR	Description
7	Max Charge Voltage, bit 4	R/W	0b	0 = Adds 0mV of charger voltage. 1 = Adds 128mV of charger voltage.
6	Max Charge Voltage, bit 3	R/W	0b	0 = Adds 0mV of charger voltage. 1 = Adds 64mV of charger voltage.
5	Max Charge Voltage, bit 2	R/W	0b	0 = Adds 0mV of charger voltage. 1 = Adds 32mV of charger voltage.
4	Max Charge Voltage, bit 1	R/W	0b	0 = Adds 0mV of charger voltage. 1 = Adds 16mV of charger voltage.
3	Max Charge Voltage, bit 0	R/W	0b	0 = Adds 0mV of charger voltage. 1 = Adds 8mV of charger voltage.
2-0	Reserved	R/W	000b	Not used. Value Ignored.

7.13.7 MinSystemVoltage Register

SY20776D provides a Narrow VDC(NVDC) for system input. To set the minimum system voltage, write a 16-bit MinSystemVoltage register command (REG0x0D/0C()) using the data format listed in Table 7-15. The charger provides minimum system voltage range from 1.024V to 16.128V with 256mV step resolution. All numbers requesting minimum system voltage below 1.024V or above 16.128V will be ignored. The MinSystemVoltage register will sustain previous data.

Upon POR, the MinSystemVoltage register is 3.584V for 1s, 6.144V for 2s and 9.216V for 3s, and 12.288V for 4s according to CELL pin setting.

Table 7-15a. MinSystemVoltage (Register 0Dh)

Bit	Bit Name	Type	POR	Description
7-6	Reserved	R/W	00b	Not used. 1 = invalid write.
5	Min System Voltage, bit 5	R/W	0b	0 = Adds 0mV of system voltage. 1 = Adds 8192mV of system voltage.
4	Min System Voltage, bit 4	R/W	0b	0 = Adds 0mV of system voltage. 1 = Adds 4096mV of system voltage.
3	Min System Voltage, bit 3	R/W	0b	0 = Adds 0mV of system voltage. 1 = Adds 2048mV of system voltage.
2	Min System Voltage, bit 2	R/W	0b	0 = Adds 0mV of system voltage. 1 = Adds 1024mV of system voltage.
1	Min System Voltage, bit 1	R/W	0b	0 = Adds 0mV of system voltage. 1 = Adds 512mV of system voltage.
0	Min System Voltage, bit 0	R/W	0b	0 = Adds 0mV of system voltage. 1 = Adds 256mV of system voltage.

Table 7-15b. MinSystemVoltage (Register 0Ch)

Bit	Bit Name	Type	POR	Description
7-0	Reserved	R/W	11111111b	Not used. Value Ignored.

7.13.8 Input Current Register

Normally, input power source provide power for system load and/or charge the battery. When the input current exceeds the input current setting, the SY20776D decreases the charge current to provide priority to system load. As the system current rises, the available charge current drops accordingly toward zero. If the system load keeps increasing after charge current drops down to zero, the battery will reversely discharge to supply the heavy system load.

To set the input current limit, write a 16-bit IIN_HOST register command (REG0x0F/0E()) using a 10mΩ sense resistor, the SY20776D provides an input-current limit range of 50mA to 6.4A, with 50mA resolution. Upon POR, default input current limit is 3.25A.

There is 50mA offset for the register. With code 0, the input current limit readback is 50 mA.

The ACP and ACN pins are used to sense R_{AC} with default value of 10mΩ.However, resistors of other values can also be used. For a larger sense resistor, larger sense voltage is given, and a higher regulation accuracy with higher conduction loss.

Instead of using the internal IDPM loop, the user can build up an external input current regulation loop and have the feedback signal on the ILIM_HIZ pin. $V_{ILIM\_HIZ}=1V+40\times I_{DPM}\times R_{AC.}$ In order to disable ILIM_HIZ pin, the host can write REG0x32[7]=0 to disable ILIM_HIZ pin, or pull ILIM_HIZ pin above 4.0 V.

Table 7-16a. IIN_HOST with 10mΩ R_{IS} (Register 0Fh) [reset = 40h]

Bit	Bit Name	Type	POR	Description
7	Reserved	R/W	0b	Not used. 1 = invalid write.
6	Input Current set by host, bit 6	R/W	1b	0 = Adds 0mA of input current. 1 = Adds 3200mA of input current.
5	Input Current set by host, bit 5	R/W	0b	0 = Adds 0mA of input current. 1 = Adds 1600mA of input current.
4	Input Current set by host, bit 4	R/W	0b	0 = Adds 0mA of input current. 1 = Adds 800mA of input current.
3	Input Current set by host, bit 3	R/W	0b	0 = Adds 0mA of input current. 1 = Adds 400mA of input current.
2	Input Current set by host, bit 2	R/W	0b	0 = Adds 0mA of input current. 1 = Adds 200mA of input current.
1	Input Current set by host, bit 1	R/W	0b	0 = Adds 0mA of input current. 1 = Adds 100mA of input current.
0	Input Current set by host, bit 0	R/W	0b	0 = Adds 0mA of input current. 1 = Adds 50mA of input current.

Table 7-16b. IIN_HOST with 10mΩ R_{IS} (Register 0Eh) [reset = FFh]

Bit	Bit Name	Type	POR	Description
7-0	Reserved	R	11111111b	Not used. Value Ignored.

IIN_DPM register reflects the actual input current limit programmed in the register, either from host or from AICL. After AICL, the current limit used by DPM regulation may differ from the IIN_HOST register settings. The actual DPM limit is reported in REG0x25/24().

Table 7-17a. IIN_DPM with 10mΩ R_{IS} (Register 25h) [reset = 40h]

Bit	Bit Name	Type	POR	Description
7	Reserved	R/W	0b	Not used. 1 = invalid write.
6	Input Current set by host, bit 6	R/W	1b	0 = Adds 0mA of input current. 1 = Adds 3200mA of input current.
5	Input Current set by host, bit 5	R/W	0b	0 = Adds 0mA of input current. 1 = Adds 1600mA of input current.

4	Input Current set by host, bit 4	R/W	0b	0 = Adds 0mA of input current. 1 = Adds 800mA of input current.
3	Input Current set by host, bit 3	R/W	0b	0 = Adds 0mA of input current. 1 = Adds 400mA of input current.
2	Input Current set by host, bit 2	R/W	0b	0 = Adds 0mA of input current. 1 = Adds 200mA of input current.
1	Input Current set by host, bit 1	R/W	0b	0 = Adds 0mA of input current. 1 = Adds 100mA of input current.
0	Input Current set by host, bit 0	R/W	0b	0 = Adds 0mA of input current. 1 = Adds 50mA of input current.

Table 7-17b. IIN_DPM with 10mΩ R_{IS} (Register 24h) [reset = FFh]

Bit	Bit Name	Type	POR	Description
7-0	Reserved	R	11111111b	Not used. Value Ignored.

7.13.9 Input Voltage Register

To set the input voltage limit, write a 16-bit InputVoltage register command (REG0x0B/0A()) using the data format listed in Table 7-18.The input voltage DPM setting voltage is 1.28 V below the no-load VBUS voltage with 3.2 V DC offset.

When the input voltage drops less than the input voltage DPM setting voltage, the SY20776D decreases the charge current to provide priority to system load. As the system current rises, the available charge current drops accordingly toward zero. If the system load keeps increasing after charge current drops down to zero, the battery will reversely discharge to supply the heavy system load.

Table 7-18a. InputVoltage (Register 0Bh) [reset = VBUS-1.28V]

Bit	Bit Name	Type	POR	Description
7-6	Reserved	R/W	00b	Not used. 1 = invalid write.
5	Input Voltage, bit 7	R/W	0b	0 = Adds 0mV of input voltage. 1 = Adds 8192mV of input voltage.
4	Input Voltage, bit 6	R/W	0b	0 = Adds 0mV of input voltage. 1 = Adds 4096mV of input voltage.
3	Input Voltage, bit 5	R/W	0b	0 = Adds 0mV of input voltage. 1 = Adds 2048mV of input voltage.
2	Input Voltage, bit 4	R/W	0b	0 = Adds 0mV of input voltage. 1 = Adds 1024mV of input voltage.
1	Input Voltage, bit 3	R/W	0b	0 = Adds 0mV of input voltage. 1 = Adds 512mV of input voltage.
0	Input Voltage, bit 2	R/W	0b	0 = Adds 0mV of input voltage. 1 = Adds 256mV of input voltage.

Table 7-18b. InputVoltage (Register 0Ah) [reset = VBUS-1.28V]

Bit	Bit Name	Type	POR	Description
7	Input Voltage, bit 1	R/W	0b	0 = Adds 0mV of input voltage. 1 = Adds 128mV of input voltage.
6	Input Voltage, bit 0	R/W	0b	0 = Adds 0mV of input voltage. 1 = Adds 64mV of input voltage.
5-0	Reserved	R/W	000000b	Not used. Value Ignored.

7.13.10 OTGVoltage Register

When SY20776D reversely supply energy to input, the OTG output voltage can be programmable. To set the OTG output voltage limit, write to REG0x07/06() using the data format listed in Table 7-19.
SY20776D provides a OTG output voltage range of 3V to 20.8V with 8mV resolution. All numbers requesting OTG output voltage below 3V or above 20.8V will be ignored. When REG0x34[2] = 1, there is no OTG setting voltage offset. When REG0x34[2] = 0 the OTG setting voltage offset is 1.28V

Table 7-19a. OTGVoltage (Register 07h) [reset = 00h]

Bit	Bit Name	Type	POR	Description
7-6	Reserved	R/W	00b	Not used. 1 = invalid write.
5	OTG Voltage, bit 11	R/W	0b	0 = Adds 0mV of OTG voltage. 1 = Adds 16656mV of OTG voltage.
4	OTG Voltage, bit 10	R/W	0b	0 = Adds 0mV of OTG voltage. 1 = Adds 8328mV of OTG voltage.
3	OTG Voltage, bit 9	R/W	0b	0 = Adds 0mV of OTG voltage. 1 = Adds 4164mV of OTG voltage.
2	OTG Voltage, bit 8	R/W	0b	0 = Adds 0mV of OTG voltage. 1 = Adds 2082mV of OTG voltage.
1	OTG Voltage, bit 7	R/W	0b	0 = Adds 0mV of OTG voltage. 1 = Adds 1041mV of OTG voltage.
0	OTG Voltage, bit 6	R/W	0b	0 = Adds 0mV of OTG voltage. 1 = Adds 521mV of OTG voltage.

Table 7-19b. OTGVoltage (Register 06h) [reset = 00h]

Bit	Bit Name	Type	POR	Description
7	OTG Voltage, bit 5	R/W	0b	0 = Adds 0mV of OTG voltage. 1 = Adds 260mV of OTG voltage.
6	OTG Voltage, bit 4	R/W	0b	0 = Adds 0mV of OTG voltage. 1 = Adds 130mV of OTG voltage.
5	OTG Voltage, bit 3	R/W	0b	0 = Adds 0mV of OTG voltage. 1 = Adds 65mV of OTG voltage.
4	OTG Voltage, bit 2	R/W	0b	0 = Adds 0mV of OTG voltage. 1 = Adds 33mV of OTG voltage.
3	OTG Voltage, bit 1	R/W	0b	0 = Adds 0mV of OTG voltage. 1 = Adds 16mV of OTG voltage.
2	OTG Voltage, bit 0	R/W	0b	0 = Adds 0mV of OTG voltage. 1 = Adds 8.1mV of OTG voltage.
1-0	Reserved	R/W	00b	Not used. Value Ignored.

7.13.11 OTGCurrent Register

When SY20776D reversely supply energy to input, the OTG output current limit can be programmable. To set the OTG output current limit, write to REG0x09/08() using the data format listed in Table 7-20.
SY20776D controls the OTG output current limit by controlling the ACN-ACP voltage. The OTG output current limit range of the SY20776D is 50mA to 6.35A (using a 10mΩ current-sense resistor R_{AC}).

Table 7-20a. OTGCurrent (Register 09h) [reset = 00h]

Bit	Bit Name	Type	POR	Description
7	Reserved	R/W	0b	Not used. 1 = invalid write.
6	OTG Current set by host, bit 6	R/W	0b	0 = Adds 0mA of OTG current. 1 = Adds 3200mA of OTG current.
5	OTG Current set by host, bit 5	R/W	0b	0 = Adds 0mA of OTG current. 1 = Adds 1600mA of OTG current.
4	OTG Current set by host, bit 4	R/W	0b	0 = Adds 0mA of OTG current. 1 = Adds 800mA of OTG current.
3	OTG Current set by host, bit 3	R/W	0b	0 = Adds 0mA of OTG current. 1 = Adds 400mA of OTG current.
2	OTG Current set by host, bit 2	R/W	0b	0 = Adds 0mA of OTG current. 1 = Adds 200mA of OTG current.
1	OTG Current set by host, bit 1	R/W	0b	0 = Adds 0mA of OTG current. 1 = Adds 100mA of OTG current.
0	OTG Current set by host, bit 0	R/W	0b	0 = Adds 0mA of OTG current. 1 = Adds 50mA of OTG current.

Table 7-20b. OTGCurrent (Register 08h) [reset = FFh]

Bit	Bit Name	Type	POR	Description
7-0	Reserved	R/W	11111111b	Not used. Value Ignored.

7.13.12 ADCVBUS/PSYS Register

PSYS full range: 3.06 V, LSB: 12 mV
VBUS full range: 3.2V to 19.52 V, LSB: 64 mV

Table 7-21a. ADCVBUS/PSYS (Register 27h)

Bit	Bit Name	Type	POR	Description
7-0	ADC_VBUS	R		ADC Output of Input Voltage

Table 7-21b. ADCVBUS/PSYS (Register 26h)

Bit	Bit Name	Type	POR	Description
7-0	ADC_PSYS	R		ADC Output of System Power

7.13.13 ADCIBAT Register

ICHG full range: 8.128 A, LSB: 64 mA
IDCHG full range: 32.512 A, LSB: 256 mA

Table 7-22a. ADCIBAT (Register 29h)

Bit	Bit Name	Type	POR	Description
7	Reserved	R		Not used. Value ignored.
6-0	ADC_ICHG	R		ADC Output of Battery Charge Current

Table 7-22b. ADCIBAT (Register 28h)

Bit	Bit Name	Type	POR	Description
7	Reserved	R		Not used. Value ignored.
6-0	ADC_IDCHG	R		ADC Output of Battery Discharge Current

7.13.14 ADCIIN/CMPI Register

IIN full range: 12.75 A, LSB: 50 mA
CMPI full range: 3.06 V, LSB: 12 mV

Table 7-23a. ADCIIN/CMPI (Register 2Bh)

Bit	Bit Name	Type	POR	Description
7-0	ADC_IIN	R		ADC Output of Input Current

Table 7-23b. ADCIIN/CMPI (Register 2Ah)

Bit	Bit Name	Type	POR	Description
7-0	ADC_CMPI	R		ADC Output of CMPI voltage

7.13.15 ADCVSYS/VBAT Register

VSYS full range: 2.88 V to 19.2 V, LSB: 64 mV
VBAT full range: 2.88 V to 19.2 V, LSB: 64 mV

Table 7-24a. ADCVSYS/VBAT (Register 2Dh)

Bit	Bit Name	Type	POR	Description
7-0	ADC_VSYS	R		ADC Output of System Voltage

Table 7-24b. ADCVSYS/VBAT (Register 2Ch)

Bit	Bit Name	Type	POR	Description
7-0	ADC_VBAT	R		ADC Output of Battery Voltage

7.13.16 ManufactureID Register

Table 7-25. ManufactureID (Register 2Eh)

Bit	Bit Name	Type	POR	Description
7-0	MANUFACTURE_ID	R		B6h

7.13.17 Device ID Register

Table 7-26. Device ID (Register 2Fh)

Bit	Bit Name	Type	POR	Description
7-0	DEVICE_ID	R		77h

8 Application Information

The application information for typical application refers to Figure 8-1 as below. This section describes how to select the external components and layout the printed circuit board (PCB).

8.1 Typical Application

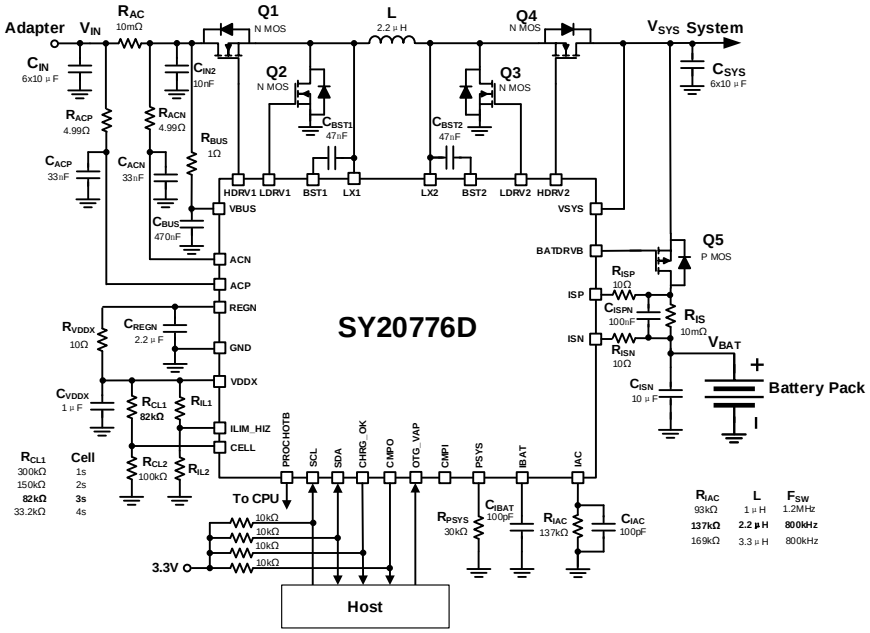


Figure 8-1. Application Diagram (3 cell battery as example)

8.2 External Components Selection

The simplified application circuit Figure 8-1 shows the minimum component requirements. Inductor, capacitor, and power MOSFET selection are explained in the rest of this section. Refer to the EVB file for the complete application schematic.

8.2.1 ACP-ACN Input Filter

SY20776D is average current mode control. The input current sensing through ACP/ACN pin is critical to recover inductor current information. Parasitic inductance on board will generate high frequency ringing on ACP-ACN which overwhelms converter sensed inductor current information, so it is difficult to manage parasitic inductance created based on different PCB layout. Bigger parasitic inductance will generate bigger sense current ringing which will cause the average current control loop to go into oscillation. For real system board condition, we suggest to use below circuit design to get best result and filter noise induced from different PCB parasitic factor. With $R_{ACP/N}C_{ACP/N}$ time constant of filter from 100nsec to 200nsec, the filtering on ringing is effective and, in the meantime, the delay of on the sensed signal is small and therefore poses no concern for average current mode control. $R_{ACP}=R_{ACN}=4.99\Omega$, $C_{ACP}=C_{ACN}=33nF$ is recommended for system design.

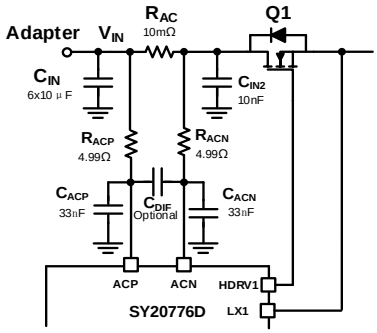


Figure 8-2. ACP-ACN Input Filter

8.2.2 Inductor Selection

Inductor selection trades off between inductor and capacitor size, and power converter loss. SY20776D has two selectable fixed switching frequency. Higher switching frequency allows the use of smaller inductor and capacitor values, but may get more switching loss. An inductor must not saturate under the worst case condition. So inductor saturation current should be higher than the charging current (I_{CHG}) plus the system load current (I_{SYS}) plus half the ripple current (I_{RIPPLE}). Usually inductor ripple is designed in the range of (20 – 40%) maximum charging current plus the system load current as a trade-off between inductor size and efficiency for a practical design. 1μH to 3.3μH inductor is recommended for most application.

In charge mode (OTG mode is similar as below calculation), the saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{L\_SATMIN} > I_{SYS} + I_{CHG} + \frac{V_{SYS}(V_{IN\_MAX} - V_{SYS})}{2 \times V_{IN\_MAX} \times F_{SW} \times L \times \eta} (V_{IN\_MAX} > V_{SYS})$$

$$I_{L\_SATMIN} > \frac{V_{SYS} \times (I_{SYS} + I_{CHG})}{V_{IN\_MIN} \times \eta} + \frac{V_{IN\_MIN} \times (V_{SYS} - V_{IN\_MIN} \times \eta)}{2 \times V_{SYS} \times F_{SW} \times L} (V_{IN\_MIN} \le V_{SYS})$$

Where F_{SW} is the switching frequency, I_{SYS} is the system load current, I_{CHG} is the charging current, V_{IN_MAX} and V_{IN_MIN} is the maximum and minimum input voltage, η is the power conversion efficiency. User can use 90% for calculation. The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. The inductor DC resistance value (DCR) affects the conduction loss of switching converter, so low DCR inductor is recommended especially for high power application. The conductor loss of inductor can be calculated roughly as:

$$P_{L\_DC} = I_L^2 \times DCR$$

I_L is the average value of inductor current, and it equals to I_{CHG} plus I_{SYS} in buck mode.

Besides DC power loss, there are also inductor AC winding loss and inductor core loss, which are related to inductor peak current. Normally, higher peak current causes higher AC loss and core loss. The user can consult with the inductor vendor to select the inductors which have low ESR and low core loss at high frequency.

8.2.3 Input Capacitor

Input capacitor should have enough ripple current rating to absorb input switching ripple current. The input capacitor RMS current in buck mode is calculated as below:

$$I_{CIN\_RMS} = (I_{SYS} + I_{CHG}) \times \sqrt{D_{Buck} \times (1 - D_{Buck})}$$

Where D_{Buck} is power converter duty cycle in buck mode. When duty cycle is 50% in buck mode, the worst case RMS ripple current of input capacitor is half of the output current, which includes charging current plus system load current. Low ESR ceramic capacitor such as X7R or X5R is preferred for input capacitor and should be placed in front of input current sensing resistor (R_{AC}). Voltage rating of the capacitor must be higher than normal input voltage level, 25V or higher rating capacitor is preferred for 19V to 20V input voltage.

Ceramic capacitor (MLCC) shows dc-bias effect, which reduces the effective capacitance when a dc-bias voltage is applied across the ceramic capacitor. The dc-bias effect may lead to a significant capacitance drop, especially for high input voltage and small capacitor package. The derating performance with a dc bias voltage could be obtained through the MLCC datasheet. It may be necessary to choose a higher voltage rating or a higher capacitance value in order to get the required effective capacitance value at the operating voltage point. Considering the 25 V/0603 package MLCC

capacitance derating under 19V to 20V input voltage, the minimum input effective capacitance and practical capacitors configuration is recommended in Table 8-1. Tantalum capacitors (POSCAP) can avoid dc-bias effect and temperature variation effect which is recommended for 90 W to 130 W higher power application.

Table 8-1. Minimum Input Capacitance Requirement

Input Capacitors VS Total Input Power	65W	90W	130W
Minimum effective input capacitance	6μF	9μF	9μF
Minimum practical input capacitors configuration	6x10μF (25V/0603 MLCC)	9x10 μF (25V/0603 MLCC)	9x10μF (25V/0603 MLCC)

8.2.4 Output Capacitor

Output capacitor also should have enough ripple current rating to absorb output switching ripple current. The preferred ceramic capacitor is 25V/X7R or X5R for output capacitor. The MLCC capacitor is suggested to be placed as close as possible to Q_3&Q_4 half bridge (between Q_4 drain and Q_3 source terminal).
Considering MLCC dc-bias effect as described on section 8.2.3, the 25 V/0603 package MLCC capacitance also need to be derated, the recommended practical capacitors configuration at VSYS output terminal is recommended in Table 8-2. Tantalum capacitors (POSCAP) can avoid dc-bias effect and temperature variation effect which are recommended to be used along VSYS output distribution line to meet total minimum effective output capacitance requirement.

Table 8-2. Minimum Output Capacitance Requirement

Output Capacitors VS Total Output Power	65W	90W	130W
Minimum effective output capacitance	28 μF	30 μF	30 μF
Minimum practical output capacitors configuration	6 x10 μF (25V/0603 MLCC)	8 x 10 μF (25V/0603 MLCC)	8 x 10 μF (25V/0603 MLCC)
Additional output capacitors along VSYS distribution line	1 x 22 μF (25-35V POSCAP)	1 x22 μF (25-35V POSCAP)	1 x22 μF (25-35V POSCAP)

8.2.5 Power MOSFETs Selection

Four external N-channel MOSFETs are used for buck-boost switching converter. The gate drivers are internally integrated into the IC with 5.2V of gate drive voltage. 30 V or higher voltage rating MOSFETs are preferred for 19V-20V input voltage. Usually lower $R_{DS(ON)}$ has higher cost with the same package size. The switching MOSFET loss includes conduction loss and switching loss.

For example,in buck mode,it is a function of switching MOSFET duty cycle(D_{buck}), charging current (I_{CHG}), system load current (I_{SYS}), MOSFET's on-resistance ($R_{DS(ON)\_Q1}$), input voltage (V_{IN}), switching frequency (F_{SW}),turn on time (t_{on}) and turn off time (t_{off}):

$$P_{Q1}=D_{buck} \times (I_{SYS}+ I_{CHG})^2 \times R_{DS(ON)\_Q1}+0.5 \times V_{IN} \times (I_{SYS}+ I_{CHG}) \times (t_{on}+t_{off}) \times F_{SW}$$

The first item represents the conduction loss of Q_1. Usually MOSFET $R_{DS(ON)}$ increases by about 50% with 100°C junction temperature rise. The second item represents the switching loss.

The conduction loss of the synchronous MOSFET(Q_2) is calculated with the following equation when it operates in synchronous continuous conduction mode:

$$P_{Q2}=(1-D_{buck}) \times (I_{SYS}+ I_{CHG})^2 \times R_{DS(ON)\_Q2}$$

8.2.6 Current Sensing Resistor Selection

The input current(output current in OTG mode) sense resistor R_{AC} and charge current(discharge current in OTG mode or supplement mode in forward mode) sense resistor R_{IS} is used with 10mΩ by default setting(REG0x31[3:2]=00). Resistor of 1% or higher accuracy and low temperature coefficient is recommended. The resistor power rating should be considered, especially in high current application. The power dissipation of current sense resistor is calculated as $P=I_{RMS}^2R_{AC(or\ IS)}$, and I_{RMS} is the highest current RMS value through the current sense resistor. The resistor power rating should be higher than the calculated value with power derating consideration.

8.3 Layout Guidelines

Proper PCB layout could minimize high frequency current path loop to prevent electrical and magnetic field radiation that could induce high frequency resonant problems. For the efficiency, thermal, noise consideration, the following layout guidelines are recommended. Refer to Figure 8-3 to get a general reference for layout design.

1. It is desirable to maximize the PCB copper area connecting to power ground to achieve the best thermal and noise performance. A power ground plane layout is highly desirable. The via size and number among different power ground layers should be enough for high current path. Especially, the exposed power GND pad on the backside of the IC should be soldered to the PCB power ground. Ensure that there are sufficient vias directly under the IC, connecting to the power plane on the other power ground layers.
2. Route signal ground (SGND) separately from power ground (PGND). PGND should be used for all power stage related ground net. SGND should be used for all sensing, and control network ground for example ACP/ACN/CMPI/CMPO/IAC/IBAT/PSYS. Connect all signal ground to a dedicated low-impedance copper plane, which is tied to the power ground underneath the IC exposed pad. Connect signal ground and power ground together with a single ground connection point. A signal ground copper plane layout beneath the IC is highly desirable.
3. Place the input capacitor C_{IN}, input current sense resistor R_{AC}, buck MOSFET bridge (Q_1 and Q_2) as close as possible to form a small loop (refer $Loop_{IN}$ in Figure 8-3). After R_{AC} and before Q_1 and Q_2 power stage，a 10nF decoupling capacitors is recommend to put as close as possible to IC to decouple switching loop high frequency noise.
4. The current path from V_{IN} to V_{SYS}, through R_{AC}, Q_1, L, Q_4 should be low impedance to carry the high switching current. Pay attention to via resistance if they are not on the same side.
5. Place the output capacitor C_{SYS}, boost MOSFET bridge (Q_3 and Q_4) as close as possible to form a small loop (refer $Loop_{SYS}$ in Figure 8-3). It is best to put them on the same side. Connect them with large copper to reduce the parasitic resistance.
6. Place BATFET Q_5 and charge/discharge current sense resistor R_{IS} near the battery terminal. The current path from V_{BAT} to V_{SYS}, through R_{IS} and Q_5, should be low impedance to carry the high charge/discharge current. Pay attention to via resistance if they are not on the same side.
7. Place buck-boost power converter,Q_1, Q_2, L, Q_3 and Q_4 next to each other. Allow enough copper area for thermal dissipation. Multiple thermal vias could be used to connect more copper layers together and dissipate more heat.
8. Use Kelvin-sensing technique for R_{AC} and R_{IS} current sense resistors. Connect the current sense traces to the center of the sense resistor pads, and run current sense traces as differential pairs. Do not route the sense leads through a high-current path.
9. Place VBUS/REGN/VDDX/IBAT/IAC ceramic capacitors to near the IC pins as close as possible.
10. Place high-side MOSFET boost strap capacitor close to the IC pins and on the same side of PCB board. Ceramic capacitors LX1 and LX2 nodes are recommended to use wide copper polygon to connect to power stage. Ceramic capacitors BST1 and BST2 node are recommended to use wide trace to connected to IC pins.
11. The PCB copper area associated with LX1 and LX2 must be minimized to avoid the potential noise problem. But make the trace wide enough to carry the switching current. Do not use multiple layers in parallel for the LX1 and LX2 connection.

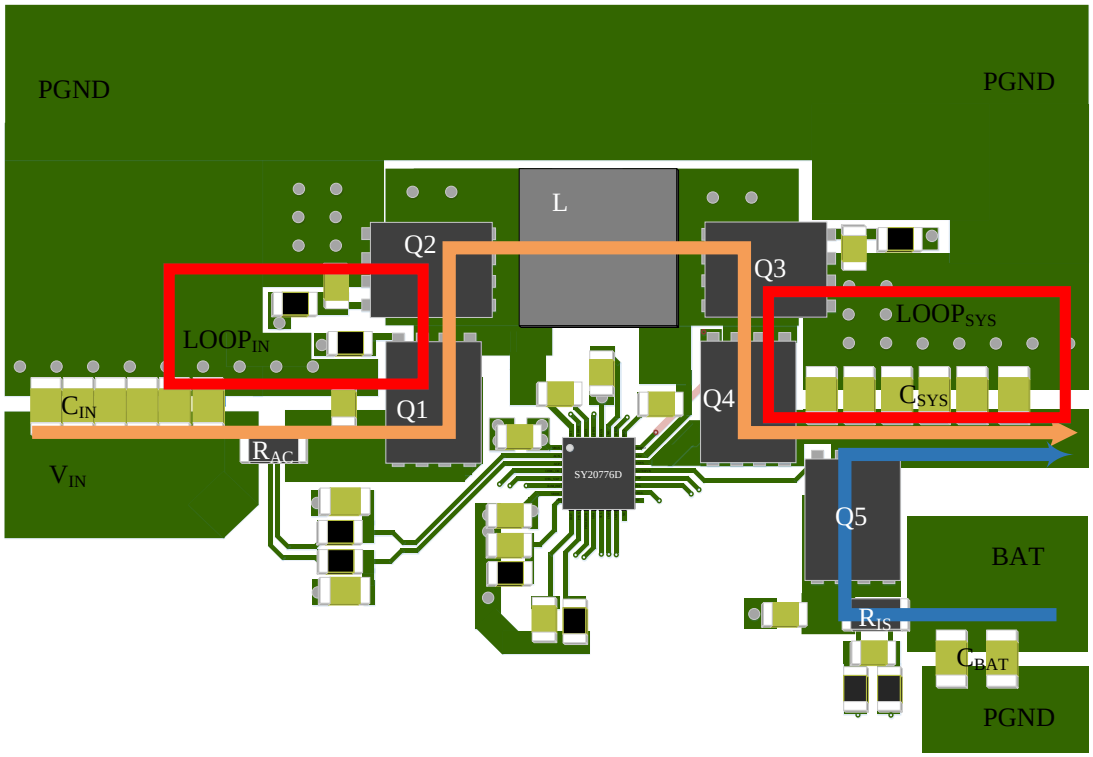
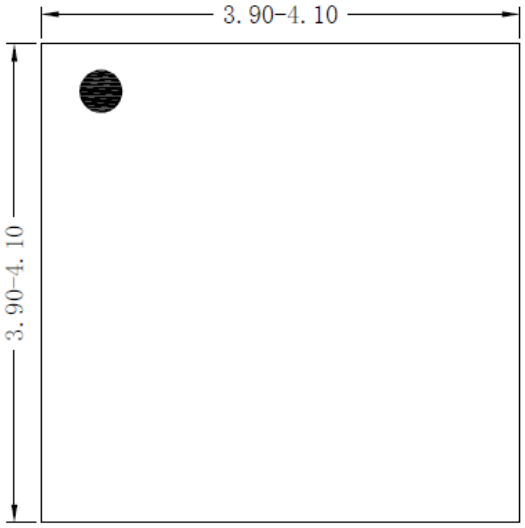
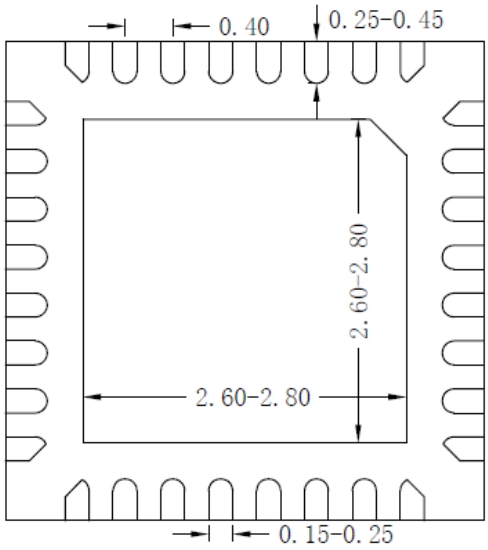


Figure 8-3. Layout Reference Example In Top View

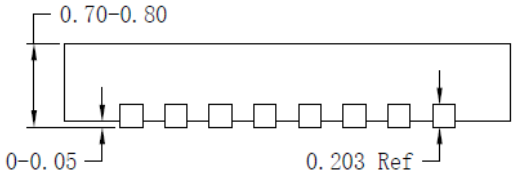
QFN4*4-32 Package Outline Drawing



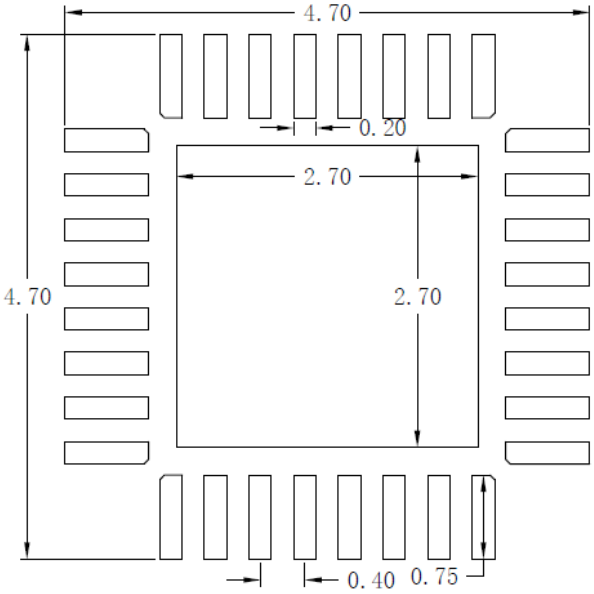
Top View



Bottom View



Side View

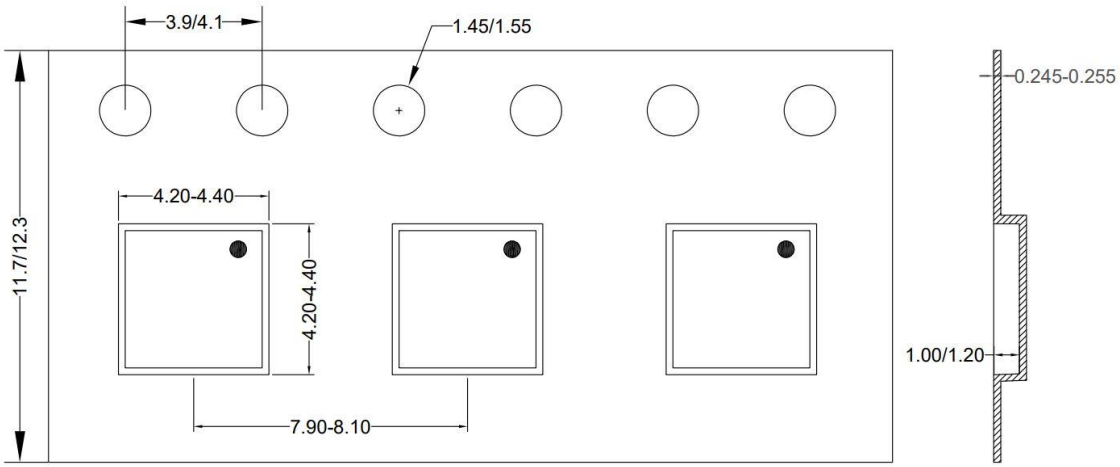


Recommended PCB layout (Reference only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

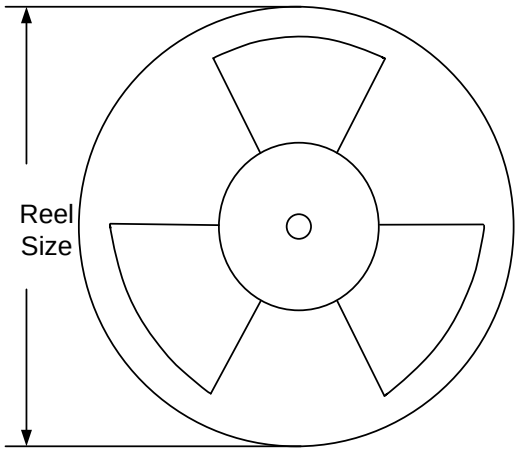
Taping & Reel Specification

1. QFN4×4 taping orientation



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN4×4	12	8	13"	400	400	5000

3. Others: NA