SY2A29705

Boost/Flyback Current Mode Controller

General Description

SY2A29705 is a fixed frequency and current mode controller for Boost/ Flyback/Sepic topology. Typical 4ms internal soft-start time to force a controlled start-up when start up or fault happened. UVLO、OCP and OTP protection are available to protect IC. Typical 150-μA starting up current and 800-μA operating supply current exclude MOS driving current. Flexible frequency and minimum off time set by FS pin and up to 1 MHz switching frequency. Up to 1A GATE sourcing and sinking capability.

Ordering Information

SY2A29705 □(□□□)

Package Code

Optional Spec Code

Ordering Number	Package Type	Note
SY2A29705FAP	SO8	------

Features

- AEC-Q100-Grade 1: -40°C ~125°C
- 5.0-11V Input Voltage Range
- ±2% Accuracy for REF and FB Reference
- Typical 150-μA Starting up Current and 800-μA Operating Supply Current Exclude MOS Driving Current
- Flexible Frequency and Minimum off Time Set by FS Pin and up to 1 MHz Switching Frequency
- Cycle by Cycle Current Limit(1V) and over Current Limit (1.5V) for ISEN
- Typical 4ms Internal Soft Start and Fault Soft-start(OCP、OTP、REF_UVLO、VIN_UVLO)
- Package:SO8

Applications

- Switch Mode Power Supplies (SMPS)
- DC-to-DC Converters
- Power Modules
- Automotive Power Supply Unit
- Battery-operated Power Supply Unit

Typical Applications

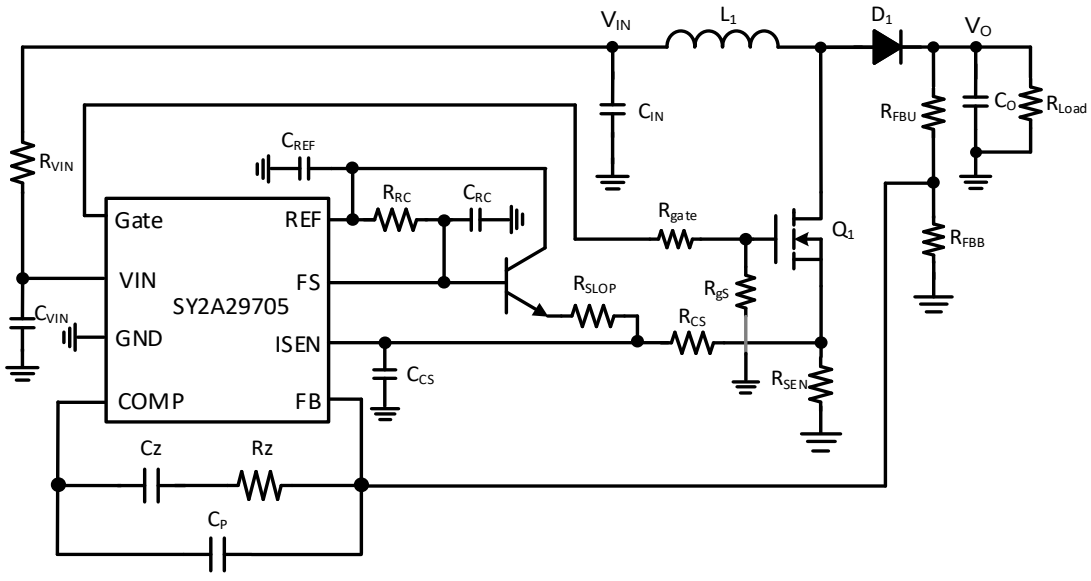


Fig.1 Schematic Diagram (Boost Topology)

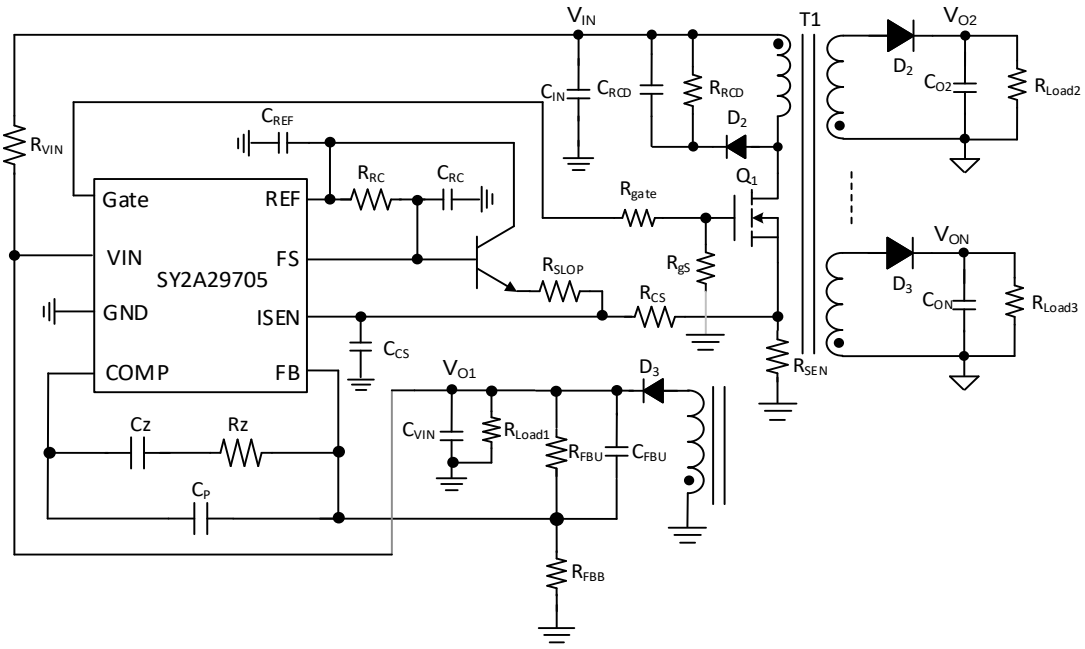


Fig.2 Schematic Diagram (Flyback Topology)

Block Diagram

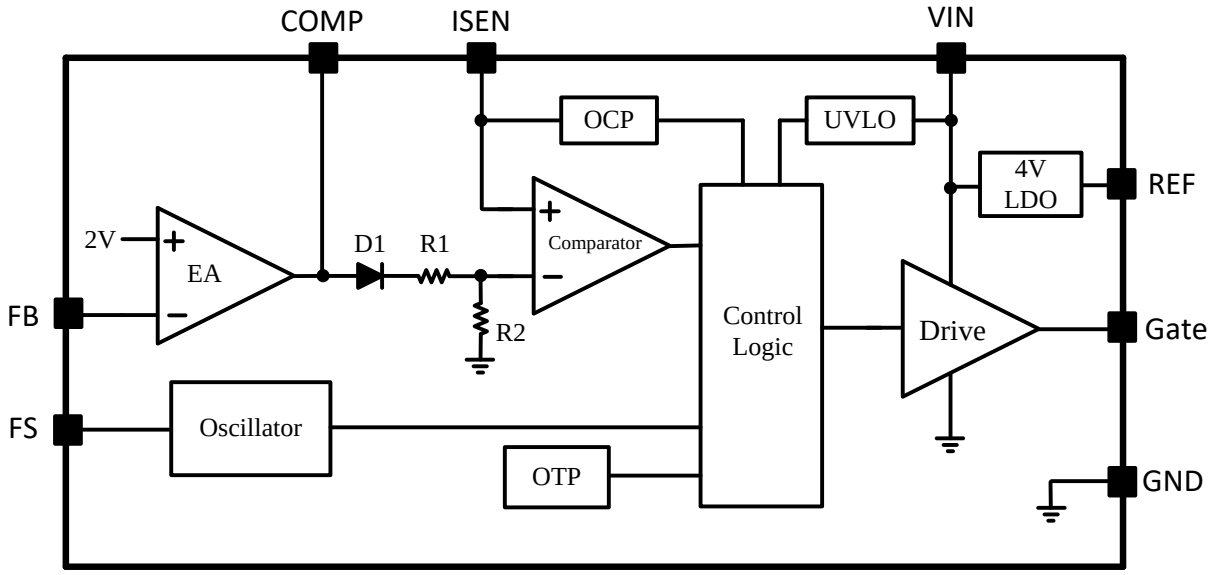
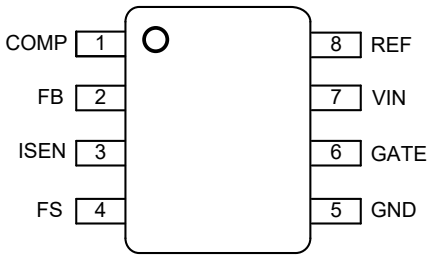


Fig.3 Detailed Block Diagram

Pinout (top view)



(SO8)

Top Mark: **EUQ*xyz***, **(**Device code: EUQ; ***x=year code, y=week code, z= lot number code*****)**

Pin Name	Pin Description	
COMP	1	External compensation pin. Connect RC network from this pin to GND to compensate the control loop.
FB	2	Output voltage feedback pin. The output voltage reference is 2V.
ISEN	3	Current sense pin. Connect an external current sensing resistor RSEN from this pin to GND. The voltage on this pin is used to provide mosfet current feedback in the control loop and peak current limit. The cycle-by-cycle peak current limit threshold and the hiccup peak current limit threshold are 1V and 1.5Vrepectively.
FS	4	FS is used to set the oscillator frequency and minimum off time pin. Connecting a resistor from REF to FS and a capacitor from FS to GND to set the frequency and minimum off time. The frequency can be calculated as follow: $f_{OSC} = \frac{K_{RC}}{R_{RC} \times C_{RC}}$ Where • K_{RC} is the frequency coefficient K_{RC}=1 • frequency is in Hz • resistance is in Ω • capacitance is in farads The recommended R_{RC} is between 10 k and 200 k, and C_{RC} is 100 pF to 1000 pF. Never use a resistor less than 10 k.
GND	5	Ground Pin.
GATE	6	GATE is the MOSFET driving pin. Connect to the gate of power MOSFET.
VIN	7	Input supply pin. Decouple this pin to GND pin with at least 1uF ceramic capacitor.
REF	8	4V Internal LDO output from VIN. A 100nF capacitor is recommended to be connected from this pin to GND.

Absolute Maximum Ratings (Note 1)

VIN, GATE ---------- -0.3V to 12V
COMP, REF ---------- -0.3V to the lesser of VIN+0.3 / 6V
FB, ISEN, FS ---------- -0.3V to the lesser of VIN+0.3 / 4V
Power dissipation @ T_A = 25°C ---------- 0.65W
Package Thermal Resistance (Note 2)
Θ_{JA} ---------- 107°C/W
Θ_{JC}(Top)---------- 49°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
ESD Susceptibility (Note3)
HBM (Human Body Mode) ---------- 2000V
CDM (Charge Device Mode) All pins---------- 500V
Corner pins---------- 750V

Recommended Operating Conditions (Note 3)

Supply Voltage VIN ---------- 5V to 11V
COMP, REF ---------- -0.3 to 6V
FB, ISEN, FS ---------- -0.3V to 3.6V
Junction Temperature Range ---------- -40°C to 125°C

Electrical Characteristics

(-40°C≤T_j≤125°C, VIN = 10V, C_{VIN}=1uF, C_{REF}=100nF, R_{RC}=100k, C_{RC}=330pF unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VIN Pin						
VIN UVLO ON Threshold	V_{VIN_START}		3.7	4.1	4.5	V
UVLO ON OFF Hysteresis	V_{UVLO_HYS}			0.5		V
Start Up Current	I_{START}	V_{VIN}=3V, V_{FB}=0V		0.15	0.25	mA
Operating Current	I_{OP}	V_{ISEN}=0V, V_{FB}=0V		0.8	1.25	mA
VIN Pin Clamping Voltage	V_{IN_CL}	I_{VIN}=10mA	14	15.4	16.8	V
REF Pin						
Output Voltage Of REF	V_{REF}	I_{REF} = 0.2 mA	3.92	4	4.08	V
Drop Out Voltage	V_{REF_HR}	I_{REF} = 5mA		0.12	0.25	V
Load Regulation	$\triangle V_{REF\_LOR}$	0.2 mA ≤ I_{REF} ≤5 mA		10	30	mV
Line Regulation	$\triangle V_{REF\_LIR}$	T_J= 25°C, V_{VIN} = 5V to 11V (I_{VIN} =5mA)			1.9	mV/V
		T_J= –40°C to 125°C, V_{VIN} =5V to 11V (I_{VIN} =5 mA)			2.5	mV/V
REF Short Circuit Current	I_{REF_LIMH}		6	11	17	mA
FS Pin						
Oscillator Frequency	F_{OSC}	R_{RC}=100k, C_{RC}=330pF	26	31	36	kHz
Oscillator Upper Threshold	V_{OSC_H}			2.55		V
Maximum Duty Cycle	D_{MAX}	R_{RC}=100k, C_{RC}=330pF	97	99		%
FB&COMP Pins (ERROR AMPLIFIER)						
Output Feedback Reference	V_{FB}		1.96	2	2.04	V
FB Input Bias Current	I_{FB_BIAS}		-1		1	μA
COMP Sinking Current	I_{COMP_SINK}	FB=2.7V, COMP=1.1V	0.3	1.1	2.1	mA
COMP Sourcing Current	I_{COMP_SOURCE}	FB=1.8V, COMP=2.7V	-0.1	-0.4	-0.8	mA
Soft-start Time Of COMP	T_{SS}	V_{FB} = 1.8 V, COMP rise from 0.5V to 3.0V		4	10	ms
ISEN Pins						
COMP To ISEN Coefficient	K_{COMP_ISEN}		1.40	1.65	1.9	V/V
COMP to ISEN Offset	V_{OFFSET}	ISEN=0V, I_{F_DIODE}=200nA	0.30	0.70	1.0	V
ISEN Input Bias Current	I_{ISEN_BIAS}			1.2		μA
Cycle By Cycle Current Limit Threshold	V_{ISEN_OCP}	COMP=3V	0.9	1.0	1.1	V
Hiccup Operation Current Limit Threshold	V_{ISEN_HICCUP}		1.38	1.50	1.62	V
Thermal						
Thermal Shutdown Threshold	T_{SD}		150	165	180	ºC
Thermal Shutdown Hysteresis	T_{SDHYS}			15		ºC

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

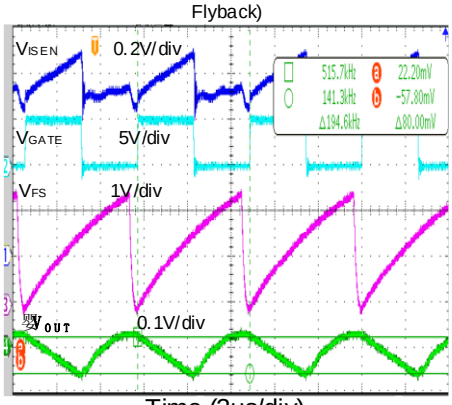
Note 2: θJA is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Operation Characteristics

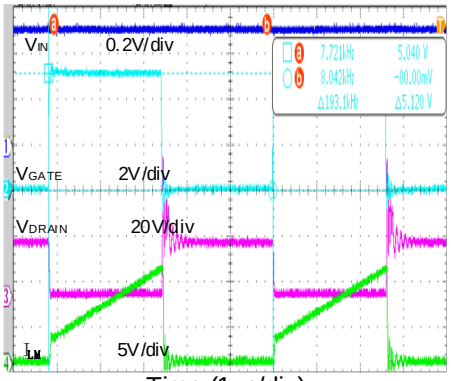
Steady State

(V_{IN}=5V, P_{VIN}=12V, V_{OUT}=12V, I_{OUT}=1A, Fsw=193kHz, Flyback)



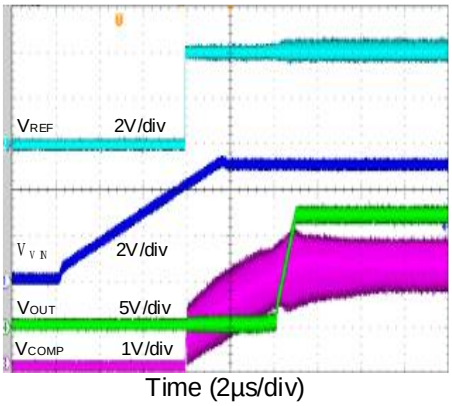
Steady State

(V_{IN}=5V, P_{VIN}=12V, V_{OUT}=12V, I_{OUT}=1A, Fsw=193kHz, Flyback)



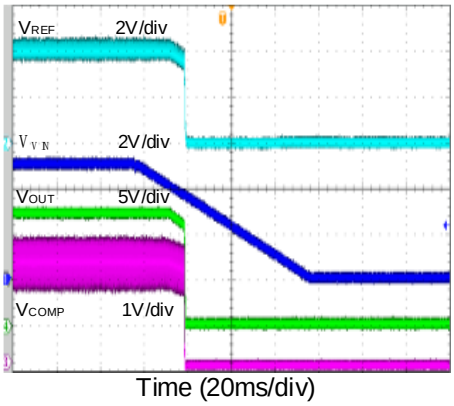
Start Up

(V_{IN}=5V, P_{VIN}=12V, V_{OUT}=12V, I_{OUT}=1A, Fsw=193kHz, Flyback)



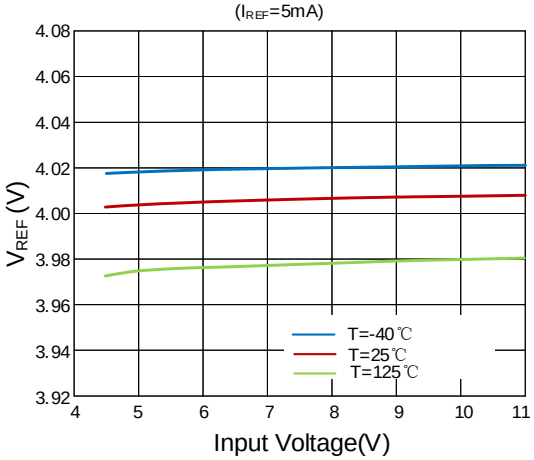
Shut Down

(V_{IN}=5V, P_{VIN}=12V, V_{OUT}=12V, I_{OUT}=1A, Fsw=193kHz, Flyback)

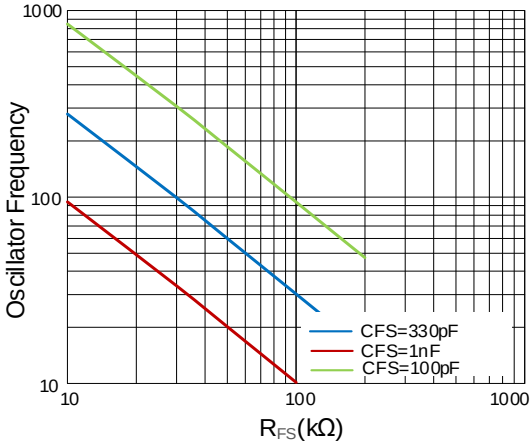


V_{REF} vs. V_{IN}

(I_{REF}=5mA)



Oscillator Frequency vs. RFS and CFS



Operation Principle

SY2A29705 is a fixed frequency and current mode controller for Boost/Flyback/Sepic topology. External compensation provides flexible adjustment of control loops for different applications. Up to 1A GATE sourcing and sinking capability. It adopts fixed frequency peak current mode control to ensure reliable over current protection and cycle by cycle switch current limit.SY2A29705 provides reliable protections such as Over Current Protection (OCP), Over Temperature Protection (OTP), etc.

Applications Information

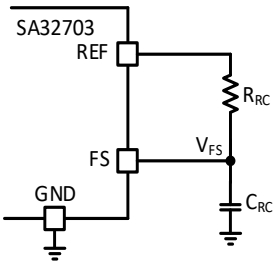
1、Switching Frequency Formula:

FS is the frequency set pin. Connect a resistor R_{RC} to REF pin and a C_{RC} to GND pin to set f_{SW}.

F_{SW} can be calculated to be:

$$f_{SW} \approx \frac{1}{R_{RC} \times C_{RC}} \qquad (1)$$

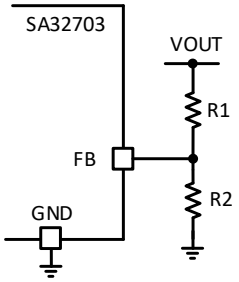
1:The recommended R_{RC} range is from 10KΩ to 200KΩ and C_{RC} range is from 100pF to 1nF.



2、Feedback resistor dividers R1 and R2:

Choose R1 and R2 to program the output voltage under CV mode. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R1 and R2. A value of between 1k and 100k is highly recommended for R2. VOUT can be calculated to be:

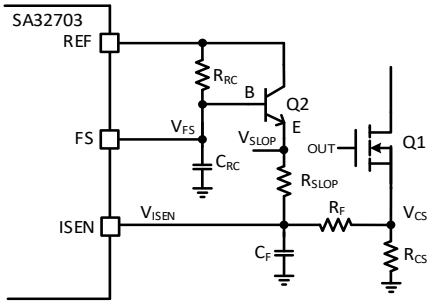
$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) \qquad (2)$$



3、Peak Current Sense Resistor

An external sensing resistor Rcs is used to sense the current flow through the MOSFET. The sensed voltage is for peak current mode control and cycle by cycle peak current limit. The cycle-by-cycle current limit threshold is 1V and hiccup current limit threshold is 1.5V.

In current mode control applications, when duty cycles exceeds 50%, it is easy to cause subharmonic oscillation.so slope compensation is necessary to avoid this issue, especially in continuous current mode. Slope compensation can be added as follow:



The slope compensation slew-rate Se is calculated by:

$$Se \approx 1.95V \times \frac{1}{t_{SW}} \times \frac{R_F}{R_F + R_{SLOP}} \qquad (3)$$

Select the suitable R_{CS} if slope compensation is applied as follow:

$$R_{CS} = \frac{1 \times (R_{SLOP} + R_F) - 1.95 \times D \times R_F}{R_{SLOP}} \times \frac{1}{I_{PKH}} \qquad (4)$$

4、MOSFET and Diode

When power MOS is turned off, the drain to source voltage is equal to Vin plus Vo*Nps, so the break down voltage of power MOS should be larger than the maximum value of Vin plus Vo*Nps. When power MOS is turned off, a voltage spike is always generated due to the parasitic inductance, so voltage rating safe margin should be taken into consideration.

$$V_{MOS\_MAX} = V_{IN} + (V_{OUT} + V_f) \times N_{ps} \qquad (5)$$

Where N_{ps} is the turns ratio of the Flyback transformer

Average current flowing through the diode is equal to the output current, so the diode current rating should be larger than the maximum output current. Reverse voltage of the diode is equal to VIN plus VO, so the reverse voltage of the diode should be selected to be larger than the maximum value of VIN plus Vo. It is better to select a Schottky diode to reduce the reverse recovery loss.

$$V_{D1\_MAX} = V_{OUT} + V_{IN} \times \frac{1}{N_{ps}} \qquad (6)$$

5、Main inductor L for Flayback Design:

Choose proper inductance to achieve desired current ripple.It is suggested to choose the ripple current rate Krp to be about 50% of the maximum input current. The inductance is calculated as:

$$L_m = \frac{V_{IN}^{\ 2} \times N_{ps}^{\ 2} \times \frac{V_{OUT}}{(V_{IN} + N_{ps} \times V_{OUT})^2} \times (1 - \frac{Krp}{2})}{Krp \times I_{OUT} \times f_{SW}} \qquad (7)$$

Layout Design

(a)The circuit loop of all switching circuit should be kept small: primary power loop, secondary loop, and auxiliary power loop.

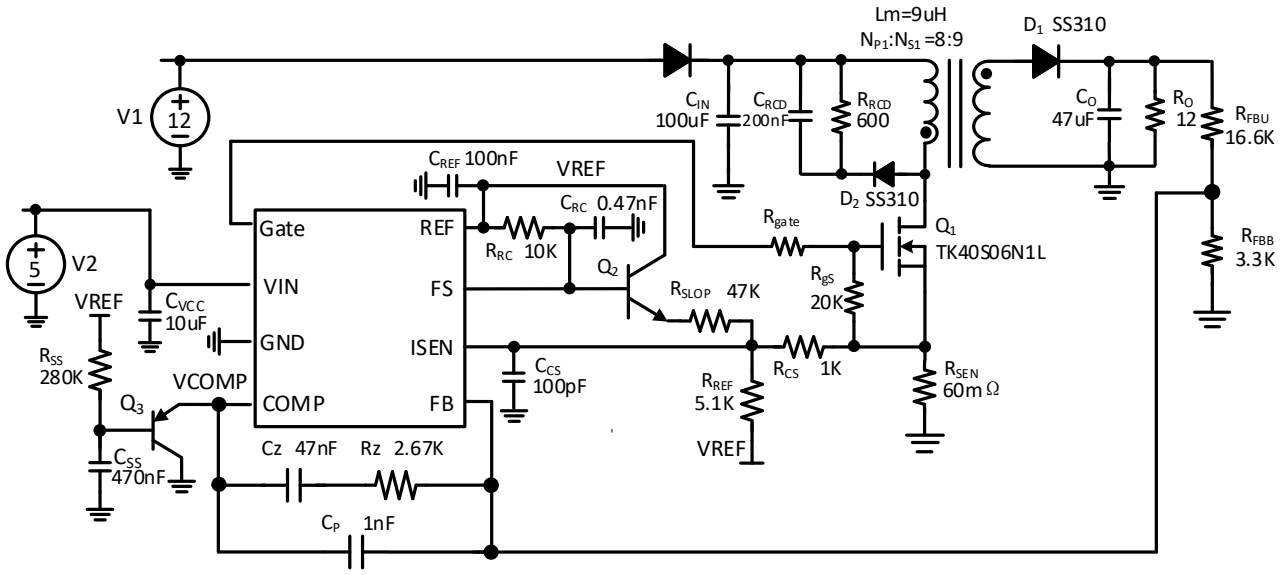
(b)A decoupling capacitor is required for both the VIN pin and REF pin and both must be returned to GND as close to the IC as possible.

(c)The ISEN pin filter capacitor must be as close to the IC possible and grounded right at the IC ground pin.

(d)Gate driver loop area must be minimized to reduce the EMI noise because of the high di/dt current in the loop

Design Example

A design example of Flyback application is shown below.



Identify design specification

Design Specification			
V_{IN}	9V~12V	V_{OUT}	12V
Fsw	212kHz	I_{OUT}	1A
		η	85%

Switching Frequency

For this example, R_{RC}=10k and C_{RC}=470pf were selected to operate at 212kHz

$$fsw \approx \frac{1}{R_{RC} \times C_{RC}} = 212kHz$$

Inductor Selection

The transformer turns ratio can be selected as:

$$N_{ps} = \frac{8}{9}$$

The maximum input current I_{IN_MAX} and duty cycle D_{MAX} can be calculated as:

$$I_{IN\_MAX} = \frac{V_{OUT} \times I_{OUT}}{V_{IN\_MIN} \times \eta} = 1.569A$$

$$D_{MAX} = \frac{Nps \times V_{OUT}}{V_{IN\_MIN} + N_{ps} \times V_{OUT}} = 0.542$$

The Primary inductor peak current I_{PK_P} and valley current I_{VAL_P} can be calculated as:

$$I_{PK\_P}=\frac{P_{IN}}{V_{IN\_MIN}\times(1-\frac{Krp}{2})\times\frac{t_{ON\_MAX}}{t_{SW}}}=4.252A$$

$$I_{VAL\_P}=I_{PK\_P}\times(1-Krp)=1.701A$$

The primary inductor L_m can be calculated as:

$$L_m=\frac{V_{IN\_MIN}\times t_{ON\_MAX}}{Krp\times I_{PK\_P}}=9uH$$

The primary inductor RMS Current I_{RMS_P} can be calculated as:

$$I_{RMS\_P}=\sqrt{\frac{1}{t_{SW}}\times\int_0^{t_{ON\_MAX}}(I_{PK\_P}(t))^2\,dt}=2.258A$$

It is important that the RMS current and saturation current ratings of the inductor are not exceeded.

Transformer Design Specifications

Item	Partnumber
Bobbin	PQ2016
Lm(uH)	9.0uH
Llk(uH)	0.53uH
Primary Turns	8
Secondary Turns	9
Primary Winding(mm)	Φ0.23×7
Secondary Winding(mm)	Φ0.23×7

MOSFET and Diode Selection

The peak current and RMS current of MOSFET are same as primary inductor.

$$V_{MOS\_MAX}\geq 1.2\times(V_{IN}+(V_{OUT}+Vf)\times N_{ps})=24\ V$$

$$I_{MOS\_RMS}>2\times I_{RMS\_P}=4.5\ A$$

TK40S06N1L is used in this design. The TK40S06NIL have $R_{DS(ON)}$ = 8.7 mΩ, V_{DSS}=60V and I_D=40A.

Output diode RMS current I_{RMS} and maximum voltage can be calculated as:

$$I_{D\_RMS}>2\times I_{OUT}=2\ A$$

$$V_{D1\_MAX}\geq 1.2\times(V_{OUT}+\frac{V_{IN\_MAX}}{N_{ps}})=26.5\ V$$

SS310 diode is used in this design.

Output capacitor Selection

Output capacitor is selected according to the output voltage ripple requirement. Suppose the output voltage ripple is 0.5% of V_{OUT}, the capacitor valley can be calculated as:

$$C_{OUT} \geq \frac{I_{OUT} \times D_{MAX}}{0.5\% \times V_{OUT} \times f_{SW}} = 47uF$$

5 PCS low ESR 10uF ceramic capacitor is recommended.

Current Sense Resistor Selection

The current sensing network consists of R_{SEN}, R_{REF}, R_{SLOP}, R_{CS}, C_{CS}. For this example, to achieve 3.844A primary side peak current, a 60mΩ resistor is chosen for R_{SEN}.

C_{CS} is chosen to be 100pf to provide enough filtering to suppress the leading-edge spike.

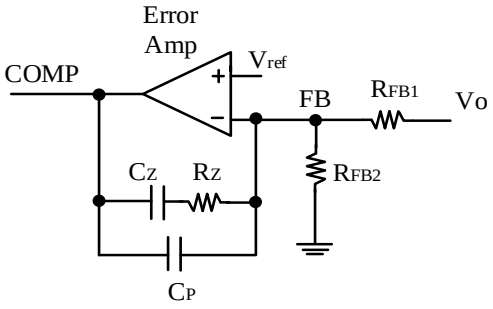
R_{REF} and R_{CS} form a resistor divider network from the current sense signal to the reference voltage to offset the current sense voltage. Offset voltage can be calculated when chose R_{REF}=5.1kΩ and R_{CS}=1kΩ：

$$V_{offset} = \frac{R_{CS}}{R_{CS} + R_{REF}} \times V_{REF} = 0.655V$$

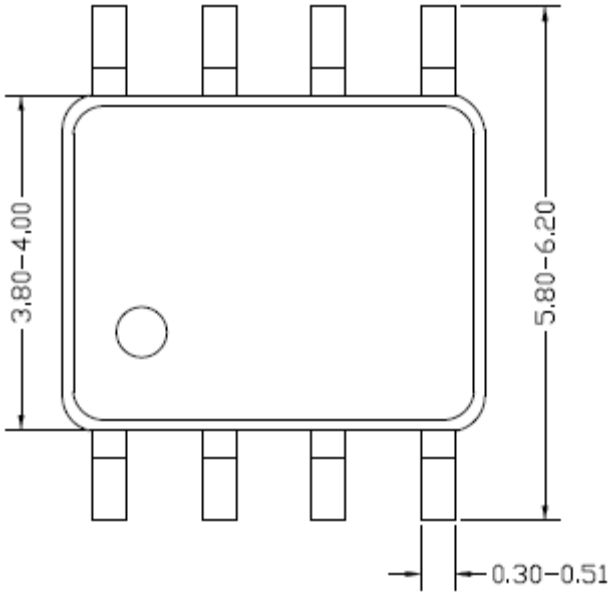
R_{SLOP}=47kΩ and Q2=MMBT3904 were chosen as slope compensation network.

Control Loop Compensation Design:

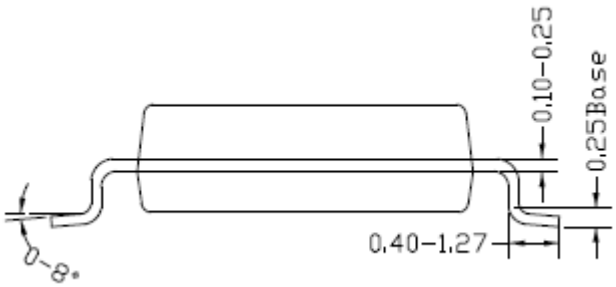
SY2A29705 is a fixed frequency and current mode controller. It integrates a volage mode error amplifier. For this example, a type II compensator is applied to stable the system. Rz=2.67k, Cz=47nF, Cp=1nF in this example is recommended.



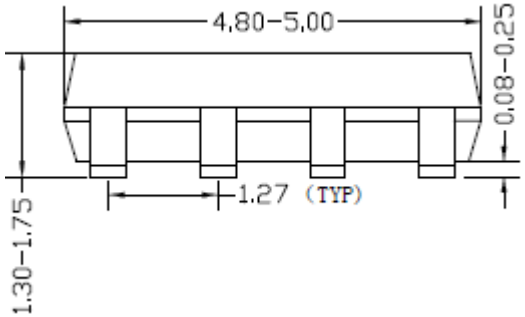
SO8 Package outline & PCB layout design



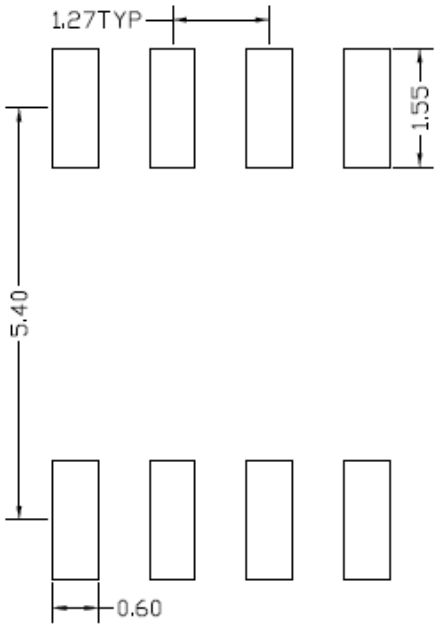
Top view



Side view



Front view

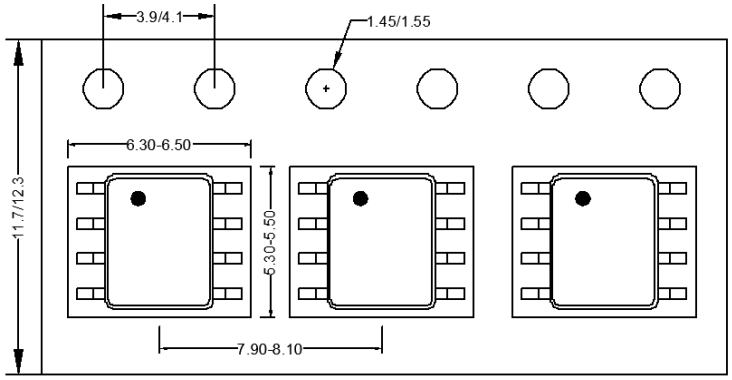


Recommended Pad Layout
(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

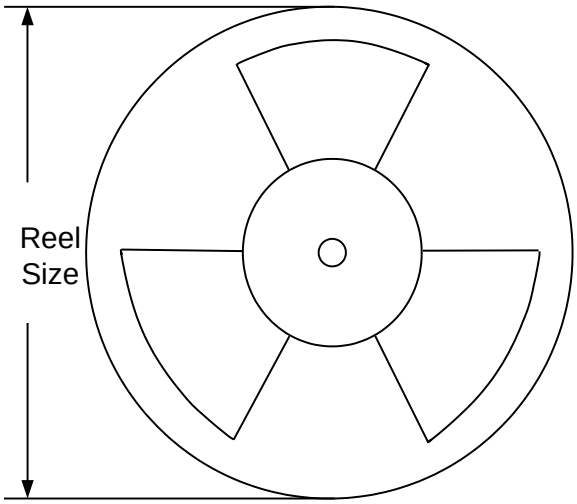
Taping & Reel Specification

1. Taping orientation for packages（SO8）



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SO8	12	8	13"	400	400	2500

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Dec. 27, 2022	Revision 0.9	Initial Release

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