SY23212A

IEEE 802.3 af/at-Compatible PoE Power Device Interface with 13W High-frequency PSR Flyback Converter

General Description

The SY23212A is a combined Power over Ethernet (PoE) powered device (PD) solution with PD interface and optimized PSR Flyback converter integrated.

The SY23212A supports the IEEE 802.3 af/at Standard as a 13W powered device. It includes detection and classification modes, a 100V hot-swap switch, as well as the maintain power signature function. To achieve higher efficiency and better EMI performance, the SY23212A drives Flyback converters in Quasi-Resonant mode and adaptive PWM/PFM control, the maximum switching frequency is up to 600 kHz. The internal 180V, 0.65Ω MOSFET achieves good thermal performance in compact package, QFN4×5-28.

The SY23212A provides comprehensive and reliable protections including OLP, VCC OVP, cycle by cycle peak current limit, internal OTP, etc.

Features

- Supports the IEEE 802.3 af/at Standard
- 100V, 0.45Ω Hot-swap Switch
- Adaptor ORing Support
- Power up to 13W(Input) PDs
- Primary Side Control and Internal Current Sense to Minimize Components Number
- QR-mode Operation and PWM/PFM Control for High Efficiency
- Integrate 180V,0.65Ω MOSFET for Converter
- RoHS Compliant and Halogen Free
- Compact Package: QFN4×5-28

Applications

- IEEE 802.3af/at Complaint Devices
- Video and VoIP Telephones
- RFID Readers
- Multi-band Access Points
- Security Cameras

Ordering Information

SY23212□(□□□)

Package Code

Optional Spec Code

Ordering Number	Package type	Note
SY23212ATQQ	QFN4 × 5-28	----

Typical Applications

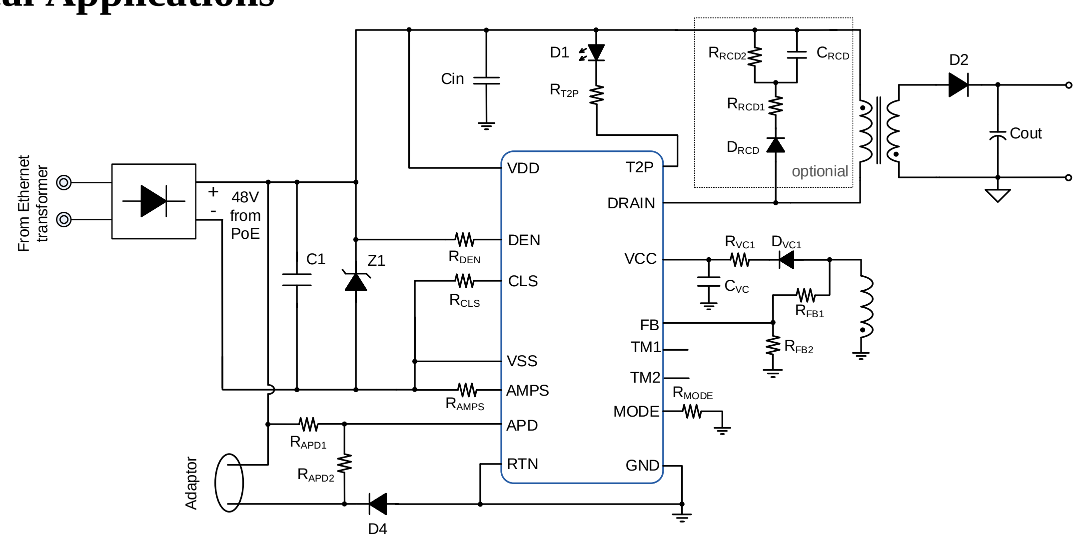
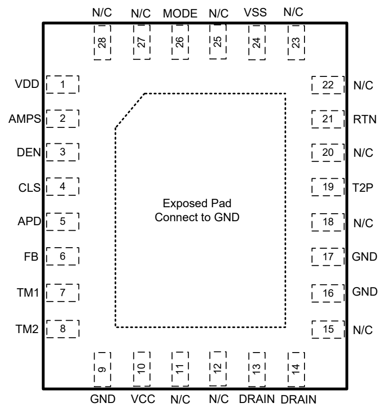


Figure 1. Schematic Diagram

Pinout (top view)

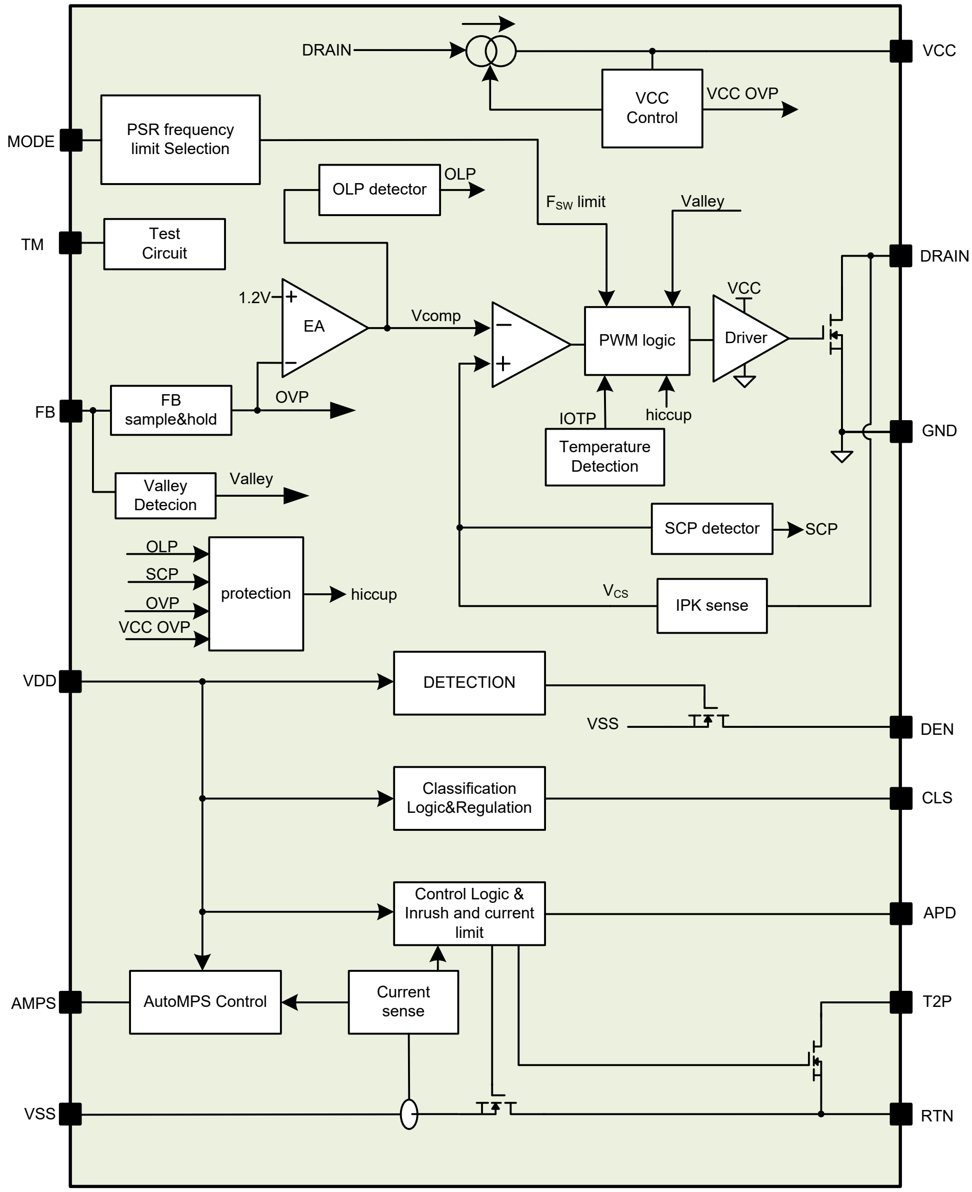


QFN4×5-28

Top Mark: EDX*xyz* (device code: EDX, ***x=year code, y=week code, z= lot number code*)**

Pin Name	**Pin number**	**Pin Description**
VDD	1	Positive power supply pin for PoE and converter input power rail.
AMPS	2	Automatic maintain power signature control pin. Connect a resistor with appropriate power rating (to support the maintain power signature current) from AMPS to VSS to program the MAINTAIN POWER SIGNATURE current amplitude. Leave AMPS open to disable the automatic maintain power signature function.
DEN	3	Detection pin. Connect a 24.9kΩ resistor between VDD and DEN for PoE detection.
CLS	4	Classification pin. Connect a resistor from CLS to VSS to program the classification current.
APD	5	Auxiliary power input detection pin. Drive VDD-ADP higher than 1.5V to disable hot-swap MOSFET and CLS pin function, and force T2P active.
FB	6	Output voltage feedback pin. Connect one resistor divider from sensing winding to regulate output voltage.
TM1, TM2	7,8	Factory test pin only. Leave it floating in application.
GND	9,16,17	Negative rail input pin of the DC/DC converter.
VCC	10	DC/DC internal circuit supply pin. Connect a capacitor between this pin and GND to bypass VCC supply.
DRAIN	13.14	Drain pin of internal power MOSFET.
T2P	19	Type-2 PSE indication pin. T2P is an open-drain output. T2P pulled low to RTN indicates the presence of a Type-2 PSE or the presence of a wall adapter.
RTN	21	Drain pin of internal hot-swap MOSFET.
VSS	24	Negative power supply pin from PoE input power rail.
MODE	26	Frequency selection pin. Detail information refers to “Work Mode Detection” section.
N/C	11,12,15,18,20, 22,23,25,27,28	Not connect this pin internally.

Block Diagram



Absolute Maximum Ratings [1]

Pins Voltage Respects to VSS:

VDD, RTN, APD, T2P, DEN--- -0.3V to +100V
AMPS[2], CLS[2] --- -0.3V to +5.5V

Pins Voltage Respects to RTN:

VDD, T2P-- -0.3V to +100V

Pins Voltage Respects to GND:

DRAIN-- -0.3V to +180V
VCC--- -0.3V to +23V
FB--- -0.3V to +10V
MODE, TM1, TM2-- -0.3V to +3.3V

Pins Current:

FB Sink Current --- ±2mA [3]
T2P Sink Current--- 5mA
AMPS Source Current---15mA
Junction Temperature--- 150℃
Lead Temperature-- 260℃
Storage Temperature-- -55℃ to +150℃

Recommended Operating Conditions

Supply Voltage VDD--- 0V to 57V
Maximum T2P Sink Current--- 3mA
Maximum AMPS Source Current--- 13mA
Maximum FB Sink Current-- ±1mA
Operating Junction Temperature (T_J)-- -40℃ to +125℃

Notes:

(1) Exceeding these ratings may damage the device.
(2) Voltage should not be externally applied to this pin.
(3) FB is clamped by internal circuit. The sink/ source current should be limited. Detail information please refer to “Voltage Control” section.

Electrical Characteristics (Interface Part)

VDD, CLASS, DEN and RTN voltages are referred to VSS, T2P voltage is referred to RTN. VDD-VSS=48V, VSS=0V, R_{DEN}=24.9 kΩ, R_{CLS}=90.9 Ω, T_J=-40°C to +125°C [4], typical values are tested at T_J=25°C, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Detection						
Detection on	V_{DET_ON}	V_{DD} rising		1.1	1.4	V
Detection off	V_{DET_OFF}	V_{DD} rising		11		V
DEN Leakage Current	V_{DET_LK}	V_{DET}=V_{DD} =57V, measure I_{DET}		0.1	5	μA
Bias Current		V_{DD} =10.1V, float DET pin, not in Mark event, measure I_{SUPPLY}			12	μA
Detection Current	I_{DET}	V_{DD}=1.4V, measure I_{SUPPLY}	53.8	55.6	58.3	μA
		V_{DD}=10.1V, measure I_{SUPPLY}	395	410	425	μA
Classification						
V_{CLASS} Output Voltage	V_{CLASS}	13V<VDD<21V, 1mA<I_{CLASS}<42mA	2.37	2.5	2.63	V
Classification Current	I_{CLASS}	13V ≤ V_{DD}≤ 21V, Not tested in production, guaranteed by V_{CLASS}				
		R_{CLASS} = 1270Ω, 13V ≤ V_{DD}≤ 21V	1.8	2	2.4	mA
		R_{CLASS} = 243Ω, 13V ≤ V_{DD}≤ 21V	9.9	10.55	11.3	mA
		R_{CLASS} = 137Ω, 13V ≤ V_{DD}≤ 21V	17.7	18.7	19.8	mA
		R_{CLASS} = 90.9Ω, 13V ≤ V_{DD}≤ 21V	26.6	28.15	29.7	mA
		R_{CLASS} =63.4Ω, 13V ≤ V_{DD}≤ 21V	38.2	40.4	42.6	mA
Classification Lower Threshold	V_{CL_ON}	V_{DD} rising, Class regulator turns on	11	12	13	V
Classification upper Threshold	V_{CL_OFF}	V_{DD} rising, Class regulator turns off	21	22	23	V
Classification Hysteresis	V_{CL_H}	Low side hysteresis		0.94		V
		High side hysteresis		0.5		V
Mark Event Reset Threshold	V_{MARK_L}		4	5	6	V
Max Mark Event Voltage	V_{MARK_H}		10.2	11	11.8	V
Mark Event Resistance	R_{MARK}	2-point measure at 7V and 10V			12	kΩ
IC Supply Current during Classification	I_{IN_CLASS}	V_{DD}=17.5V, CLASS floating		200	270	μA
Class Leakage Current	I_{LK}	V_{DD}=57V, V_{CLASS}=0V			1	μA
PD UVLO						
VDD Turn on Threshold	V_{DD_R}	VDD rising	33	35	37	V
VDD Turn off Threshold	V_{DD_F}	VDD falling	29	31	33	V
VDD UVLO Hysteresis	V_{DD_HYS}			4		V
IC Supply Current during Operation	I_{IN}		280	380	480	μA
PASS Device and Current Limit						
ON Resistance	R_{DS_RTN}	I_{RTN}=100mA		0.45		Ω
Leakage Current	I_{RTN_LK}	V_{DD}=V_{RTN}=57V		1	15	μA
Current Limit	I_{LIMIT}	V_{RTN}=1V	500	570	650	mA
Inrush Current Limit	I_{INRUSH}	V_{RTN}=2V		95		mA
Inrush Current Termination		V_{RTN} falling		1.2		V
Inrush to Operation Mode Delay	T_{DELAY}		80	100	120	ms
Current Fold-back Threshold		V_{RTN} rising		10		V

Fold-back Deglitch Time		V_{RTN} rising to inrush current fold-back		1.1		ms
APD						
Adaptor Detection Threshold Voltage	$V_{APD\text{-}EN}$	Respect to VDD		-1.5		V
	$V_{APD\text{-}Hys}$	Respect to VDD		0.5		V
AMPS						
MAINTAIN POWER SIGNATURE DC Supply Current		Startup has completed, I_{RTN} = 0mA			0.8	mA
Auto Maintain Power Signature Pulsed Voltage		Startup has completed, I_{RTN}<15mA, $R_{MAINTAIN\ POWER\ SIGNATURE}$ ≥165Ω		2.5		V
Automatic Maintain Power Signature Falling Current Threshold		Startup has completed, I_{RTN} threshold to generate Maintain Power Signature pulses		29		mA
		Hysteresis on RTN current		7		mA
POE Maintain Power Signature Time High	T_{MPSH}		85	106	127	ms
POE Maintain Power Signature Time Low	T_{MPSL}		173	216	259	ms

Notes:
(4) Not tested in production. Guaranteed by over-temperature correlation.

Electrical Characteristics (Flyback Part)

All voltages are referred to GND. T_J=-40°C to +125°C [(4)], typical values are tested at T_J=25°C, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VCC Power Supply and UVLO						
VCC Turn on Threshold	V_{VCC_ON}	V_{VCC} rising	7.3	8	8.7	V
VCC Min Voltage	V_{VCC_MIN}	V_{VCC} falling	4.9	5.5	6.3	V
VCC Turn off Threshold	V_{VCC_OFF}	V_{VCC} falling	3.9	4.5	4.9	V
VCC OVP Threshold	V_{VCC_OVP}	V_{VCC} rising	18	22	22.5	V
Quiescent Current	I_Q		0.8	1.2	1.6	mA
HV Start-up Current	I_{VCC_Charge}	V_{VCC}=0V, V_{DRAIN}=18V		3		mA
Voltage Feedback						
FB Reference Voltage	V_{REF}	T_J= 25°C	1.188	1.2	1.212	V
FB OVP Threshold	V_{FB_OVP}		1.35	1.45	1.55	V
Primary Side Sample Blanking Time	$T_{Blanking}$	Internal V_{COMP}=0V		270		ns
		Internal V_{COMP}=3V		440		ns
PWM Switching						
Switching Frequency Limit	F_{SW_MAX}	MODE is shorted to GND	510	600	690	kHz
Minimum Fold-back Frequency in PFM Mode				4		kHz
Soft Start						
Default Maximum Internal Soft-start Time	T_{SS}	Not tested in production, guaranteed by design		22		ms
Peak Current Limit						
Maximum Peak Current Limit	I_{pk_Limit}		2	2.5	3	A
Low Threshold Current Limit	I_{pk_MIN}		0.7	0.8	0.9	A

SCP Limit	I_{pk_SCP}		2.4	3.1	4	A
Leading Edge Blanking Time, same as T_{ON_MIN}	T_{LEB} T_{ON_MIN}		100	150	250	ns
Max T_{ON}	T_{ON_MAX}		3.8	5.2	6.6	μs
Internal Power MOSFET						
Breakdown Voltage	V_{DS_MAX}	I_D=250μA, T_J=25℃	180			V
On Resistance	R_{DS_ON}	V_{VCC}=10V, I_D=0.1A, T_J=25℃		0.65	0.88	Ω
MODE Pin						
MODE Pin Detection Current	I_{MODE}		30	40	50	μA
MODE Pin Detection Period	T_{MODE}	Not tested in production, guaranteed by design		100		μs
Protection						
Over Load Protection Hiccup on Time		Not tested in production, guaranteed by design		8.6		ms
OVP/OLP/SCP Hiccup off Time		Not tested in production, guaranteed by design		68		ms
Thermal Shutdown Temperature	T_{SD}			155		℃
Thermal Shutdown Hysteresis	T_{HYS}			20		℃

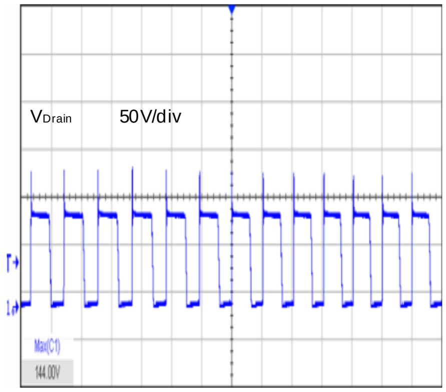
Notes:
(5) Refer to “work mode detection” for the function with different voltage level program options.

Typical Performance Characteristics

(Test condition: input voltage: 37~57Vdc before the bridge rectifiers; output spec: 12Vdc/1A; Ambient temperature: 25±5 ℃.)

Steady

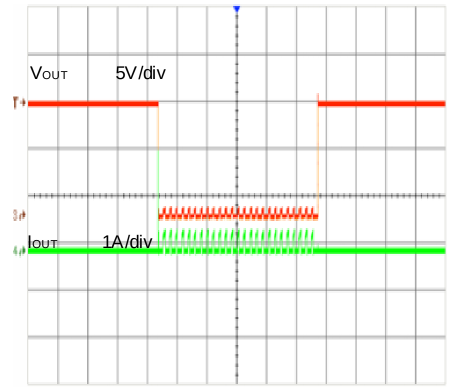
(V_{IN}=57V,I_O=1A, CH1-V_{Drain})



Time (100µs/div)

Output Short Protection

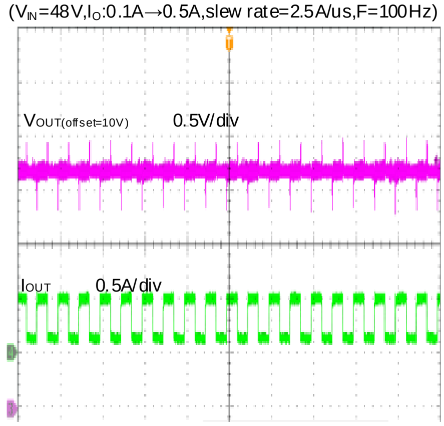
(V_{IN}=57V)



Time (500ms/div)

Load Transient

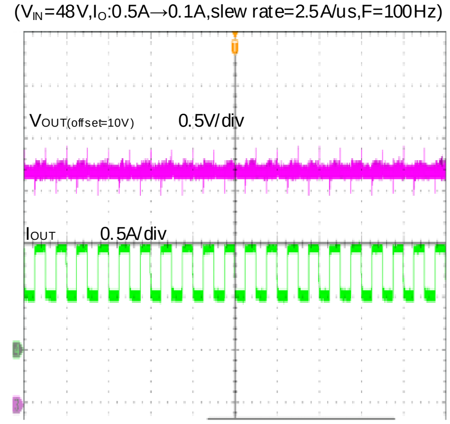
(V_{IN}=48V,I_O:0.1A→0.5A,slew rate=2.5A/us,F=100Hz)



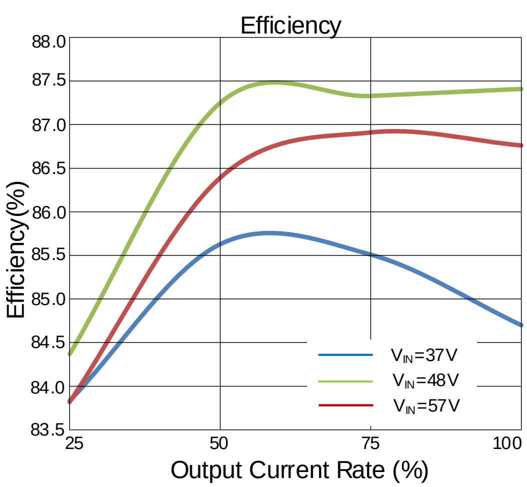
Time (20ms/div)

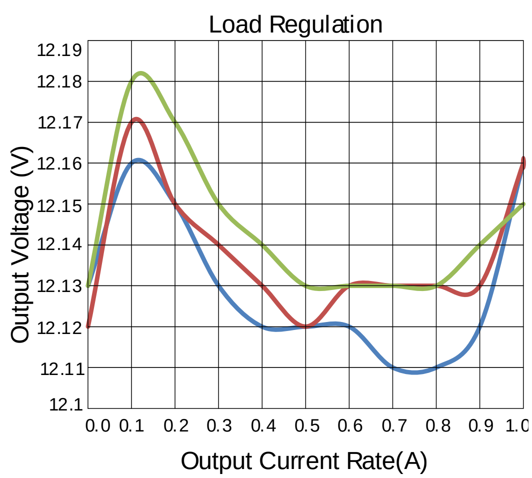
Load Transient

(V_{IN}=48V,I_O:0.5A→0.1A,slew rate=2.5A/us,F=100Hz)



Time (20ms/div)





Operation Principles

Protocol Section

PoE Start-up Sequence

IEEE 802.3at requires two detection levels, two classes and mark cycles, and start-up from the second mark event. The voltage between RTN and VSS will fall when the SY23212A charges C_{IN} following application of full voltage. Subsequently, the converter will start up and will decrease the current draw.

Detection

In order to identify a device as a valid PD, the Power Sourcing Equipment (PSE) senses the Ethernet connection by applying two voltages in a range of 2.8V to 10V on the Ethernet cable and measuring the corresponding currents. An equivalent resistance is calculated using the $\Delta V/\Delta I$. During this phase, the PD must present a resistance between 23.75kΩ and 26.25kΩ. The value of the detection resistance has to be selected in consideration of the typical drop in voltage of the diode bridges. The typical value of the resistance that can be used in most applications is 24.9 kΩ.

Classification

In the classification mode, the PSE classifies the PD for one of five power levels or classes, which allows the PSE to efficiently manage the power distribution. The five different classes are shown in Table 1, which determine the class the PD must declare. An external resistor (R_{CLS}) connected between CLS and VSS sets the classification current. The PSE may disconnect a PD if it draws more than its stated class power. During hardware classification, the PSE presents a fixed voltage between 15.5V and 20.5V to the PD, which draws in turn a fixed current set by R_{CLS}. PD current is measured by the PSE to choose one of the five available classes (see Table 1). The SY23212A disables the classification while the adaptor input is used for avoiding excessive power dissipation. If the PD thermal limit is triggered or the DEN is active, the CLS reference voltage will be turned off.

Table 1. Class Resistor Selection

Class	Power at PD(W)	Class current (mA)	Resistor(Ω)
0	0.44~12.95	0~4	1270
1	0.44~3.84	9~12	243
2	3.84~6.49	17~20	137
3	6.49~12.95	26~30	90.9
4	-	36~44	63.4

Inrush and Operational Current Limit

Once the classification is successfully completed, the PSE will rise its voltage. When the input voltage is above the UVLO turn on threshold, the hot-swap switch will be turned on, and the input capacitor of downstream DC/DC converter will be charged with a low current (inrush current) limit. The inrush phase will be end, current limit will be changed to its operating limit and VCC of DC/DC converter will be charged only when both of the following conditions are met.

1) RTN drops below 1.2V.

2) From VDD>UVLO begins, a 100ms timing named inrush delay is satisfied.

As shown in below figure, there are two sections for the inrush current during inrush interval after VDD>UVLO. When RTN is higher than 20V, the inrush current will be kept around 60mA. As the RTN voltage decreases below 20V, the inrush current will rise to around 100mA until RTN voltage falls below 1.2V and inrush delay is finished.

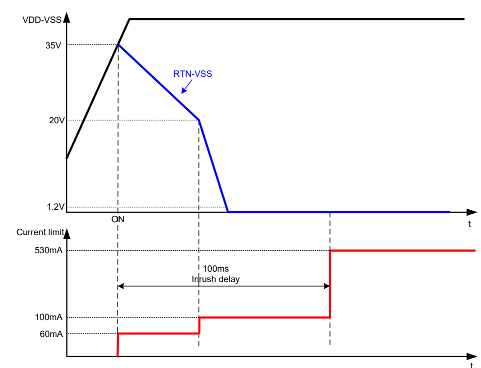


Fig. 2 Inrush Current and Inrush Delay

T2P Indicator

The T2P pin is an open-drain output. It is pulled low to RTN to indicate the presence of a type 2 PSE or a wall adapter input. The T2P is intended to drive the diode side of an optocoupler. It should be left open or tied to RTN if not used.

Auto-Maintain Power Signature

The maintain power signature is an electrical signature presented by the PD to make the PSE think that it still presents after operating voltage is applied. For a Type 1 or Type 2 PD, a valid MAINTAIN POWER SIGNATURE consists of a minimum dc current of 10mA, or a 10mA pulsed current for at least 75ms every 325ms.

If the current through the RTN-to-VSS path is below 29mA, the SY23212A will automatically generate the 2.5V maintain power signature pulsed voltage to the

AMPS pin, the current amplitude can be adjusted through an external resistor. When the current through the RTN-to-VSS path is beyond 36mA, the SY23212A will exit maintain power signature mode and clear maintain power signature flag immediately. Note that the maintain power signature function be enabled only after the PoE input has been detected.

Adapter Power Input

In some applications, it is desirable to power the PD from an auxiliary power source such as a wall adapter.

The adaptor detection can be enabled as long as the VDD-RTN voltage exceeds 9V. The voltage divider for adaptor detection is connected as shown in below figure. There is a -1.5V reference referring to VDD. When a wall adapter is detected, the internal hot-swap MOSFET between RTN and VSS will be turned off, classification current will be disabled and the T2P will become active low. The maintain power signature pulsed mode is enabled.

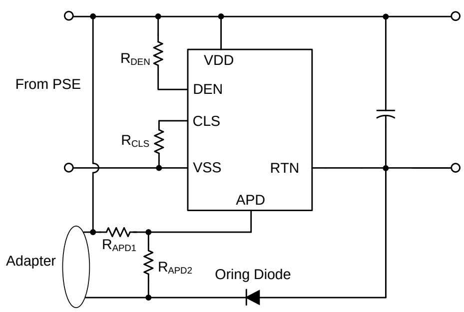


Fig. 3 Connection of Adaptor Detection

Current Fold-back of RTN MOS

In order to protect the hot-swap MOSFET from damage when OLP/SCP/hot plug/Surge happens, if VRTN rises above 10V for longer than 1.1ms during normal operation, the current limit of hot-swap MOS will revert to the inrush value. When the RTN falls below 1.2V again, the current limit can recover to the operating value.

DC/DC Converter Operation

Start-up Operation

After 100ms inrush delay, the RTN voltage will be almost as low as VSS, the capacitor across VCC and GND pins, C_{VCC}, will be charged up by the DRAIN voltage through internal start-up circuit. Once the VCC voltage reaches V_{VCC_ON}, the start-up circuit will be disabled and the DC/DC converter will start to work if no faults are present and MODE pin detection finished. The start-up circuit will turn ON again once VCC reaches V_{VCC_MIN} (5.5V) due to power consumption. After soft-start ends, the V_{VCC_MIN} will change to 7V to provide relatively stable VCC power supply until the auxiliary winding of Flyback transformer can supply sufficient energy to maintain V_{VCC} above V_{VCC_OFF}.

If faults happen, the PWM switching will stop, the V_{VCC_MIN} will change from 7V back to 5.5 V, the hiccup off timer (64ms) will start, the start-up circuit will turn on to maintain the VVCC between 8V and 5.5V. If the timing is over, the start-up circuit will be disabled, the converter will enter re-start mode, the VCC voltage will be allowed to decrease to 4.5 V. Once the 4.5 V threshold is reached, the internal circuit will be reset and the start-up circuit will charge the VCC capacitor again. The VCC control logic is shown as below figure.

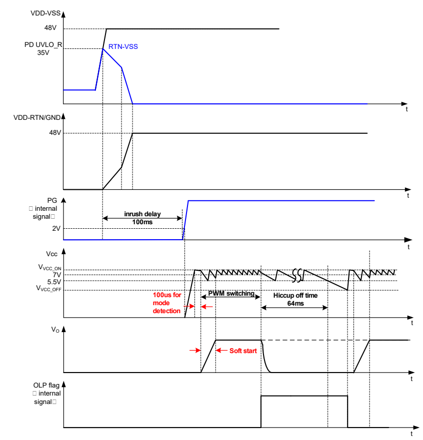


Fig. 4 Waveform of VCC Logic

Work Mode Detection

After enabled, the SY23212A will output 40µA current to MODE pin to detect the resistor setting. There are three levels of frequency limit which can be selected by setting the resistance value that connected between MODE pin and GND. Refer to the below table for details.

Table 2. MODE Pin Program Options

MODE to RTN Resistance	QR Frequency
0	600kHz limit
12.1kΩ (±1% precision)	500kHz limit
float	400kHz limit

Quasi-Resonant Operation

QR mode operation provides low turn-on switching losses for Flyback converter.

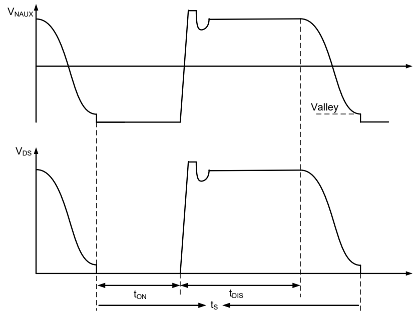


Fig.5 QR Mode Operation

The voltage across drains and source of the primary MOSFET is reflected by the auxiliary winding of the Flyback transformer. FB pin detects the voltage across the auxiliary winding by a resistor divider. When the voltage across drains and source of the primary MOSFET is at voltage valley, the MOSFET will be turned on.

Output Voltage Control

In order to achieve primary side constant voltage control, the output voltage is detected by the auxiliary winding voltage.

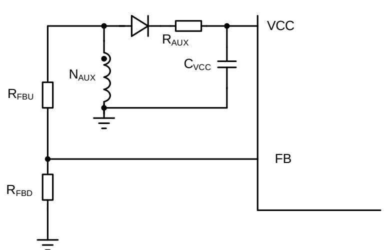


Fig.6 FB Sample Connection

As shown in Fig.7, during OFF time, the voltage across the auxiliary winding is

$$V_{AUX} = (V_{OUT} + V_{D\_F}) \times \frac{N_{AUX}}{N_S} \quad (1)$$

N_{AUX} is the turns of auxiliary winding; N_S is the turns of secondary winding; V_{D_F} is the forward voltage of the power diode.

At the current zero-crossing point, V_{D_F} is nearly zero, so V_{OUT} is proportional with V_{AUX} exactly. The voltage of this point is sampled by the IC as the feedback of output voltage. The resistor divider is designed by

$$\frac{V_{FB\_REF}}{V_{OUT}} = \frac{R_{FBD}}{R_{FBU} + R_{FBD}} \times \frac{N_{AUX}}{N_S} \quad (2)$$

Where V_{FB_REF} is the internal voltage reference.

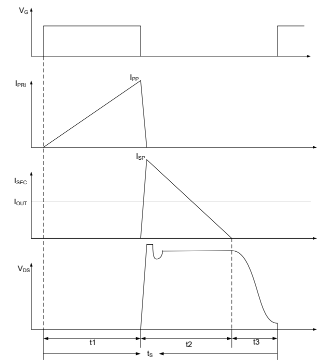


Fig.7 Auxiliary Winding Voltage Waveforms

The SY23212A regulates primary side MOSFET switching to make peak current always ≥800mA, and will start sampling the auxiliary-winding voltage after the power MOSFET is turned off. A blanking time is added to avoid the spike ringing affection due to leakage inductance. To guarantee long enough FB sample period, the output diode current conduct time T_{DIS} in light load (before diode current drops to 0A in each cycle) should be longer than 400ns.

Normally, design the transformer and insure the T_{DIS} higher than 400ns in light load or no load.

Fault Protection Modes

Over Load Protection

The DC/DC converter sets the over load detection by continue monitoring the V_{COMP} (the output of internal EA). Once the soft-start finishes, the OLP protection will be enabled. If the load continues increasing after I_{PK} reaching its maximum value, the output voltage will decrease and the V_{COMP} will rise to abnormal high level. When V_{COMP} exceeds OLP threshold and lasts for 8ms, OLP protection will be triggered, the IC will immediately terminate PWM switching. VCC will be maintained between 8V and 5.5V for 64ms hiccup off time. After 64ms hiccup off timer ending, VCC will be allowed to decrease to turn off threshold then try to restart.

Short Circuit Protection (SCP)

If the peak current cannot be limited by V_{COMP} in every cycle due to minimum gate on time in some abnormal cases, the current may run out of control and transformer may be confronted saturation. If the peak current reaches 3.1A once, the off time will be forced to max toff, then if the peak current reaches 3.1A three times in succession, the SY23212A will register it as SCP, it will immediately terminate PWM switching and run into hiccup mode with 64ms hiccup off time.

Output Over Voltage Protection

If the sample voltage at FB pin exceeds 120% of V_{FB_REF} in 4 consecutive cycles, which means OVP condition has been occurred, the SY23212A will shut off the power MOSFET and enter hiccup mode immediately. After 64ms hiccup off time ends, the SY23212A will try to re-start. In case the OVP is removed, the output voltage will recover.

VCC Over Voltage Protection

When the VCC voltage exceeds V_{VCC_OVP} threshold, the SY23212A will stop switching and discharge the VCC voltage. Once V_{VCC} is below V_{VCC_OFF}, the SY23212A will shut down and the VCC will be charged again by DRAIN.

Power Device Design

MOSFET and DIODE

When the operation condition is with maximum input voltage and full load, the voltage stress of MOSFET and secondary power diode will be maximized;

$$V_{MOS\_DS\_MAX} = V_{DC\_MAX} + N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S \quad (3)$$

$$V_{D\_R\_MAX} = \frac{V_{DC\_MAX}}{N_{PS}} + V_{OUT} \quad (4)$$

Where V_{DC_MAX} is maximum input DC voltage; N_{PS} is the turn's ratio of the Flyback transformer; V_{OUT} is the rated output voltage; V_{D_F} is the forward voltage of secondary power diode; ΔV_S is the overshoot voltage clamped by RCD snubber during OFF time.

When the operation condition is with minimum input voltage and full load, the current stress of MOSFET and power diode will be maximized.

$$I_{MOS\_PK\_MAX} = I_{P\_PK\_MAX} \quad (5)$$

$$I_{MOS\_RMS\_MAX} = I_{P\_RMS\_MAX} \quad (6)$$

$$I_{D\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} \quad (7)$$

$$I_{D\_AVG} = I_{OUT} \quad (8)$$

Where $I_{P\_PK\_MAX}$ and $I_{P\_RMS\_MAX}$ are maximum primary peak current and RMS current, which will be introduced later.

Transformer (N_{PS} and L_M)

N_{PS} is limited by the electrical stress of the power MOSFET:

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - V_{DC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \quad (9)$$

Where $V_{MOS\_(BR)DS}$ is the breakdown voltage of the power MOSFET.

In Quasi-resonant mode, each switching period cycle t_S consists of three parts: current rising time t_1, current falling time t_2 and quasi-resonant time t_3 shown in Fig.8.

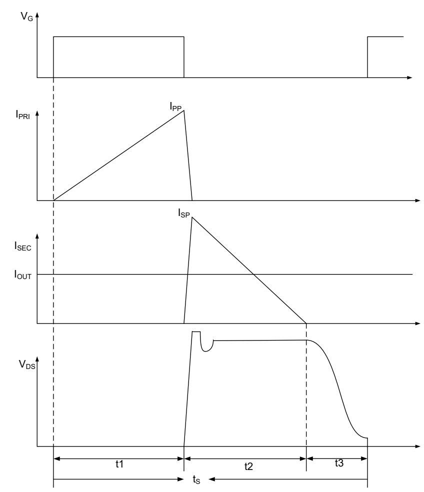


Fig.8 switching waveforms

When the operation condition is with minimum input DC RMS voltage and full load, the switching frequency will be minimum frequency, the maximum peak current through MOSFET and the transformer will happen.

Once the minimum frequency f_{S_MIN} is set, the inductance of the transformer could be induced. The design flow is shown as below:

(a) Select N_{PS}

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - V_{DC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \quad (10)$$

(b) Preset minimum frequency f_{S_MIN}

(c) Compute inductor L_M and maximum primary peak current $I_{P\_PK\_MAX}$

$$I_{P\_PK\_MAX} = \frac{2P_{OUT}}{\eta \times V_{DC\_MIN}} + \frac{2P_{OUT}}{\eta \times N_{PS} \times (V_{OUT} + V_{D\_F})} + \pi \sqrt{\frac{2P_{OUT}}{\eta} \times C_{Drain} \times f_{S\_MIN}} \quad (11)$$

$$L_M = \frac{2P_{OUT}}{\eta \times I^2_{P\_PK\_MAX} \times f_{S\_MIN}} \quad (12)$$

Where C_{Drain} is the parasitic capacitance at drain of MOSFET; η is the efficiency; P_{OUT} is rated full load power.

(d) Compute current rising time t_1 and current falling time t_2

$$t_1 = \frac{L_M \times I_{P\_PK\_MAX}}{V_{BUS}} \quad (13)$$

$$t_2 = \frac{L_M \times I_{P\_PK\_MAX}}{N_{PS} \times (V_{OUT} + V_{D\_F})} \quad (14)$$

$$t_S = \frac{1}{f_{S\_MIN}} \quad (15)$$

(e) Compute primary maximum RMS current $I_{P\_RMS\_MAX}$ for the transformer fabrication.

$$I_{P\_RMS\_MAX} = \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \times \sqrt{\frac{t_1}{t_S}} \quad (16)$$

(f) Compute secondary maximum peak current $I_{S\_PK\_MAX}$ and RMS current $I_{S\_RMS\_MAX}$ for the transformer fabrication.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} \quad (17)$$

$$I_{S\_RMS\_MAX} = \frac{\sqrt{3}}{3} N_{PS} \cdot I_{P\_PK\_MAX} \cdot \sqrt{\frac{t_2}{t_S}} \quad (18)$$

Transformer Design (N_P, N_S, N_{AUX})

The design of the transformer is similar with ordinary Flyback transformer. The parameters below are necessary:

Necessary parameters	
Turns ratio	N_{PS}
Inductance	L_M
Primary maximum current	$I_{P\_PK\_MAX}$
Primary maximum RMS current	$I_{P\_RMS\_MAX}$
Secondary maximum RMS current	$I_{S\_RMS\_MAX}$

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area A_e.

(b) Preset the maximum magnetic flux ΔB

ΔB=0.22~0.26T

(c) Compute primary turn N_P

$$N_P = \frac{L_M \times I_{P\_PK\_MAX}}{\Delta B \times A_e} \quad (19)$$

(d) Compute secondary turn N_S

$$N_S = \frac{N_P}{N_{PS}} \quad (20)$$

(e) Compute auxiliary turn N_{AUX}

$$N_{AUX} = N_S \times \frac{V_{VCC}}{V_{OUT}} \quad (21)$$

Where V_{VCC} is the working voltage of VCC pin (10V~15V is recommended).

(f) Select an appropriate wire diameter

With $I_{P\_RMS\_MAX}$ and $I_{S\_RMS\_MAX}$, select appropriate wire to make sure the current density ranges from 4A/mm^2 to 10A/mm^2.

(g) If the winding area of the core and bobbin is not enough, reselect the core style, back to **(a)** and redesign the transformer until the ideal transformer is achieved.

RCD Snubber for MOSFET

The power loss of the snubber P_{RCD} is evaluated first

$$P_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{\Delta V_S} \times \frac{L_K}{L_M} \times P_{OUT} \quad (22)$$

Where N_{PS} is the turns ratio of the flyback transformer; V_{OUT} is the output voltage; V_{D_F} is the forward voltage of the power diode; ΔV_S is the overshoot voltage clamped by RCD snubber; L_K is the leakage inductor; L_M is the inductance of the Flyback transformer; P_{OUT} is the output power.

The R_{RCD} is related with the power loss,

$$R_{RCD} = \frac{(N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S)^2}{P_{RCD}} \quad (23)$$

The C_{RCD} is related with the voltage ripple of the snubber ΔV_{C_RCD}:

$$C_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{R_{RCD} \times f_S \times \Delta V_{C\_RCD}} \quad (24)$$

CLS Resistor Selection

A resistor from CLS to V_{SS} programs the classification current per the IEEE standard. The PD power ranges and corresponding resistor values are listed in following table. The power assigned should correspond to the maximum average power drawn by the PD during operation. The SY56805A supports class 0-3 power levels.

Table2. Class Resistor Selection

Class	Power at PD		Resistor (Ω)
	Minimum (W)	Maximum (W)	
0	0.44	12.95	1270
1	0.44	3.84	243
2	3.84	6.49	137
3	6.49	12.95	90.9

APD Resistor Selection

APD forces power to come from an external adapter connected from VDD to RTN by opening the hot-swap switch. Select the APD divider resistors per Equation (25) where V_{APDTR_ON} is the desired adapter voltage that enables the APD function as adapter voltage rises.

$$R_{APD1} / R_{APD2} = V_{APDEN} / (V_{APDTR\_ON} - V_{APDEN}) \quad (25)$$

DEN Resistor Selection

The standard specifies a detection signature resistance, R_{DEN} between 23.7kΩ and 26.3kΩ. Connect a 24.9kΩ resistor from DEN to VDD to provide the PoE detection signature.

VDD to VSS ESD Protection

Voltage transients caused by surge or other special applications may occur, a TVS (D1, see in Fig.9) must limit this voltage to be within the absolute maximum ratings. The TVS such as SMBJ58A can be used. A TVS with negative resistance characteristic is not recommended.

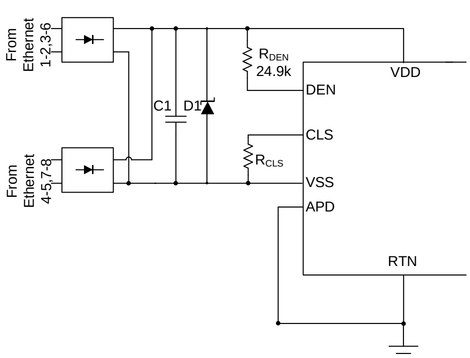


Fig.9 VDD to VSS ESD Protection

Input Bypass Capacitor Selection

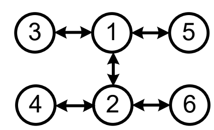
The standard specifies an input bypass capacitor of 0.05μF to 0.12μF. Typically a 0.1μF, 100V ceramic capacitor between VDD and VSS (C1 on the Fig.9) is used.

Layout

(a) To achieve better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to the BUS line capacitor first, then to the switching circuit.

(b) The circuit loop of all switching circuit should be kept small: primary power loop, secondary loop and auxiliary power loop.

(c) The connection of primary ground is recommended as:



Ground ①: ground of BUS capacitor.

Ground ②: ground of bias supply capacitor.

Ground ③: ground node of auxiliary winding.

Ground ④: ground node of divider resistor.

Ground ⑤: primary ground node of Y capacitor.

Ground ⑥: ground of IC GND.

(d) Bias supply trace should be connected to the bias supply capacitor first instead of GND pin. The bias supply capacitor should be put beside the IC.

(e) The resistor divider connected to FB pin is recommended to be put beside the IC.

(f) The trace spacing between AMPS (low voltage pin) and adjacent pins (high voltage pin) shouldn't be less than the pitch. It is the same case with CLS pin.

Design Notice

1. At no load secondary side diode freewheeling time should be more than 1.5*T_{OFF_MIN} for sufficient sampling time.
2. VCC voltage prefer to larger than 9V for all conditions.
3. At heavy load, the peak-to-peak voltage at the FB pin should be less than approximately 50mV after T_{OFF_MIN} time. This can be guaranteed by decreasing the leakage inductance and using proper RCD snubber.
4. R_{FBU} is the upper resistor of the divider. Normally, its value is recommended between 18kΩ~51kΩ.

Design Example

A design example of typical application is shown below step by step.

#1. Identify design specification

Design Specification			
V_{DC}	37V~57V	V_{OUT}	12V
I_{OUT}	1A	η	85%

#2. Transformer design (N_{PS}, L_M)

Refer to Power Device Design

Conditions			
V_{DC_MIN}	37V	V_{DC_MAX}	57V
ΔV_S	50V	$V_{MOS\text{-}(BR)DS}$	180V
P_{OUT}(max)	12W	V_{D_F}	1V
C_{Drain}	72pF	f_{S_MIN}	340kHz

(a) Compute turns ratio N_{PS} first

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\%\text{-}V_{DC\_MAX}\text{-}\Delta V_S}{V_{OUT}+V_{D,F}}$$
$$=\frac{180V \times 0.9\text{-}57V\text{-}50V}{12V+1V}$$
$$=4.23$$

N_{PS} is set to

N_{PS}=3

(b)$f_{S,MIN}$ is preset

F_{S_MIN}=500kHz

(c) Compute inductor L_M and maximum primary peak current $I_{P,PK,MAX}$

$$I_{P\_PK\_MAX} = \frac{2P_{OUT}}{\eta \times V_{DC\_MIN}} + \frac{2P_{OUT}}{\eta \times N_{PS} \times (V_{OUT}+V_{D\_F})} + \pi\sqrt{\frac{2P_{OUT}}{\eta} \times C_{Drain} \times f_{S\_MIN}}$$
$$= \frac{2\times 12W}{0.85\times 37V} + \frac{2\times 12W}{0.85\times 3\times(12V+1V)} + \pi\sqrt{\frac{2\times 12W}{0.85}\times 72pF \times 340k}$$
$$=1.57A$$

$$L_M = \frac{2P_{OUT}}{\eta \times I_{P\_PK\_MAX}^2 \times f_{S\_MIN}} = \frac{2\times 12W}{0.85\times(1.57A)^2\times 340kHz} = 33.69\mu H$$

Set: L_M=34μH

(d) Compute current rising time t_1 and current falling time t_2

$$t_1 = \frac{L_M \times I_{P\_PK\_MAX}}{V_{DC\_MIN}} = \frac{34\mu H\times 1.57A}{37V} = 1.443\mu s$$

$$t_2 = \frac{L_M \times I_{P\_PK\_MAX}}{N_{PS}\times(V_{OUT}+V_{D\_F})} = \frac{34\mu H\times 1.57A}{3\times(12V+1V)} = 1.369\mu s$$

$$t_3 = \pi\times\sqrt{L_M\times C_{Drain}} = \pi\times\sqrt{34\mu H\times 72pF} = 0.155\mu s$$

$$t_S = t_1 + t_2 + t_3 = 1.443\mu s + 1.369\mu s + 0.155\mu s = 2.957\mu s$$

(e) Compute primary maximum RMS current $I_{P\text{-}RMS\text{-}MAX}$ for the transformer fabrication.

$$I_{P\_RMS\_MAX} = \frac{\sqrt{3}}{3} I_{P\_PK\_MAX}\times\sqrt{\frac{t_1}{t_S}} = \frac{\sqrt{3}}{3}\times 1.57A\times\sqrt{\frac{1.443\mu s}{2.957\mu s}} = 0.633A$$

(f) Compute secondary maximum peak current $I_{S\text{-}PK\text{-}MAX}$ and RMS current $I_{S\text{-}RMS\text{-}MAX}$ for the transformer fabrication.

$$I_{S\_PK\_MAX} = N_{PS}\times I_{P\_PK\_MAX} = 3\times 1.57A = 4.71A$$

$$I_{S\_RMS\_MAX} = N_{PS}\times\frac{\sqrt{3}}{3} I_{P\_PK\_MAX}\times\sqrt{\frac{t_2}{t_S}} = 3\times\frac{\sqrt{3}}{3}\times 1.57A\times\sqrt{\frac{1.369\mu s}{2.957\mu s}} = 1.85A$$

#3. Select secondary power diode

Refer to Power Device Design

Known conditions at this step			
V_{DC_MAX}	57V	N_{PS}	3
V_{OUT}	12V	V_{D_F}	1V

Compute the voltage and the current stress of secondary power diode

$$V_{D\_R\_MAX} = \frac{V_{DC\_MAX}}{N_{PS}} + V_{OUT} = \frac{57V}{3} + 12V = 31V$$

$$I_{D\_PK\_MAX} = N_{PS}\times I_{P\_PK\_MAX} = 3\times 1.57A = 4.71A$$

#4. Set FB pin

Refer to V_{OUT}

First identify R_{FBU} need for line regulation.

Parameters Designed			
R_{FBU}	20kΩ		

Then compute R_{FBD}

Conditions			
V_{OUT}	12V	V_{FB_REF}	1.2V
R_{FBU}	20kΩ	N_S	9
N_{AUX}	7		

$$R_{FBD}=\frac{R_{FBU}}{\dfrac{V_{OUT}\times N_{AUX}}{V_{FB\_REF}\times N_S}-1}=\frac{20K}{(\dfrac{12V\times 7}{1.2V\times 9}-1)}=2.95K$$

Set R_{FBD}

R_{FBD}=3kΩ

#5. Set DEN pin
Connect a 24.9kΩ resistor from DEN to VDD

#6. Set CLS pin
Connect a 1.27kΩ resistor from CLS to VSS

#7. Set APD pin
Generally there is no need of adapter power supply in this application, so the APD is pulled up to the VDD through a resistor.
If you need adaptor ORing function, refer to the 'Adaptor power input' part.

Set R_{APD1}=0Ω

#8. Set MODE pin

Connect a 0Ω resistor between MODE and GND to set a 600 kHz frequency limit.

#9. Final result

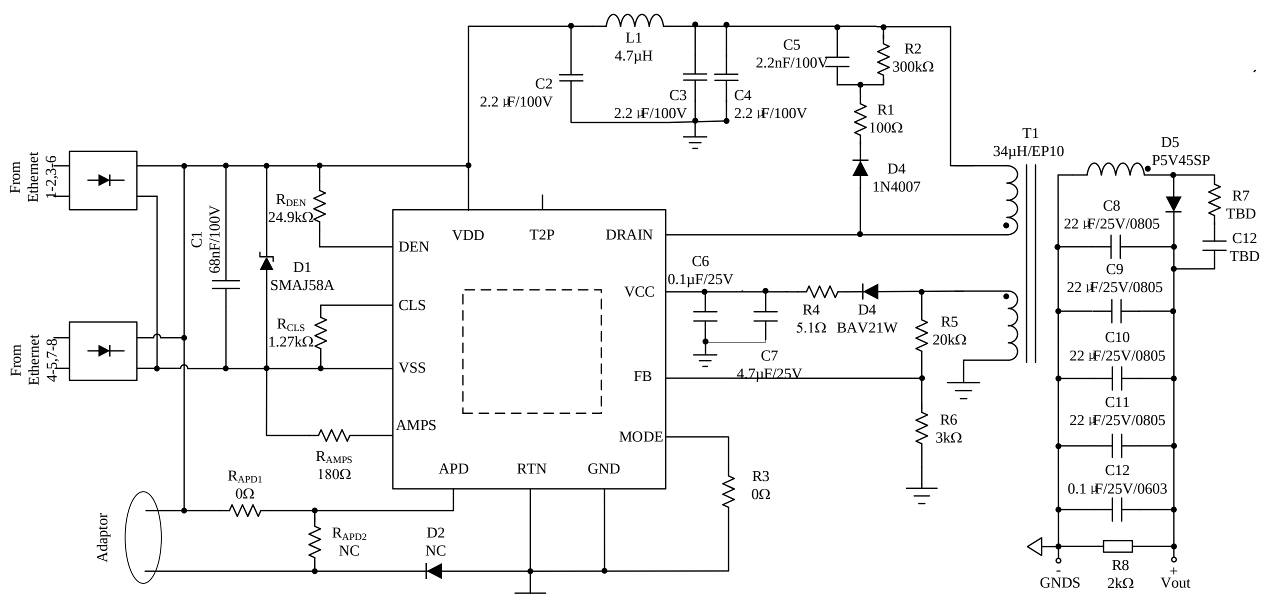
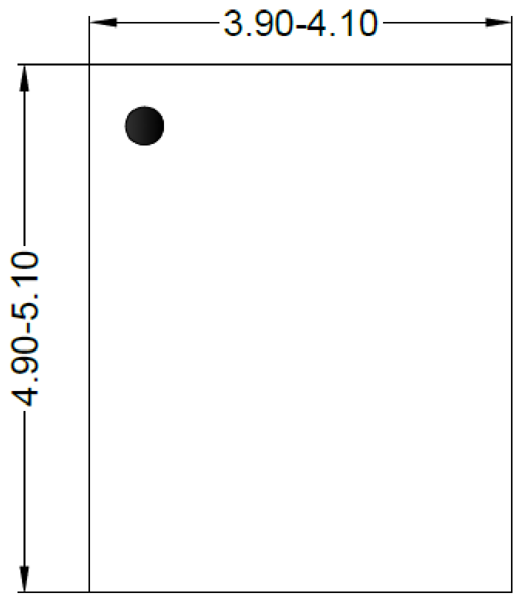
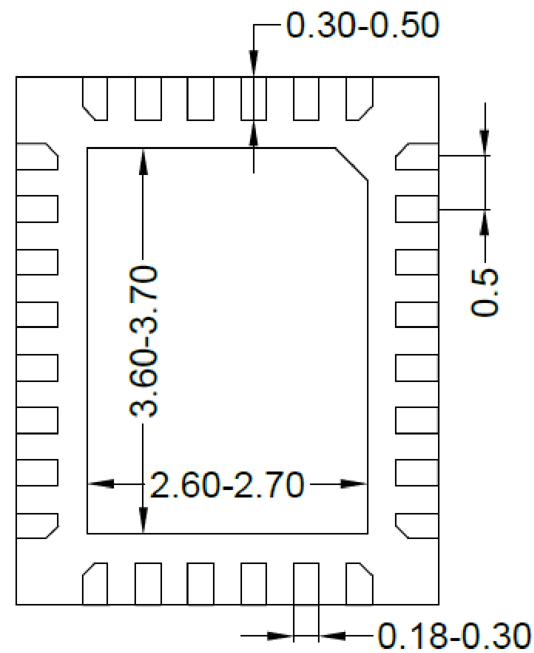


Fig.10 Design example VIN=37V-57V， PoE application, Vout=12V@1A

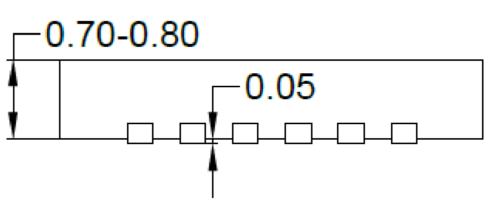
QFN4X5-28 Package Outline Drawing



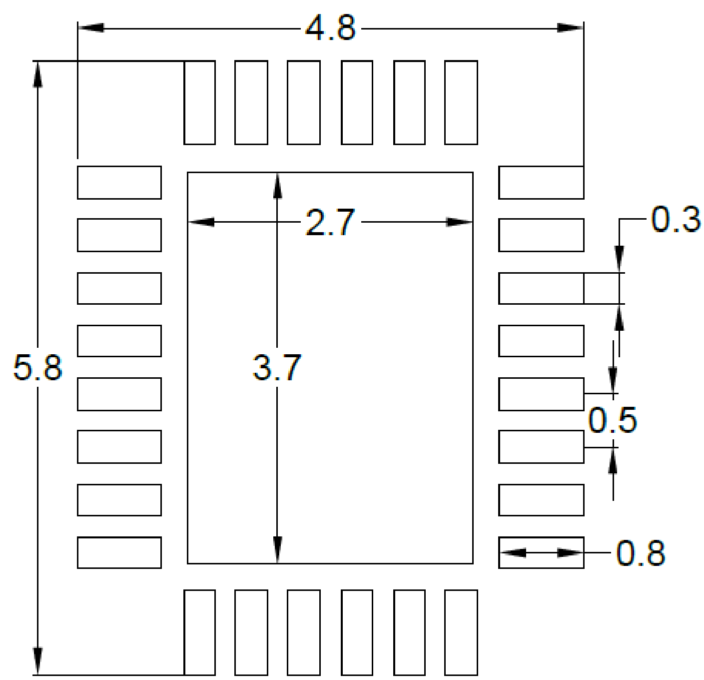
Top view



bottom view



Front view

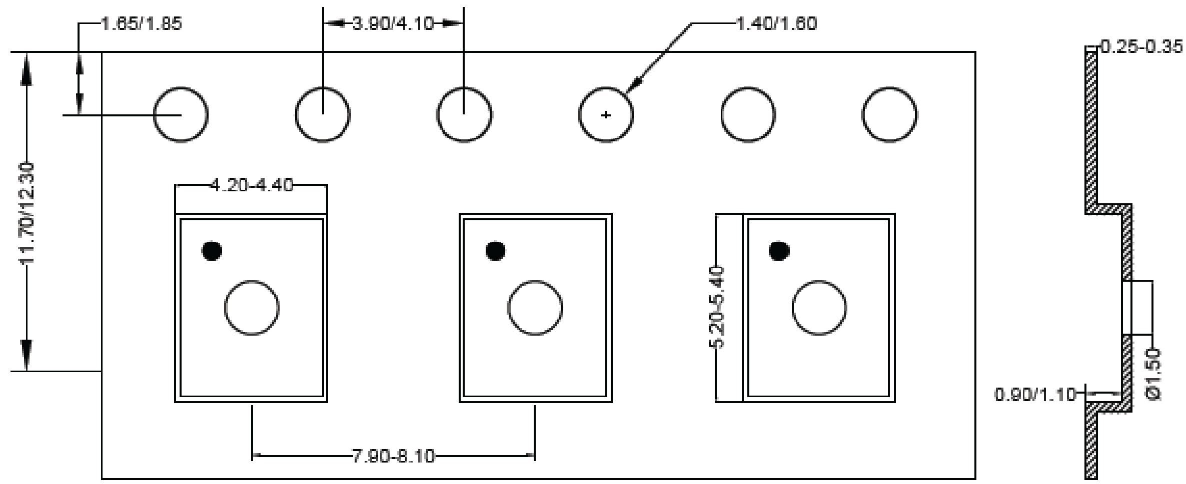


Recommended PCB layout
(Reference only)

Notes: 1, All dimension in millimeter and exclude mold flash & metal burr;

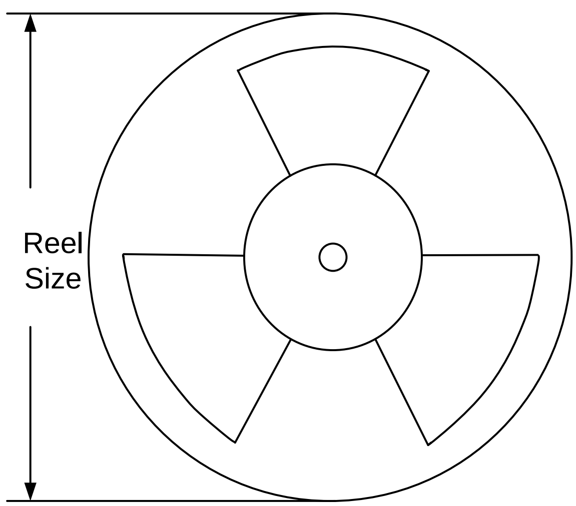
Taping & Reel Specification

1. QFN4×5 taping orientation



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
QFN4×5	12	12	13"	400	400	5000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	**Revision**	**Change**
August 18, 2023	Revision 0.9	Initial Release

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