SY23434

ZVS Flyback SR Controller

General Description

The SY23434 is a Flyback SR controller compatible with QR mode converter to achieve ZVS operation. The primary side PWM converter must work in the quasi-resonant mode. The SY23434 adopts proprietary operation mode to achieve Flyback ZVS turn-on, which can greatly improve Flyback efficiency and power density. The SY23434 also adopts the adaptive gate voltage control for safe operation.

The SY23434 adopts DSEN voltage falling slope rate detecting technology to avoid SR MOSFET false turn-on by parasitic ring in DCM or QR mode.

The SY23434 is available in a CPC8 package.

Features

- Proprietary Operation Mode for Flyback ZVS
- Adaptive Gate Voltage Control
- DSEN Falling Slope Rate Detecting to Prevent SR False Trigger
- 130V DSEN Pin to Directly Sense DRAIN Voltage of SR MOS
- Power Saving Mode to Improve Light Load Efficiency
- Dual Power Supply Channel for 3.3V to 21V Output Systems
- Compact Package: CPC8

Applications

- USB PD, Fast Charger
- AC/DC Adaptor

Typical Applications

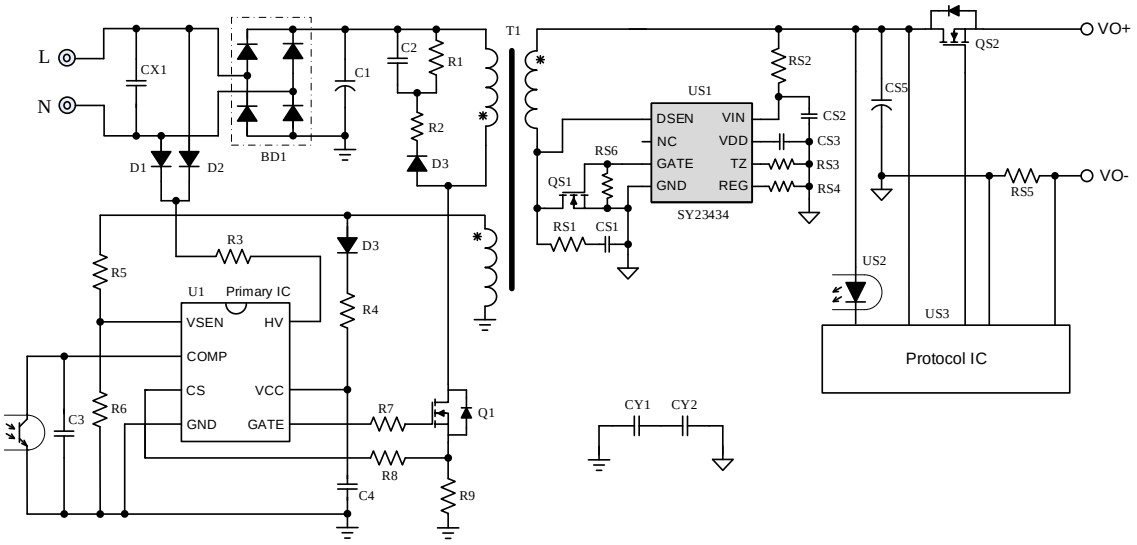


Fig. 1 Typical Application Circuit (SR MOSFET Location: Low Side)

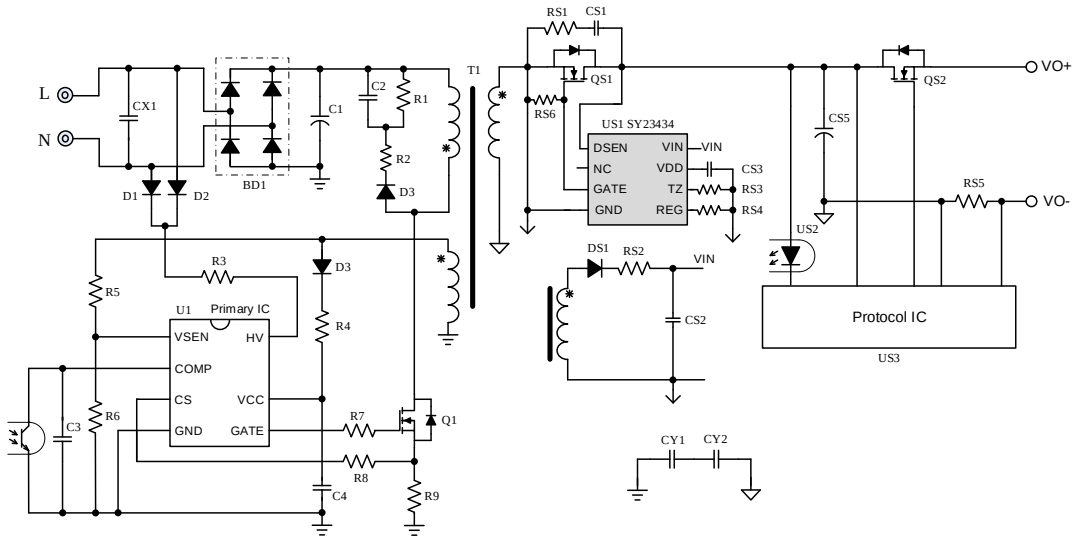


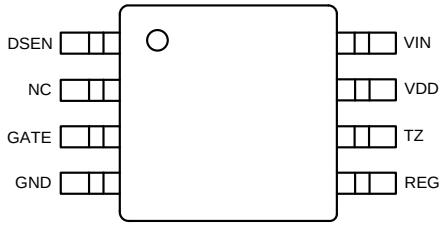
Fig. 2 Typical Application Circuit (SR MOSFET location: High Side)

Ordering Information

SY23434□(□□□)

Package Code

Optional Spec Code



(CPC8**)**

Pinout (top view)

Ordering Number	Package	Top Mark
SY23434FPP	CPC8	GMLxyz

x=year code, y=week code, z= lot number code

Pinout (top view)

Pin number	Pin Name	Pin Description
1	DSEN	Drain sense input, and used as a self-supply channel.
2	NC	Not connected.
3	GATE	Gate drive pin.
4	GND	Ground pin.
5	REG	Connect a resistor between this pin and GND to set the falling slope ref time threshold.
6	TZ	Connect a resistor to program ZVS coefficient.
7	VDD	Output of internal LDO, power supply for control unit and GATE drive circuit. Connect a 0.47μF or larger ceramic capacitor between VDD and GND pin.
8	VIN	Input of low voltage power supply.

Block Diagram

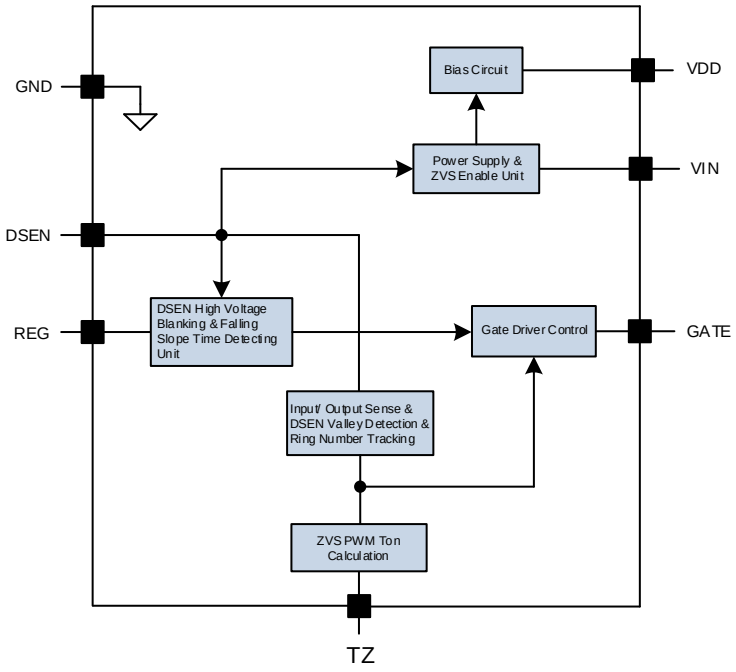


Fig.3 Block Diagram

Absolute Maximum Ratings (Note1)

DSEN ---------- -1V ~ 130V
VIN ---------- -0.3V ~ 30V
VDD ---------- -0.3V ~ 15V
GATE ---------- -0.3V ~ VDD+0.3V
TZ, REG ---------- -0.3V ~ 4V
Power Dissipation, @ T_A = 25°C CPC8 ---------- 0.9W
Package Thermal Resistance (Note 2)
CPC8, θ_{JA}---------- 145°C/W
CPC8, θ_{JC}---------- 47°C/W
Maximum Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Electrical Characteristics

(V_{VIN} = 12V, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Pin						
VDD ON Threshold	V_{VDD_ON}		3.1	3.35	3.6	V
UVLO Hysteresis	V_{VDD_HYS}		100	200	300	mV
VDD Regulation Voltage when VIN Pin is Active to Supply IC	$V_{VDD\_REG\_VIN}$		8.6	9.4	9.95	V
VDD Regulation Voltage when DSEN Pin is Active to Supply IC	$V_{VDD\_REG\_DSEN}$		4.7	5.1	5.5	V
Operating Current (Note3)	I_{VDD_OP}	V_{DD}=9V, C_{GATE}=2.2nF, F_{SW}=200kHz		5.35	6.4	mA
		V_{DD}=5V, C_{GATE}=2.2nF, F_{SW}=200kHz		3.5	4.2	mA
Maximum VDD Pin Capacitor Charging Current	$I_{VDD\_CHARGE\_MAX}$	VIN pin is active to charge VDD capacitor	25	35		mA
		DSEN pin is active to charge VDD capacitor	40	50		mA
Quiescent Current	I_Q	Under Sleep Mode	280	350	430	μA
VIN Pin						
Threshold of Switching to VIN Supply Channel	V_{VIN_VINSPY}	V_{VIN} is rising	4.4	4.7	4.9	V
Threshold of Switching to DSEN Supply Channel	$V_{VIN\_DSENSPY}$	V_{VIN} is falling	4.3	4.6	4.8	V
REG Pin						
Resistor to Program Drain Falling Slope to Enable SR(Note3)	R_{REG}	R_{REG}=50kΩ	60	80	100	ns
		R_{REG}=300kΩ	115	155	195	ns
TZ Pin						
ZVS Time Program Coefficient	k_{TZ}			4.5		10^{-9}
DSEN Pin						
Operating Voltage Range	V_{DS_OP}				110	V
Ratio of PVS to DSEN	$K_{\_PVS\_RATIO}$			50		
PVS Initial Enable Threshold	$V_{PVS\_INITIAL\_EN}$			150		mV
Turn on Threshold	V_{ON_TH}		-115	-85	-55	mV
V_{DS} Regulation Voltage	V_{DS_REG}		-52	-35	-20	mV
Turn off Threshold	V_{OFF_TH}		9	20	31	mV
Force Turn off Threshold	$V_{DS\_FORCE\_TH}$		35	48	61	mV
Force Turn off Debounce Time (Note3)	T_{DBC_FORCE}		50	71	90	ns
Enter Sleep Mode Time Threshold	T_{SLP_TH}		50	67	80	μs

GATE Pin						
GATE Pin Clamped Current before VDD ON(Note3)	I_{CLP}	Vgs=1V	160	200		mA
Max. Source Current (Note3)	I_{SOURCE_MAX}	C_{LOAD}=2.2nF, Vgs from 1V to 6V	0.375	0.5		A
Max. Sink Current (Note3)	I_{SINK_MAX}	C_{LOAD}=2.2nF, Vgs from 6V to 1V	1.5	2		A
Minimum ON Time	T_{ON_MIN}		550	700	850	ns
Minimum OFF Time	T_{OFF_MIN}		400	530	660	ns
Turn on Delay Time (Note3)	T_{ON_DLY}	C_{GATE}=2.2nF		35	50	ns
Turn off Delay Time (Note3)	T_{OFF_DLY}	C_{GATE}=2.2nF		10	20	ns
OTP						
Thermal Shutdown Temperature (Note3)	T_{SD}			165		°C
Hysteresis to Resume Operating (Note3)	T_{OTP_HYS}			20		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause perm anent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: Guarantee by design.

Operation Principles

Introduction

The SY23434 is a Flyback SR with proprietary operation mode to achieve Flyback ZVS function. It supports primary side PWM IC which has QR mode and valley number lock function, and the valley lock numbers should be 1 to 6. To ensure safe operation, SR control functions include turn on/off control, Vds regulation, slope program, etc. The ZVS control logic helps primary side FET to turn on at a low DRAIN voltage to reduce the switching losses, thereby maximizing system efficiency and achieving high power density.

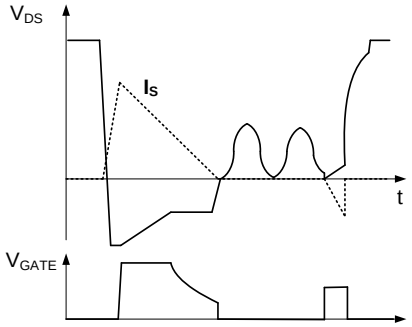


Fig. 4 SR Operation Diagram

SR Turn on

The traditional method of turning ON the SR MOSFET is to use a set turn-on threshold V_{ON_TH}.

When the DSEN voltage falls and reaches V_{ON_TH}, the SR MOSFET is turned ON after a short delay.

While in DCM or QR operating modes, a resonant waveform may appear after the transformer secondary current decreases to zero. Sometimes, the amplitude of this resonant waveform can be large enough to cause the DSEN voltage to drop below the turn-on threshold V_{ON_TH}, which may lead to the false turn-on of the SR MOSFET. To address this issue, a circuit to detect the falling slope rate of V_{DSEN} is used.

When the primary MOSFET Q1 is turned off, the V_{DSEN} falling slope rate is very high, and the SR MOSFET will turn on. During the resonant phase, the V_{DSEN} falling slope rate is relatively low, and the SR MOSFET will not turn on. The SY23434 uses a resistor divider circuit to sense the DSEN voltage, where V_{PVS} is 0.02 x V_{DSEN}.

Two thresholds are set to sense the V_{PVS} falling slope rate. △T is the time duration measured when V_{PVS} is falling between the high-level threshold V_{PVS_HTH} and the low-level threshold V_{DSEN_LTH} (0mV). △T is compared with a falling slope reference time T_{REF} using a counter.

A blanking period is used to prevent external noise (such as ESD noise) from falsely turning on the SR MOSFET.

If V_{PVS} is above V_{PVS_HTH}, lasts for T_{PVS_BLK} (200ns) and the falling slope time △T <T_{REF}, the IC considers this action as a primary MOSFET turn-off event, and will turn ON the SR MOSFET after a short delay. In all other cases the SR MOSFET will not be turned ON.

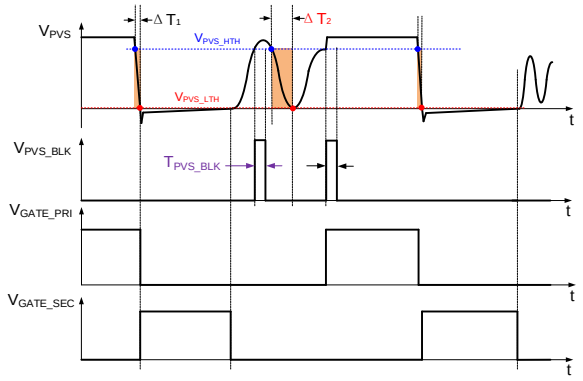


Fig. 5 SR MOSFET Turn ON Time Diagram

V_{PVS_HTH} is a dynamically adjusted value, and it has a value of 0.85 x V_{DSEN}.

The falling slope ref time threshold T_{REF} is controlled by REG resistor as shown below:

T_{REF} setting has 4 steps:		
Step	T_{REF}	R_{REG}
1	80ns	50kΩ
2	105ns	100kΩ
3	130ns	175kΩ
4	155ns	300kΩ

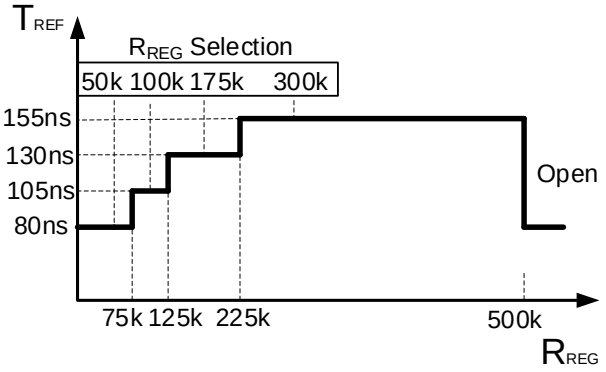


Fig. 6 T_{REF} Programming

SR Gate Control

In DCM mode, the current through the SR MOSFET will decrease before the primary MOSFET is turned on. The closed-loop V_{DS} regulation circuit will gradually reduce V_{GATE} once V_{DS} is above the V_{DS_REG} (-35mV) level. As the current through the SR MOSFET decreases, V_{GATE} drops close to the turn-off threshold of the SR MOSFET. At this point, the product of the (I_D x R_{DSON}) can no longer be regulated to V_{DS_REG}, causing V_{DS} to increase beyond V_{OFF_TH}. After a short time delay (T_{OFF_DLY}), a large sink current will pull down the gate voltage to zero to turn OFF the SR MOSFET.

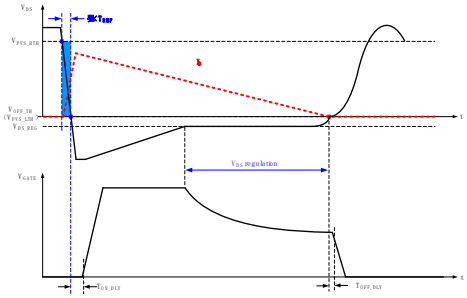


Fig. 7 SR MOSFET Control in DCM Mode

Min ON Time& Min OFF Time

When primary MOSFET is turned off, the DRAIN voltage of the secondary SR MOSFET will drop rapidly to about -700mV, due to the circuit parasitic resonance. To void false turn-off of the SR MOSFET, a blanking time T_{ON_MIN} is applied after the SR MOSFET is turned ON. During this blanking time, the GATE pin output is latched off.

After SR MOSFET is turned OFF, a ringing will appear on DRAIN voltage waveform. To avoid the internal logic circuit false trigger, a blanking time T_{OFF_MIN} used.

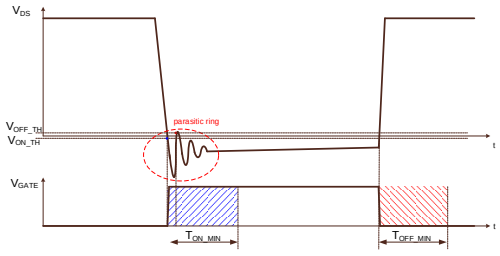


Fig. 8 Timing Diagram of Min ON/OFF Time

ZVS Operation

The key function of the SY23434 is to achieve primary MOS ZVS turn-on for high efficiency and high-power density. The SY23434 is compatible with primary side QR IC which has valley number lock operation mode to achieve this function.

The SY23434 adopts the proprietary drive method to increase the resonation magnitude of switching node, which pulls V_{DRAIN_P} to approximately around 50V to achieve primary side MOSFET ZVS conduction. The ZVS PWM is only activated in QR mode within 6 valleys, beyond this range, the ZVS is disabled.

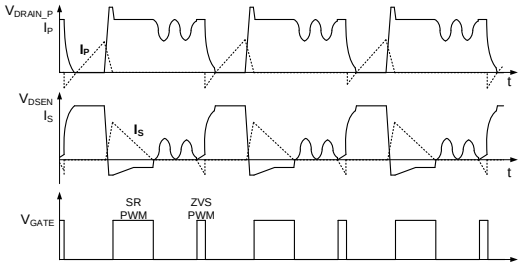


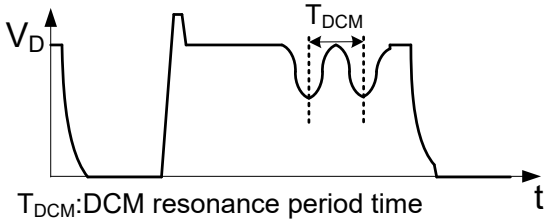
Fig. 9 ZVS Control Diagram

ZVS Coefficient R_{TZ} Setting

The ZVS performance is affected by transformer's magnetizing inductance (Lm) and the total equivalent capacitance (Csw) of switching node. For the best operation efficiency, the resistor value of TZ pin to GND can be adjusted. The resistor sets ZVS PWM turn on time coefficient; it is choosing as follows.

$$R_{TZ} = \frac{\sqrt{C_{SW} \cdot Lm}}{4.5 \cdot 10^{-9}} (k\Omega)$$

Method 1, calculate the coefficient based on magnetizing inductance and equivalent switching node capacitance.



$$R_{TZ} = \frac{T_{DCM}}{2 \cdot \pi} \cdot \frac{1}{4.5 \cdot 10^{-9}} (k\Omega)$$

Method 2, calculate the coefficient based on DCM resonance period time.

The resistor can be adjusted slightly around the calculated value. The resistance range is preferred to be 20kΩ-80kΩ, if the range is <10kΩ or >100kΩ, range, the ZVS function will be disabled.

ZVS Enable Condition

1. Power supply: when the VIN supply is active, ZVS will be enabled. When the DSEN supply is active, the ZVS will be disabled. (DSEN pin supply power loss is

much higher, the extra driving loss may be greater than ZVS effect)

2. Input voltage condition: at low line input, the efficiency has hardly improved by ZVS function. So, the input voltage range is limited to maximize ZVS effect. The input voltage condition calculation is shown as below with hysteresis:

$$\text{ZVS enable: } V_{BULK} > N \cdot (0.333 \cdot V_{OUT} + 24)$$

$$\text{ZVS disable: } V_{BULK} < N \cdot (0.333 \cdot V_{OUT} + 21)$$

ZVS Protection

To guarantee ZVS logic working correctly, the maximum ZVS on time is limited to 2.5us.

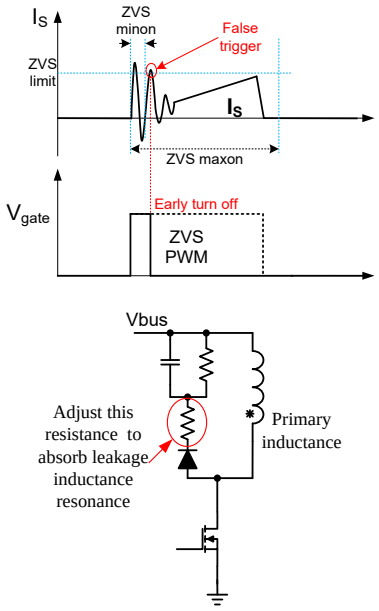


Fig. 10 ZVS Limit Protection

To prevent the excessive ZVS current or primary false conduction, the secondary current is limited during ZVS. However, the primary leakage inductance resonance may trigger the ZVS limit and cause the ZVS PWM to be turned off in advance, it is recommended to add the primary inductance resonance absorption resistor.

ZVS Performance Adjust

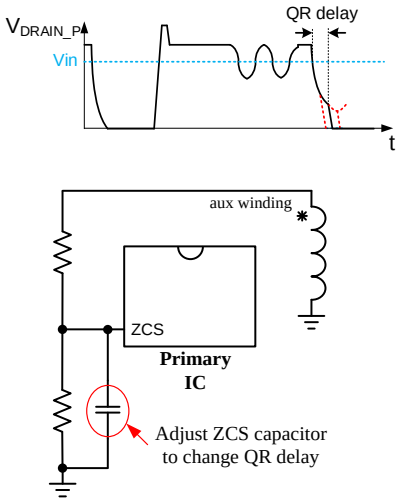


Fig. 11 Adjust ZVS Performance

To achieve the best ZVS performance, the primary IC QR delay time needs slightly adjusted. The best working condition is that the primary IC is turned on at the time of DCM resonance valley.

Dual Channel Power Supply

The device optimizes the overall efficiency by using two possible power sources during normal operation.

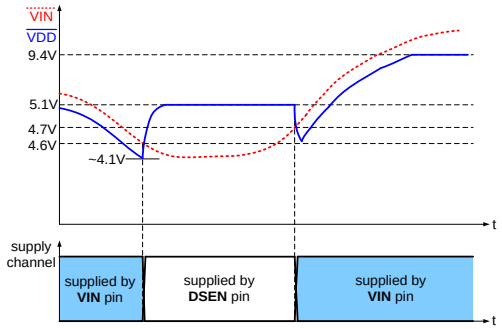


Fig. 12 Timing Diagram of Dual Channel Supply

Before VDD voltage reaches the V_{VDD_ON} threshold, the voltage is supplied by DSEN pin. When the voltage exceeds the V_{VIN_VINSPY} threshold, the VIN pin will be used instead.

As VIN increases, VDD will follow VIN (with about 0.5V voltage drop). When the voltage goes above 9.4V, the rail is regulated internally to this value.

When VIN is decreasing and crossing $V_{VIN\_DSENSPY}$, the device will switch to using the DSEN pin, and VDD will be regulated to 5.1V. The timing diagram is shown in Fig. 9.

Power Saving Mode

Under light load conditions, the SY23434 will enter power saving mode to improve light load efficiency.

During the switching cycle, a timer will start to count after SR MOSFET is turned off. If the timer counts to 67us before next SR turn ON, the device will enter the power saving mode to reduce the power consumption. The SY23434 will exit power saving mode on the next SR MOSFET turn ON event.

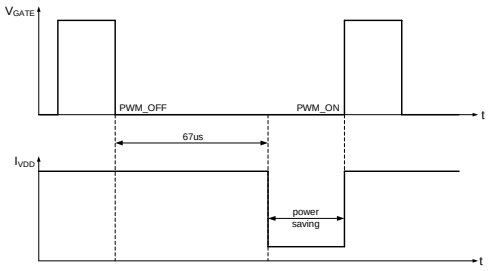


Fig. 13 Timing Diagram of Power Saving Mode

Force Turn off

To prevent the primary MOSFET and secondary MOSFET turned on at the same time, the IC adopts the force turn-off function, which has higher priority than T_{ON_MIN}. When the V_{DS} is above DSEN force turn-off threshold $V_{DS\_FORCE\_TH}$ lasting for debounce time T_{DBC_FORCE}, SR GATE will turn off immediately; When V_{DS} is below $V_{DS\_FORCE\_TH}$, SR GATE can be restored within T_{ON_MIN}.

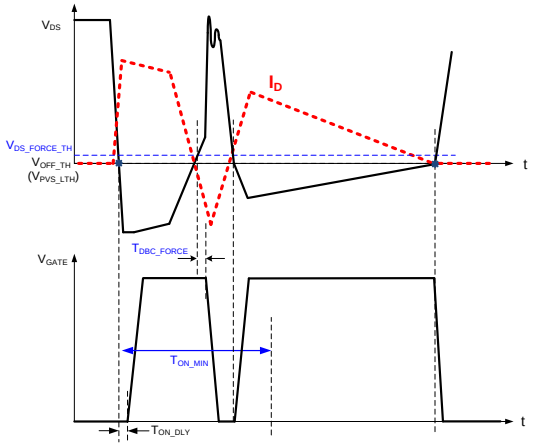


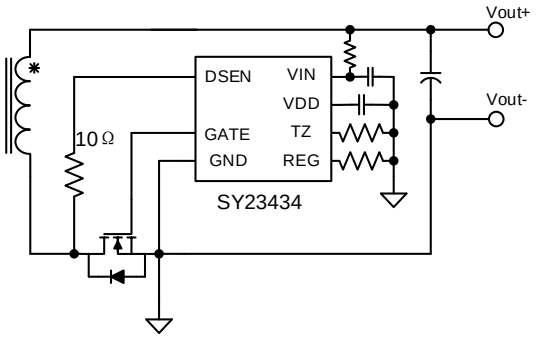
Fig.14 Timing Diagram of Forced Turn off

OTP

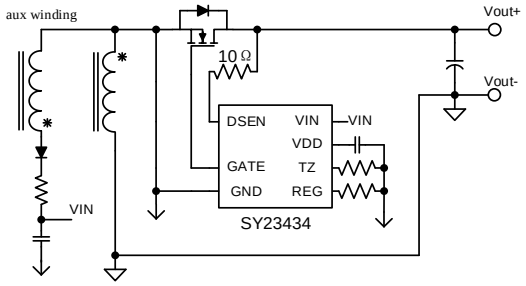
IC die temperature is monitored, if the die temperature rises above 165℃, IC will stop driving SR MOSFET and the keep gate voltage to 0V. When die temperature drops below 145℃, IC will resume normal operating again.

Application Information

Typical System Implementations



Low Side Rectification with Vout Supply Power

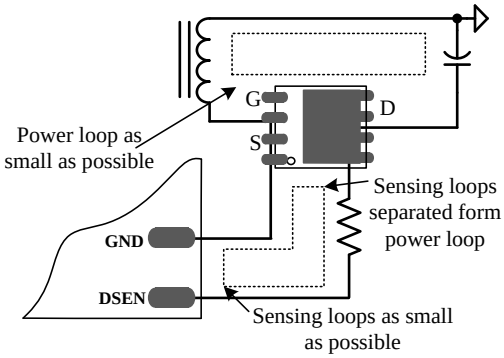


High Side Rectification with Aux Winding Supply Power

Layout Guideline

Sensing for DSEN/GND

1. Make the sensing connection (DSEN/GND) as close as possible to the MOSFET (drain/source).
2. Keep the IC out of the power loop to prevent the sensing loop and power loop from interrupting each other.



(a) Minimize the size of the switching loops: secondary power loop, secondary RC snubber circuit loop and IC power supply loop.

(b) To achieve better EMI and Efficiency performance, use a decoupling capacitor between the output

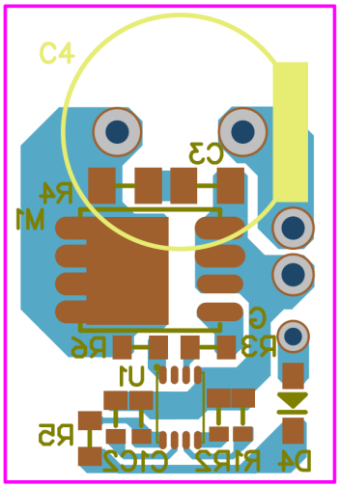
connector and the SR MOSFET output.

(c) GND pin should be connected to the Source of the SR MOSFET using a short trace.

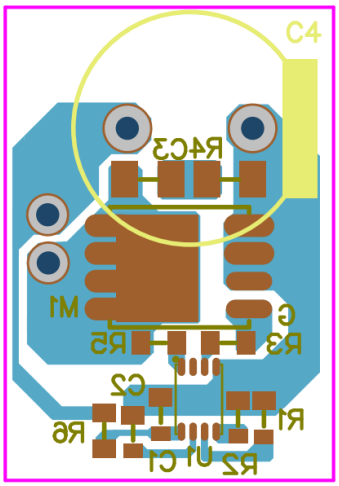
(d) DSEN pin should be connected to the Drain of the SR MOSFET using a short connection.

(e) Due to the high resistance on REG and TZ pin, the layout size and length of each loop should be as small as possible. Meanwhile, the layer directly under these two loops better connected to IC GND to shield switching noise.

Layout Example



High Side SR Layout @Bottom View

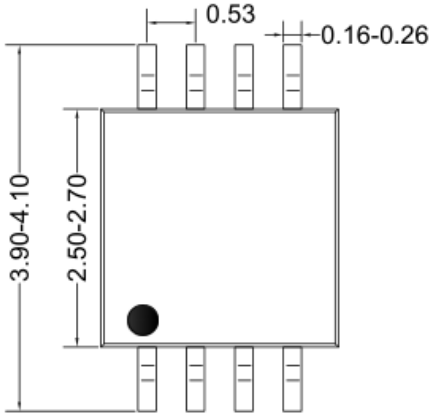


Low Side SR Layout @Bottom View

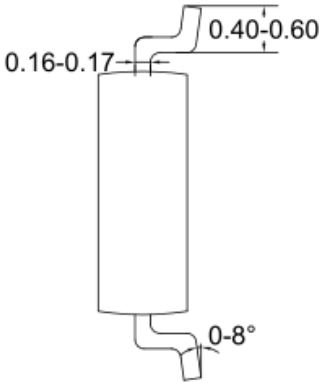
Design Notice

1. To improve the system ESD performance, a 10Ω~51Ω resistor should be used in series between VIN pin and output terminal, and at least 100nF cap should be used in parallel between VIN pin and GND pin.
2. To achieve better ZVS effect, the SR MOSFET is recommended to use DFN or SO-8 package, which has a smaller package inductance that will not cause SR or ZVS turn off early.
3. To achieve better ZVS effect, the Ciss and Coss capacitors of SR MOSFET should be chosen as small as possible, Ciss is recommended not to exceed 6nF.

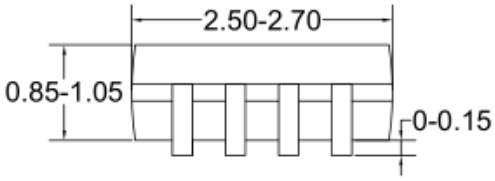
CPC8 Package Outline & PCB Layout Design



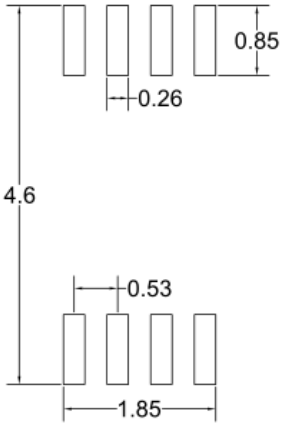
Top view



Side view



Front view

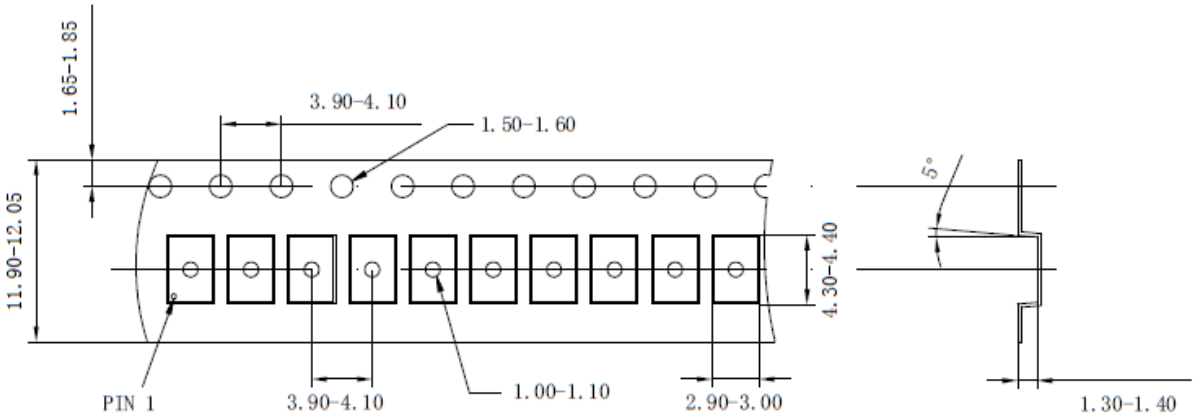


Recommended PCB Layout (Reference Only)

Notes: All dimension in MM and exclude mold flash & metal burr.

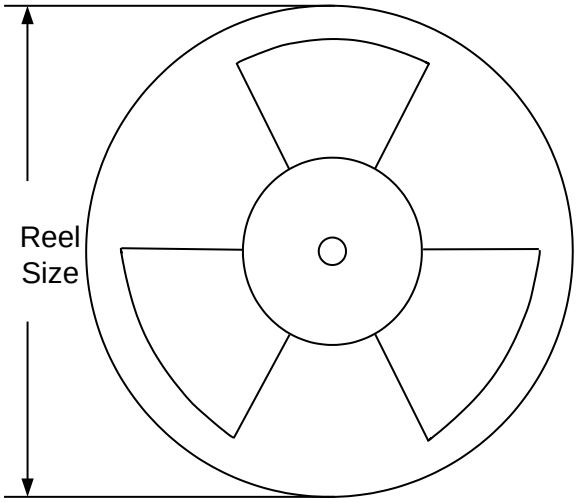
Taping & Reel Specification

1. Taping orientation for packages（CPC8）



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
CPC8	12	4	13"	400	400	7500

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
September 15, 2023	Revision 0.9	Initial Release

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