SA22300

36V, Boost/Flyback/Sepic Controller

General Description

The SA22300 is a non-synchronous Boost/Flyback/ Sepic controller with built-in protection features. The device is suitable for harsh automotive environment. It features several built-in protection such as cycle-by-cycle current limit, overcurrent protection, FB short protection, etc.

The SA22300 integrates a gate driver to drive external N-channel MOSFET and also adopts peak current control strategy with built-in slope compensation to improve the stability.

The SA22300 is available in a SOP8 package.

Key Features

- Wide Input Voltage Range: 3.45V to 36V
- 1.2V ±2% Reference Voltage
- Fixed Frequency Operation
- Internal Soft-Start
- Typical 1.6μA Shutdown Current
- Cycle-by-Cycle Current Limit Protection
- Hiccup-Mode Overcurrent Protection (OCP)
- Hiccup-Mode Short-Circuit Protection (SCP)
- 1.5A Peak Gate Source Current
- 1.5A Peak Gate Sink Current
- Thermal Shutdown
- Package: SOP8
- Automotive AEC- Q100 Grade 1 Certified

Applications

- Automotive 12-V Battery Application
- DC-to-DC Converters
- LIDAR Power Supply
- Battery-powered Boost, Flyback, Sepic

Typical Application Circuit

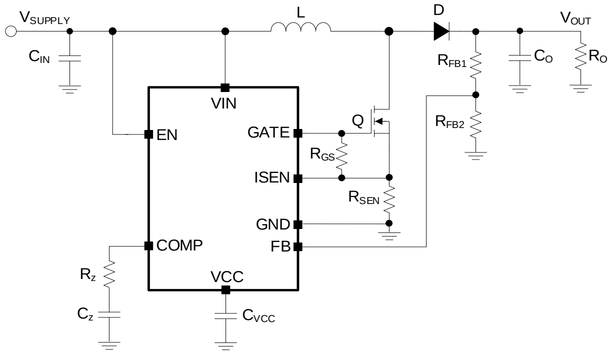

Figure 1. Boost Application

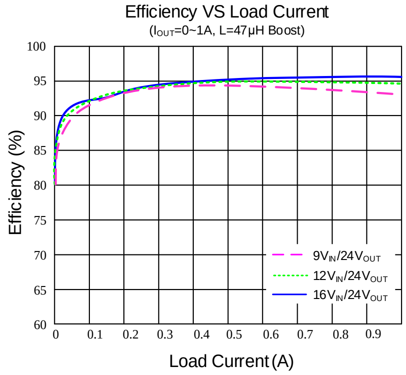

Figure 2. Efficiency vs. Output Current

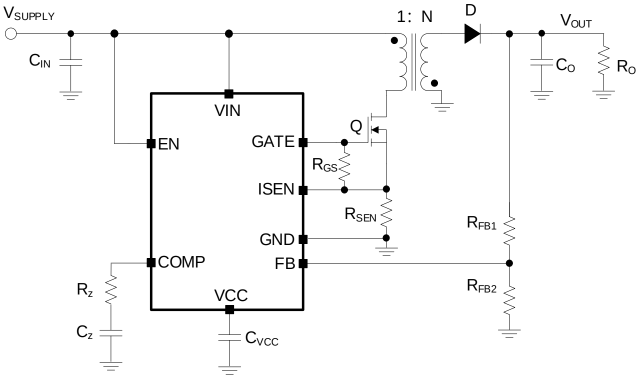

Figure 3. Flyback Application

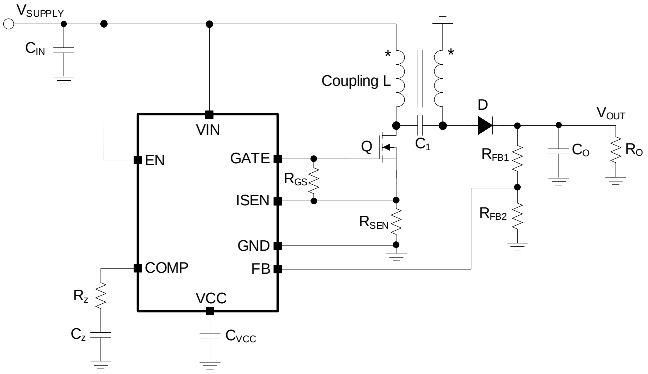

Figure 4. Sepic Application

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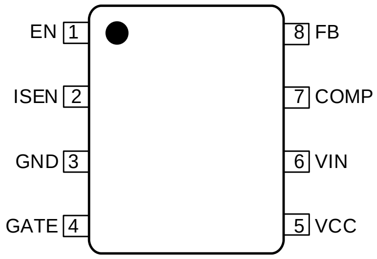
Ordering Information

Ordering Part Number	Package Type	Top Mark
SA22300FAP	SOP8 RoHS-Compliant, Halogen-Free	**FEM*xyz***

***x* = year code, *y* = week code, *z* = lot number code**

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	EN	Enable pin, apply logic high signal to enable the device.
2	ISEN	Current sense input pin. Voltage generated across an external sense resistor is fed into this pin.
3	GND	Ground pin.
4	GATE	Gate driver output. Connect to the gate of the external N-channel MOSFET. GATE pin will turn into high impedance state when EN is off. Put a 10kΩ resistor between MOSFET gate and source or GND to prevent electric accumulation of gate charge.
5	VCC	10.5V internal LDO output from VIN. Do not leave open, bypass with 1μF ceramic capacitor.
6	VIN	Power supply input pin. A 100nF ceramic capacitor is recommended to be placed close to VIN and GND pin.
7	COMP	External compensation pin. Connect RC network from this pin to GND to compensate the control loop.
8	FB	Output voltage feedback pin. The output voltage reference is 1.2V.

Block Diagram

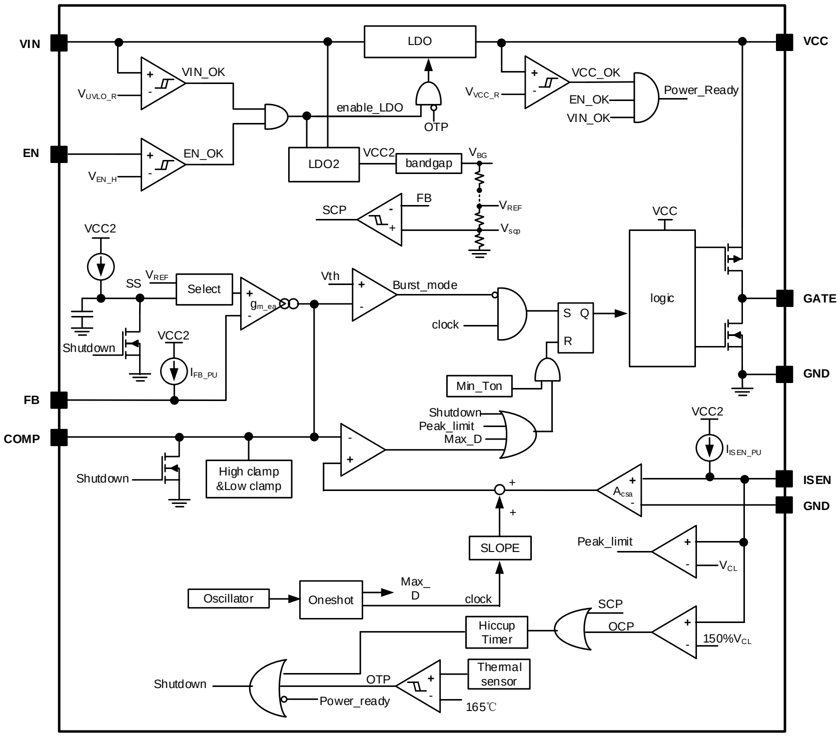


Figure 5. Block Diagram

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Absolute Maximum Ratings

Parameter (Note 1)	**Min**	**Max**	**Unit**
VIN, EN	-0.3	40	V
FB, ISEN, COMP	-0.3	6	
GATE, VCC	-0.3	13	
Junction Temperature Range	-40	150	°C
Lead Temperature (Soldering, 10 sec.)		260	
Storage Temperature Range	-65	150	
ESD Susceptibility			
HBM (Human Body Mode)	2000		V
CDM (Charge Device Mode)All pins	500		

Thermal Information

Parameter (Note 2)	**Typ**	**Unit**
θ_{JA}	98.5	°C/ W
θ_{JB}	58	
Ψ_{JT}	10	
P_D Power Dissipation T_A = 25°C	1.26	W

Recommended Operating Conditions

Parameter (Note 3)	**Min**	**Max**	**Unit**
Supply Voltage VIN	3.45	36	V
EN	0	36	
Ambient Temperature Range	-40	125	°C

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Electrical Characteristics

(3.45V≤V_{IN}≤36V,-40°C≤T_A≤125°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
VIN	VIN UVLO Rising Threshold	V_{UVLO_R}		3.05	3.225	3.45	V
	UVLO Falling	V_{UVLO_F}		2.9	3.1	3.35	V
	Shutdown Current	I_{SD}	V_{EN}=0V		1.6	3	μA
	Operating Current	I_{OP}	V_{EN}=3V, no switching	0.5	1.5	2.5	mA
VCC	VCC Output Voltage	V_{VCC}	I_{VCC}=10mA, V_{IN}=12V	9.2	10.5	11.8	V
	Drop Out Voltage	V_{DROP}	I_{VCC} = 50mA		0.4	1	V
	VCC Current Limit	I_{VCC_LIMH}	VCC drop 10%	60		120	mA
	VCC Under Voltage Reset Rising Threshold	V_{VCC_R}		2.85	3.0	3.15	V
	VCC Under Voltage Reset Falling Threshold	V_{VCC_F}		2.75	2.9	3.05	V
EN	EN Pull-Down Current	I_{EN}			0.5	1	μA
	EN Logic '1' Threshold	V_{EN_H}		1.425	1.5	1.575	V
	EN Logic '0' Threshold	V_{EN_L}		1.380	1.45	1.520	V
	EN Hysteresis Voltage	V_{EN_hys}		0.03	0.05	0.08	V
Oscillator	Switching Frequency	f_{SW}		153	170	187	kHz
	Minimum On Time	t_{ON_MIN}		85	140	210	ns
	Minimum Off Time	t_{OFF_MIN}		280	450	620	ns
FB&SS	Output Feedback Reference	V_{ref}		1.176	1.2	1.224	V
	FB Pull up Current	I_{FB_PU}			0.1	0.2	μA
	Soft-start Time	T_{ss}	From 10%V_{ref} to 90%V_{ref}	4.8	6	7.2	ms
Error Amplifier	Transconductance of Error Amplifier	g_{m_ea}		800	1200	1680	μS
	COMP Sourcing Current	I_{COMP_SOURCE}		80	130	180	μA
	COMP Sinking Current	I_{COMP_SINK}		80	130	180	μA
	COMP High Clamp	V_{COMP_HIGH}		1.15	1.2	1.25	V
	COMP Low Clamp	V_{COMP_LOW}		320	350	380	mV
	COMP Low Threshold Stop Switching	V_{COMP_BURST}		370	400	430	mV
	Slope Compensation	V_{SLOPE}	D=100%	90	110	130	mV
Current Sense	ISEN Pull up Current	I_{ISEN_PU}		10	30	50	μA
	Cycle by Cycle Current Limit Threshold Voltage	V_{CL}		360	400	440	mV
	Over Current Protection Threshold Voltage	%V_{CL}	Percent of V_{CL}	125	150	175	%
Gate Driver	Gate Driver HSFET Ron	R_{HS_ON}		1.4	2.8	4.9	Ω
	Gate Driver LSFET Ron	R_{LS_ON}		0.65	1.5	2.9	Ω

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Thermal Shutdown	Thermal Shutdown Threshold	T_{SD}		150	165	180	ºC
	Thermal Shutdown Hysteresis	T_{SDHYS}		10	15	20	ºC
FB Short Circuit Protection	Short Circuit Threshold Voltage	V_{scp}	V_{FB} as percent of V_{ref}	60	67	75	%V_{REF}

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C. Device mounted on an 8.5x8.5cm FR-4 substrate PCB, 2oz copper, 2 layers.

Note 3: Electrical characteristics are not guaranteed outside its operating conditions.

Note 4: Guaranteed by design. Not tested in production.

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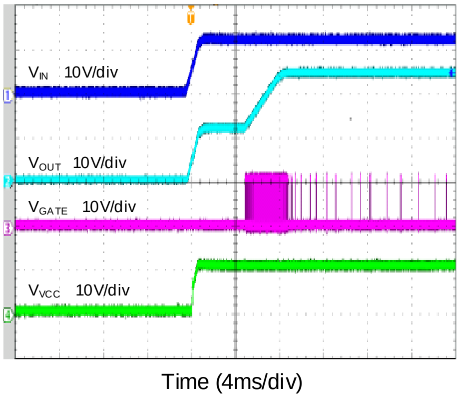
Typical Performance Characteristics

(T_A=25°C Boost Application)

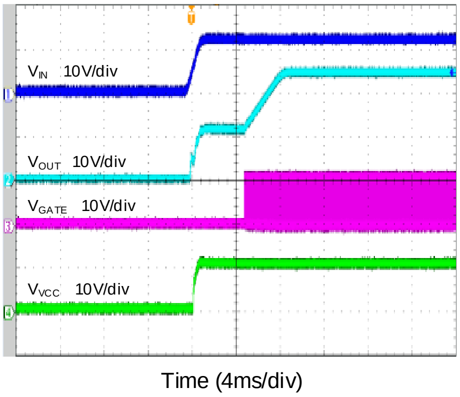
Startup from V_{IN}

(V_{IN}=12V,V_{OUT}=24V,I_{OUT}=0A)



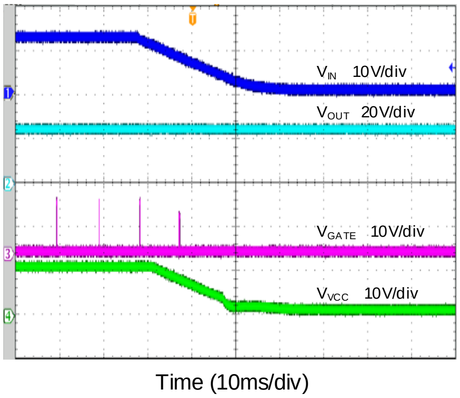
Startup from V_{IN}

(V_{IN}=12V,V_{OUT}=24V,I_{OUT}=1A)



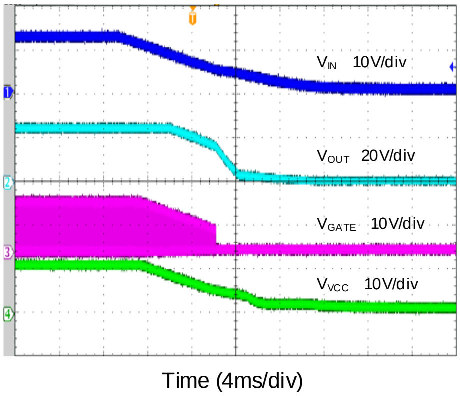
Shutdown from V_{IN}

(V_{IN}=12V,V_{OUT}=24V,I_{OUT}=0A)



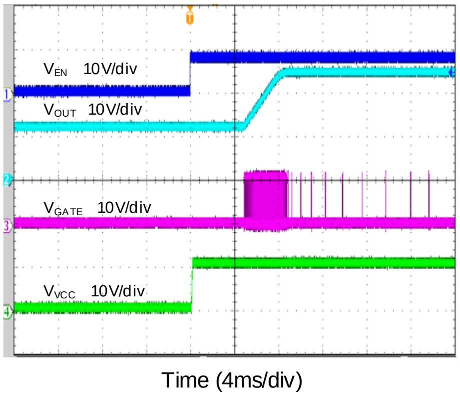
Shutdown from V_{IN}

(V_{IN}=12V,V_{OUT}=24V,I_{OUT}=1A)



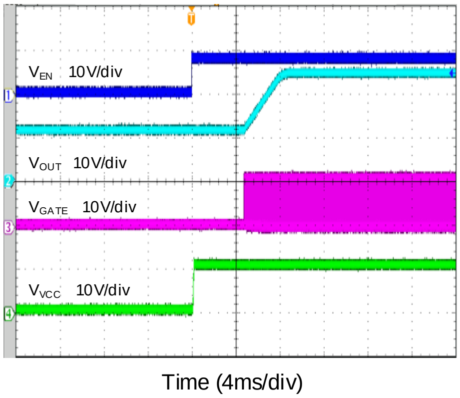
Startup from Enable

(V_{IN}=12V,V_{OUT}=24V,I_{OUT}=0A)

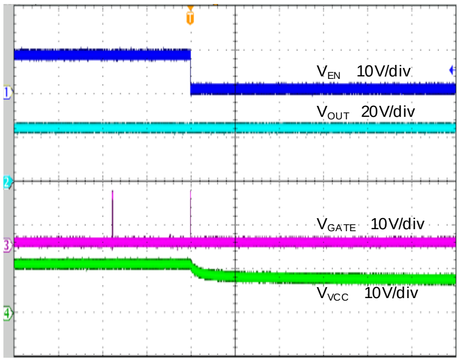


Startup from Enable

(V_{IN}=12V,V_{OUT}=24V,I_{OUT}=1A)

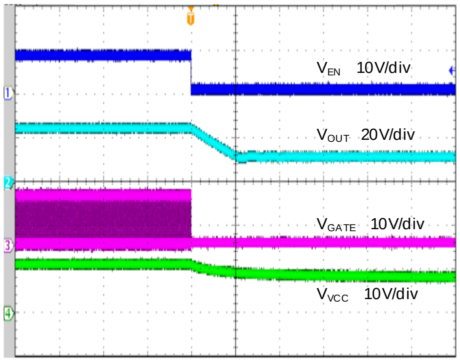


Shutdown from Enable
(V_{IN}=12V,V_{OUT}=24V,I_{OUT}=0A)



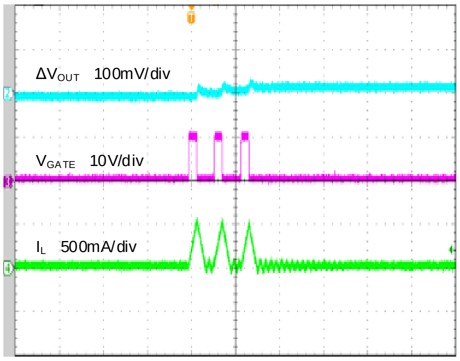
Time (4ms/div)

Shutdown from Enable
(V_{IN}=12V,V_{OUT}=24V,I_{OUT}=1A)



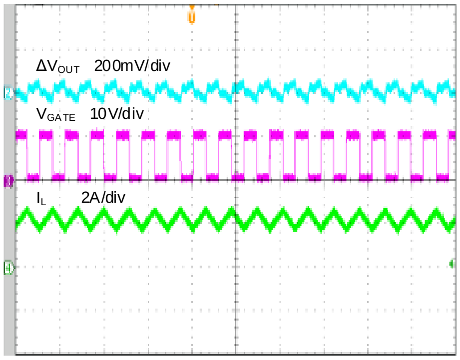
Time (800us/div)

Output Voltage Ripple
(V_{IN}=12V,V_{OUT}=24V,I_{OUT}=0A)



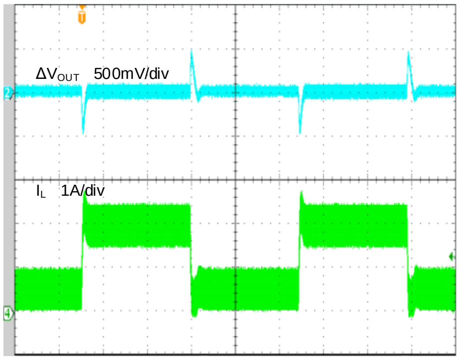
Time (10us/div)

Output Voltage Ripple
(V_{IN}=12V,V_{OUT}=24V,I_{OUT}=1A)



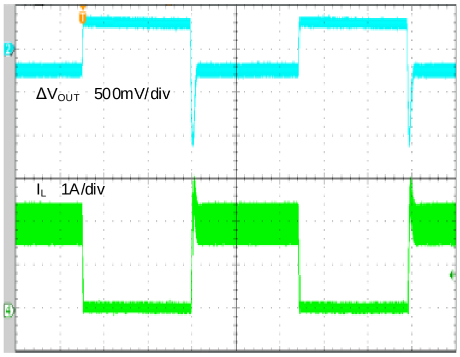
Time (10us/div)

Load Transient Response
(V_{IN}=12V,V_{OUT}=24V,I_{OUT}=0.25A~1A)



Time (2ms/div)

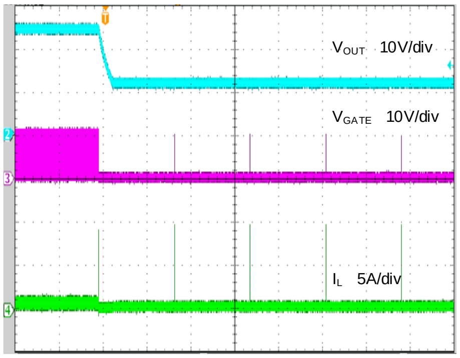
Load Transient Response
(V_{IN}=12V,V_{OUT}=24V,I_{OUT}=0~1A)



Time (2ms/div)

Output Over Current Protection

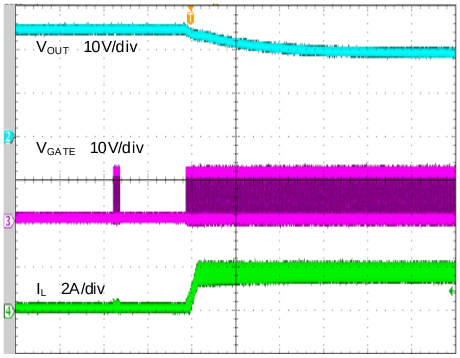
(V_{IN}=12V,V_{OUT}=24V,I_{OUT}=0.2A)



Time (20ms/div)

CBC current limit protection

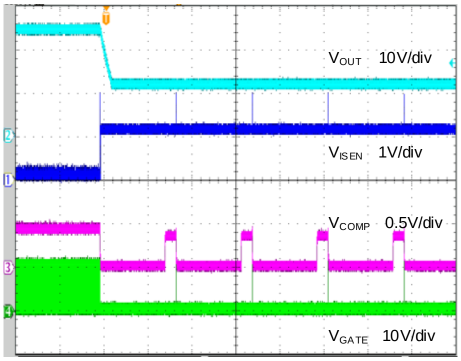
(V_{IN}=12V,set V_{OUT}=24V, V_{OUT} force 22.8V)



Time (800us/div)

ISEN Open Protection

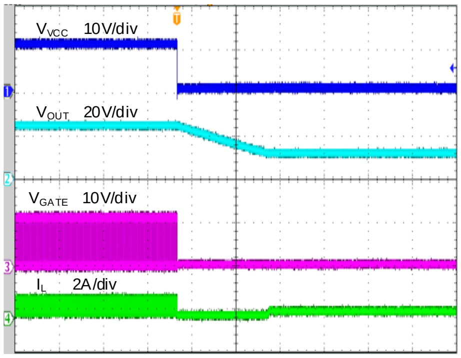
(V_{IN}=12V,V_{OUT}=24V,I_{OUT}=0.2A)



Time (20ms/div)

VCC Short Circuit Protection

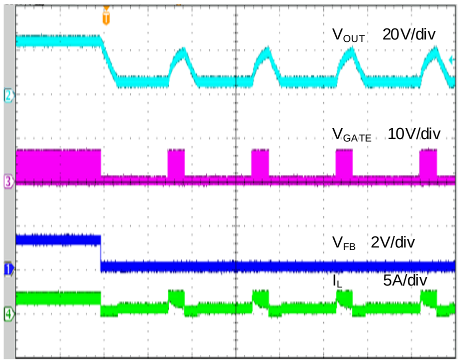
(V_{IN}=12V,V_{OUT}=24V,I_{OUT}=0.2A)



Time (2ms/div)

FB Short Protection

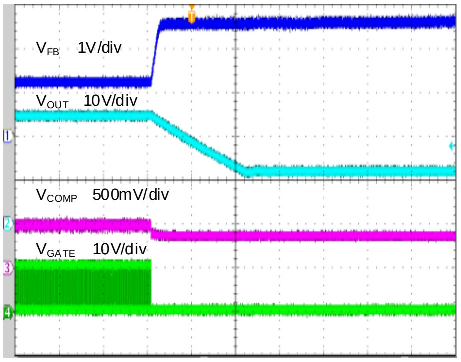
(V_{IN}=6V,V_{OUT}=24V,I_{OUT}=0.35A)



Time (20ms/div)

FB open Protection

(V_{IN}=12V,V_{OUT}=24V,I_{OUT}=0.5A)



Time (800us/div)

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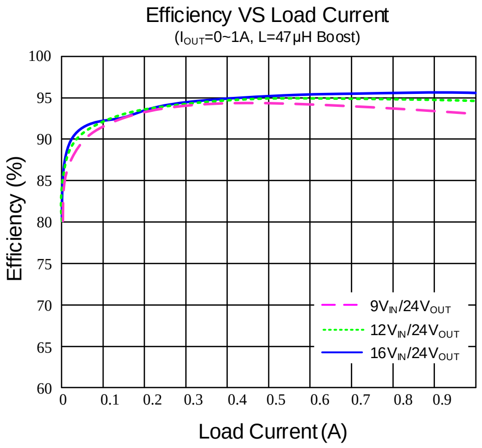

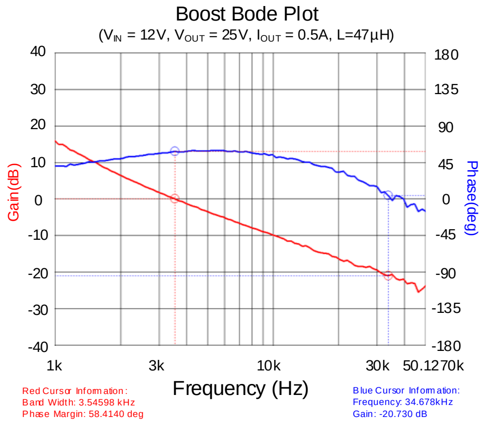

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Detailed Description

The SA22300 is a non-synchronous controller for Boost, Flyback and Sepic applications. The controller integrates a gate driver with 1.5A current capability, which can drive external MOSFET fast. Considering the operation stability and ease of use, peak current control strategy with built-in slope compensation is adopted, where the switching current is sensed through an external resistor to control the on-time. The SA22300 has a fixed-frequency clock (170kHz) to ensure constant operational frequency. During light load operation, the controller will enter burst mode to improve light-load efficiency.

The SA22300 has several built-in protection features and is suitable for harsh automotive environment. On the basis of peak current control, the SA22300 possesses fast and accurate cycle-by-cycle current limit and over current protection (OCP). Once the voltage drop of sense resistor exceeds OCP threshold, the controller will enter hiccup mode to prevent overheating of the external MOSEFT. Besides, the SA22300 also has VCC short, FB short, ISEN pin open and FB pin open protection. These protection measures help to improve the system reliability and make the controller robust for complicated automotive environment.

Current Mode Control

The SA22300 uses a fixed frequency peak current mode control architecture. The peak current through the external MOSFET is sensed through an external sense resistor and fed into the ISEN pin. The sensed current is added to the slope compensation ramp and fed into the positive input of the PWM comparator. The output voltage is also sensed through an external feedback resistor divider network and fed into the error amplifier negative input (feedback pin, FB). The output of the error amplifier (COMP pin) is fed into the negative input of the PWM comparator. At the start of any switching cycle, the oscillator sets the RS latch using the switch logic block. This forces a high signal on the GATE pin and the external MOSFET turns on. When the voltage on the positive input of the PWM comparator exceeds the negative input, the RS latch is reset and the external MOSFET turns off.

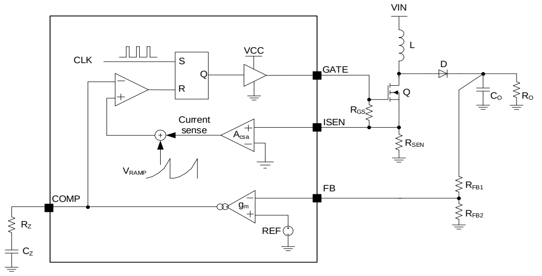

Figure 6. Peak Current Mode Control Scheme

Under Voltage Lockout

The SA22300 has input undervoltage lockout (UVLO) protection. If VIN pin voltage drops below the UVLO falling threshold, the device will shut down. It will not restart until VIN pin voltage surpasses the UVLO rising threshold when enabled.

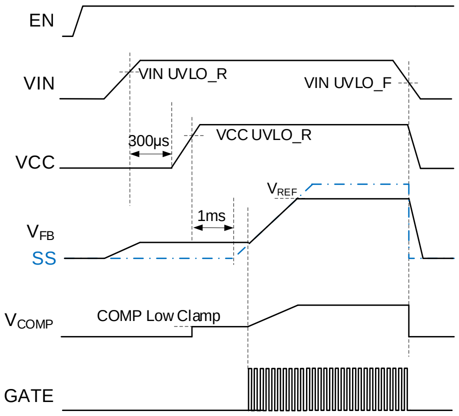

Figure 7. Start-up by VIN

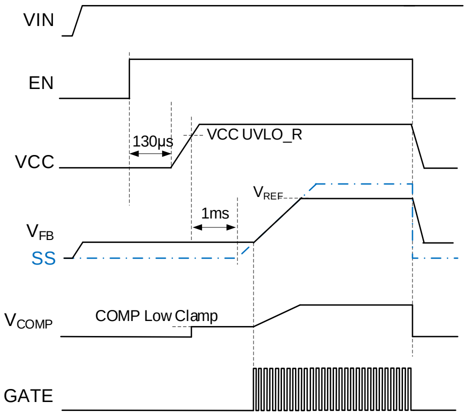

Figure 8. Start-up by EN

The minimum supply voltage after start-up can be further decreased by supplying the VIN pin from the Boost converter output or an external power supply.

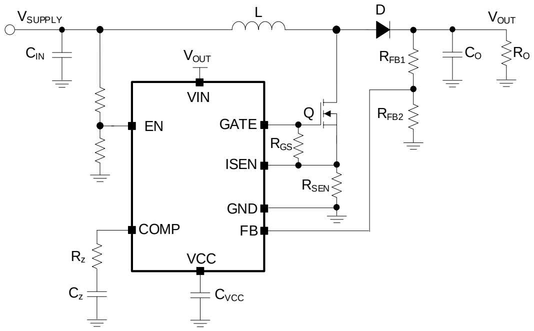

Figure 9. Decrease the Minimum Operating Voltage after Start-up

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Protection Features

The SA22300 has integrated output short circuit protection, output over current protection, thermal shutdown protection features, etc.

Table 1. Protection Features

Protection	Threshold	Response Time	Operation
Thermal Shutdown	Rising: 165℃ Falling: 150℃	-	Shutdown when temperature>165℃ Restart when temperature<150℃
Cycle-by-Cycle Current Limit	V_{CL}=400mV	80ns	cycle-by-cycle current limit.
Output Over Current (OCP)	150%V_{CL}	80ns	Hiccup mode auto recover.
VCC Under Voltage	V_{VCC_F}	15μs	Turn off GATE, reset COMP and SS.
VCC Short Circuit	50%V_{VCC}	80ns	Reduce current limit by 30%.
FB Open	-	-	100nA pull-up current, FB voltage increase and stop switching.
ISEN Open	-	-	30μA pull-up current, trigger OCP.
FB Short Circuit	67%V_{REF}	400ns	Hiccup mode auto recover, typical 30ms hiccup period.

VCC Over Current Protection

The SA22300 features VCC over current protection. When the VCC voltage drop below UVLO falling threshold, the GATE will turn off after 15μs delay and the SS and COMP will be pulled down. When VCC voltage drop 50%, the VCC current limit will be reduced by 30%.

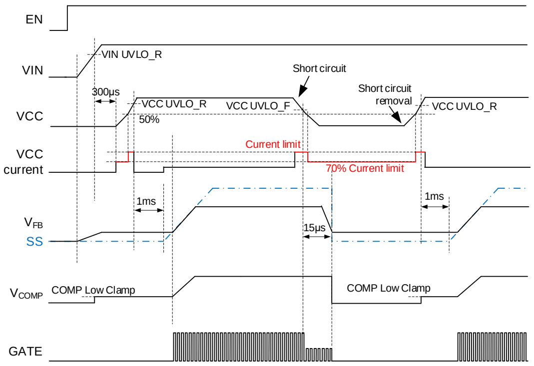

Figure 10. VCC Over Current Protection

Output Current Limit

The voltage drop of external current sense resistor reflects the current information of the external MOSFET and is fed to ISEN pin. On this basis, SA22300 features cycle-by-cycle current limit and over current protection. If the voltage between ISEN and GND pin exceeds cycle-by-cycle current limit value (V_{CL}), the external MOSFET will be turned off for the remainder of the cycle. In cycle-by-cycle current limit state, the IC still operates with the internal fixed frequency.

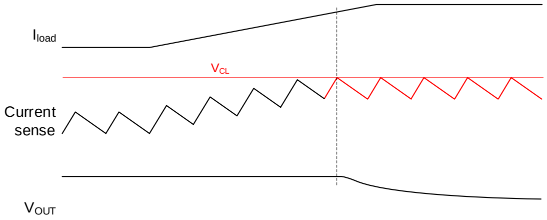

Figure 11. Cycle by Cycle Current Limit

If the voltage between ISEN and GND pin exceeds over current protection threshold (typically 150% V_{CL}), the device will enter hiccup operation until the over current situation is removed. In hiccup operation, the internal SS will be pulled down and the device will remain off for around 30ms. After the hiccup time, the device will restart.

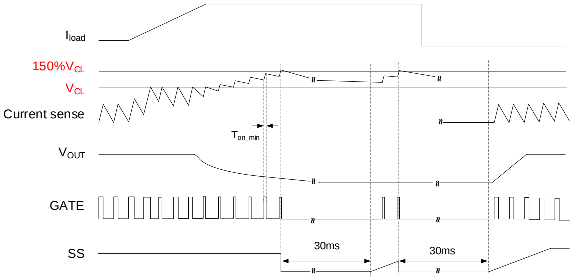

Figure 12. Output Over Current Hiccup Protection

Overtemperature Protection

The SA22300 provides thermal shutdown protection. The device goes into thermal shutdown when the junction temperature exceeds typically 165℃. In this mode, the gate is turned off and the VCC is shut down. When the junction temperature falls below typically 150℃, the controller will be re-enabled automatically.

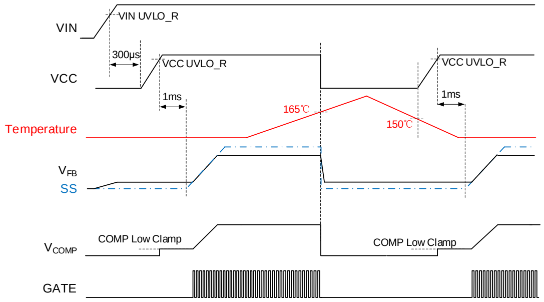

Figure 13. Overtemperature Protection

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Short Circuit Protection

When the FB voltage falls below the short circuit threshold, the device will enter short circuit shutdown mode and will remain off for a hiccup time and then go through the soft-start. Notice that the short circuit detection is inactivated during soft-start time.

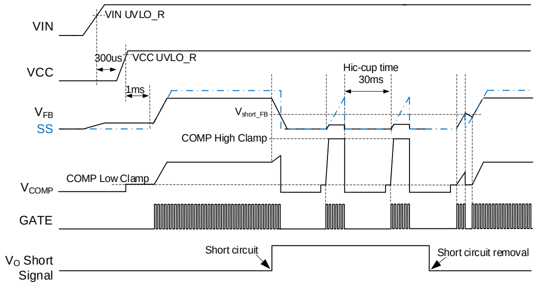


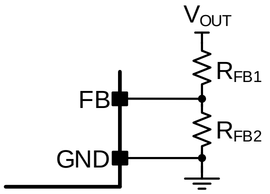
Figure 14. Short Circuit Protection

Applications Information

Feedback Resistor Dividers R_{FB1} and R_{FB2}

Choose R_{FB1} and R_{FB2} to program the proper output voltage. Choose large resistance values for both R_{FB1} and R_{FB2} to minimize the power consumption under light loads. It's highly recommended for R_{FB2} to choose value between 1k and 50k, then R_{FB1} can be configured using the following equation:

$$R_{FB1} = \frac{V_{OUT} - 1.2V}{1.2V} R_{FB2}$$



Current Sense Resistor

An external current sense resistor R_{SEN} is used to sense the current flowing through the MOSFET. The sensed voltage is fed to the ISEN pin for peak current control and current limit protection. The SA22300 features two current limit protections, cycle-by-cycle current limit (V_{CL}=400mV) and over current hiccup protection (150%V_{CL}). The sense resistor should be selected as follows:

$$R_{SEN} = \frac{400\text{mV}}{I_{CBC}}$$

I_{CBC}: desired cycle-by-cycle peak current limit value(A).

It is recommended that the voltage of the ISEN pin do not exceed 250mV during normal operation.

Diode

The output diode rectifies the output current. The average current through the diode is equal to the output current, so the current rating of selected diode should be larger than the maximum output current. In Boost application, the maximum reverse voltage of the diode is equal to V_{OUT}. Choose diode with voltage rating larger than 150%V_{OUT}. It is better to select a Schottky diode to reduce the reverse recovery loss.

Power MOSFET

The selection of MOSFET mainly focus on the aspects of voltage rating, gate driver capability and power dissipation. In Boost application, the maximum voltage across MOSFET is equal to V_{OUT}. Considering the voltage spike caused by parasitic capacitance, it's recommend to choose the Power MOS with voltage rating larger than 150%V_{OUT}.

The total gate charge (Q_g) should be within the following range to prevent VCC current limit:

$$Q_g < \frac{I_{VCC\_LIMH}}{f_{SW}} \text{ (Minimum } I_{VCC\_LIMH}\text{=60mA)}$$

The power dissipation of MOSFET consists of conduction losses and switching losses. Conduction losses are determined by R_{ON} of the Power MOS. Switching losses occur during the rising and falling time of the switch node and can be reduced by selecting MOSFET with small parasitic capacitances. However, small parasitic capacitance usually means large R_{ON}. Try to achieve a balance between conduction losses and switching losses when selecting the Power MOS.

It should be noted that the gate pin goes into high impedance state when EN is off. Put a 10kΩ resistor between MOSFET gate and source or GND to prevent electric accumulation of gate charge.

Inductor

The inductor value affects current ripple rate (CRR), the location of right half plane (RHP) zero and the slope compensation. Large CRR will cause more power loss of the magnetic component. CRR around 0.4 is a reasonable value. In this way, inductor value can be decided as follow:

$$L = \frac{(1-D)^2 DR_O}{CRR \cdot f_{SW}}$$

It is obvious that CRR changes when the operating duty varies. Choose D=0.33 or D near 0.33 to calculate, where CRR becomes the biggest.

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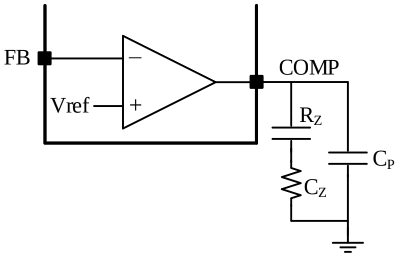
After the calculation above, RHP zero and slope compensation needed to be considered. Inductor of too large will cause low crossover frequency, which is not beneficial to the control loop speed. Inductor of too small may result in sub-harmonic oscillation. So, the calculated inductor value can be adjusted properly if needed.

Loop Compensation

The SA22300 incorporates peak current mode control strategy. To achieve a balance between the stability and speed of the control loop, we need a compensation network on COMP pin. In most applications, network shown in the following figure is widely used. The function of C_P is to generate a high-frequency pole which can counteract the high-frequency zero brought by output capacitor ESR. In applications where capacitor ESR is very small, C_P can be eliminated.



1) Select crossover frequency f_c.

Boost converters have RHP zero (f_{RHP_z}). It can raise the gain and lower the phase margin, to make stability of system. The location of f_c should be away from f_{RHP_z}. Generally, f_c should be lower than 1/10~1/5 f_{sw} or 1/10~1/5 f_{RHP_z}, depending on the smaller one. The f_{RHP_z} changes with R_o and D. Calculate the minimum f_{RHP_z} as following:

$$f_{RHP\_Z} = \frac{(1-D_{max})^2 R_O}{2\pi L}$$

2) Select resistor R_Z.

Resistor R_Z is selected according to the location of f_c. It can be calculated with the following equation:

$$R_Z = \frac{2\pi R_{SEN} f_c C_o V_o}{(1-D_{max}) g_{m\_ea} V_{REF}},$$

where g_{m_ea} is the transconductance of error amplifier.

3) Select capacitor C_Z.

Capacitor C_Z together with R_Z provides a zero compensation (f_Z) to improve the system stability.

$$f_Z = \frac{1}{2\pi R_Z C_Z}$$

Frequency f_Z should be lower than f_c to raise the phase margin. However, if f_Z is too low, the system response will be overdamped. It is recommended to set f_Z between f_c and the low frequency pole (f_{P_L}) brought by output load.

$$f_{P\_L} = \frac{1}{2\pi R_O C_O}$$

After choosing a proper value of f_Z, capacitor C_Z can be calculated as:

$$C_Z = \frac{1}{2\pi f_z R_Z}$$

Design Example

A design example of Boost application is shown below step by step.

Identify Design Specification

V_{IN}	V_{OUT}	I_O
9V~16V	24V	1A

Inductor Selection

Firstly, operating duty range can be calculated according to the design specification above.

$$D_{max} = 1 - \frac{V_{IN\_min}}{V_{OUT}} = 1 - \frac{9V}{24V} = 0.625$$

$$D_{min} = 1 - \frac{V_{IN\_max}}{V_{OUT}} = 1 - \frac{16V}{24V} = 0.33$$

Choose D=0.33 and CRR=0.4 to calculate L.

$$L = \frac{(1-D)^2 D R_O}{CRR \cdot f_{SW}} = \frac{(1-0.33)^2 \times 0.33 \times \frac{24V}{1A}}{0.4 \times 170\text{kHz}} \approx 52.3\mu H$$

Considering standard inductor value, we choose 47μH in this example.

MOSFET Selection

According to the design specification, a 60V MOSFET with small R_{ON} is chosen in this example. Make sure Q_g of the selected MOSFET satisfies:

$$Q_g < \frac{60\text{mA}}{170\text{kHz}}$$

In this example, it's recommended to put a 10kΩ resistor between MOSFET gate and source. This can prevent electric accumulation on MOSFET gate.

R_{SEN} Selection

Firstly, inductor current during normal operation should be calculated. When V_{IN} voltage is low, input current will be large. In this example, we choose V_{IN}=9V to calculate.

When V_{IN}=9V, duty cycle D=0.625. Inductor current ripple is:

$$\Delta I_L = \frac{V_{IN}}{L f_{SW}} D = \frac{9V \times 0.625}{47\,\mu H \times 170\,\mathrm{kHz}} = 0.7A$$

Assuming converter efficiency=0.9, the average input current is:

$$I_{\mathrm{ave}} = \frac{V_O I_O}{V_{IN} \times 0.9} = \frac{24V \times 1A}{9V \times 0.9} \approx 3A$$

Peak and valley inductor current is:

$$I_{\mathrm{peak}} = I_{\mathrm{ave}} + \frac{1}{2}\Delta I_L \approx 3.35A$$

$$I_{\mathrm{valley}} = I_{\mathrm{ave}} - \frac{1}{2}\Delta I_L \approx 2.65A$$

Considering the operating margin, we choose R_{SEN}=50mΩ in this example. Cycle-by-cycle current limit value is:

$$I_{\mathrm{CBC}} = \frac{400\,\mathrm{mV}}{50\,\mathrm{m}\Omega} = 8A$$

Finally, check whether the slope compensation is enough by comparing the falling slope of current sense signal with the internal slope rate.

The falling rate of inductor can be calculated as:

$$S_{\mathrm{f}} = \frac{V_O - V_{IN}}{L} R_{SEN} = \frac{24V - 9V}{47\mu H} \times 50\mathrm{m}\Omega \approx 16\,\mathrm{mV}/\mu s$$

Internal slope rate can be roughly estimated as:

$$S_{\mathrm{e}} = V_{SLOPE} f_{SW} = 110\,\mathrm{m}V \times 170\mathrm{kHz} \approx 18.7\,\mathrm{mV}/\mu s$$

It is obvious that $S_f \approx S_e$ and the slope compensation is enough.

It should be noted that the estimation of the slope rate above is based on the constant slope assumption. Actually, the internal slope rate is bigger than the estimation above when D>0.5. It is specially designed to offer sufficient slope compensation.

C_{OUT} Selection

Output capacitor is used to smooth the voltage ripple. The following equation is used to calculate the minimum capacitance. Assuming the output voltage ripple is 1%, we have:

$$C_{OUT} = \frac{I_O D}{\Delta V_O f_{SW}} = \frac{1A \times 0.625}{1\% \times 24V \times 170\mathrm{kHz}} \approx 15\mu F$$

Considering the voltage drop during the load transient, as well as the capacitance drop of ceramic capacitor, we choose four 10μF ceramic capacitors. A 47μF electrolytic capacitor is also chosen in this example.

Loop Compensation

1) Calculate the RHP zero frequency f_{RHP_Z} and crossover frequency f_c.

$$f_{RHP\_Z} = \frac{(1-D_{\max})^2 R_O}{2\pi L} = \frac{(1-0.625)^2 \times \frac{24V}{1A}}{2\pi \times 47\,\mu H} \approx 11.43\mathrm{kHz}$$

Set f_c=f_{RHP_Z}/6=1.9kHz.

2) Calculate R_Z according to the following equation:

$$R_Z = \frac{2\pi R_{SEN} f_c C_o V_o}{(1-D_{\max}) g_{m\_ea} V_{REF}} = \frac{2\pi \times 50\mathrm{m}\Omega \times 1.9\mathrm{kHz} \times 67\mu\mathrm{F} \times 24\mathrm{V}}{(1\text{-}0.625) \times 1200\mu S \times 1.2V} \approx 1.78k\Omega$$

We choose R_Z=2kΩ in this example, and the f_c becomes 2.2kHz.

When calculating R_Z above, 50% capacitance decrease of ceramic capacitor is considered.

3) Finally, we need to choose proper C_Z.
If C_Z=47nF, the compensated zero can be calculated as:

$$f_Z = \frac{1}{2\pi R_Z C_Z} = \frac{1}{2\pi \times 2\mathrm{k}\Omega \times 47\mathrm{nF}} = 1.7\mathrm{kHz}$$

In this way, f_z<f_c and the compensated zero can raise the phase margin around the crossover frequency.

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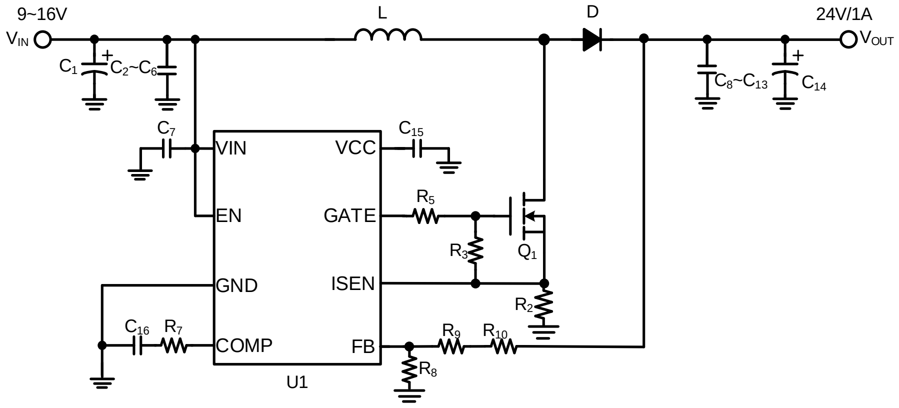
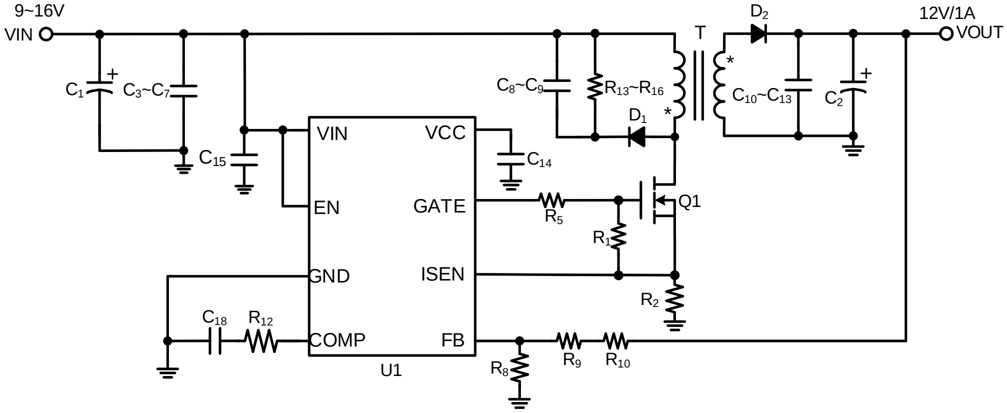
Boost Application Schematic (Typical V_{IN}=12V, V_{OUT}=24V, I_{OUT}=1A)



Boost BOM List

Reference Designator	Description	Part Number	Manufacturer
R_2	50mΩ, 1206		YAGEO
R_3, R_8	10kΩ, 0603		YAGEO
R_5	0Ω, 0603		YAGEO
R_7	2kΩ, 0603		YAGEO
R_9	91kΩ, 0603		YAGEO
R_{10}	100kΩ, 0603		YAGEO
C_1, C_{14}	E-Cap 47μF, 80V	EEHZC1K470P	Panasonic
C_2~C_6, C_8~C_{13}	Cap 10μF, 50V, 1206	GCM31CD71H106KE36L	Murata
C_7	Cap 100nF, 50V, 0603	GCM188R71H104KA57D	Murata
C_{15}	Cap 1μF, 25V, 0603	GCM188R71E105MA64D	Murata
C_{16}	Cap 47nF, 50V, 0603	GCM188R71H473KA55D	Murata
L	Inductor 47μH	SLF12575T-470M	TDK
D	SMT Schottky	SS310	CJ
Q_1	SMT MOSFET	BSC0804LSATMA1	Infineon
U	Controller	SA22300	Silergy

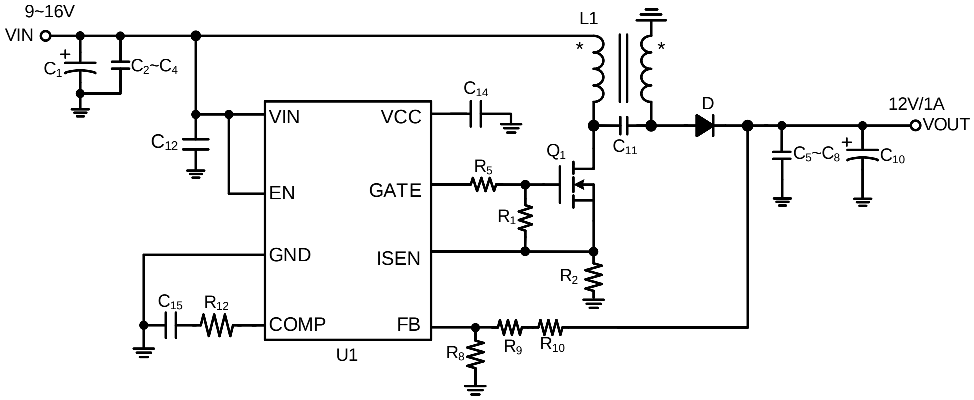
Flyback Application Schematic (Typical V_{IN}=12V, V_{OUT}=12V, I_{OUT}=1A)



Flyback BOM List

Reference Designator	Description	Part Number	Manufacturer
R_5	Res 0Ω, 0603		YAGEO
R_2	Res 50mΩ, 1206		YAGEO
R_1, R_8	Res 10kΩ, 0603		YAGEO
R_{13}~R_{16}	Res 6.8kΩ, 1206		YAGEO
R_{12}	Res 3.9kΩ, 0603		YAGEO
R_9	Res 15kΩ, 0603		YAGEO
R_{10}	Res 75kΩ, 0603		YAGEO
C_1, C_2	E-cap 47μF, 80V	EEHZC1K470P	Panasonic
C_3~C_7, C_{10}~C_{13}	Cap 10μF, 50V, 1206	GCM31CD71H106KE36L	Murata
C_8, C_9	Cap 47nF, 250V, 1206	GCJ31CR72E473KXJ3L	Murata
C_{18}	Cap 47nF, 50V, 0603	GCM188R91H473KA37D	Murata
C_{15}	Cap 100nF, 50V, 0603	GCM188R71H104KA57D	Murata
C_{14}	Cap 1μF, 25V, 0603	GCM188R71E105MA64D	Murata
T	Transformer L=9μH	750313443	Wurth
D_1, D_2	SMT Schottky, 100V, 3A	SS310	CJ
Q_1	SMT MOSFET, 100V, 40A	BSC0804LSATMA1	Infineon
U_1	Controller	SA22300	Silergy

Sepic Application Schematic (Typical V_{IN}=12V, V_{OUT}=12V, I_{OUT}=1A)



Sepic BOM List

Reference Designator	Description	Part Number	Manufacturer
R_5	Res 0Ω, 0603		YAGEO
R_2	Res 50mΩ, 1206		YAGEO
R_1, R_8	Res 10kΩ, 0603		YAGEO
R_{12}	Res 3.9kΩ, 0603		YAGEO
R_9	Res 15kΩ, 0603		YAGEO
R_{10}	Res 75kΩ, 0603		YAGEO
C_1, C_{10}	E-cap 47μF, 80V	EEHZC1K470P	Panasonic
C_2~C_4, C_5~C_8	Cap 10μF, 50V, 1206	GCM31CD71H106KE36L	Murata
C_{11}	Cap 4.7μF, 100V, 1210	GCM32DC72A475KE02L	Murata
C_{15}	Cap 47nF, 50V, 0603	GCM188R91H473KA37D	Murata
C_{12}	Cap 100nF, 50V, 0603	GCM188R71H104KA57D	Murata
C_{14}	Cap 1μF, 25V, 0603	GCM188R71E105MA64D	Murata
L_1	Coupled Inductor 22μH	7448709220	Wurth
D	SMT Schottky, 60V, 10A	PMEG060V100EPDZ	NXP
Q_1	SMT MOSFET, 100V, 40A	BSC0804LSATMA1	Infineon
U_1	Controller	SA22300	Silergy

Layout Design

The layout design of the SA22300 is relatively simple. For the best efficiency and minimum noise problem, the following components should be placed close to the IC: C_{in}, C_{VCC}, R_1, C_1, R_2, R_3.

- Maximize the PCB copper area connected to the GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable. Place some vias in GND copper for heat sinking too.
- C_{in} must be close to Pins VIN and GND. The loop area formed by C_{in} and GND must be minimized.
- Minimize the PCB copper area LX-V_{OUT}-GND-LX to avoid the potential noise problem.
- To avoid the noise problem, ensure that the feedback components R2 and R3 and the trace connecting to the FB pin are not adjacent to the LX net on the PCB layout.
- The feedback sampling point should be connected with C_{OUT}.
- If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the VIN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1MΩ resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

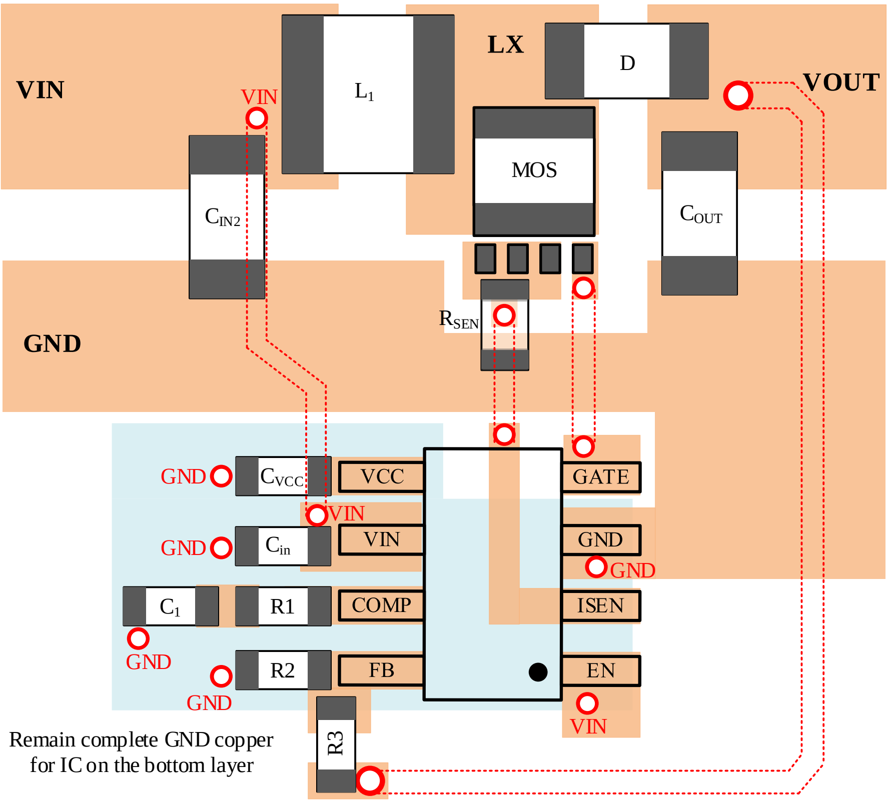
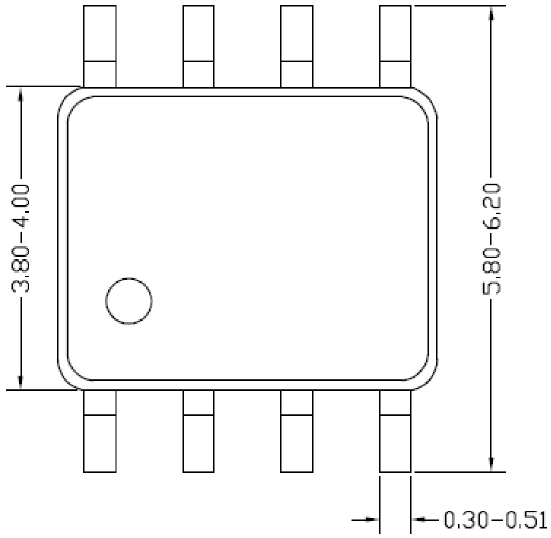
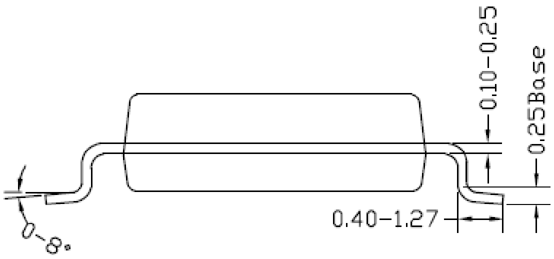


Figure 15. Layout Design

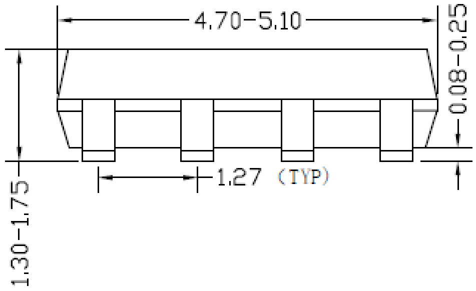
SOP8 Package Outline and PCB Layout Design



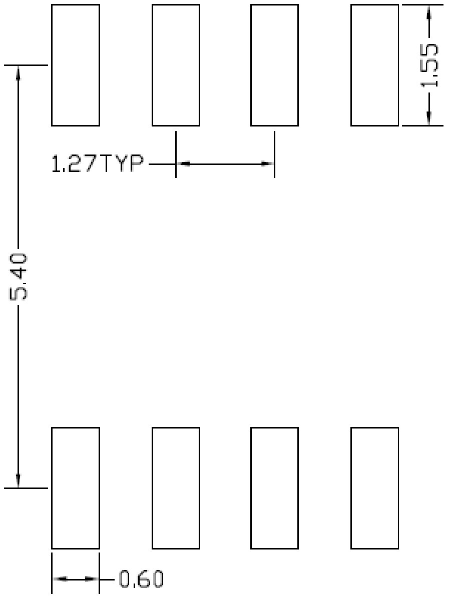
Top view



Side view



Front view



Recommended Pad Layout (Reference only)

Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

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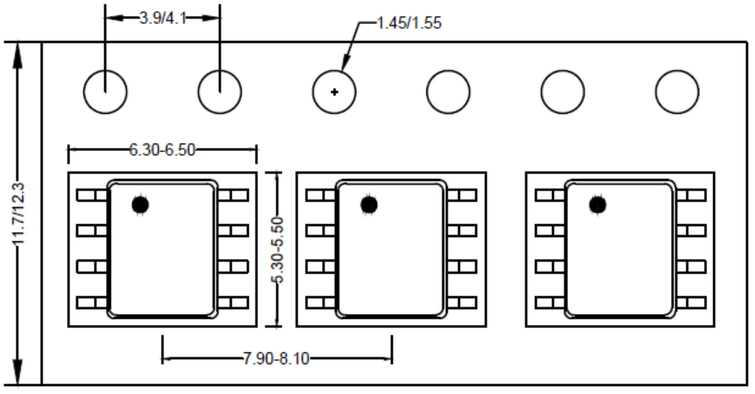
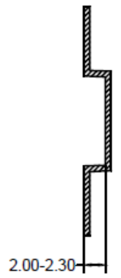
Taping & Reel Specification

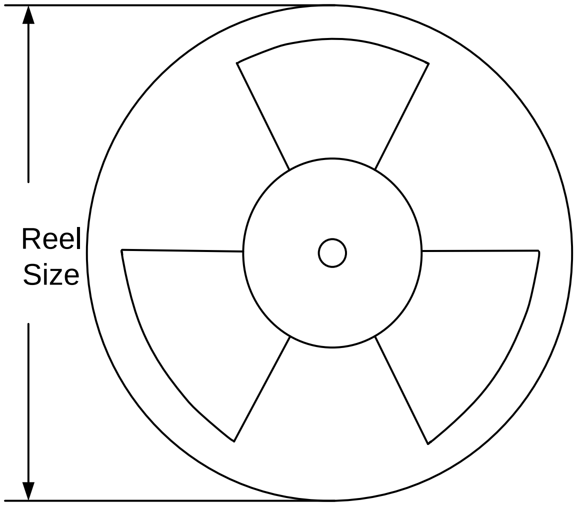
Taping Orientation





Feeding direction →

Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOP8	12	8	13"	400	400	2500

Others: NA

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Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change	Pages changed
Oct. 17, 2023	Revision 0.9	Initial Release.	-
Aug. 01, 2024	Revision 1.0	Update Output Typical Performance Characteristics of over current protection, ISEN open protection, FB short protection.	6

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