SY7T610E

Energy Measurement IC With Integrated Oscillator

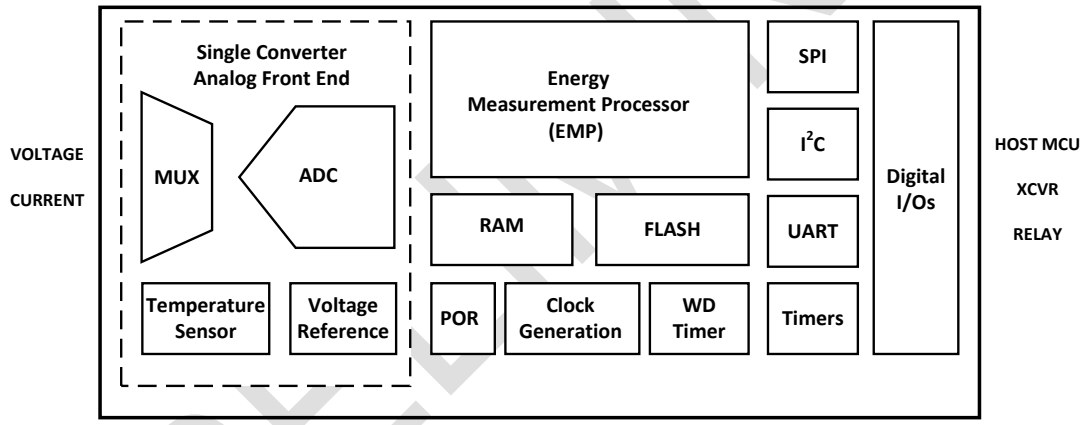
General Description

The SY7T610E is an energy measurement processor (EMP) designed specifically for BOM optimized applications, requiring measurements in single-phase systems (2 or 3 wires) and two-phase (i.e. Japan). The device features SPI, I^2C and UART interfaces. The UART allows for low baud rates to further lower isolation costs.

The analog front end (AFE) provides three differential analog inputs for interfacing to current sensors and voltage sensors respectively. Scaled voltages from the sensors are fed to a high-resolution delta-sigma converter. A low Power Energy Measurement Processor (EMP) with embedded firmware performs all the necessary computation, compensation, and data formatting for interfacing to any host controller. With integrated flash memory for storing nonvolatile data such as calibration coefficients and input configuration settings, the SY7T610E provides an autonomous solution that simplifies system integration.

Features

- High resolution Delta-Sigma ADC with two analog (sensor) inputs
- Precision internal voltage and timing references minimize external components
- Energy Measurement Processor with nonvolatile storage of calibration and configuration data
- Extended Temperature Range -40°C to 105°C
- Flexible SPI, UART, I^2C, or PWM interface options with configurable DIO for alarm signaling, address pins, or user control
- Small 16-pin TSSOP package



Ordering Information

Ordering Number	Carrier Type	Temperature Range	Package	Top Marking	Firmware Revision
SY7T610E B [1)]	Tray (Bulk)	-40°C to +105°C	TSSOP-16	SY7T610E	None
SY7T610E T [1)]	Tape & Reel				

Notes:

1) Ordering Numbers for pre-programmed devices with firmware include a '+' character followed by one or more alphanumeric characters (Example: SY7T610EB+ABC123 for ABC123 firmware shipped in bulk). To support re-programmability, the top marking is the same for both all programmed and unprogrammed ordering options. Material traceability is digitally maintained within the device.

Pinout

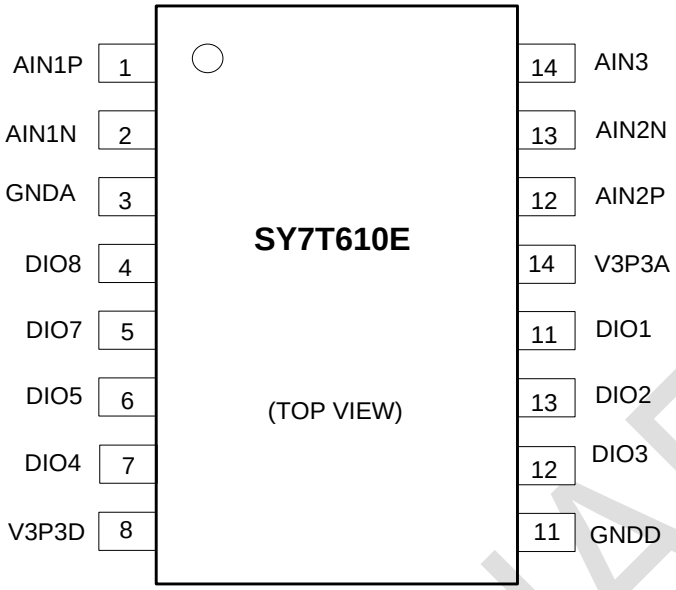


Table 1. SY7T610E Pin Description/Assignment

Pin	Name	Description
1	AIN1P	Analog Input 1 (Positive)
2	AIN1N	Analog Input 1 (Negative)
3	GNDA	Ground pin (Analog)
4	DIO8	Interface Select, and Digital I/O. Pin is sampled upon reset to select the serial interface.
5	DIO7	Digital I/O
6	DIO5	SPI SSB, I^2C SCL, or Digital I/O
7	DIO4	Digital I/O
8	V3P3D	3.3VDC Supply (Digital)
9	GNDD	GROUND (Digital)
10	DIO3	SPI MISO, UART TX, or I^2C SDAo (Data Out)
11	DIO2	SPI MOSI, UART RX, or I^2C SDAi (Data In)
12	DIO1	SPI SCK or Digital I/O
13	V3P3A	3.3VDC Supply (Analog)
14	AIN2P	Analog Input 2 (Positive)
15	AIN2N	Analog Input 2 (Negative)
16	AIN3	Analog Input 3 (Single-End)

Notes:

DIO8 is sampled at power-on or reset to determine the selection of SPI (DIO8 = low) or UART/I^2C (DIO8 = high). The selection of I^2C or UART is determined by the FW.

Block Diagram

The SY7T610E integrates all the functional hardware blocks required for power, energy measurement and auxiliary measurements such as harmonics and THD. Only a few external resistors and capacitors are required. Included on the device are:

- Temperature compensated oscillator and clock management logic
- Integrated power-on reset and watchdog timer
- High-accuracy analog front-end (AFE) with trimmed voltage reference and temperature sensor
- Energy Measurement Processor with RAM and flash memory
- Peripheral interfaces (UART, I2C or SPI) with Digital I/O and PWM outputs

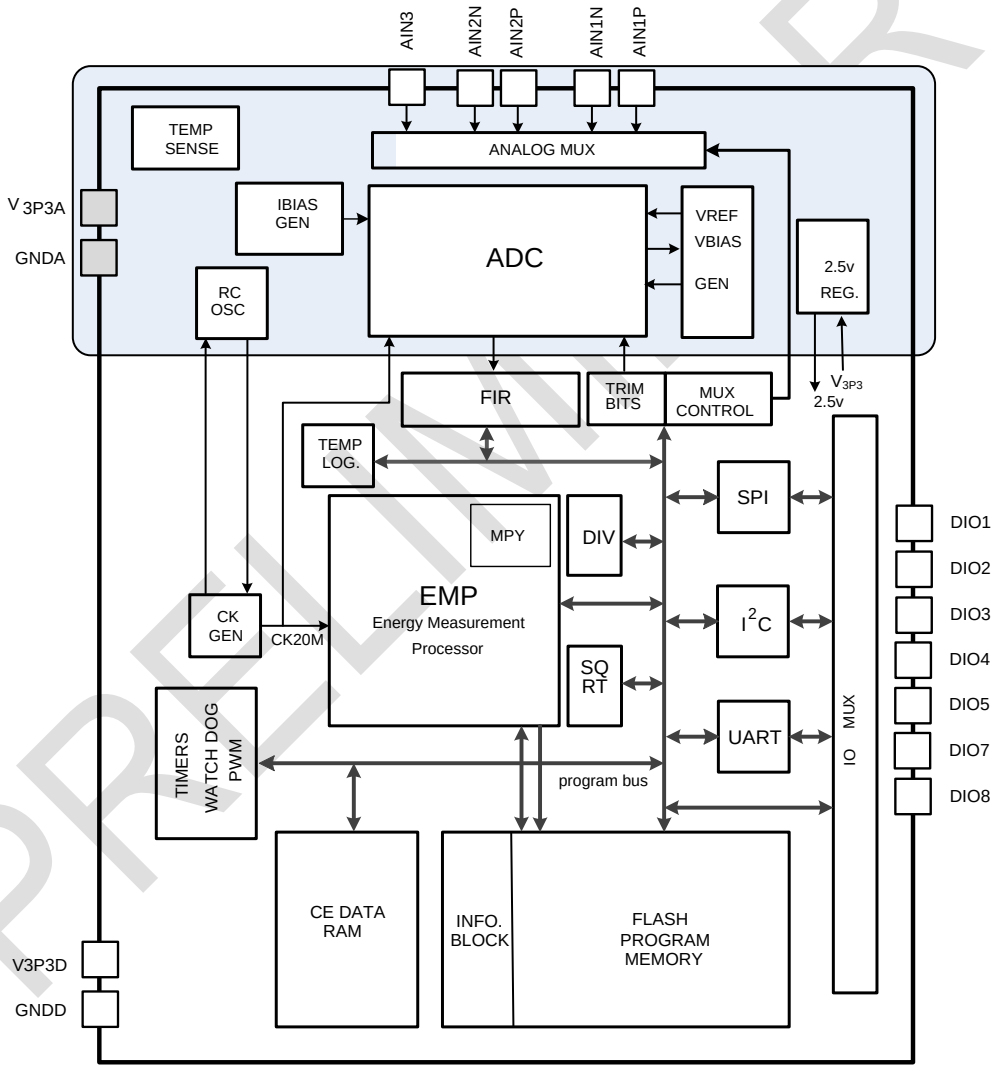


Figure 1. SY7T610E Functional Block Diagram

Electrical Specifications

Absolute Maximum Ratings

Supplies and Ground Pins:	
V_{3P3D}, V_{3P3A}	-0.5V to 4.6V
GNDD, GNDA	-0.5V to +0.5V
Analog Input Pins:	
AIN1P, ANI1N, AIN2P, ANI2N AIN3	-10mA to +10mA -0.5V to (V_{3P3} + 0.5V)
Digital Pins:	
DIO1, DIO2, DIO3, DIO4, DIO5, DIO7, DIO8	-30mA to +30mA, -0.5V to (V_{3P3D}+ 0.5V)
Temperatures:	
Operating Junction Temperature (peak, 100ms)	+140°C
Operating Junction Temperature (continuous)	+125°C
Storage Temperature	-45°C to +165°C
Soldering Temperature (10-second duration)	+250°C
ESD Stress on All Pins	±4kV

Stresses beyond Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND.

Recommended Operating Conditions

Parameter	Condition	Min	Typ	Max	Unit
3.3V Supply Voltage (V_{3P3})	Normal Operation	3.0	3.3	3.6	V
Operating Temperature		-40	–	+105	ºC

Performance Specifications

Production tests are performed at room temperature.

Input Logic Levels

Parameter	Condition	Min	Typ	Max	Unit
Digital high-level input voltage, V_{IH}		2	–	–	V
Digital low-level input voltage, V_{IL}		–	–	0.8	V

Output Logic Levels

Parameter	Condition	Min	Typ	Max	Unit
Digital high-level output voltage V_{OH}	I_{LOAD} = 1 mA	V_{3P3} –0.4	–	–	V
	I_{LOAD} = 10 mA	V_{3P3}-0.6	–	–	V
Digital low-level output voltage V_{OL}	I_{LOAD} = 1 mA	0	–	0.4	V
	I_{LOAD} = 10 mA	–	–	0.5	V

Supply Current

Parameter	Condition	Min	Typ	Max	Unit
V_{3P3D} and V_{3P3A} current (compounded)	Normal Operation, V3P=3.3V	–	8.1	10.3	mA

Internal RC Oscillator

Parameter	Condition	Min	Typ	Max	Unit
Nominal Frequency	V3P=3.3V, 25ºC	–	20.000	–	MHz
Accuracy	V3P=3.3V, -40ºC to +85ºC	–	±1.5	–	%
Accuracy	V3P=3.3V, -40ºC to +105ºC	–	±2.0	–	%

ADC Converter (V3P3 Referenced)

LSB values do not include the 9-bit left shift at processor input.

Parameter	Condition	Min	Typ	Max	Unit
Usable Input Range (AINxP-AINxN), (AIN3-V_{3P3})		-250	–	250	mV peak
THD (First 10 harmonics)	Vin=65Hz, 64kpts FFT, Blackman-Harris window	–	-85	–	dB
Input Impedance	Vin=65Hz	30	–	90	kΩ
Temperature coefficient of Input Impedance	Vin=65Hz	–	1.7[1]	–	Ω/°C
ADC Gain Error vs %Power Supply Variation $\frac{10^6\,\Delta Nout_{PK}\;357nV/V_{IN}}{100\,\Delta V3P3A/3.3}$	Vin=200mVpk, 65Hz V_{3P3}=3.0V, 3.6V	–	–	50	ppm/%
Input Offset (Vin-V_{3P3})		-10		10	mV

[1] Guaranteed by design, not subject to test.

Timing Specifications

SPI Slave Port

Parameter		Condition	Min	Typ	Max	Unit
t_{SPIcyc}	SPCK cycle time		1	–	–	μs
$t_{SPILead}$	Enable lead time		15	–	–	ns
t_{SPILag}	Enable lag time		0	–	–	ns
t_{SPIW}	SPCK pulse width: High Low		 250 250	 –	 –	 ns ns
t_{SPISCK}	SSB to first SPCK fall	Ignore if SPCK is low when SSB falls.	–	2[1]	–	ns
t_{SPIDIS}	Disable time		–	0[1]	–	ns
t_{SPIEV}	SPCK to Data Out (MISO)			–	25	ns
t_{SPISU}	Data input setup time (MOSI)		10	–	–	ns
t_{SPIH}	Data input hold time (MOSI)		5	–	–	ns

Notes:

1) Guaranteed by design, not subject to test.

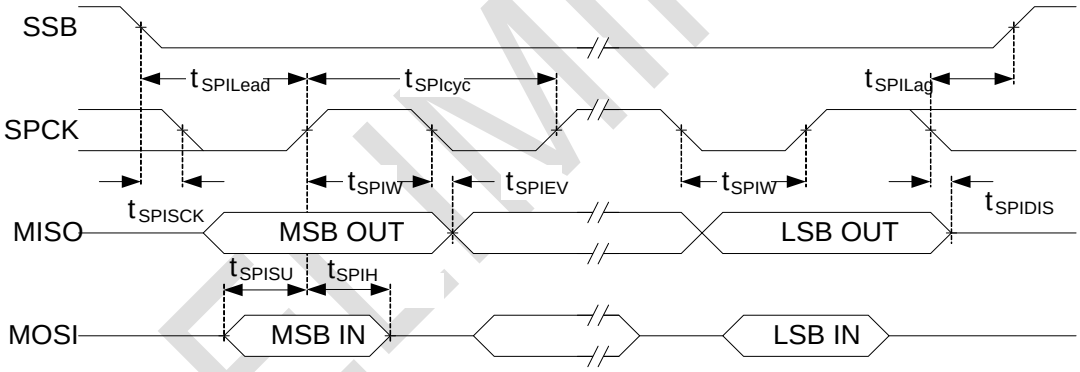


Figure 2. SPI Slave Port Timing

I2C Slave Port

I²C Slave Port Timing[2]

Parameter	Condition	Min	Typ	Max	Unit
t_{BUF} Bus Idle (Free) time between transmissions (STOP/START)		1500	-	–	ns
t_{ICF} I²C input Fall Time		20[1]	–	300	ns
t_{ICR} I²C input Rise Time		20[1]	–	300	ns
t_{STH} I²C START or repeated START condition hold time		500	–	–	ns
t_{STS} I²C START or repeated START condition setup time		600	–	–	ns
t_{SCH} I²C clock high time		600	–	–	ns
t_{SCL} I²C clock low time		1300	–	–	ns
t_{SDS} I²C serial data setup time		100	–	–	ns
t_{SDH} I²C serial data hold time		10	–	–	ns
t_{VDA} I²C Valid data time: - SCL low to SDA output valid - ACK signal from SCL low to SDA (out) low		–	–	900	ns

Notes:

[1] Dependent on bus capacitance.

[2] Guaranteed by design, not subject to test.

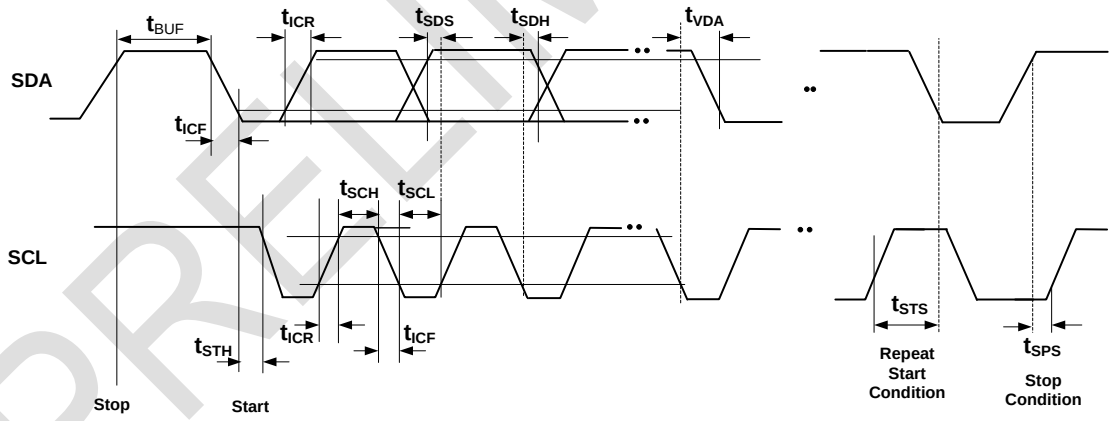


Figure 3. I²C Port Timing

Hardware Resources Overview

Power-On Reset (POR)

An on-chip Power-On Reset (POR) block monitors the supply voltage (V_{3P3D}) and initializes the internal digital circuitry at power-on. Once V_{3P3D} is above the minimum operating threshold, the POR circuit triggers and initiates a reset sequence. It will also issue a reset to the digital circuitry if the supply voltage falls below the minimum operating level.

Watchdog Timer (WDT)

A Watchdog Timer (WDT) block detects any software processing errors. The embedded software periodically refreshes the free-running watchdog timer to prevent it from timing out. If the WDT times out, it is an indication that software is no longer being executed in the intended sequence; thus, a system reset is initiated.

Internal Oscillator

The internal RC oscillator is factory-trimmed and temperature-compensated. It provides an accurate clock source for all the internal logic and analog circuitry. For applications requiring highest accuracy of the time-based measurements (i.e. line frequency, energy, etc.), the use of a device of the same family (SY7T60x/SY7T60xE), with provision for external crystal is recommended.

Analog Front-End and Conversion

The SY7T610E's Analog Front-End (AFE) includes an input multiplexer, delta-sigma A/D converter, voltage reference, bias current reference, temperature sensor, voltage fault comparators, and POR circuitry.

Delta-Sigma A/D Converter

A second-order delta-sigma converter digitizes the analog inputs. The converted data is then filtered and decimated through a FIR filter.

Voltage Reference

The device includes an on-chip precision bandgap voltage reference that incorporates auto-zero techniques as well as production trims to minimize errors caused by component mismatch and drift. The voltage reference is digitally compensated over temperature.

Die Temperature Measurement

The device includes an on-chip die temperature sensor used for digital compensation of the voltage reference. It is also used to report temperature information to the user.

Voltage and Current Inputs

The external voltage and current sensors are connected to analog input pins. The full-scale signal level that can be applied to the voltage input pins is V3P3A ±250 mVpk. With a sinusoidal waveform, the maximum RMS voltage is:

$$Vrms(Max) = \frac{250\text{mVpk}}{\sqrt[2]{2}}$$

A common-mode voltage of less than ±25 mV is recommended in order to fully utilize the available dynamic range.

Energy Measurement Processor

The SY7T610E integrates a dedicated processor that performs all the digital signal processing necessary for measurement, calibration, compensation, analysis, alarms generation, relay control, etc.

Flash and RAM

The SY7T610E includes on-chip flash memory for storing program code, coefficients, calibration data, and configuration settings. The SY7T610E also includes on-chip RAM which is used to store the values of input and output registers and utilized by the firmware for its operations.

Digital I/O

The SY7T610E features 7 general purpose digital I/O. The digital I/O are either managed directly by the user, by the embedded firmware, or multiplexed with the serial communication interfaces. The device also includes the necessary hardware to generate free-running PWM signals at either DIO7 or DIO8 with configurable period and pulse width. The following table summarizes the multiplexing and pin assignment on the SY7T610E.

Table 2. Digital I/O Assignments

Pin Name	Pin #	Function at Power-On	Function by Interface		
			SPI	UART	I²C
DIO8	4	Interface Selection	DIO8		
DIO7	5	--	DIO7		
DIO5	6	--	SSB	DIO5	SCL
DIO4	7	--	DIO4		
DIO3	10	--	MISO	TX	SDAo
DIO2	11	--	MOSI	RX	SDAi
DIO1	12	--	SCK	DIO1	

Notes:

1) Digital I/O's can be configured to specific function by the FW.

Warning: Where applicable, pins should be configured via pull-up and pull-down resistors as these pins could become outputs after initialization. Therefore, direct connection to GNDD/GNDA or V3P3D/V3P3A supplies must be avoided.

Serial Interfaces

The SY7T610E provides UART, I²C, and SPI interface options. Since the digital I/O pins are shared, only one interface can be active at a time. In the SY7T610E, pin DIO8 is sampled following a power-on or reset to select between SPI or UART/I2C interface.
The selection between UART and I²C is determined by the FW.
The user should allow at least 10ms from a power-on reset event for the selection pin status to be latched and the serial interface selected. During this time the status of DIO8 must not change.

Selected Interface	DIO8
SPI	**0**
UART Or **I²C**	**1**

UART Interface

The SY7T610E features a UART interface with a data rate ranging from 2400 up to 115k Baud. The UART interface has a fixed configuration supporting: 8-bit, one start bit, one stop bit and no-parity. The UART interface hardware does not provide handshaking hardware signals (i.e. RTS, CTS etc.).
Once the UART interface is activated, it utilizes the following digital I/Os:

- **DIO3**: Transmit (TX) output
- **DIO2**: Receive (RX) input.

The UART clock is derived from the 20MHz system clock. The error due to the clock division is reported in the following Table.

Table 3. UART Baud Rate Error

Baud Rate	Actual Baud Rate	Error [percent]
2400	2399.808	0.008
4800	4800.768	0.016
9600	9596.929	-0.032
19200	19193.858	-0.032
38400	38461.538	0.160
57600	57541.264	-0.223
115200	114942.529	-0.223

SPI Interface

The SPI featured in the SY7T610E is slave-only. Once the SPI interface is activated, it utilizes the following digital I/O as the SPI interface:

- **DIO5**: Slave select (SSB) is an active low input.
- **DIO1**: Serial Data Clock (SCK) input.
- **DIO3**: Master Input, Slave Output (MISO), serial data output.
- **DIO2**: Master Output, Slave Input (MOSI), serial data input.

The SPI interface allows read and write accesses to the data RAM specified in the command bit field ADDR[5:0]. The command limits the access to RAM locations 0x00 through 0x3F. Refer to the **Error! Reference source not found.** section for details on accessing other RAM locations.

SPI Mode

The device operates in mode 3 (CPOL=1, CPHA=1) and as such the data is captured on the rising edge and propagated on the falling edge of the serial data clock (SCK). The figure below shows a single-byte transaction on the SPI bus. Bytes are transmitted/received MSB first.

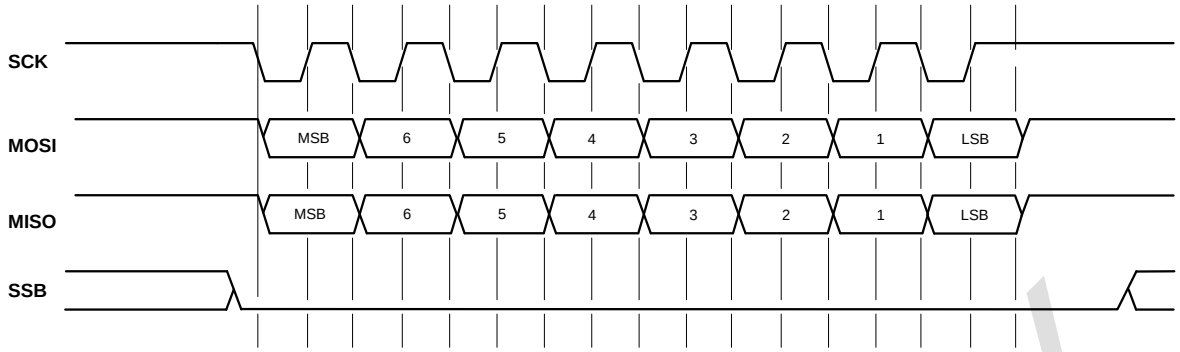


Figure 4. Signal Timing on the SPI Bus (Single Byte Transaction)

Single Word SPI Reads

The device supplies direct read access to the device RAM memory. To read the RAM the master device must send a read command to the slave device and then clock out the resulting read data. SSB must be kept active low for the entire read transaction (command and response). SCK may be interrupted as long as SSB remains low. ADDR[5:0] is filled with the word address of the read transaction. RAM data contents are transmitted most significant byte first. ADDR[5:0] cannot exceed 0x3F. RAM words, and therefore the results, are natively 24 bits (3 bytes) long.

Table 4: Single-Word Read Command (MOSI)

Byte #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0		ADDR[5:0]					0x0	
1		0						
2		0						
3		0						

The slave responds with the data contents of the requested RAM addresses.

Table 5: Single-Word Read Response (MISO)

Byte #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Hi-Z (during Read Command)							
1	DATA[23:16] @ ADDR							
2	DATA[15:8] @ ADDR							
3	DATA[7:0] @ ADDR							

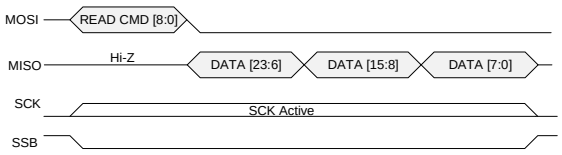


Figure 5. Single Word Read Access Timing

Single Word SPI Writes

The device supplies direct write access to the device RAM memory. To write the RAM the master device must send a write command to the slave device and then clock out the write data. SSB must be kept active low for the entire write transaction (command and data). SCK may be interrupted as long as SSB remains low. ADDR[5:0] is filled with the word address of the write transaction. RAM data contents are transmitted most significant byte first. ADDR[5:0] cannot exceed 0x3F. RAM words are natively 24 bits (3 bytes) long.

Table 6: Single-Word Write Command (MOSI)

Byte #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	ADDR[5:0]						0x02	
1	DATA[23:16] @ ADDR							
2	DATA[15:8] @ ADDR							
3	DATA[7:0] @ ADDR							

The slave SDO remains Hi-Z during a write access.

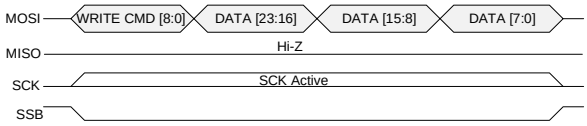


Figure 6. Single Word Write Access Timing

I2C Interface

The SY7T610E features an I²C interface available at the DIO2, DIO3, and DIO5 pins. The interface supports I²C slave mode with a 7-bit address and operates at a data rate up to 400kHz (Fast-mode). The SY7T610Ehas separate SD (serial data) input and output pins to allow the use of opto-couplers to isolate the serial bus.

The figure below shows two possible configurations. Configuration A is the standard configuration. The double pin for SDA allows the isolated configuration B

The I²C interface allows access to read and write registers contained in a 256-word (24-bit) area of the on-chip RAM. The **Error! Reference source not found.** section contains the address and assignment of each register.

Bus Characteristics

- A data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

.

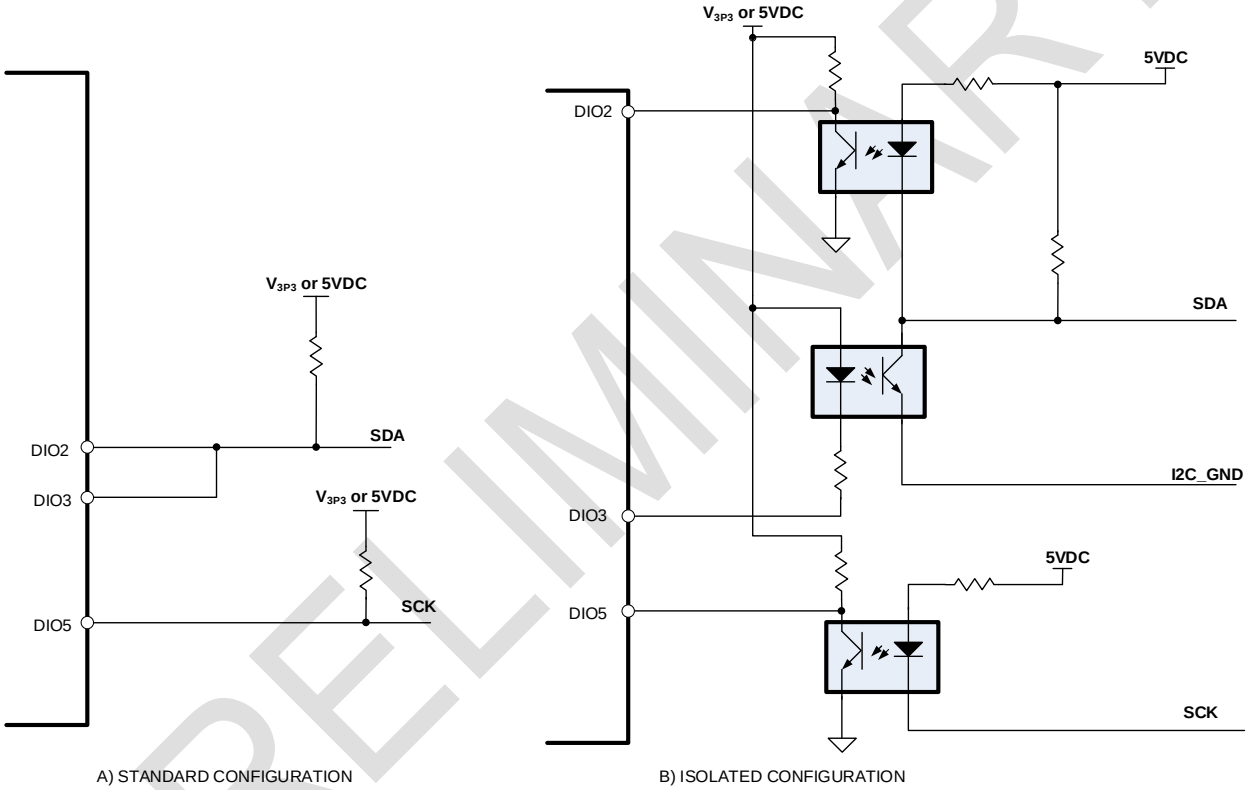


Figure 7: I2C Bus Connection in Standard (A) and Isolated (B) Configuration

Bus Conditions

- **Bus not Busy (I):** Both data and clock lines are HIGH indicating an Idle Condition.
- **Start Data Transfer (S):** a HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.
- **Stop Data Transfer (P):** a LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.
- **Data Valid:** The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition.

- **Acknowledge (A):** Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse, which is associated with this Acknowledge bit. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by not generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave SY7T610Ewill leave the data line HIGH to enable the master to generate the STOP condition

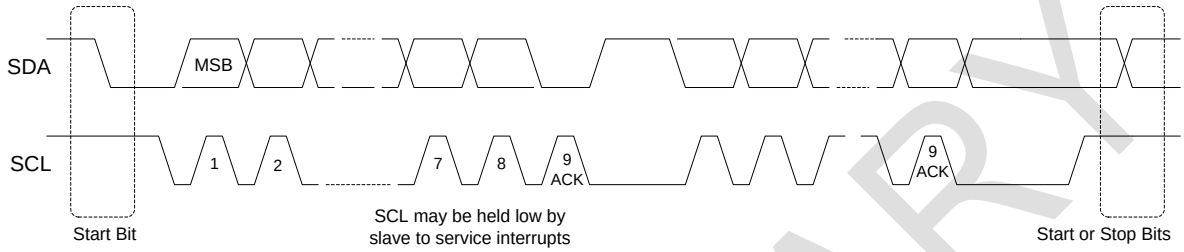
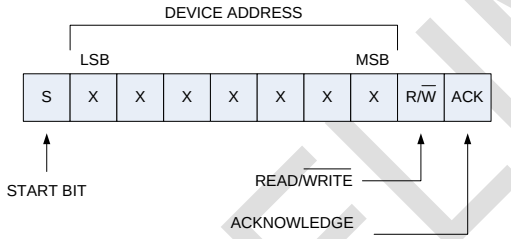


Figure 8: I2C Bus Conditions

Device Addressing

A control byte is the first byte received following the START condition from the master device.
The control byte consists of a seven-bit address and a bit (LSB) indicating the type of access (0=write; 1=read).



Write Operations

Following the START (S) condition from the master, the device address (7-bits) and the R/W bit (logic low for write) are clocked onto the bus by the master. This indicates to the addressed slave receiver that the register address will follow after it has generated an acknowledge bit (A) during the ninth clock cycle. Therefore, the next byte transmitted by the master is the register address and will be written into the address pointer of the SY7T611. After receiving another acknowledge (A) signal from the SY7T611, the master device will transmit the data byte(s) to be written into the addressed memory location. The data transfer ends when the master generates a STOP (P) condition. This initiates the internal write cycle. The example in Figure 9 shows a 3-byte data write (24-bit register write).

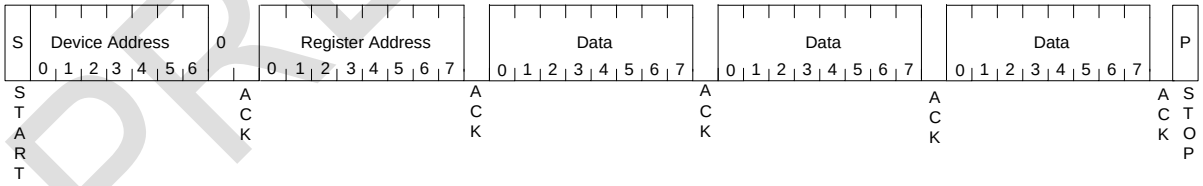


Figure 9: I2C Bus 3-byte Data Write

Upon receiving a STOP (P) condition, the internal register address pointer will be incremented.
The write access can be extended to multiple sequential registers.

The figure below shows a transaction where multiple registers are written sequentially.

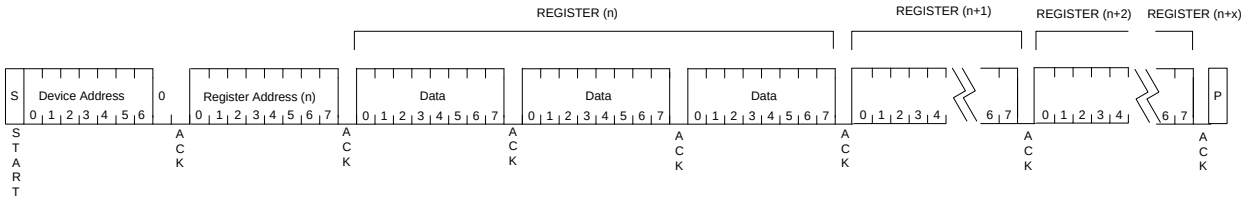


Figure 10: I2C Bus Multiple Sequential Register Write

Read Operations

Read operations are initiated in the same way as write operations with the exception that the R/W bit of the control byte is set to one. There are two basic types of read operations: current address read and random read.

Current Address Read: the SY7T610E contains an address counter that maintains the address of the last register accessed, internally incremented by one when the STOP bit is received. Therefore, if the previous read access was to register address n, the next current address read operation would access data from address n + 1.

Upon receipt of the control byte with R/W bit set to one, the SY7T610E issues an acknowledge (A) and transmits the eight-bit data byte. The master will not acknowledge the transfer, but generates a STOP condition to end the transfer and the SY7T610E will discontinue the transmission.

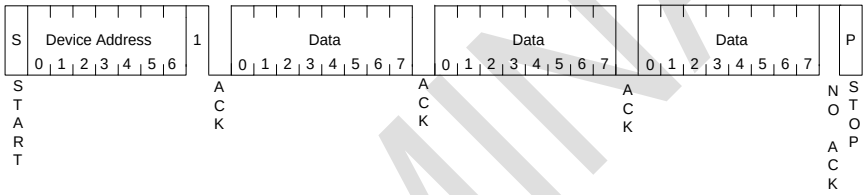
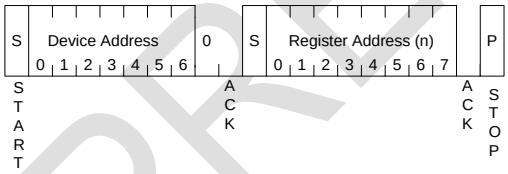


Figure 11: I2C Bus 3-byte Data Read

This read operation is not limited to 3 bytes but can be extended until the register address pointer reaches its maximum value.

If the register address pointer has not been set by previous operations, it is necessary to set it issuing a command as follows:



Random Read Operations

Random read operations allow the master to access any register in a random manner. To perform this operation, the register address must be set as part of the write operation. After the address is sent, the master generates a START condition following the acknowledge response. This sequence completes the write operation. The master should issue the control byte again this time, with the R/W bit set to 1 to indicate a read operation. The SY7T610Ewill issue the acknowledge response and transmit the data.

At the end of the transaction the master will not acknowledge the transfer and generate a STOP condition. Random read operations are not limited to 3 bytes but can be extended until the register address pointer reaches its maximum value.

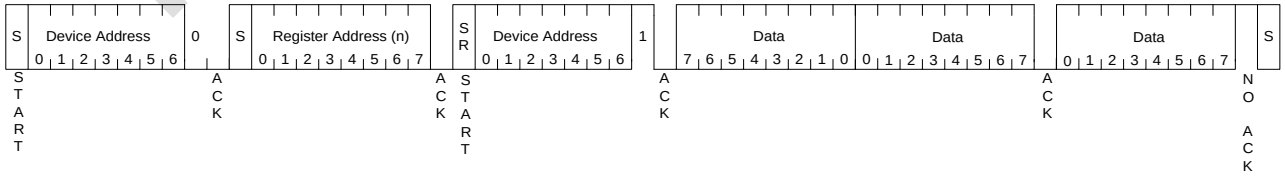
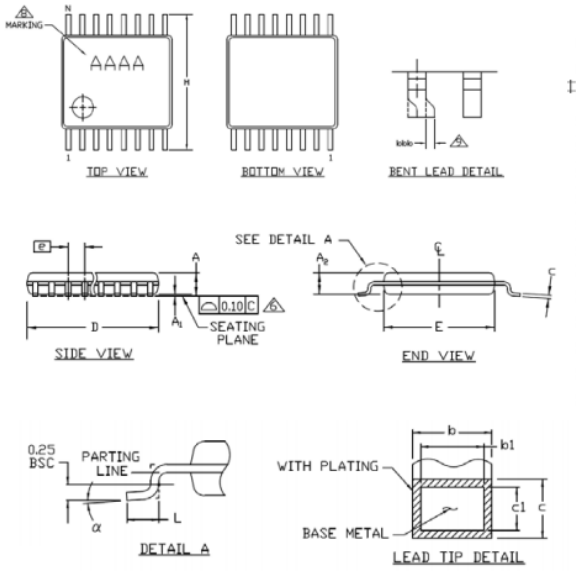


Figure 12: I2C Bus 3-byte Random Data Read

Functional (Firmware) Description

This datasheet only contains a description of the various on-chip hardware resources, electrical specifications, mechanical specifications, and ordering numbers.

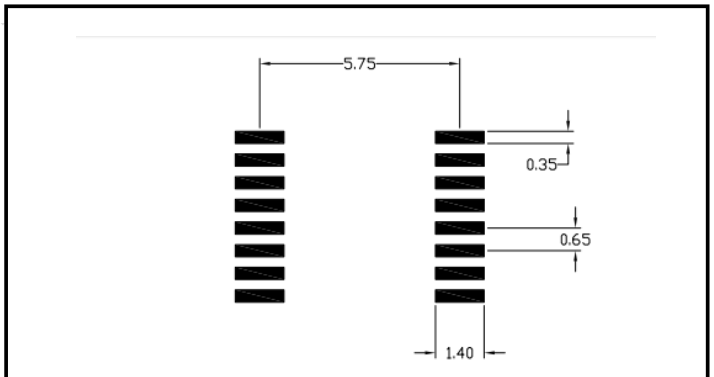
Packaging



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	4.90	5.10	.193	.201
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	0.10 MAX			

NOTES
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. LEAD COPLANARITY 0.10 MM MAX.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY
9. BENT LEAD 0.10 MM MAX.
10. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC # 10-0131.
11. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PBFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

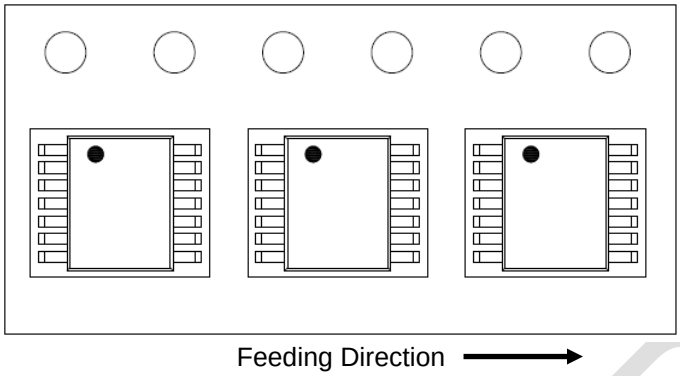


NOTES:

1. LAND PATTERN COMPLIES TO: IPC7351A.
2. TOLERANCE: +/- 0.02 MM.
3. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.
4. ALL DIMENSIONS IN MM.

-DRAWING NOT TO SCALE-

Tape & Reel Orientation



Contact Information

For more information about the SY7T609, contact support.em@silergy.com

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0.0	11/16/22	Initial Release	--

IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.

2. Applications. Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.

3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.

4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

5. **Terms and conditions of commercial sale**. Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at http://www.silergy.com/stdterms, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.

6. **No offer to sell or license**. Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com