SY7T612E

Energy Measurement IC

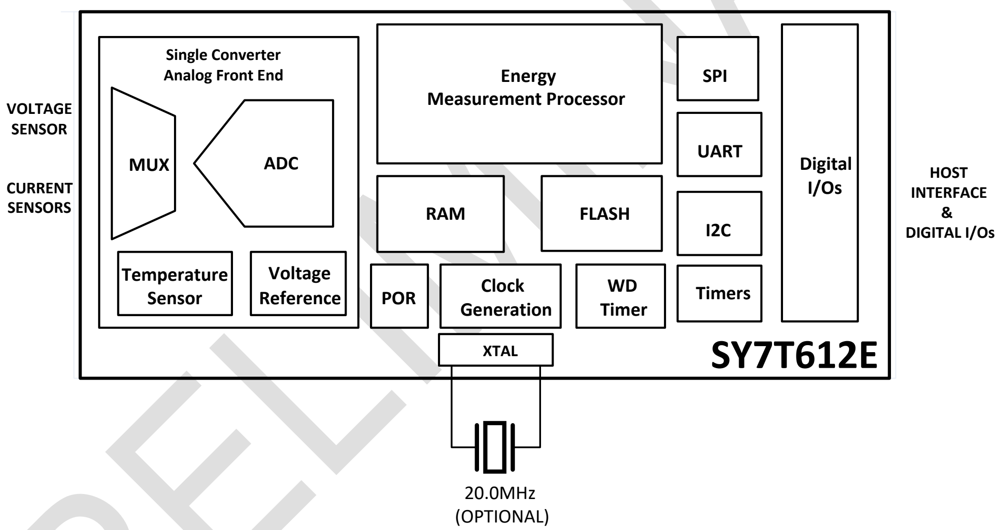
General Description

The SY7T612 is an energy measurement processor (EMP), in a 32QFN package, designed specifically for BOM optimized applications. It suited for accurate measurement and power quality analysis in single-phase (multiple branches) or polyphase systems.

The analog front end (AFE) provides configurable analog inputs for interfacing to current sensors and voltage sensors respectively. Scaled voltages from the sensors are fed to a high-resolution delta-sigma converter. A low power Energy Measurement Processor (EMP) performs the signal processing and data formatting for interfacing to any host controller. With integrated flash memory for storing nonvolatile data such as calibration coefficients and input configuration settings, the device provides an autonomous solution that simplifies system integration.

Features

- Small 32-pin QFN package
- High resolution delta-sigma ADC with four differential analog (ADC) inputs.
- Precision internal voltage and timing references minimize external components
- Energy Measurement Processor
- SPI, UART, I^2C host interface options
- configurable DIOs for alarm signaling, relay control, address pins, energy pulse output, or user control.
- Nonvolatile storage of calibration and configuration data
- Provision for optional external 20MHz crystal.



Ordering Information

Ordering Number	Carrier Type	Temperature Range	Package	Top Marking	Firmware Revision
SY7T612E B	Tray (Bulk)	-40°C to +105°C	TQFN-32	SY7T612E	None
SY7T612E T	Tape & Reel				

Notes:

1) Ordering Numbers for pre-programmed devices with firmware include a '+' character followed by one or more alphanumeric characters (Example: SY7T611B+ABC123 for ABC123 firmware shipped in bulk). To support re-programmability, the top marking is the same for both all programmed and unprogrammed ordering options. Material traceability is digitally maintained within the device.

Pinout

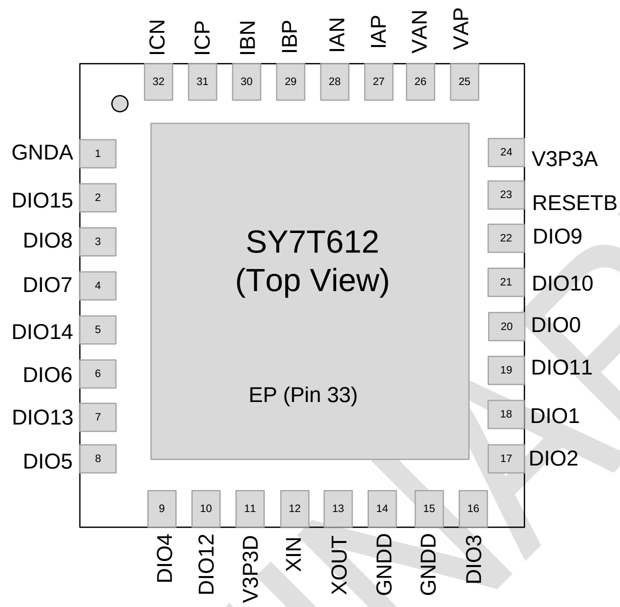


Table 1. SY7T612E Pin Description/Assignment

Pin Number	Pin Name	Pin Description / Assignment
1	GNDA	Ground (Analog)
2	DIO15	Digital I/O
3	DIO8	Digital I/O, Interface Select (1)
4	DIO7	Digital I/O
5	DIO14	Digital I/O
6	DIO6	Digital I/O, ADDRSEL0
7	DIO13	Digital I/O
8	DIO5	Digital I/O, SPI SSB, UART TXEN, SCL(1)
9	DIO12	Digital I/O
10	DIO4	Digital I/O
11	V3P3D	3.3VDC Supply (Digital)
12	XIN	Crystal Oscillator Input
13	XOUT	Crystal Oscillator Output
14	GNDD	Ground (Digital)
15	GNDD	Ground (Digital)
16	DIO3	Digital I/O, SPI MISO, UART TX, SDAo(1)
17	DIO2	Digital I/O, SPI MOSI, UART RX, SDAi(1)

Table 1 (Cont.). SY7T612E Pin Description

18	DIO1	Digital I/O, SPI SCK(1), ADDRSEL1
19	DIO11	Digital I/O
20	DIO0	Digital I/O
21	DIO10	Digital I/O
22	DIO9	Digital I/O
23	RESETB	Reset Input (Active Low)
24	V3P3A	3.3VDC Supply (Analog)
25	AIN1P	Analog Input 1 (positive)
26	AIN1N	Analog Input 1 (negative)
27	AIN2P	Analog Input 2 (positive)
28	AIN2N	Analog Input 2 (negative)
29	AIN3P	Analog Input 3 (positive)
30	AIN3N	Analog Input 3 (negative)
31	AIN4P	Analog Input 4 (positive)
32	AIN4N	Analog Input 4 (negative)
33	EP	Thermal Pad - Tie to GND (Optional) (2)

Notes:

1) DIO8 is sampled at power-on or reset to determine the selection of SPI (DIO8 = low) or UART/I^2C (DIO8 = high). The selection of I^2C or UART is determined by the FW

2) The exposed thermal pad is connected to the device substrate. It can be connected to GND, however it cannot be used to replace the GND connection. The GND must be connected through GNDD (digital) and GNDA (analog) ground pins.

Block Diagram

The SY7T612 hardware integrates all the functional blocks required for solid-state power and energy measurement. Only a few external resistors and capacitors are required. Included on the device are:

- Temperature compensated oscillator and clock management logic
- Integrated power-on reset and watchdog timer
- High-accuracy analog front-end (AFE) with trimmed voltage reference and temperature sensor
- 24-bit energy measurement processor with RAM and flash memory
- Peripheral interfaces (UART, I2C or SPI) and Digital I/O pins – *usage varies with firmware*

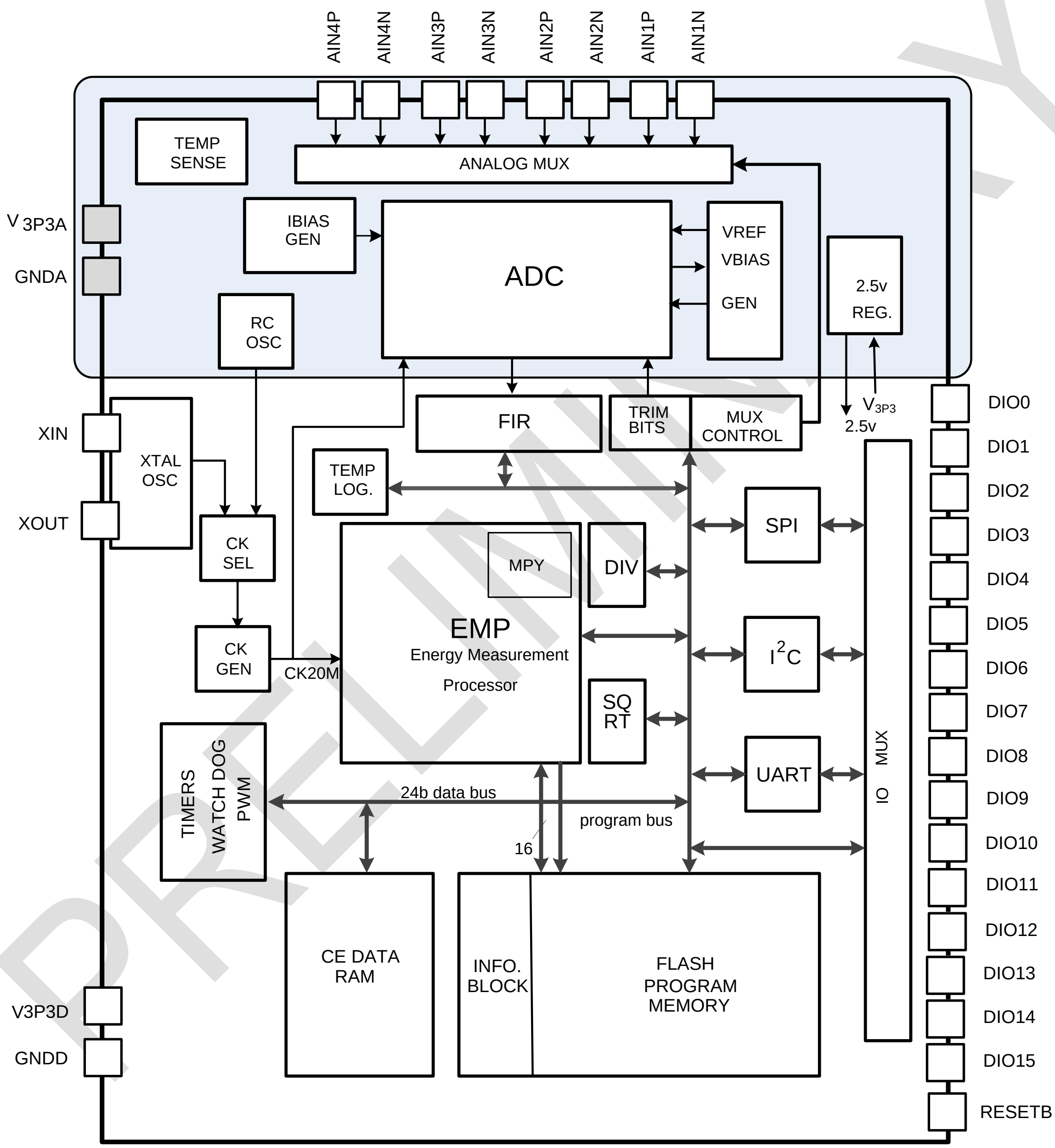


Figure 1. SY7T612E Functional Block Diagram

Electrical Specifications

Absolute Maximum Ratings

Supplies and Ground Pins:	
V_{3P3D}, V_{3P3A}	-0.5V to 4.6V
GNDD, GNDA	-0.5V to +0.5V
Analog Input Pins:	
AIN1N, AIN1P, AIN2N, AIN2P, AIN3N, AIN3P, AIN4N, AIN4P	-10mA to +10mA -0.5V to (V_{3P3} + 0.5V)
Digital Pins:	
DIO15, DIO14, DIO13, DIO12, DIO11, DIO10, DIO9, DIO8, DIO7, DIO6, DIO5, DIO4, DIO3, DIO2, DIO1, DIO0	-30mA to +30mA, -0.5V to (V_{3P3D}+ 0.5V)
Temperatures:	
Operating Junction Temperature (peak, 100ms)	+140°C
Operating Junction Temperature (continuous)	+125°C
Storage Temperature	-45°C to +165°C
Soldering Temperature (10-second duration)	+250°C
ESD Stress on All Pins	±4kV

Stresses beyond Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND.

Recommended Operating Conditions

Parameter	Condition	Min	Typ	Max	Unit
3.3V Supply Voltage (V_{3P3})	Normal Operation	3.0	3.3	3.6	V
Operating Temperature		-40	–	+105	ºC

Performance Specifications

Production tests are performed at room temperature.

Input Logic Levels

Parameter	Condition	Min	Typ	Max	Unit
Digital high-level input voltage, V_{IH}		2	–	–	V
Digital low-level input voltage, V_{IL}		–	–	0.8	V

Output Logic Levels

Parameter	Condition	Min	Typ	Max	Unit
Digital high-level output voltage V_{OH}	I_{LOAD} = 1 mA	V_{3P3} –0.4	–	–	V
	I_{LOAD} = 10 mA	V_{3P3}-0.6	–	–	V
Digital low-level output voltage V_{OL}	I_{LOAD} = 1 mA	0	–	0.4	V
	I_{LOAD} = 10 mA	–	–	0.5	V

Supply Current

Parameter	Condition	Min	Typ	Max	Unit
V_{3P3D} and V_{3P3A} current (compounded)	Normal Operation, V3P=3.3V	–	8.1	10.3	mA

Internal RC Oscillator

Parameter	Condition	Min	Typ	Max	Unit
Nominal Frequency	V3P=3.3V, 25ºC	–	20.000	–	MHz
Accuracy		–	±1.5	–	%
Accuracy	V3P=3.3V, -40ºC to +105ºC	–	±2.0	–	%

ADC Converter, V3P3 Referenced

LSB values do not include the 9-bit left shift at processor input.

Parameter	Condition	Min	Typ	Max	Unit
Usable Input Range (AINxP-AINxN)		-250	–	250	mV peak
THD (First 10 harmonics)	Vin=65Hz, 64kpts FFT, Blackman-Harris window	–	-85	–	dB
Input Impedance	Vin=65Hz	30	–	90	kΩ
Temperature coefficient of Input Impedance	Vin=65Hz	–	1.7[1]	–	Ω/°C
ADC Gain Error vs %Power Supply Variation $\frac{10^6 \Delta Nout_{PK} 357nV/V_{IN}}{100 \Delta V3P3A/3.3}$	Vin=200mVpk, 65Hz V_{3P3}=3.0V, 3.6V	–	–	50	ppm/%
Input Offset (Vin-V_{3P3})		-10		10	mV

[1] **Guaranteed by design, not subject to test.**

Timing Specifications

SPI Slave Port

Parameter		Condition	Min	Typ	Max	Unit
t_{SPIcyc}	SPCK cycle time		1	–	–	µs
$t_{SPILead}$	Enable lead time		15	–	–	ns
t_{SPILag}	Enable lag time		0	–	–	ns
t_{SPIW}	SPCK pulse width: High Low		 250 250	 –	 –	 ns ns
t_{SPISCK}	SSB to first SPCK fall	Ignore if SPCK is low when SSB falls.	–	2[1]	–	ns
t_{SPIDIS}	Disable time		–	0[1]	–	ns
t_{SPIEV}	SPCK to Data Out (MISO)			–	25	ns
t_{SPISU}	Data input setup time (MOSI)		10	–	–	ns
t_{SPIH}	Data input hold time (MOSI)		5	–	–	ns

[1] Guaranteed by design, not subject to test.

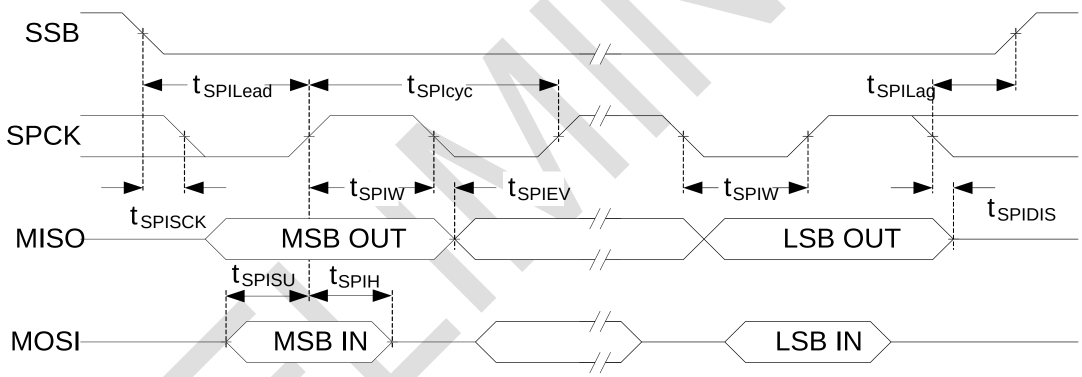


Figure 2. SPI Slave Port Timing

I2C Slave Port

I²C Slave Port Timing[2]

Parameter	Condition	Min	Typ	Max	Unit
t_{BUF} Bus Idle (Free) time between transmissions (STOP/START)		1500	-	–	ns
t_{ICF} I²C input Fall Time		20[1]	–	300	ns
t_{ICR} I²C input Rise Time		20[1]	–	300	ns
t_{STH} I²C START or repeated START condition hold time		500	–	–	ns
t_{STS} I²C START or repeated START condition setup time		600	–	–	ns
t_{SCH} I²C clock high time		600	–	–	ns
t_{SCL} I²C clock low time		1300	–	–	ns
t_{SDS} I²C serial data setup time		100	–	–	ns
t_{SDH} I²C serial data hold time		10	–	–	ns
t_{VDA} I²C Valid data time: - SCL low to SDA output valid - ACK signal from SCL low to SDA (out) low		–	–	900	ns

Notes:

[1] Dependent on bus capacitance.

[2] Guaranteed by design, not subject to test.

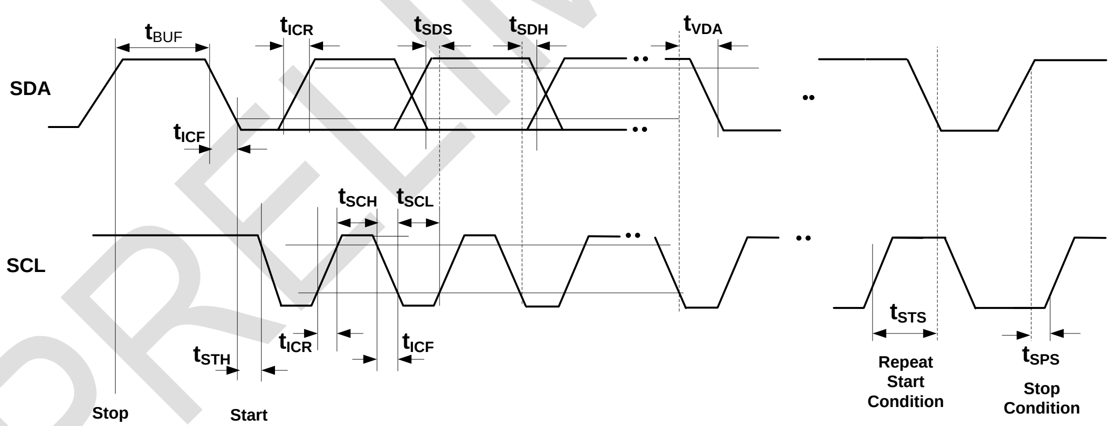


Figure 3. I²C Port Timing

Hardware Resources Overview

Power-On Reset (POR)

An on-chip Power-On Reset (POR) block monitors the supply voltage (V_{3P3D}) and initializes the internal digital circuitry at power-on. Once V_{3P3D} is above the minimum operating threshold, the POR circuit triggers and initiates a reset sequence. It will also issue a reset to the digital circuitry if the supply voltage falls below the minimum operating level.

Watchdog Timer (WDT)

A Watchdog Timer (WDT) block detects any software processing errors. The embedded software periodically refreshes the free-running watchdog timer to prevent it from timing out. If the WDT times out, it is an indication that software is no longer being executed in the intended sequence; thus, a system reset is initiated.

External Reset Pin (RESETB Pin)

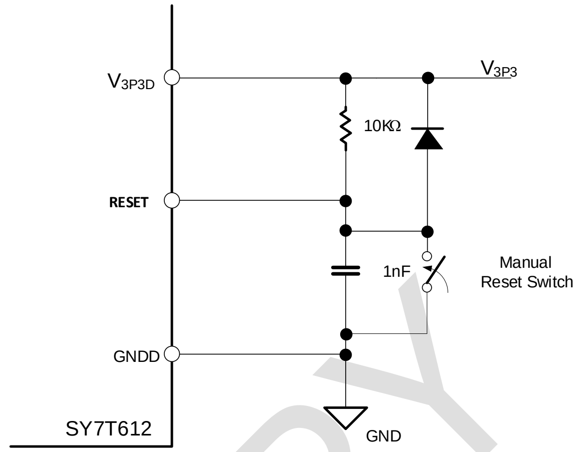
In addition to the internal reset sources, a reset can be forced by applying a low level to the RESETB pin.

If the RESETB pin is pulled low, all digital activities in the device stop, except the clock management circuitry and oscillators, which continue to run. The external reset input is filtered to prevent spurious reset events in noisy environments. The reset does not occur until RESETB has been held low for at least 1 µs.

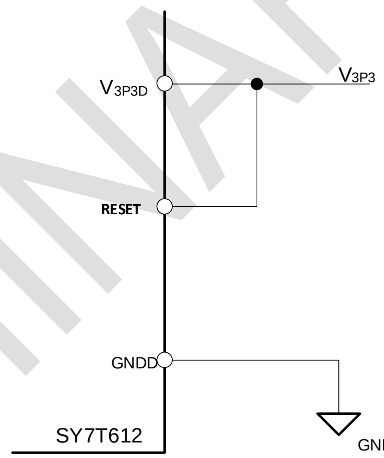
Once initiated, the reset mode persists until the RESETB is set high and the reset timer times out (4096 clock cycles). At the completion of the reset sequence, the internal reset is released and the processor (EMP) begins executing from address 0.

RESETB pin can be driven by a host processor or connected to a pushbutton as indicated in Figure 4.

If not used, the RESETB pin can be connected either directly or through a pull-up resistor to V_{3P3D} supply.



a) RESETB External Connection Example



b) Unused RESETB Connection Example

Figure 4. Reset Pin Connections Examples

Clock Management

The SY7T612 integrates a trimmed and temperature compensated RC oscillator. The device also includes the circuitry to handle an external crystal or ceramic resonator. The clock management unit of the SY7T612 automatically handles the clock sources logic and distributes the clock to the rest of the device.

Upon reset or power-on, the SY7T612 starts up on the internal RC oscillator. After 1024 clock cycles of the internal RC oscillator, the clock management logic will switch to the external 20MHz clock (if available), allowing the external crystal an adequate start-up time. If no valid external clock is detected,
the clock management logic will keep clocking the device using the internal RC oscillator. If the device is normally clocked using the external 20MHz crystal, the clock management logic continuously monitors

the status of the clock. The clock management logic of the SY7T612E will automatically switch to the internal oscillator in the event of a failure of the external oscillator.

The internal RC oscillator is factory-trimmed and temperature-compensated. It provides an accurate clock source, however for applications requiring highest accuracy of the time-based measurements (i.e. line frequency, energy, etc.), the use of an external crystal is recommended.

The SY7T612E external clock circuitry requires a 20.000MHz crystal. The circuitry includes two 18pF ceramic capacitors. Figure 5 shows the typical connection of the external crystal. This oscillator is self-biasing and therefore an external resistor should NOT be connected across the crystal.

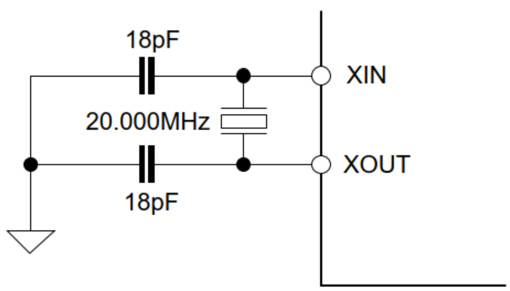


Figure 5. XTAL Connection

Alternatively, an external clock signal can be utilized instead of the crystal. In this case, the external clock should be connected to the XOUT pin while the XIN pin should be connected to GNDD.

If the external crystal is not utilized (not mounted), the XOUT pin should be connected to GNDD and the XIN pin left unconnected.

Analog Front-End and Conversion

The SY7T612E's Analog Front-End (AFE) includes an input multiplexer, delta-sigma A/D converter, voltage reference, bias current reference, temperature sensor, voltage fault comparators, and POR circuitry .

Delta-Sigma A/D Converter

A second-order delta-sigma converter digitizes the analog inputs. The converted data is then filtered and decimated through a FIR filter.

Voltage Reference

The device includes an on-chip precision bandgap voltage reference that incorporates auto-zero techniques as well as production trims to minimize errors caused by component mismatch and drift. The voltage reference is digitally compensated over temperature.

Die Temperature Measurement

The device includes an on-chip die temperature sensor used for digital compensation of the voltage reference. It is also used to report temperature information to the user.

Voltage and Current Inputs

The external voltage and current sensors are connected to analog input pins. The full-scale signal level that can be applied to the voltage input pins is V3P3A ±250 mVpk. With a sinusoidal waveform, the maximum RMS voltage is:

$$Vrms(MAX) = \frac{250mVpk}{\sqrt[2]{2}} = 176.78mVRMS$$

A common-mode voltage of less than ±25 mV is recommended in order to fully utilize the available dynamic range.

Energy Measurement Processor

The SY7T612E integrates a dedicated processor that performs all the digital signal processing necessary for measurement, calibration, compensation, analysis, alarms generation, relay control, etc.

Flash and RAM

The SY7T612E includes on-chip flash memory for storing program code, coefficients, calibration data, and configuration settings. The SY7T612 also includes on-chip RAM which is used to store the values of input and output registers and utilized by the firmware for its operations.

Digital I/O

The SY7T612 features 16 general purpose digital I/Os. The digital I/Os are either managed directly by the user, by the embedded firmware, or multiplexed with the serial communication interfaces. The device also includes the necessary hardware to generate free-running PWM signals at either DIO7 or DIO8 with configurable period and pulse width (PWM functionality is not supported in this firmware revision). The following table summarizes the multiplexing and pin assignment on the SY7T612.

Table 2. Digital I/O Assignments

Pin Name	Pin #	Function at Power-On Reset	Function by Interface		
			SPI	UART	I^2C
DIO15	2	--	DIO15		
DIO14	5	--	DIO14		
DIO13	7	--	DIO13		
DIO12	10	--	DIO12		
DIO11	19	--	DIO11		
DIO10	21	--	DIO10		
DIO9	22	--	DIO9		
DIO8	3	Interface Selection	DIO8		
DIO7	4	--	DIO7		
DIO6	6	--	DIO6		
DIO5	8	--	SSB	DIO5	SCL
DIO4	9	--	DIO4		
DIO3	16	--	MISO	TX	SDAo
DIO2	17	--	MOSI	RX	SDAi
DIO1	18	--	SCK	DIO1	
DIO0	20	--	DIO0		

Notes:

[1] Relay outputs can be configured (assigned to different DIO pins, for single and dual coil relays) and unused relay outputs can be used as general purpose DIOs.

Warning: Where applicable, pins should be configured via pull-up and pull-down resistors as these pins could become outputs after initialization. Therefore, direct connection to GNDD/GNDA or V3P3D/V3P3A supplies must be avoided.

Serial Interfaces

The SY7T612E features UART, I^2C, and SPI interface options. Only one interface can be active at a time as the Digital I/O pins are shared. In the SY7T612E, pin DIO8 is sampled following a power-on or reset to select between SPI or UART/ I^2C interface. The selection between UART and I^2C is determined by the FW.
The user should allow at least 10ms from a power-on reset event for the selection pin status to be latched and the serial interface selected. During this time the status of DIO8 must not change.

Selected Interface	DIO8
SPI	**0**
UART Or **I^2C**	**1**

UART Interface

The SY7T612 features a UART interface with a data rate ranging from 2400 up to 115k Baud. The UART interface has a fixed configuration supporting: 8-bit, one start bit, one stop bit and no-parity. The UART interface hardware does not provide handshaking hardware signals (i.e. RTS, CTS etc.).
Once the UART interface is activated, it utilizes the following digital I/Os:

- **DIO3**: Transmit (TX) output
- **DIO2**: Receive (RX) input.
- **DIO5**: Optional (DIR) output, to drive a RS-485 transceiver's direction pin

The communication protocol is described in the **Error! Reference source not found.** section.

The UART clock is derived from the 20MHz system clock. The error due to the clock division is reported in the following Table.

Table 3. UART Baud Rate Error

Baud Rate	Actual Baud Rate	Error [percent]
2400	2399.808	0.008
4800	4800.768	0.016
9600	9596.929	-0.032
19200	19193.858	-0.032
38400	38461.538	0.160
57600	57541.264	-0.223
115200	114942.529	-0.223

SPI Interface

The SPI featured in the SY7T612 is slave only. Once the SPI interface is activated, it utilizes the following digital I/O as the SPI interface:

- **DIO5**: Slave select (SSB) is an active low input.
- **DIO1**: Serial Data Clock (SCK) input.
- **DIO3**: Master Input, Slave Output (MISO), serial data output.
- **DIO2**: Master Output, Slave Input (MOSI), serial data input.

The SPI interface allows read and write accesses to the data RAM specified in the command bit field ADDR[5:0]. The command limits the access to RAM locations 0x00 through 0x3F. Refer to the **Error! Reference source not found.** section for details on accessing other RAM locations.

SPI Mode

The device operates in mode 3 (CPOL=1, CPHA=1) and as such the data is captured on the rising edge and propagated on the falling edge of the serial data clock (SCK). The figure below shows a single-byte transaction on the SPI bus. Bytes are transmitted/received MSB first.

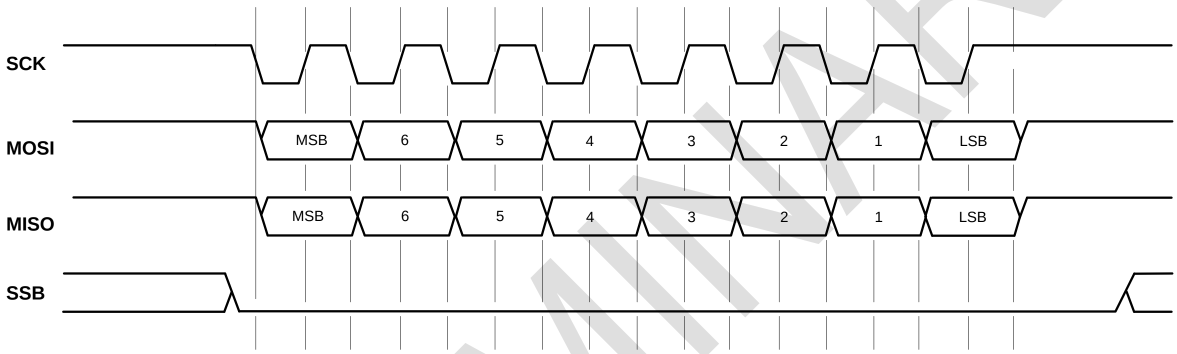


Figure 6. Signal Timing on the SPI Bus (Single ByteTransaction)

Single Word SPI Reads

The device supplies direct read access to the device RAM memory. To read the RAM the master device must send a read command to the slave device and then clock out the resulting read data. SSB must be kept active low for the entire read transaction (command and response). SCK may be interrupted as long as SSB remains low. ADDR[5:0] is filled with the word address of the read transaction. RAM data contents are transmitted most significant byte first. ADDR[5:0] cannot exceed 0x3F. RAM words, and therefore the results, are natively 24 bits (3 bytes) long.

Table 4: Single-Word Read Command (MOSI)

Byte #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0		ADDR[5:0]					0x0	
1		0						
2		0						
3		0						

The slave responds with the data contents of the requested RAM addresses.

Table 5: Single-Word Read Response (MISO)

Byte #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Hi-Z (during Read Command)							
1	DATA[23:16] @ ADDR							
2	DATA[15:8] @ ADDR							
3	DATA[7:0] @ ADDR							

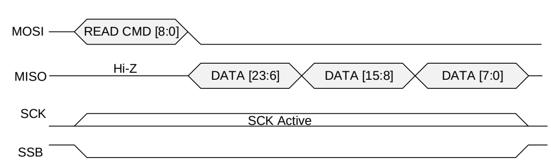


Figure 7. Single Word Read Access Timing

Single Word SPI Writes

The device supplies direct write access to the device RAM memory. To write the RAM the master device must send a write command to the slave device and then clock out the write data. SSB must be kept active low for the entire write transaction (command and data). SCK may be interrupted as long as SSB remains low. ADDR[5:0] is filled with the word address of the write transaction. RAM data contents are transmitted most significant byte first. ADDR[5:0] cannot exceed 0x3F. RAM words are natively 24 bits (3 bytes) long.

Table 6: Single-Word Write Command (MOSI)

Byte #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	ADDR[5:0]						0x02	
1	DATA[23:16] @ ADDR							
2	DATA[15:8] @ ADDR							
3	DATA[7:0] @ ADDR							

The slave SDO remains Hi-Z during a write access.

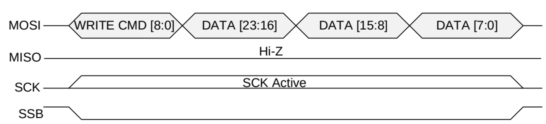


Figure 8. Single Word Write Access Timing

I²C Interface

The SY7T612+U3/I3 has an I²C interface available at the DIO2, DIO3, and DIO5 pins. The interface supports I²C slave mode with a 7-bit address and operates at a data rate up to 400kHz (Fast-mode).

The SY7T612 has separate SD (serial data) input and output pins to allow the use of digital isolators/opto-couplers to isolate the serial bus. The configuration in Figure 9 (standard) has the I²C data pins (SDAi and SDAo) shorted.

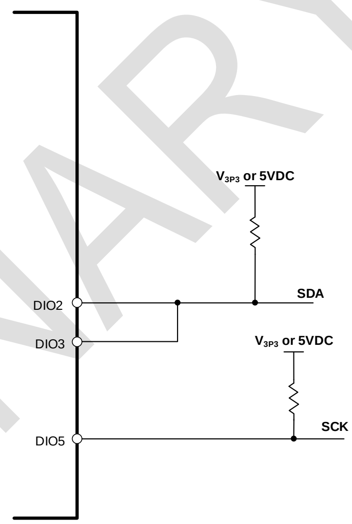


Figure 9: I2C Bus Connection (Standard Configuration)

It is possible to isolate the I²C interface utilizing the configuration indicated in Figure 10. In this case the bus is isolated using optocouplers (any other open drain isolator type can be used).

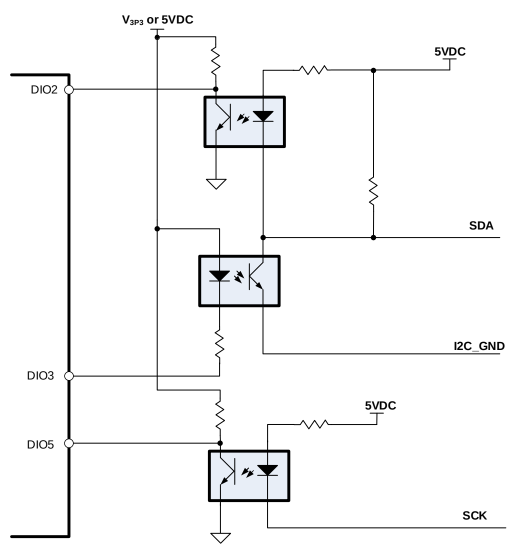


Figure 10: I2C Bus Connection (Isolated Configuration)

The I²C interface allows access to read and write registers contained in a 256-word (24-bit) area of the on-chip RAM. The **Error! Reference source not found.** section contains the address and assignment of each register.

Bus Characteristics

- A data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Bus Conditions

- **Bus not Busy (I):** Both data and clock lines are HIGH indicating an Idle Condition.
- **Start Data Transfer (S):** a HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.
- **Stop Data Transfer (P):** a LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.
- **Data Valid:** The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition.
- **Acknowledge (A):** Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse, which is associated with this Acknowledge bit. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by not generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave SY7T612 will leave the data line HIGH to enable the master to generate the STOP condition

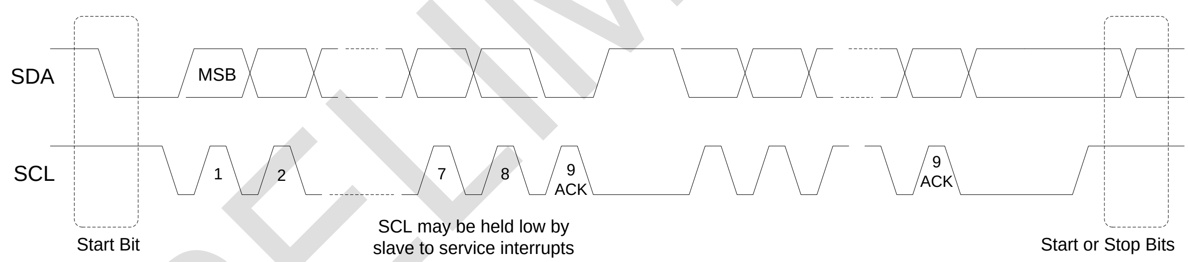
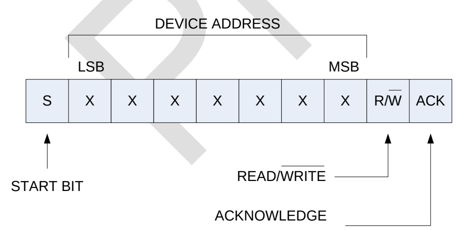


Figure 11: I2C Bus Conditions

Device Addressing



The control byte consists of a seven-bit address and a bit (LSB) indicating the type of access (0=write; 1=read).

Write Operations

Following the START (S) condition from the master, the device address (7-bits) and the R/W bit (logic low for write) are clocked onto the bus by the master. This indicates to the addressed slave receiver that the register address will follow after it has generated an acknowledge bit (A) during the ninth clock cycle.
Therefore, the next byte transmitted by the master is the register address and will be written into the address pointer of the SY7T612. After receiving another acknowledge (A) signal from the 78M6610+PSU the master device will transmit the data byte(s) to be written into the addressed memory location. The data transfer ends when the master generates a STOP (P) condition. This initiates the internal write cycle. The example in Figure 12 shows a 3-byte data write (24-bit register write).

Upon receiving a STOP (P) condition, the internal register address pointer will be incremented.
The write access can be extended to multiple sequential registers. Figure 13 shows a transaction where multiple register are written sequentially

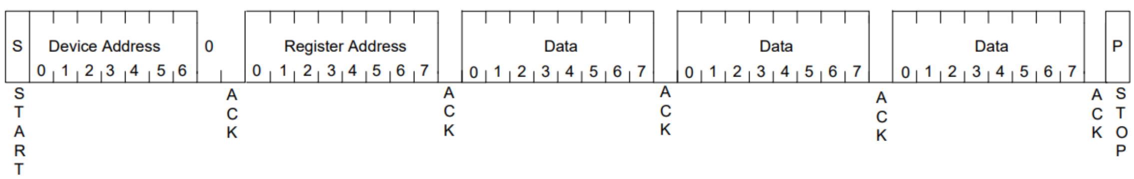


Figure 12: I²C Bus 3-byte Data Write

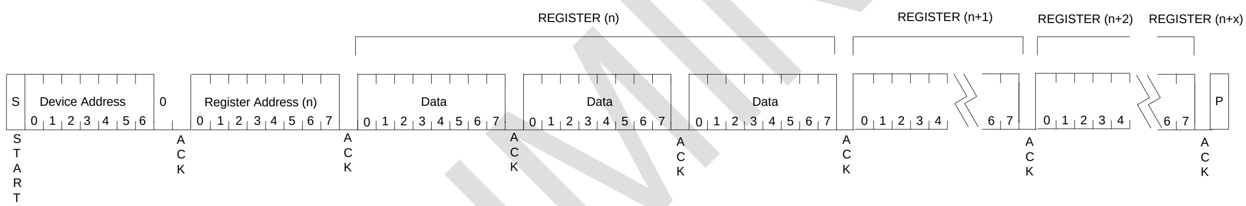


Figure 13: I2C Bus Multiple Sequential Register Write

Read Operations

Read operations are initiated in the same way as write operations with the exception that the R/W bit of the control byte is set to one. There are two basic types of read operations: current address read and random read.
Current Address Read:
The SY7T612 contains an address counter that maintains the address of the last register accessed, internally incremented by one when the STOP bit is received. Therefore, if the previous read access was to register address n, the next current address read operation would access data from address n + 1.

Upon receipt of the control byte with R/W bit set to one, the SY7T612 issues an acknowledge (A) and transmits the eight-bit data byte. The master will not acknowledge the

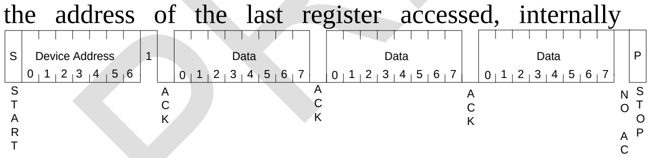
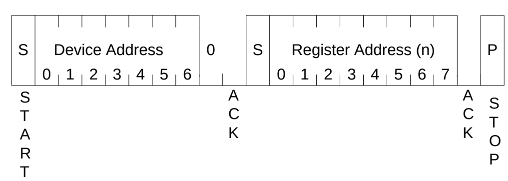


Figure 14: I2C Bus 3-byte Data Read

This read operation is not limited to 3 bytes but can be extended until the register address pointer reaches its maximum value.
If the register address pointer has not been set by previous operations, it is necessary to set it issuing a command as follows:



Random read operations allow the master to access any register in a random manner. To perform this operation, the register address must be set as part of the write operation. After the address is sent, the master generates a START condition following the acknowledge response. This sequence completes the write operation. The master should issue the control byte again this time, with the R/W bit set to 1 to indicate a read operation. The SY7T612 will issue the acknowledge response and transmit the data.

At the end of the transaction the master will not acknowledge the transfer and generate a STOP condition.

Random read operations are not limited to 3 bytes but can be extended until the register address pointer reaches its maximum value.

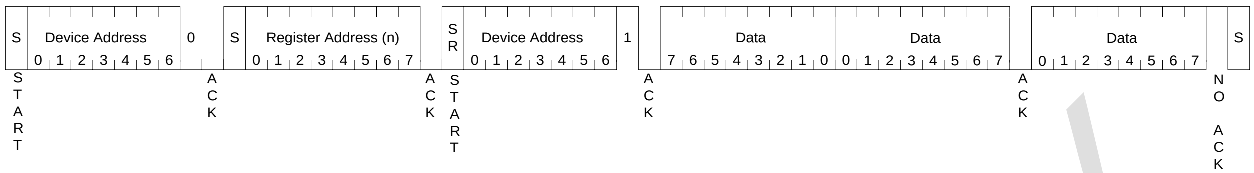


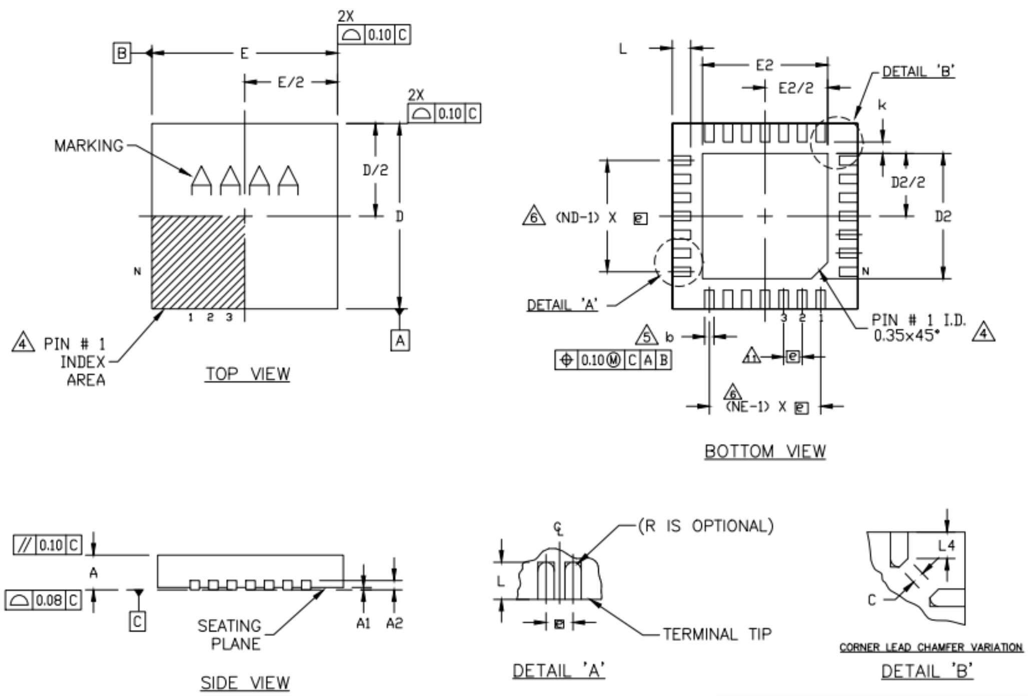
Figure 15: I2C Bus 3-byte Random Data Read

Functional (Firmware) Description

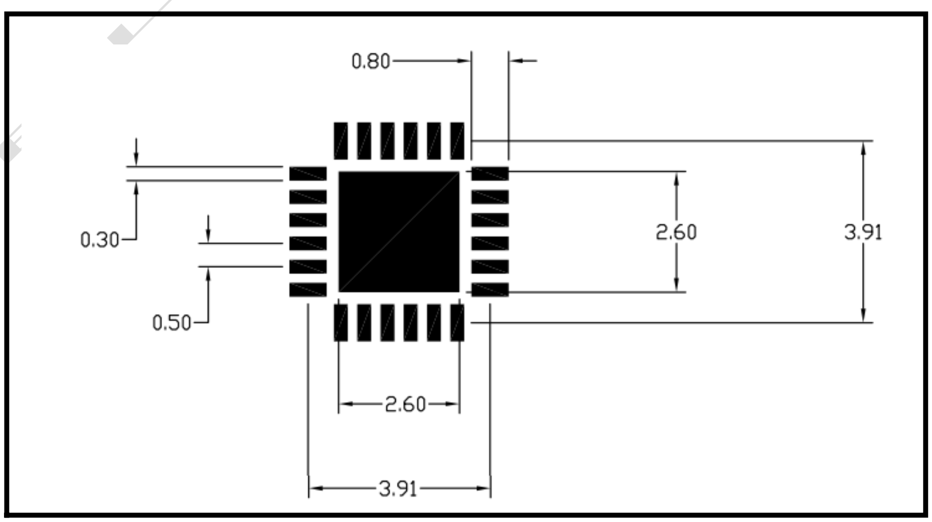
This datasheet only contains a description of the various on-chip hardware resources, electrical specifications, mechanical specifications, and ordering numbers.

Packaging

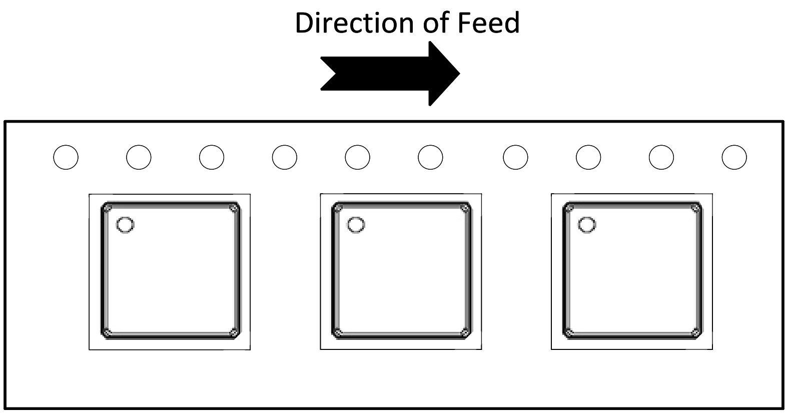
Package Outline and Land Pattern



COMMON DIMENSIONS			
PKG	24L 4x4		
REF.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.0	0.02	0.05
A2	0.20 REF		
b	0.18	0.23	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
e	0.50 BSC.		
k	0.25	–	–
L	0.30	0.40	0.50
N	24		
ND	6		
NE	6		
Jedec Var.	WGGD-2		



Tape & Reel Orientation



Contact Information

For more information about the SY7T612, contact support.em@silergy.com

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0.0	05/18/2022	Initial Release	-

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