SY20372

1.8V-5.5V Input, 20A, 10MHz High Frequency, Synchronous Step Down Regulator with I²C Interface

General Description

The SY20372 is a high-frequency synchronous step-down DC-DC regulator capable of delivering 20A continuous output current over the input range from 1.8V to 5.5V. The output voltage is adjustable from 0.4V to 1.5V.

It uses a proprietary ripple-based constant on-time architecture with frequency locked loop. The maximum operating frequency is 10MHz. The SY20372 can achieve very high loop bandwidth to support fast load transient response within ~50ns.

The operating frequency is selectable through I²C from 3.3MHz, 5MHz or 10MHz. The high switching frequency provides very compact solution size with small inductor and capacitors. The internal voltage reference provides ±1% accuracy over full junction temperature from -40°C to 125°C. The differential sense pins allow output feedback remote sensing.

The SY20372 supports forced PWM mode and automatic PWM/PFM mode, cycle-by-cycle current limit, internal soft-start, input under-voltage lock-out, output under/over voltage protection, output short circuit protection and thermal shutdown. The device provides safe operation under all conditions.

The SY20372 is available in a compact QFN3mm×4mm-16 package.

Key Features

- Wide Input Range from 1.8V to 5.5V
- Up to 20A Output Current
- Accuracy ±1% of output voltage from -40°C to 125°C
- Low $R_{DS(ON)}$ for Internal High-side FET and Synchronous FET
- Forced PWM Mode & Auto PFM Mode
- Differential Remote Sense
- Fast Transient Response
- Programmable Via I²C
  - Output Voltage from 0.4V to 1.5V
  - Switching Frequency of 3.3MHz/5MHz/10MHz
  - Dynamic Voltage Scaling (DVS) Slew Rate
- MTP Memory
- Internal Soft-start &Smooth Pre-Biased Startup
- Reliable Build-in Protections:
  - Automatic Recovery for:
    - Input Under-voltage (UVLO)
    - Output Under-voltage (UVP)
    - Output Short-Circuit (SCP)
    - Over Temperature (OTP)
  - Cycle-by-cycle Valley and Peak Current Limit (OCP)
  - Cycle-by-cycle Reverse Current Limit
- Compact Package: QFN3mm×4mm-16

Applications

- Optical Modules
- Smartphone and Portable Devices
- DC-DC Modules

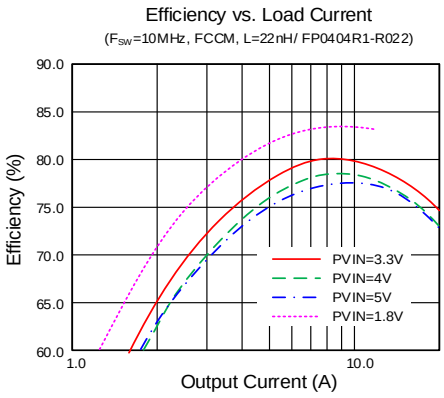


Figure 1. Efficiency vs. Load Current

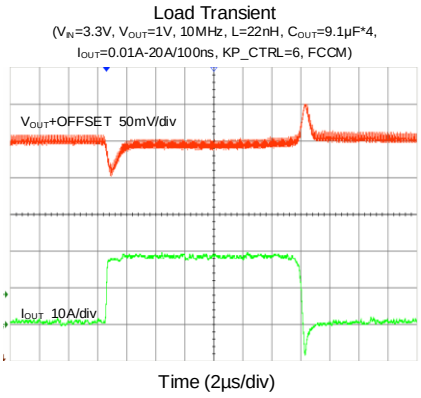


Figure 2. Load Transient

Typical Application

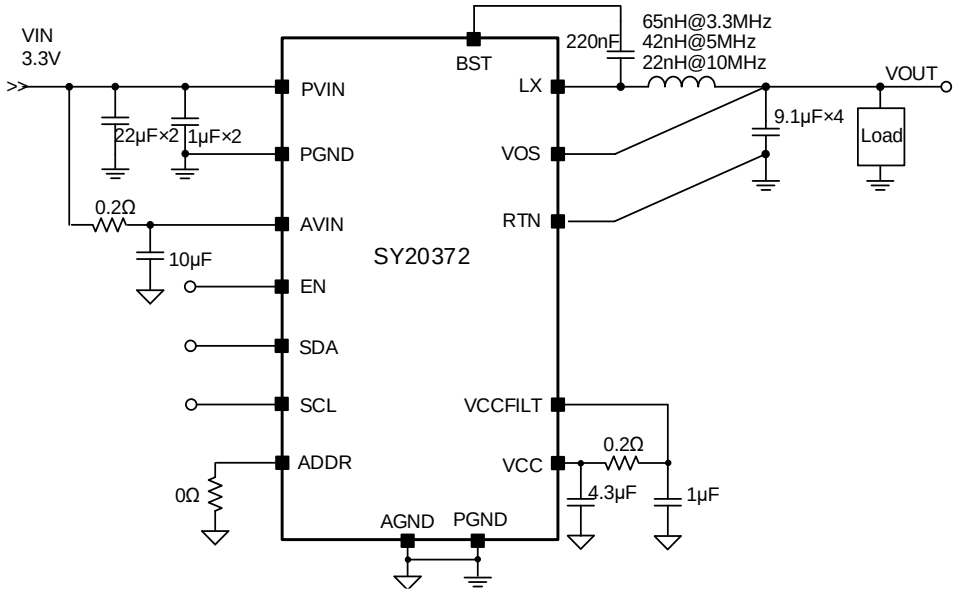


Figure 3. 3.3V PVIN Application Circuit

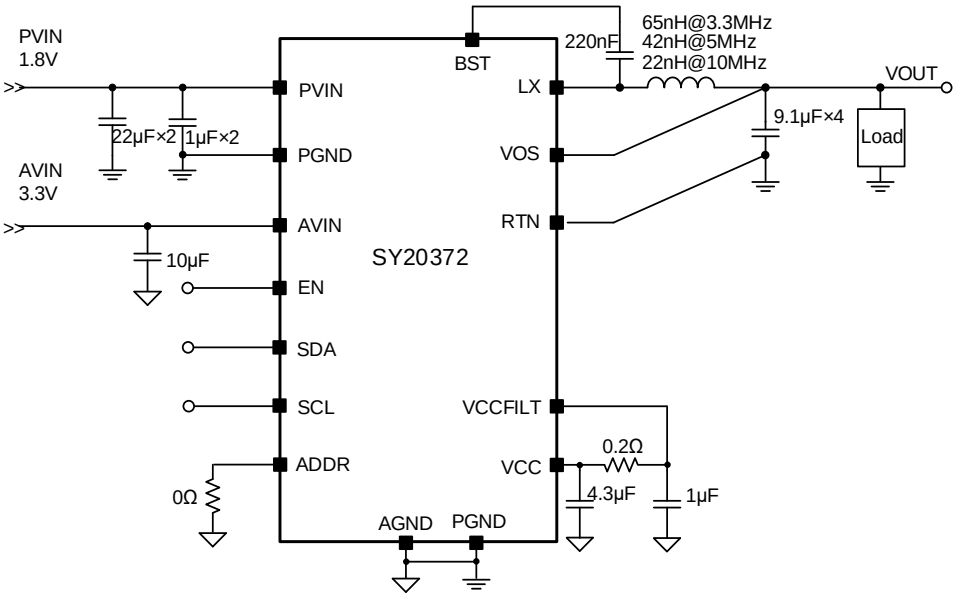


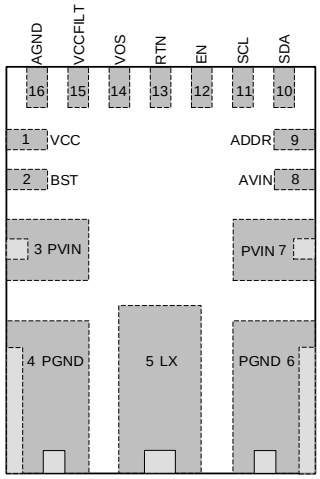
Figure 4. 1.8V PVIN Application Circuit

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY20372QLQ	QFN3x4-16 RoHS-Compliant, Halogen-Free	**DYE*xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



(QFN3×4-16)

Pin Description

Pin Number	Pin Name	Pin Description
1	VCC	Internal LDO output, power supply for the power MOSFET gate drive circuit. Decouple this pin to power ground with at least a 4.3μF ceramic capacitor.
2	BST	Bootstrap pin to supply high side gate driver. Decouple this pin to LX pin with a 220nF ceramic capacitor.
3, 7	PVIN	Input supply pin for the power circuit.
4, 6	PGND	Power GND pin.
5	LX	Switch pin connected to the internal MOSFETs. Connect the external inductor between this pin and the output capacitors.
8	AVIN	Analog VIN power supply for the control circuit. Connect to PVIN. Decouple this pin to AGND with a RC filter.
9	ADDR	Pin to set I^2C Device address. Connect a resistor from this pin to GND to program the device address.
10	SDA	I^2C data pin.
11	SCL	I^2C clock pin.
12	EN	Enable pin of the device. Pull this pin low to shut down the device, or pull this pin high to enable the device. Do not float this pin.
13	RTN	Negative input of the remote sense amplifier.
14	VOS	Positive input of the remote sense amplifier.
15	VCCFILT	Filtered analog supply input pin. Connect to VCC Pin with a RC filter, close to the IC.
16	AGND	Analog GND pin for the control circuit.

Block Diagram

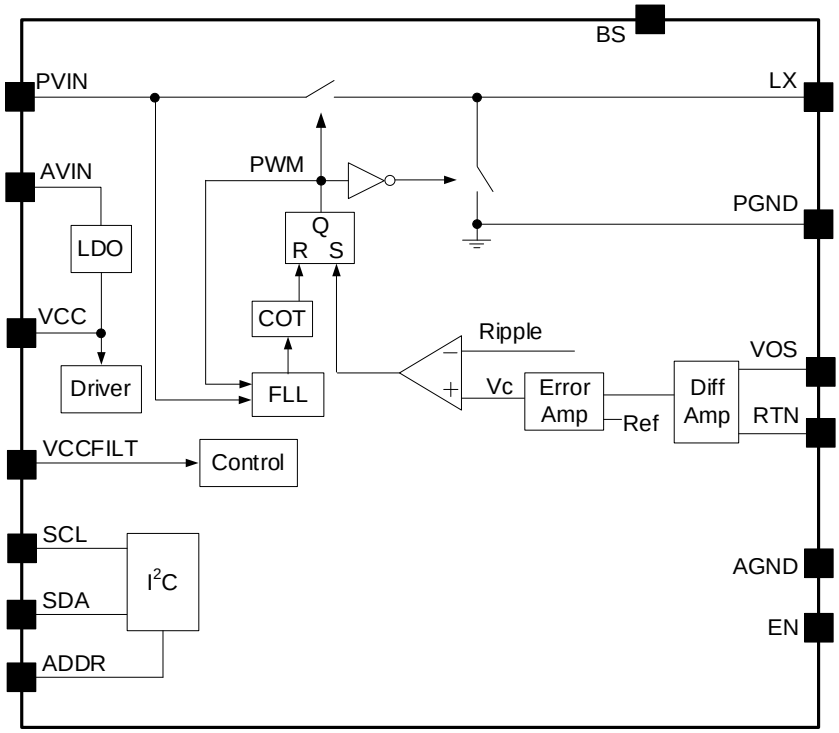


Figure 5. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
PVIN, AVIN to GND (Note 2)	-0.3	6	V
EN, SDA, SCL, ADDR to GND	-0.3	6	
VCC, VCCFILT, VOS to GND	-0.3	4	
RTN to GND	-0.3	0.3	
LX to GND (Note 3)	-0.3	V_{IN}+0.3	
BST	LX-0.3	LX+4	
Junction Temperature Range		150	°C
Lead Temperature (Soldering, 10 sec.)		260	
Storage Temperature Range	-65	150	

Thermal Information

Parameter (Note 4)	Typ	Unit
$R_{\theta JA}$ Junction-to-Ambient Thermal Resistance	21.6	°C/W
$R_{\theta JB}$ Junction-to-Board Thermal Resistance	5	
P_D Power Dissipation T_A = 25°C	4.6	W

Recommended Operating Conditions

Parameter (Note 5)	Min	Max	Unit
PVIN	1.8	5.5	V
AVIN	2.9	5.5	
Junction Temperature Range	-40	125	°C
Ambient Temperature Range	-40	105	

Electrical Characteristics

(V_{PVIN}=V_{AVIN}=3.3V, V_{OUT}=1V, T_J = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ.	Max	Unit
Input Supply	Analog Input Voltage Range	V_{AVIN}		2.8	3.3	5.5	V
	Power Input Voltage Range	V_{PVIN}		1.8	3.3	5.5	V
	UVLO Rising Threshold	V_{UVLOR_A}	V_{PVIN} =3.3V, V_{AVIN} Rising, redo soft-start	2.6	2.7	2.8	V
		V_{UVLOR_P}	V_{AVIN} =3.3V, V_{PVIN} Rising, redo soft-start	1.65	1.7	1.75	V
		V_{PORR}	V_{AVIN} Rising, enable I^2C	2.5	2.6	2.7	V
	UVLO Falling Threshold	V_{UVLOF_A}	V_{PVIN} =3.3V, V_{AVIN} Falling, stop switching	2.3	2.4	2.5	V
		V_{UVLOF_P}	V_{AVIN} =3.3V, V_{PVIN} Falling, stop switching	1.55	1.6	1.65	V
		V_{PORF}	V_{AVIN} Falling, disable I^2C	2.2	2.3	2.4	V
	Quiescent Current	I_Q	V_{IN}=5.5V, EN Pin Pull high, “Reg0x01”[2]=1,No switching		1.2	1.4	mA
	Shutdown Current	I_{SD}	V_{IN}=5.5V, EN Pin Pull high, “Reg0x01”[6]=0		0.5	0.6	mA
			V_{IN}=6.0V, EN Pin Pull low		16	22	μA
	Analog Input Voltage OVP Threshold	V_{AINOV}		5.65	5.8	5.95	V
	Analog Input Voltage OVP Hysteresis	$V_{AINOVHYS}$			110		mV
	Power Input Voltage OVP Threshold	V_{PINOV}		5.60	5.75	5.90	V
	Power Input Voltage OVP Hysteresis	$V_{PINOVHYS}$			110		mV
Power Stage	VCC Output Voltage	V_{VCC}	“Reg0x01” [0]=0		3.3		V
			“Reg0x01” [0]=1		3.0		V
	VOUT Voltage Range	V_{OUT}	V_{OUT}=V_{FB}	0.4		1.0	V
			V_{OUT}=1.5×V_{FB},	0.6		1.5	V
	VOUT Step Size	V_{STEP}	V_{OUT}=V_{FB}		10		mV
			V_{OUT}=1.5×V_{FB}		15		mV
	Output Accuracy		V_{OUT}≥0.6V, T_J = -40°C to 125°C	-1		1	%
			V_{OUT}<0.6V, T_J = -40°C to 125°C	-1.5		1.5	%
	DVS Slew Rate Accuracy		V_{OUT}=V_{FB} : 17mv/μs V_{OUT}=1.5×V_{FB} : 25mv/μs “Reg0x01”[1]=0(6)	-10		10	%
			V_{OUT}=V_{FB} : 2.5mv/μs V_{OUT}=1.5×V_{FB} : 3.7mv/μs “Reg0x01”[1]=1(6)	-10		10	%
	Top FET R_{ON}	$R_{DS(ON)\_T}$	V_{AVIN} =3.3V		1.9		mΩ
	Bottom FET R_{ON}	$R_{DS(ON)\_B}$	V_{AVIN} =3.3V		1.2		mΩ
	Soft Start Time	t_{SS}	V_{IN}=5.5V, pull EN pin high, time 0 to 100%V_{OUT}		1.3		ms

	Switching Frequency		F_{SW}	Fsw set 10MHz, "Reg0x01"[4:3]=00	9.5	10	10.5	MHz
				Fsw set 5MHz, "Reg0x01"[4:3]=01	4.75	5	5.25	MHz
				Fsw set 3.3MHz, "Reg0x01"[4:3]=10/11	3.1	3.3	3.5	MHz
	Min ON Time		$t_{ON,MIN}$	Minimum ON pulse width(6)		23		ns
	Min OFF Time		$t_{OFF,MIN}$	Minimum OFF pulse width(6)		44		ns
	Output Discharge Resistance		R_{DIS}			115		Ω
Protection	High Side Switch Positive Current Limit		I_{PLMT}	Vin=5.5V, L_{wire}≈35nH T_J= 25°C	28	30	32	A
				Vin=5.5V, L_{wire}≈35nH, T_J= -40°C to 125°C	25	30	35	A
	Low Side Switch Positive Current Limit		I_{VLMT}	Vin=5.5V, L_{wire}≈35nH, T_J = 25°C	26	28	30	A
				Vin=5.5V, L_{wire}≈35nH, T_J= -40°C to 125°C	23	28	33	A
			I_{VLMT_FDB}	Vin=5.5V, L_{wire}≈35nH		23		A
	Low Side Switch Negative Current Limit		I_{NVLMT}	Vin=5.5V, L_{wire}≈35nH		-7		A
	Thermal Shutdown Threshold		T_{SD}	Junction Temperature(6)		160		°C
	Thermal Shutdown Hysteresis		T_{HYS}			20		°C
	Thermal Warning Threshold		T_{WN}	Junction Temperature(6)		110		°C
	Thermal Warning Hysteresis		T_{WNHYS}			20		°C
	Output Over Voltage Threshold		V_{TH_OVP}		115	120	125	$\%V_{SET}$
	Output Under Voltage Threshold		V_{TH_UVP}		75	80	85	$\%V_{SET}$
	Output Short Protection Threshold		V_{TH_SCP}		35	40	45	$\%V_{SET}$
IO PINs	EN	EN Logic Level Low					0.4	V
		EN Logic Level High			1.2			V
	SCL, SDA	Low-Level Input Voltage					0.4	V
		High-Level Input Voltage			1.2			V
	I^2C Interface	I^2C Frequency Capability	F_{I2C}				3.4	MHz

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The PVIN pin can tolerate transient voltages up to 6.5V for a duration of up to 10ns. These transients can occur during normal operation of the device.

Note 3: The LX pin can tolerate transient voltages up to 9V for a duration of 6ns and -1V for a duration of 4ns. These transients can occur during normal operation of the device.

Note 4: Package thermal resistance is measured in the natural convection at T_A=25˚C on an 8cm×8cm size six-layer Silergy Evaluation Board.

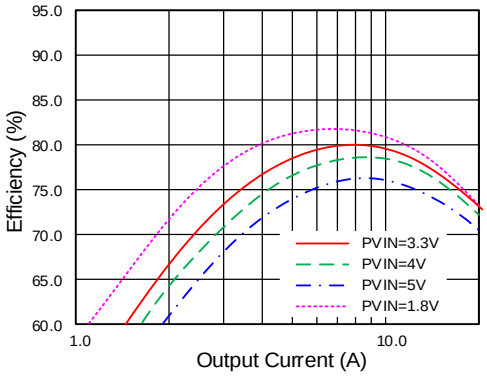
Note 5: The device is not guaranteed to function outside its operating conditions.

Note 6: Guarantee by design

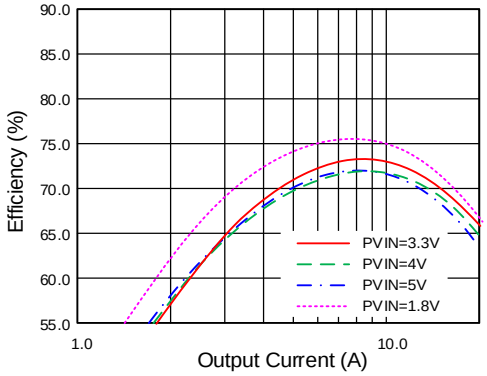
Typical Performance Characteristics

(T_A=25˚C, V_{AVIN}=3.3V, V_{OUT}=1V, L=22nH, C_{OUT}=9.1μF×4, f_{sw}=10MHz, unless otherwise noted)

Efficiency vs. Load Current
(F_{SW}=3.3MHz, 0.4V_{OUT}, FCCM, L=65nH/WPZ04044S165NKT)



Efficiency vs. Load Current
(F_{SW}=5MHz, 0.4V_{OUT}, FCCM, L=42nH/CLT-32-42N)



Efficiency vs. Load Current
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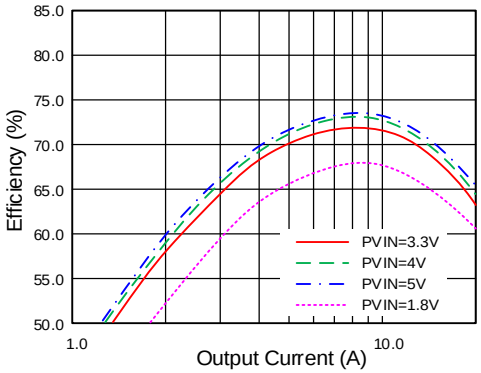
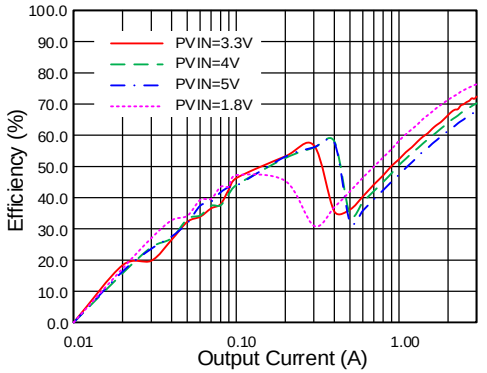


Efficiency vs. Load Current
(F_{SW}=3.3MHz, 0.4V_{OUT}, PFM, L=65nH/WPZ04044S165NKT)



Efficiency vs. Load Current
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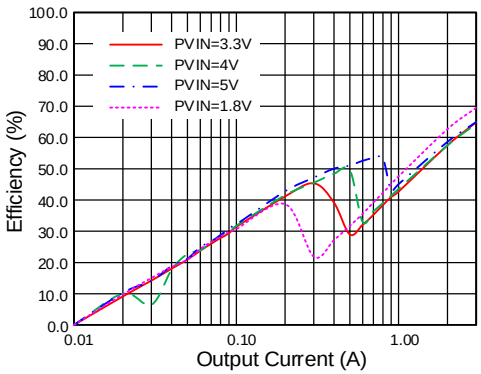
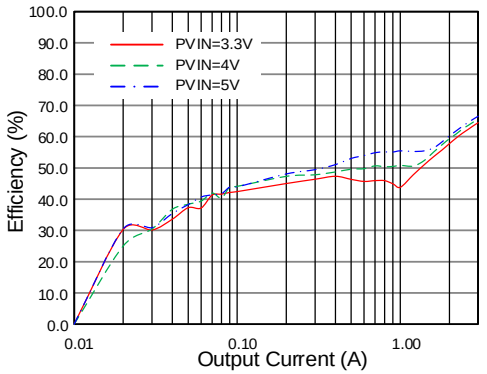
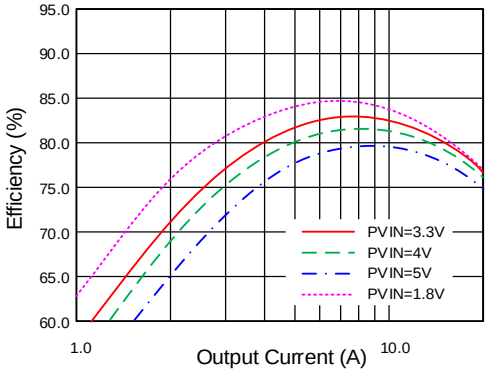


Efficiency vs. Load Current
(F_{SW}=10MHz, 0.4V_{OUT}, PFM, L=22nH/FP0404R1-R22)



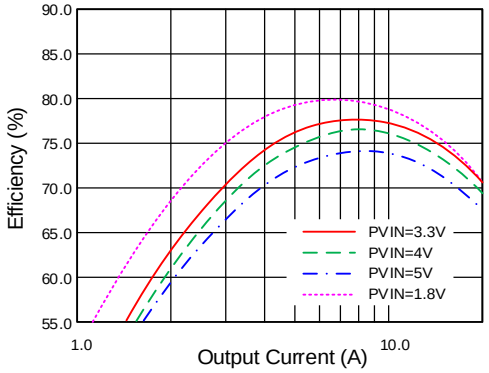
Efficiency vs. Load Current

(F_{SW}=3.3MHz, 0.5V_{OUT}, FCCM, L=65nH/WPZ04044S165NKT)



Efficiency vs. Load Current

(F_{SW}=5MHz, 0.5V_{OUT}, FCCM, L=42nH/CLT-32-42N)



Efficiency vs. Load Current

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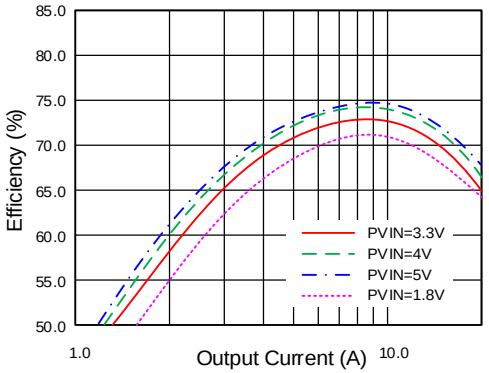
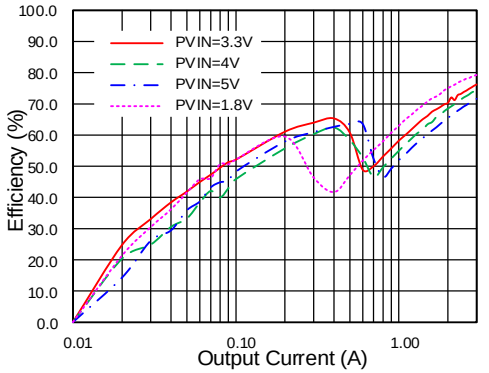


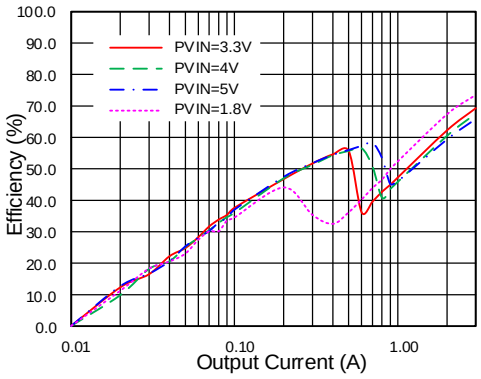
Efficiency vs. Load Current

(F_{SW}=3.3MHz, 0.5V_{OUT}, PFM, L=65nH/WPZ04044S165NKT)



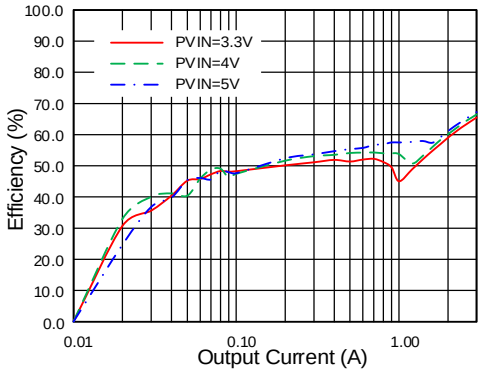
Efficiency vs. Load Current

(F_{SW}=5MHz, 0.5V_{OUT}, PFM, PFM, L=42nH/CLT-32-42N)



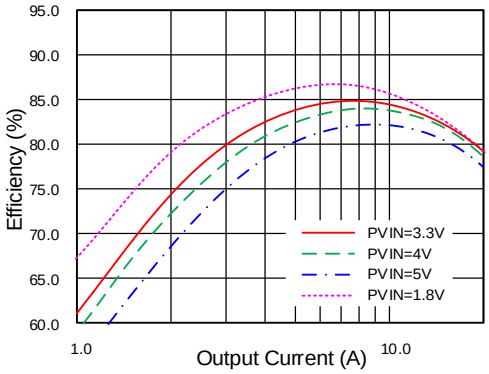
Efficiency vs. Load Current

(F_{SW}=10MHz, 0.5V_{OUT}, PFM, L=22nH/FP0404R1-R22)



Efficiency vs. Load Current

(F_{SW}=3.3MHz, 0.6V_{OUT}, FCCM, L=65nH/WPZ04044S165NKT)



Efficiency vs. Load Current

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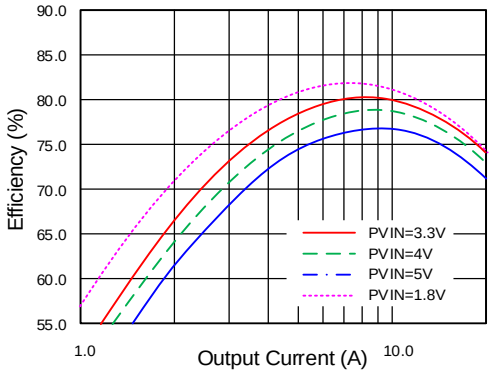

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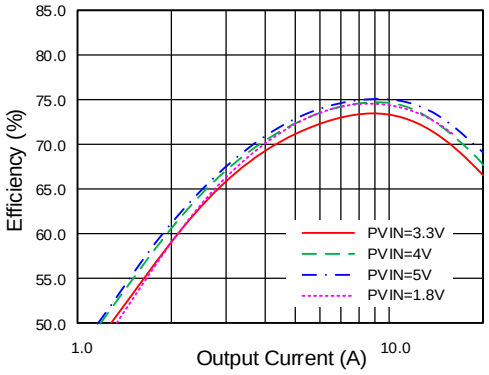
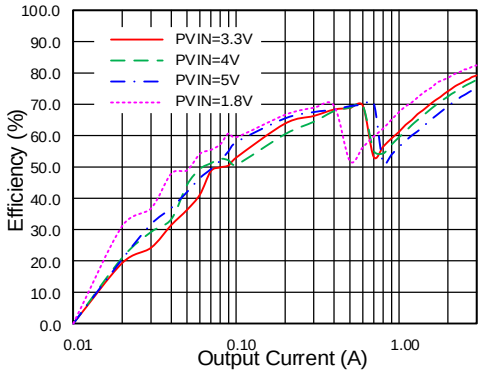


Efficiency vs. Load Current

(F_{SW}=3.3MHz, 0.6V_{OUT}, PFM, L=65nH/WPZ04044S165NKT)



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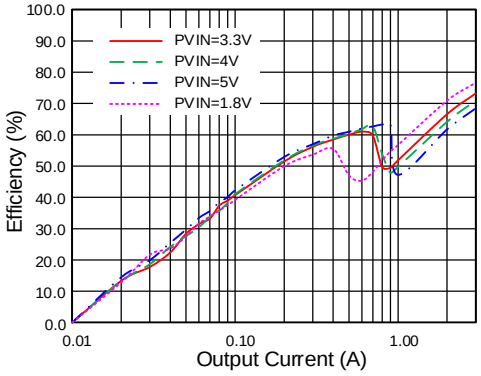
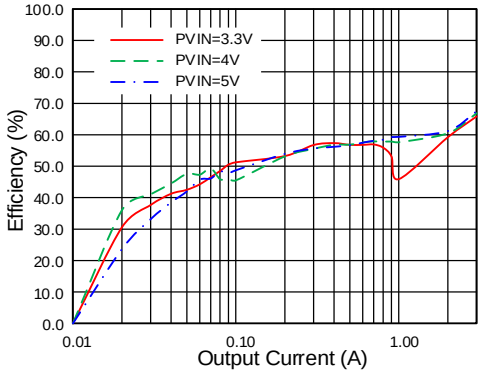


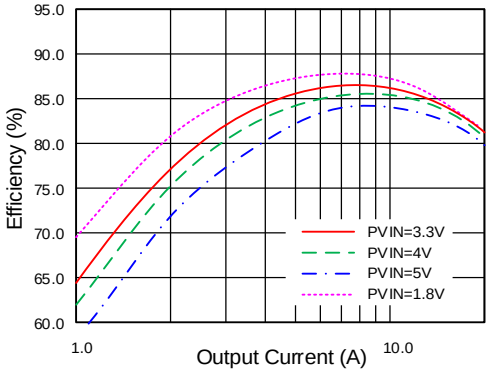
Efficiency vs. Load Current

(F_{SW}=10MHz, 0.6V_{OUT}, PFM, L=22nH/FP0404R1-R22)



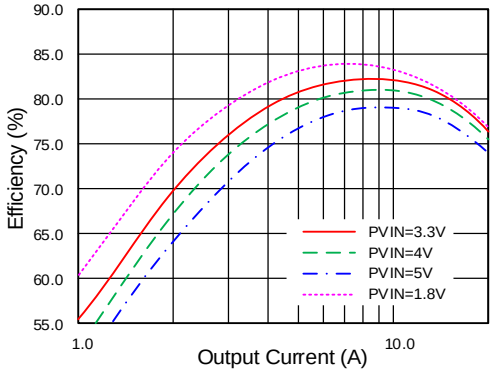
Efficiency vs. Load Current

(F_{SW}=3.3MHz, 0.7V_{OUT},FCCM, L=65nH/WPZ04044S165NKT)



Efficiency vs. Load Current

(F_{SW}=5MHz, 0.7V_{OUT}, FCCM, L=42nH/CLT-32-42N)



Efficiency vs. Load Current

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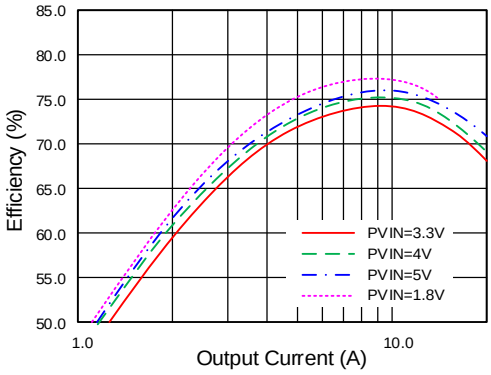
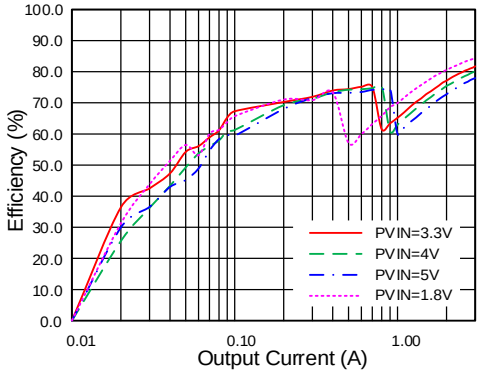


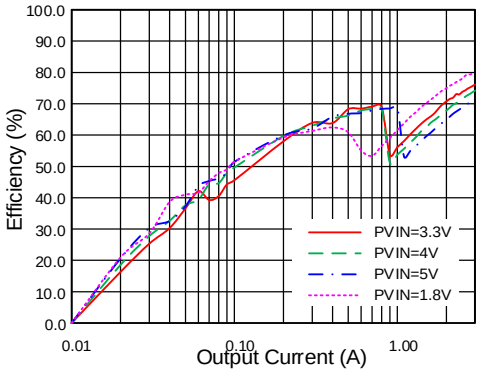
Efficiency vs. Load Current

(F_{SW}=3.3MHz, 0.7V_{OUT}, PFM, L=65nH/WPZ04044S165NKT)



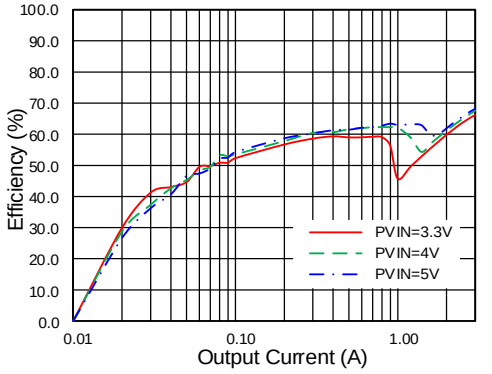
Efficiency vs. Load Current

(F_{SW}=5MHz, 0.7V_{OUT}, PFM, L=42nH/CLT-32-42N)



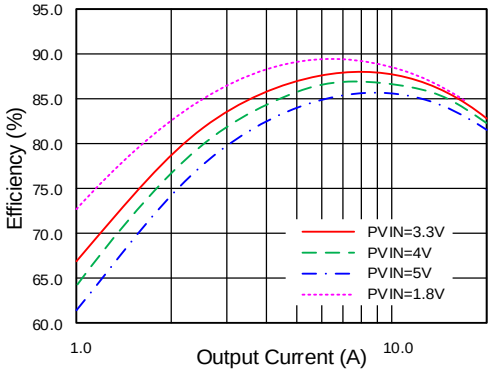
Efficiency vs. Load Current

(F_{SW}=10MHz, 0.7V_{OUT}, PFM, L=22nH/FP0404R1-R22)



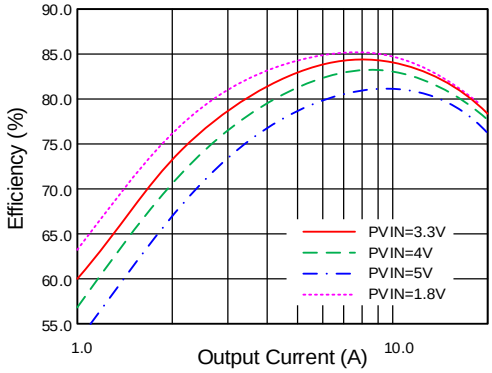
Efficiency vs. Load Current

(F_{SW}=3.3MHz, 0.8V_{OUT},FCCM, L=65nH/WPZ04044S165NKT)



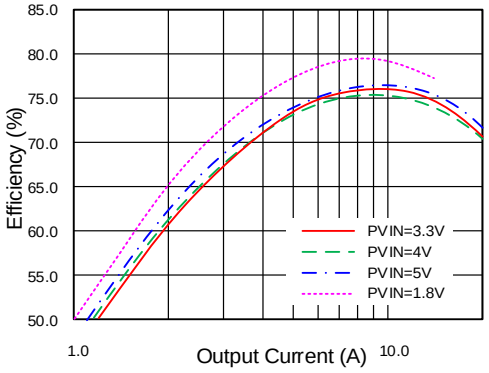
Efficiency vs. Load Current

(F_{SW}=5MHz, 0.8V_{OUT}, FCCM, L=42nH/CLT-32-42N)



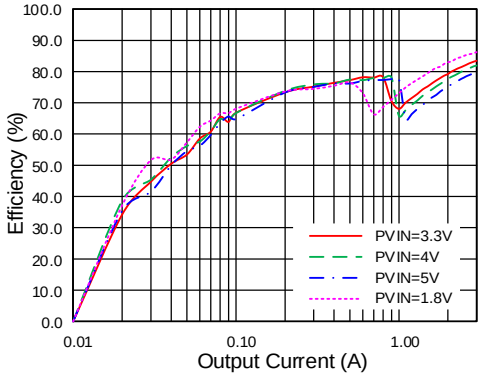
Efficiency vs. Load Current

(F_{SW}=10MHz, 0.8V_{OUT}, FCCM, L=22nH/FP0404R1-R22)



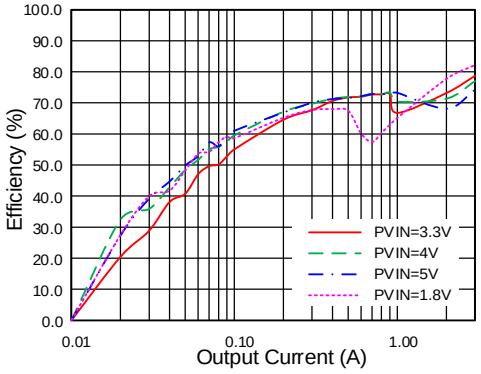
Efficiency vs. Load Current

(F_{SW}=3.3MHz, 0.8V_{OUT}, PFM, L=65nH/WPZ04044S165NKT)



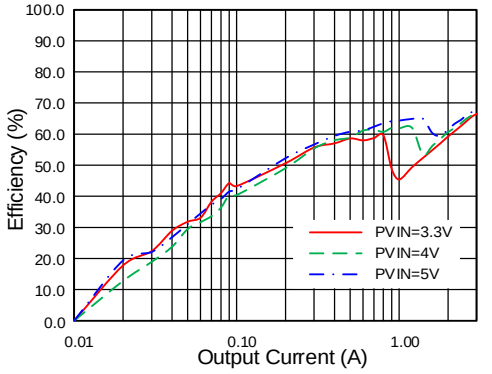
Efficiency vs. Load Current

(F_{SW}=5MHz, 0.8V_{OUT}, PFM, L=42nH/CLT-32-42N)



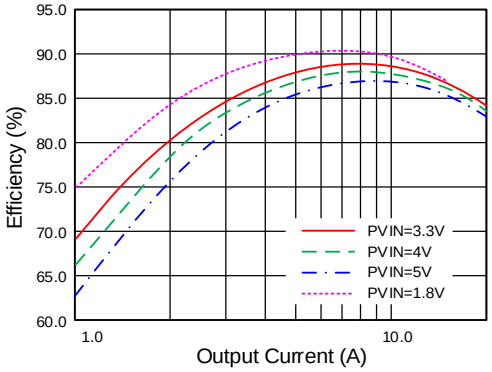
Efficiency vs. Load Current

(F_{SW}=10MHz, 0.8V_{OUT}, PFM, L=22nH/FP0404R1-R22)



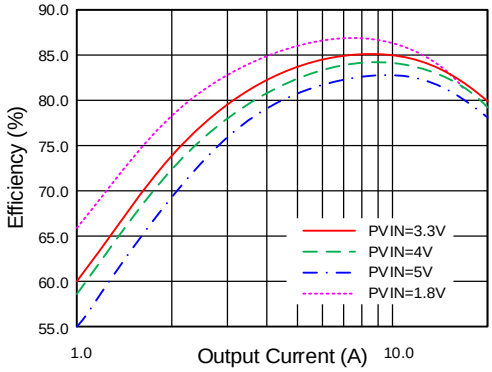
Efficiency vs. Load Current

(F_{SW}=3.3MHz, 0.9V_{OUT}, FCCM, L=65nH/WPZ04044S165NKT)



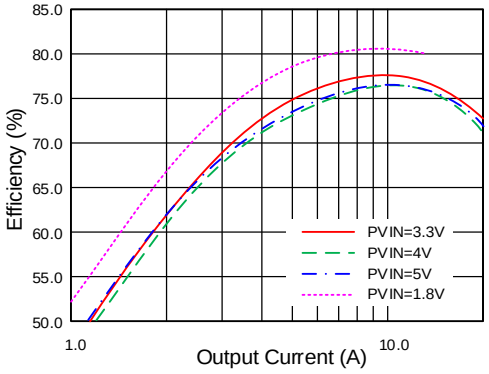
Efficiency vs. Load Current

(F_{SW}=5MHz, 0.9V_{OUT}, FCCM, L=42nH/CLT-32-42N)



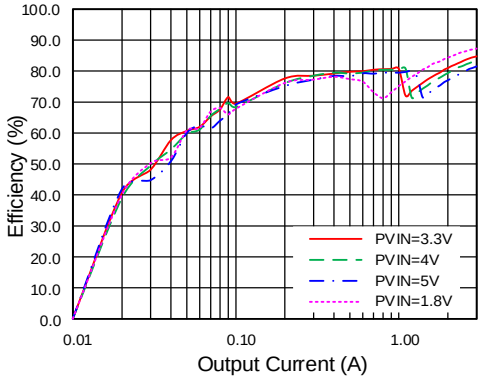
Efficiency vs. Load Current

(F_{SW}=10MHz, 0.9V_{OUT}, FCCM, L=22nH/FP0404R1-R22)



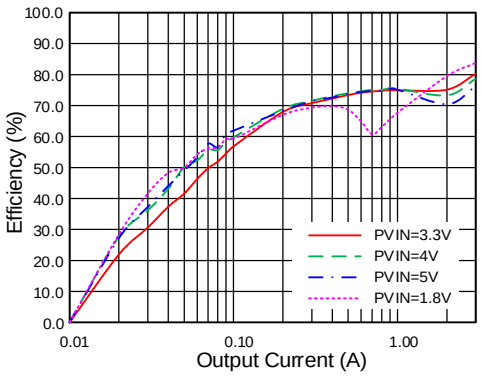
Efficiency vs. Load Current

(F_{SW}=3.3MHz, 0.9V_{OUT}, PFM, L=65nH/WPZ04044S165NKT)



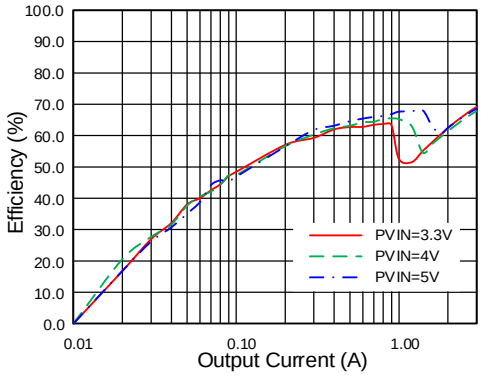
Efficiency vs. Load Current

(F_{SW}=5MHz, 0.8V_{OUT}, PFM, L=42nH/CLT-32-42N)



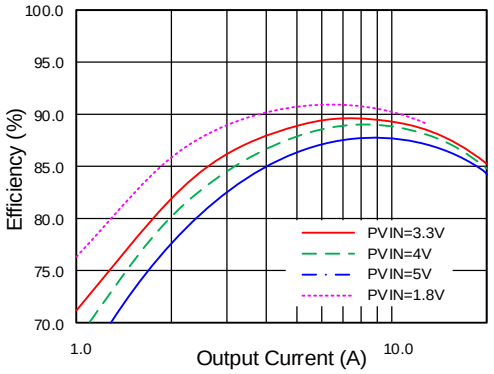
Efficiency vs. Load Current

(F_{SW}=10MHz, 0.9V_{OUT}, PFM, L=22nH/FP0404R1-R22)



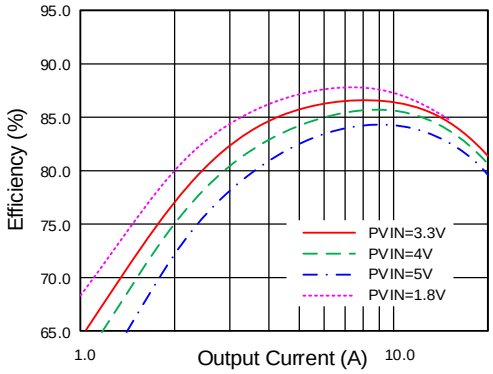
Efficiency vs. Load Current

(F_{SW}=3.3MHz, 1.0V_{OUT}, FCCM, L=65nH/WPZ04044S165NKT)



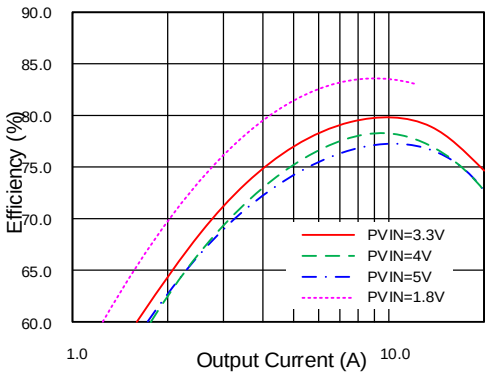
Efficiency vs. Load Current

(F_{SW}=5MHz, 1.0V_{OUT}, FCCM, L=42nH/CLT-32-42N)



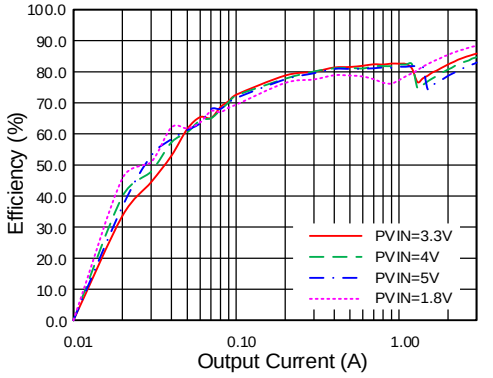
Efficiency vs. Load Current

(F_{SW}=10MHz, 1.0V_{OUT}, FCCM, L=22nH/FP0404R1-R22)



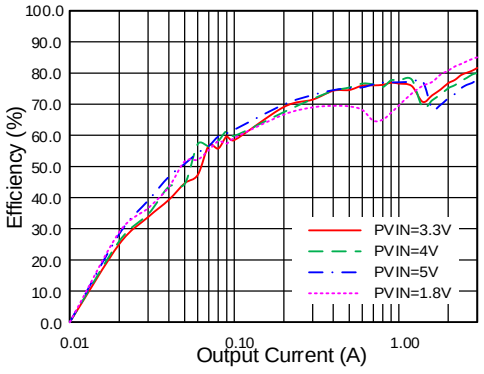
Efficiency vs. Load Current

(F_{SW}=3.3MHz, 1.0V_{OUT}, PFM, L=65nH/WPZ04044S165NKT)



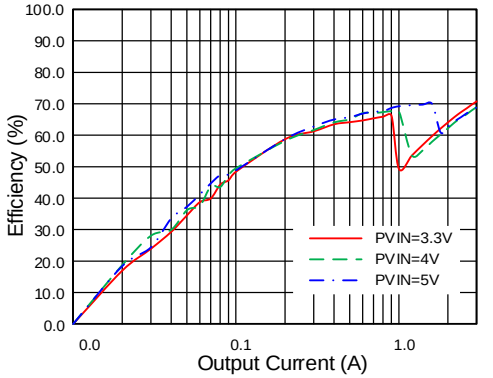
Efficiency vs. Load Current

(F_{SW}=5MHz, 1.0V_{OUT}, PFM, L=42nH/CLT-32-42N)



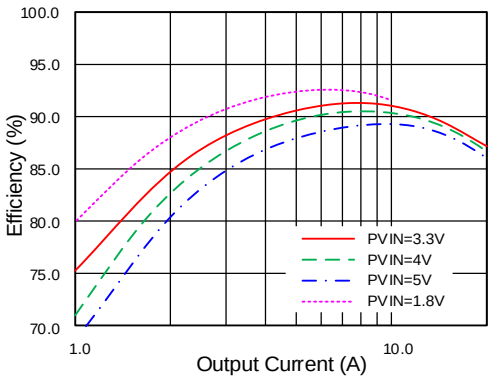
Efficiency vs. Load Current

(F_{SW}=10MHz, 1.0V_{OUT}, PFM, L=22nH/FP0404R1-R22)



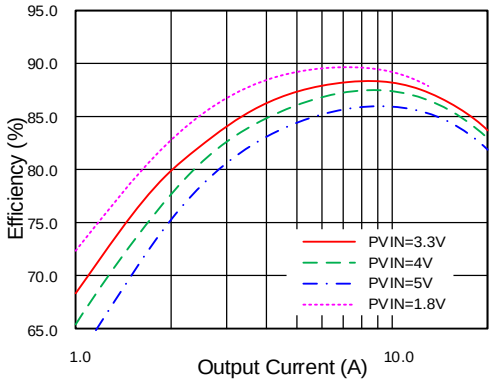
Efficiency vs. Load Current

(F_{SW}=3.3MHz, 1.2V_{OUT}, FCCM, L=65nH/WPZ04044S165NKT)



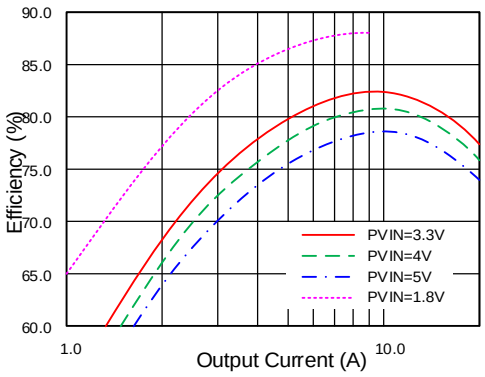
Efficiency vs. Load Current

(F_{SW}=5MHz, 1.2V_{OUT}, FCCM, L=42nH/CLT-32-42N)

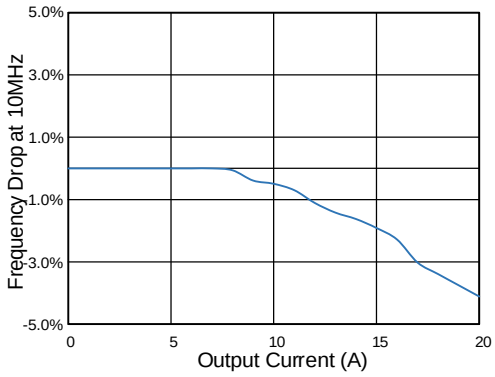


Efficiency vs. Load Current

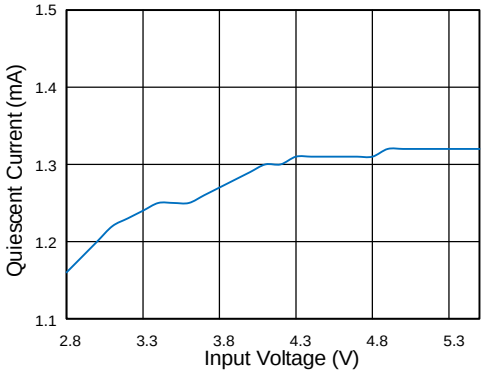
(F_{SW}=10MHz, 1.2V_{OUT}, FCCM, L=22nH/FP0404R1-R22)



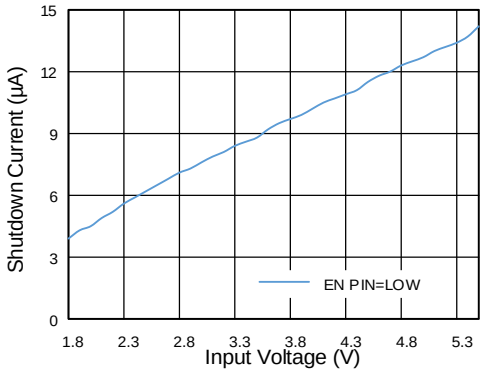
Frequency vs. Load Current



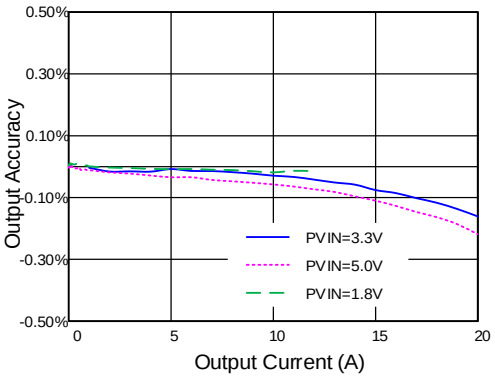
Quiescent Current



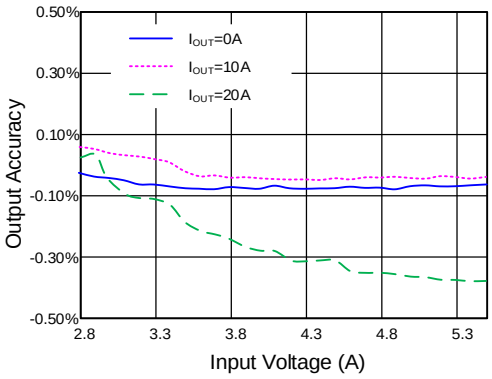
Shutdown Current



Load Regulation

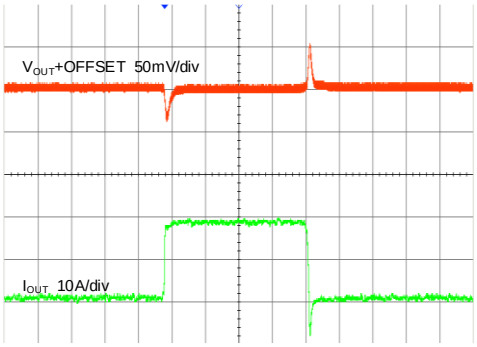


Line Regulation



Load Transient

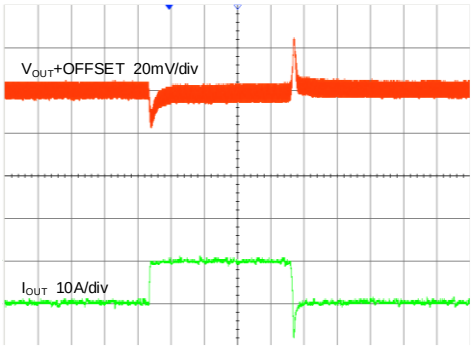
(FCCM, 10MHz, L=22nH, I_{OUT}=0.01~20A/100ns)



Time (5µs/div)

Load Transient

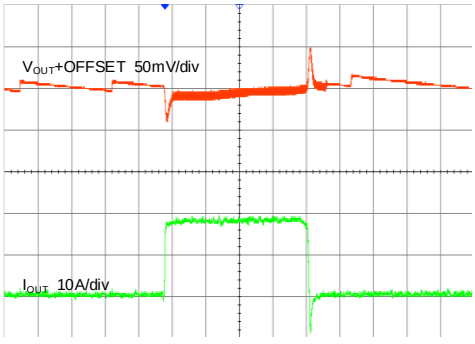
(FCCM, 10MHz, 1.8PV_{IN}, 0.6V_{OUT}, L=17nH, I_{OUT}=0.01~10A/100ns)



Time (5µs/div)

Load Transient

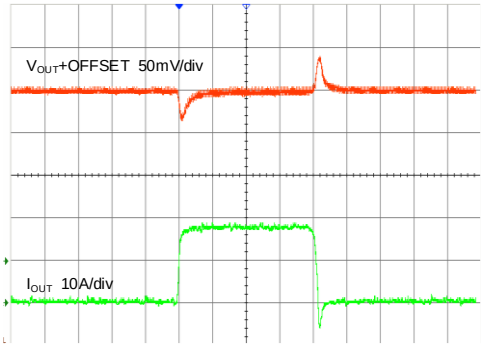
(PFM, 10MHz, L=22nH, I_{OUT}=0.01~20A/100ns)



Time (5µs/div)

Load Transient

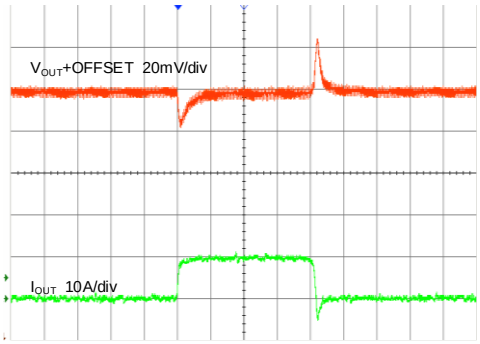
(FCCM, 5MHz, L=42nH, I_{OUT}=0.01~20A/1µs)



Time (5µs/div)

Load Transient

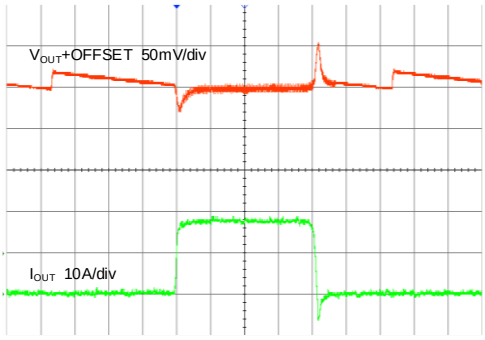
(FCCM, 5MHz, 1.8PV$_{IN}$, 0.6V$_{OUT}$, L=33nH, I$_{OUT}$=0.01~10A/1μs)



Time (5μs/div)

Load Transient

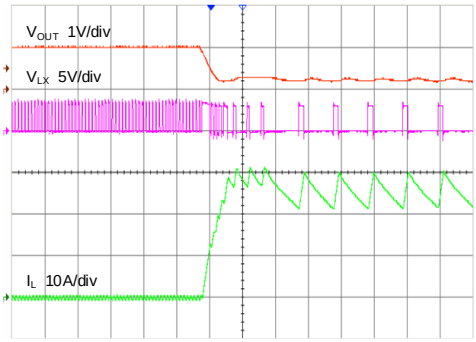
(PFM, 5MHz, L=42nH, I$_{OUT}$=0.01~20A/1μs)



Time (5μs/div)

Zoom-in Short Circuit Protection

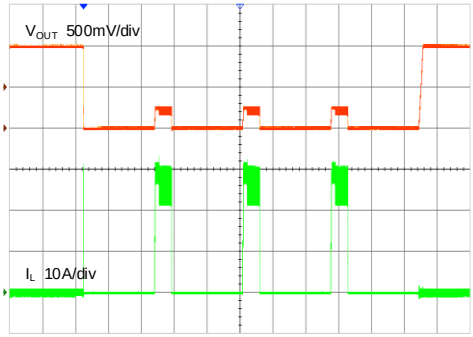
(I$_{OUT}$=0A~short, L$_{OUT}$=wire(33nH)



Time (5μs/div)

Short Circuit Protection

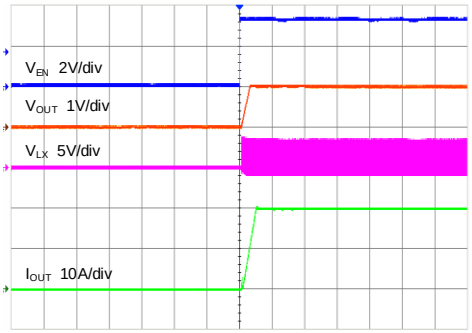
(I$_{OUT}$=0A~short, L$_{OUT}$=wire(33nH)



Time (10ms/div)

Startup from EN Pin

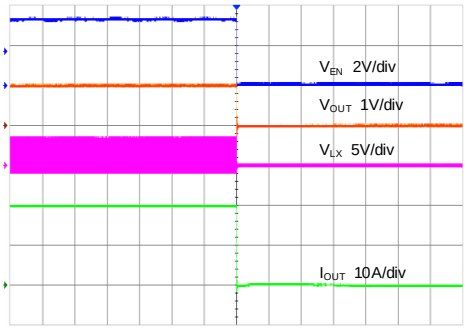
(V$_{IN}$=3.3V, V$_{OUT}$=1V, I$_{OUT}$=20A)



Time (5ms/div)

Shutdown from EN Pin

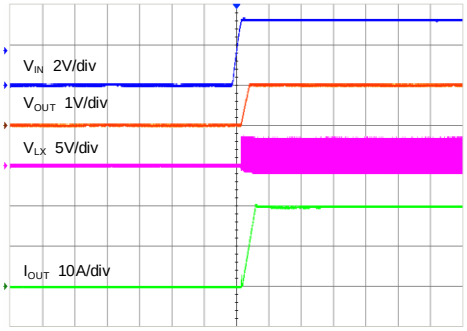
(V$_{IN}$=3.3V, V$_{OUT}$=1V, I$_{OUT}$=20A)



Time (5ms/div)

Startup from V_{IN}

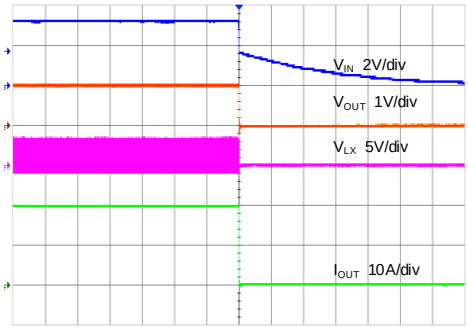
(V_{IN}=3.3V, V_{OUT}=1V, I_{OUT}=20A)



Time (5ms/div)

Shutdown from V_{IN}

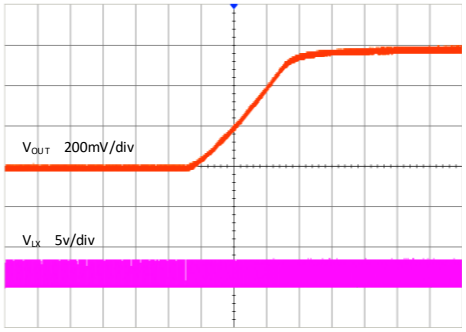
(V_{IN}=3.3V, V_{OUT}=1V, I_{OUT}=20A)



Time (5ms/div)

Dynamic Voltage Scaling

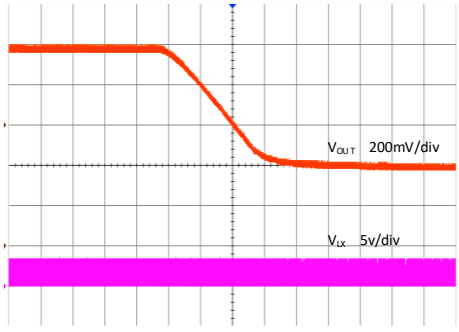
(DVS_SlewRate=17.5mV/µs, Reg"0x01"[1]=0, V_{OUT}=0.4→1V)



Time (10µs/div)

Dynamic Voltage Scaling

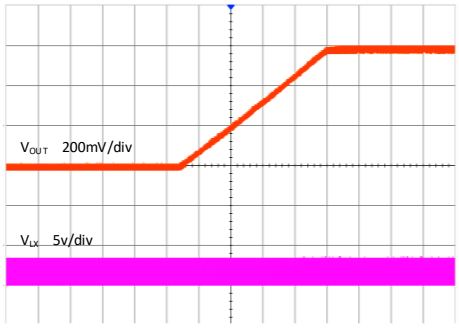
(DVS_SlewRate=17.5mV/µs,Reg"0x01"[1]=0, V_{OUT}=1→0.4V)



Time (10µs/div)

Dynamic Voltage Scaling

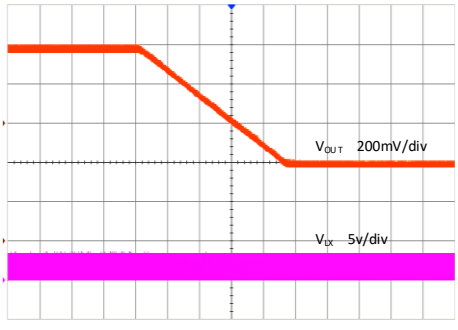
(DVS_SlewRate=2.5mV/µs, Reg"0x01"[1]=1, V_{OUT}=0.4→1V)



Time (50µs/div)

Dynamic Voltage Scaling

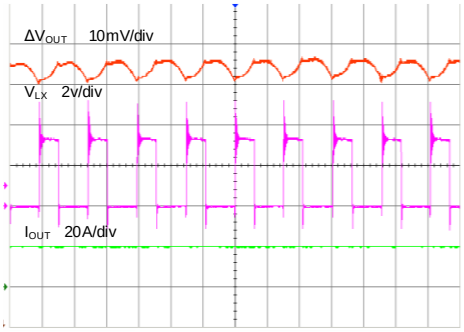
(DVS_SlewRate=2.5mV/µs, Reg"0x01"[1]=1, V_{OUT}=1→0.4V)



Time (50µs/div)

Output Ripple

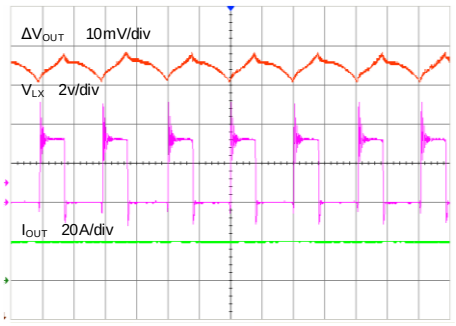
(3.3MHz, FCCM, L=80nH, I_{OUT}=20A)



Time (200ns/div)

Output Ripple

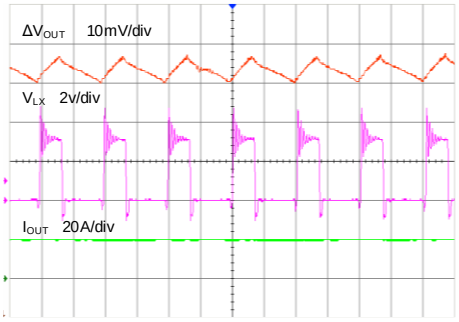
(5MHz, FCCM, L=42nH, I_{OUT}=20A)



Time (100ns/div)

Output Ripple

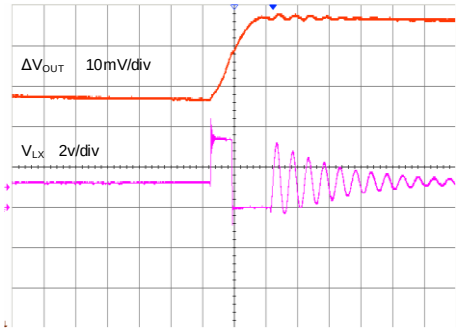
(10MHz, FCCM, L=22nH, I_{OUT}=20A)



Time (50ns/div)

Output Ripple

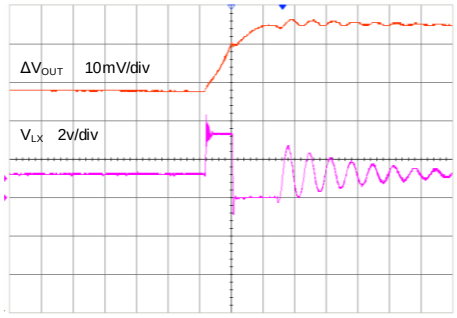
(3.3MHz, PFM, L=80nH, I_{OUT}=0.01A)



Time (200ns/div)

Output Ripple

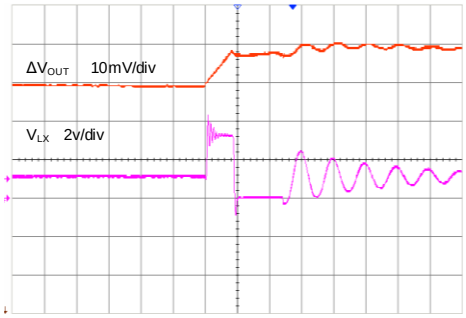
(5MHz, PFM, L=42nH, I_{OUT}=0.01A)



Time (100ns/div)

Output Ripple

(10MHz, PFM, L=22nH, I_{OUT}=0.01A)



Time (50ns/div)

Detailed Description

1 Ripple-Based Constant-on-Time Architecture

The SY20372 is a constant on-time controlled step-down DC-DC regulator. An internal triangular ripple is generated to mimic the inductor current. The output feedback and reference voltage generate a control voltage. When the ripple drops below the control voltage, the top FET is turned on for a fixed on-time. The on-time (t_{ON}) is internally calculated as $(V_{OUT}/V_{IN})\times(1/f_{SW})$ to operate the regulator at the desired switching frequency over the input and output voltage range.

The SY20372 utilizes a high bandwidth error amplifier and a fast comparator to minimize the PWM delay in the control loop for high frequency operation.

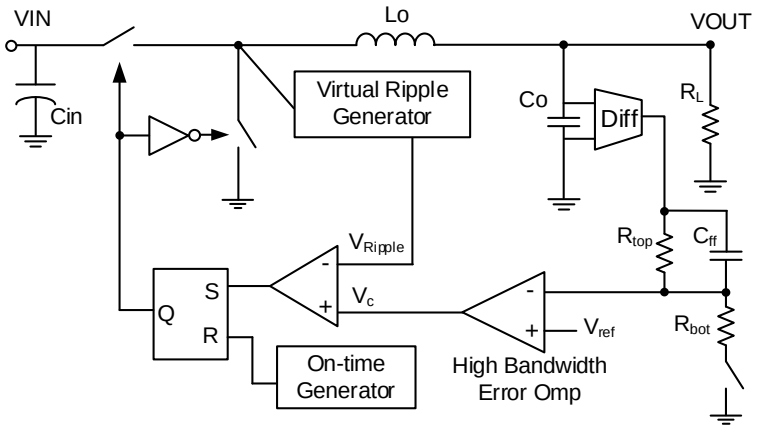


Figure 6. Ripple-based Control Scheme

2 Minimum On Time and Minimum Off Time

When SY20372 is configured to work with high input voltage and low output voltage at the 10MHz set switching frequency, it could operate with small PWM duty cycle and minimum on time. Under this scenario, the f_{SW} is automatically reduced to maintain regulation. Conversely, when operates with large PWM duty cycle and minimum off time, the f_{SW} is automatically reduced too.

3 Frequency Locked Loop (FLL)

The natural operating frequency of a COT based DC-DC converter may vary due to different operating conditions, such as input/output voltages, output loading changes. The SY20372 employs proprietary FLL technology to minimize the switching frequency variation by comparing the actual operating frequency with the desired switching frequency, and dynamically adjusting t_{ON}.

The FLL function is disabled during soft-start condition. FLL does not affect the High Side Power FET on-time during fast load transients.

4 Forced CCM Auto-Stretch Logic

For High Switching-Frequency (HF) dc-dc regulator, smaller inductor and output capacitor can be used for superior power density. But when the load of HF regulator steps down from heavy load, such as 20A to 0A, the device is very easily overshot to higher level because of small output cap. If the device operates at PFM mode and random full-null-full load transient occurs, the output voltage could lose control and the device could be easily damaged.

The SY20372 features Forced CCM stretch logic to handle this situation. By integrating a high accuracy average current sensing function, the device can judge the right time to quit FCCM operation, regulate with FCCM stretching time (2μs is for this device) when high to low load transition happens (7A is for this device's high current setting level). The following waveform shows fast load transient performance under PFM operation with/without Forced CCM Stretch Logic.

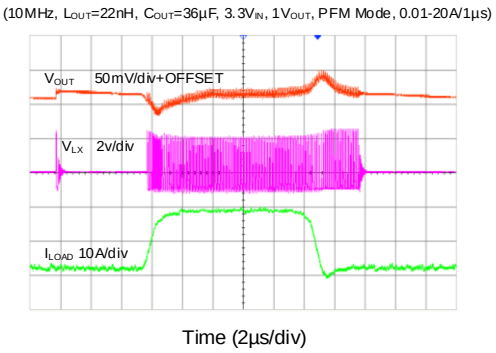


Figure 7. Forced CCM Auto-Stretch Logic Waveform

5 Differential Remote Sense (VOS, RTN)

The SY20372 provides differential remote sense capability through VOS and RTN pins. This pair of pins should be routed to directly sense at the output capacitor or at the load, thus compensating the DC voltage drop along the PCB traces which carry high current.

6 Linear Regulator (VCC and VCCFILT pins)

The VCC pin supplies internal power FET drivers, whereas VCCFILT supplies the rest of internal circuitries. The VCC pin is driven by an internal linear regulator, which produces 3.3V by default, with a minimum 4.3µF low ESR ceramic capacitor connected from VCC to GND.

The VCCFILT pin should be connected to VCC through a low-pass filter, typical value of 0.2Ω resistor and 1µF low ESR ceramic capacitor are recommended. It is shown in Figure 8.

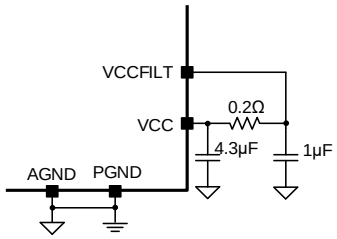


Figure 8. VCC and VCCFILT Pin Configuration

7 External Bootstrap Capacitor (C_{BST})

Proper operation requires a 0.22µF low ESR ceramic capacitor to be connected between BST pin and LX pin. This bootstrap capacitor provides the gate driver supply voltage for the high-side power MOSFET. C_{BST} voltage is refreshed by VCC when LSFET is on.

8 Enable Control

When EN pin is pulled low, the power stage and most of the internal circuitry are disabled. When EN toggles from low to high, the logic circuitry is active and the device is ready to accept I^2C command. Under this condition, the device can start and stop switching operation according to the setting of EN bit ("Register 0x01" [6]). The logic truth table is shown in Table 1.

Table 1. Enable Control

EN pin	EN bit	Status
0	x	Disable
1	0	Disable
1	1	Enable

Protection Features

The SY20372 has integrated input and output over voltage (OVP), output under voltage (UVP), output short circuit (SCP), thermal warning and thermal shutdown protection features.

Table 2. Protection Features

Protection	Threshold	Deglitch Time	Operation
Thermal Shutdown	Rising: 160°C Falling: 140°C	-	Shutdown when temperature rises above 160°C Restart when temperature falls below 140°C Record to FLT_TEMP_SD bit(“Register 0x05” [5]).
Thermal Warning	Rising: 110°C Falling: 90°C	-	Warning when temperature rises above 110°C Remove when temperature falls below 90°C Record to FLT_TEMP_DIE bit(“Register0x05” [4]).
Output UVP	80%*V_{set}	100μs	Hiccup mode auto recover. Record to FLT_VO_UVP bit(“Register0x05” [3]).
Output SCP	40%*V_{set}	10μs	Hiccup mode auto recover. Record to FLT_VO_SCP bit(“Register 0x05” [7]).
Output OVP	120%*Vset		Stop switching when V_{OUT}>120%*Vset Resume switching when V_{OUT}<117%*Vset Record to FLT_VO_OV bit (“Register 0x05” [6]).
Input OVP	5.8V	4μs	Shutdown when PVIN or AVIN>5.8V, Restart when PVIN and AVIN<5.6V Record to FLT_AVIN_OV bit(“Register 0x05” [2]). Record to FLT_PVIN_OV bit(“Register 0x05” [1]).

Note: Hiccup mode means to turn off 16 times of the soft-start time then to turn on 4 times of the soft-start time, repeatedly.

1 Thermal Shutdown and Thermal Warning

The SY20372 provides thermal warning function and thermal shutdown protection. If the junction temperature is higher than 110°C, the thermal warning [FLT_TEMP_DIE] bit will be set to 1. The bit can be reset to 0 after I²C read and the temperature drops below 90°C. The thermal warning function is activated once the EN pin is pulled high.

As the temperature goes higher, the device goes into thermal shutdown when the junction temperature exceeds 160°C. In this mode, the HSFET and LSFET are turned off, and the thermal shutdown [FLT_TEMP_SD] bit will be set to 1. When the junction temperature falls below 140°C, the IC will be re-enabled automatically, and the [FLT_TEMP_SD] bit will be reset to 0 after I²C read.

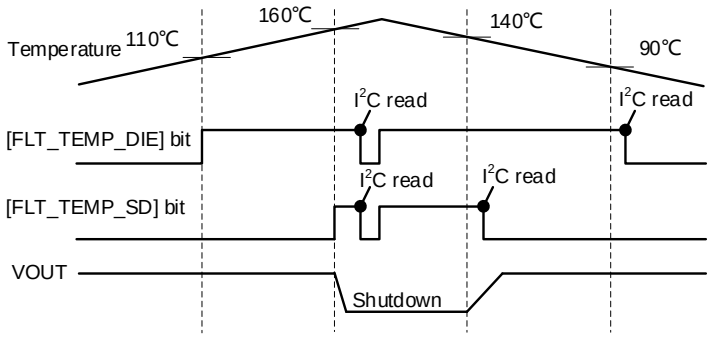


Figure 9. Thermal Shutdown and Thermal Warning Conditions

2 Cycle-by-Cycle Current Limit

The SY20372 integrates total three current limits to prevent device damage by limiting the maximum and minimum inductor current under all operating conditions.

During HSFET on time, when I_{PLMT} is reached and detected, HSFET is turned off and LSFET is turned on, even if on time timer has not expired.

In forced-CCM mode, the SY20372 also implements a negative current limit I_{NLMT}. During LSFET on time, when I_{NLMT} is reached and detected, LSFET is turned off and HSFET is turned on, regardless the command from the control loop, to prevent excessive negative inductor current.

A third current limit, I_{VLMT} is implemented as a prerequisite for the next HSFET turn on event. During LSFET on time, the inductor current must fall below I_{VLMT} before the command from the control loop to turn on the HSFET is allowed. This sets a maximum limit to the starting point of inductor current when it ramps up (HSFET is on), and helps to limit the peak inductor current under certain extreme operating scenarios. In order to reduce power consumption, the current limit threshold I_{VLMT} will be reduced to I_{VLMT_FDB} when inductor current reaches I_{PLMT} three times in a row. For example, when the device operates at 10MHz switching frequency, and very small duty cycle, I_{PLMT} is reached but not detected due to the short HSFET on time, which is smaller than peak current detection blanking time.

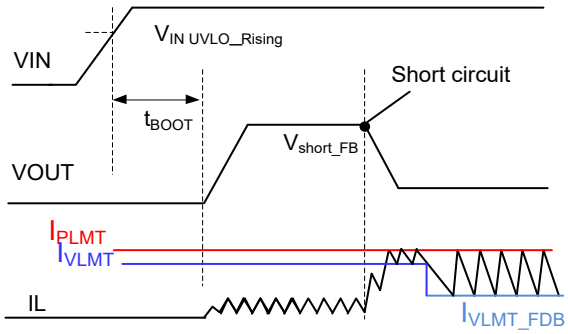


Figure 10. Current Limit Condition

3 Short Circuit Protection

In a short circuit condition, the current to the load exceeds the current to the output capacitor thus the output voltage tends to fall. As soon as the output voltage falls lower than 40% of target voltage for a duration of 10μs, the regulator will enter hiccup mode. After hiccup mode off time, the soft start will be turned on and the device will try to recover from short circuit. The device repeats this mode until the short circuit condition removes.

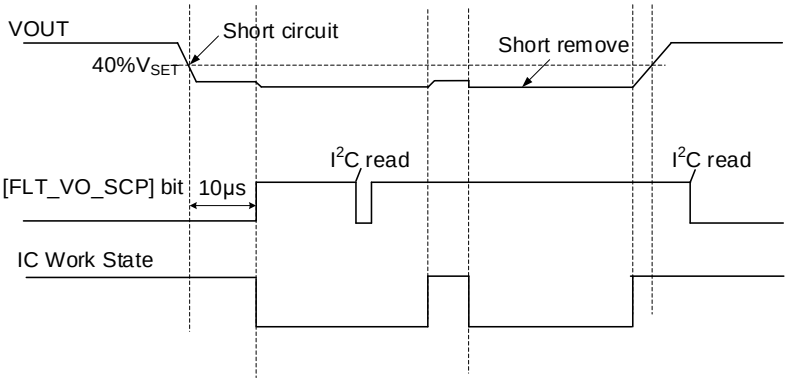


Figure 11. Short Circuit Protection Condition

4 Under Voltage Protection

Similar to short circuit protection, the SY20372 also incorporates under voltage protection function. When the output voltage drops below 80% of the target voltage for a duration of 100μs, the regulator will enter hiccup mode. This restarting pattern will continue until the over load condition is removed. The OC fault detection is disabled during the normal power up, shutdown and Dynamic Voltage Scaling (DVS).

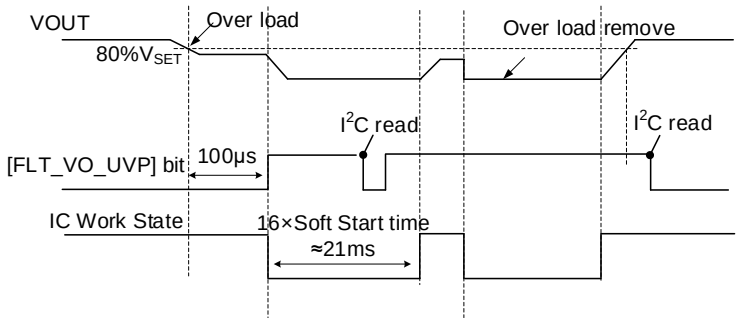


Figure 12. Under Voltage Protection Condition

5 Output Overvoltage Protection

When the output voltage reaches 120%*VSET, the regulator will enter no switching mode. Both high side and low side MOSFETS are turned off until the output voltage drops below 117%*V_{SET}.

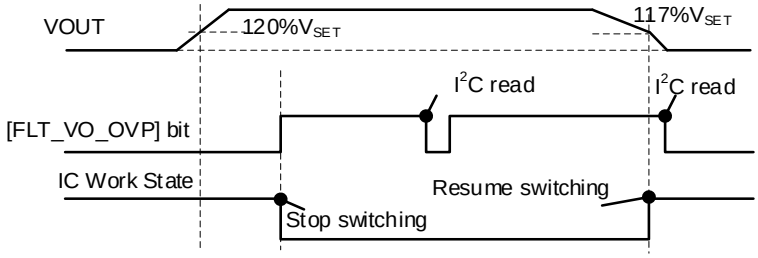


Figure 13. Output Overvoltage Protection Condition

6 Input Overvoltage Protection

The SY20372 provides input OVP function to protect the device from high voltage stress. When V_{IN} exceeds 5.8V, the regulator is turned off. When VIN decreases to 5.6V, the regulator restarts. The input OVP fault detection is activated once EN pin is pulled high.

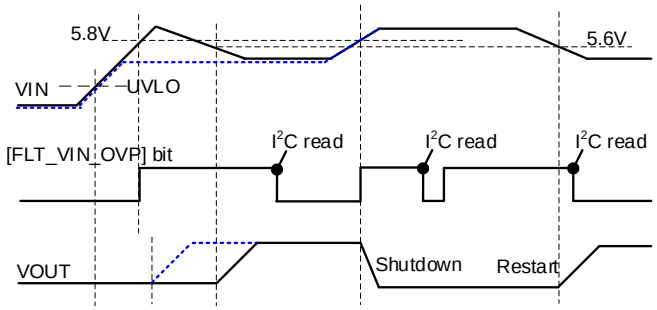


Figure 14. Input Overvoltage Protection Condition

Design Procedure

1 Input Capacitor Selection

Input filter capacitors are needed to reduce the ripple voltage on VIN pin caused by the switching current. X5R or X7R series ceramic capacitors are most often selected due to their small size, low cost, surge current capability and high RMS current ratings over a wide temperature and voltage range. When VIN pin is supplied by a long routing with higher parasitic inductance, to prevent device damage due to inductive voltage ringing, some bulk capacitance in parallel with ceramic capacitors is considered helpful. These bulk capacitors can be electrolytic, tantalum or polymer capacitors.

The max RMS ripple current of input capacitor can be calculate as:

$$I_{cin\_RMS} = I_{out} \times \sqrt{D(1-D)}$$

The input capacitor should have RMS current rating greater than half of the maximum load current when D=0.5.
Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated as:

$$V_{cin\_ripple} = \frac{D(1-D)I_{out}}{f_s \times C_{in}}$$

D=0.5 is considered as the worst case.

Four 10μF and two 1μF capacitors are sufficient in most applications. Place the ceramic input capacitor as close to the VIN and GND pins as possible.

2 Inductor Selection

The inductor selection is trade-off between efficiency, size and transient performance for the application. A lower inductance helps to reduce the size and enhance transient response, but it increases inductor ripple current and output voltage ripple. The low DC resistance (DCR) inductors usually reduces DC losses and increases efficiency. For the same size inductance series, higher inductor values tend to have higher DCR and slower transient response. Below are three considerations for choosing suitable inductor.

First, setting inductor ripple ΔIL equal to 20% ~ 40% of the desired full load current to get an inductor value range, describing as :

$$L_o = \frac{V_{out} \times (V_{in} - V_{out})}{V_{in} \times f_{sw} \times \Delta I_L}$$

Consider a typical application of 3.3V V_{IN}, 1V V_{OUT}, 20A full load current, operating at 10MHz, using a target inductor ripple current ΔI_L of 25% or 4A, the approximate inductance effective value is 17nH. Considering the inductor typical ±15% tolerance and de-rating at high DC current, 22nH, 42nH, 65nH is the true inductor component number for 10MHz, 5MHz and 3.3MHz respectively..

Second, select the nearest standard value, and choose the inductor with saturation current higher than the I_{PEAK}:

$$I_{peak} = I_{out\_max} + \frac{\Delta I_L}{2}$$

Finally, select the inductor with relatively low DCR which meets the value, size and cost requirements.

3 Output Capacitor Selection

The output ripple with 10MHz switching frequency is much different from conventional low frequency Buck regulator. As the Equivalent Series Inductance (ESL) at 10MHz is much larger than that at 2MHz, the output ripple is dominated by ESL caused square wave. Several small sized capacitors with low ESL in parallel is recommended for low output ripple. Reverse package ceramic capacitor features much lower ESL, like Murata LLL series, NFM series and so on.

The total output capacitor ripple can be calculated as:

$$v_{OUT}(t) = v_{ESR}(t) + v_{ESL}(t) + v_{COUT}(t)$$

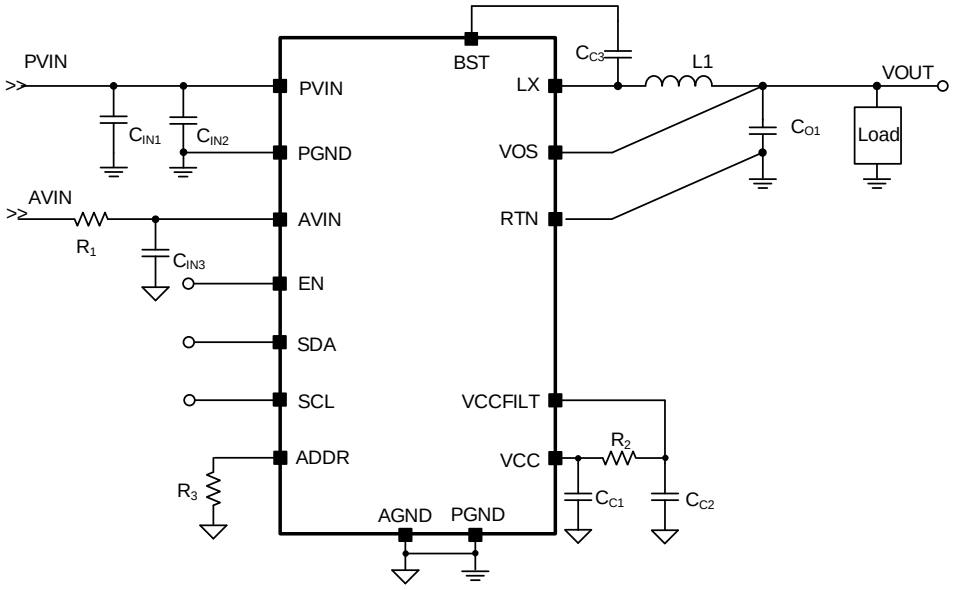
$0 \le t \le D \cdot T_{SW}$ (On-time Phase)

$$v_{ESR}(t) = R_{ESR}\left(\frac{\Delta I_L \cdot t}{D \cdot T_{SW}} - \frac{\Delta I_L}{2}\right) \quad v_{ESL}(t) = \frac{L_{ESL} \cdot \Delta I_L}{D \cdot T_{SW}} \quad v_{COUT}(t) = \frac{\Delta I_L \cdot t^2}{2C_{OUT} \cdot D \cdot T_{SW}} - \frac{\Delta I_L \cdot t}{2C_{OUT}} \quad 0 \le t \le D \cdot T_{SW}$$

$D \cdot T_{SW} \le t \le T_{SW}$ (Off-time Phase)

$$v_{ESR}(t) = R_{ESR}\left[\frac{\Delta I_L}{2} - \frac{\Delta I_L \cdot (t - D \cdot T_{SW})}{(1-D) \cdot T_{SW}}\right] \quad v_{ESL}(t) = \frac{L_{ESL} \cdot \Delta I_L}{(1-D) \cdot T_{SW}} \quad v_{COUT}(t) = \frac{\Delta I_L \cdot (t - D \cdot T_{SW})}{2C_{OUT}} - \frac{\Delta I_L \cdot (t - D \cdot T_{SW})^2}{2C_{OUT} \cdot (1-D) \cdot T_{SW}} \quad D \cdot T_{SW} \le t \le T_{SW}$$

Application Schematic



Output voltage set point is 1V, the power input voltage is from 1.8V to 5.5V, the analog input voltage is fixed 3.3V. The switching frequency is set through I²C registers. The soft-start time is 1.3ms. By following the detailed design procedure, the relevant power stage components are listed in Table 3.

BOM List

Table 3. Bill of Materials (V_{PVIN} = 1.8V to 5.5V, V_{AVIN} = 3.3V, V_{OUT} = 1V, I_{OUT} =20A, F_{SW} = 3.3/5/10MHz)

Designator	Description	Part Number	Manufacturer	Quantity
C_{IN1}	CAP, CERM, 22μF, 6.3V, ±20%, X5R, 0402	GRM158R60J226ME01DA	Murata	2
C_{IN2}	CAP, CERM, 1μF, 10V, ±10%, X7R, 0402	GRM155Z71A105KE01D	Murata	2
C_{IN3}	CAP, CERM, 10μF, 10V, ±20%, X5R, 0402	GRM155R61A106ME21D	Murata	1
C_{C1}	CAP, CERM, 4.7μF, 10V, ±10%, X5R, 0402	GRM155R61A475KEAAD	Murata	1
C_{C2}	CAP, CERM, 1μF, 10V, ±10%, X7R, 0402	GRM155Z71A105KE01D	Murata	1
C_{C3}	CAP, CERM, 220nF, 16V, ±10%, X7R, 0402	C1005X7R1C224K050BC	TDK	1
$L_{1@10MHz}$	IND, 22nH, 40A, 0.32mΩ, 4.0×4.0×3.0mm	FP0404R1-R022	EATON	1
$L_{1@5MHz}$	IND, 42nH, 52A, 1.0mΩ, 3.2×2.5×2.5mm	CLT-32-42N	TDK	1
$L_{1@3.3MHz}$	IND, 65nH, 40A, 0.30mΩ, 4.0×4.1×4.3mm	WPZ04044S165NKT	Sunlord	1
C_{O1}	CAP, CERM, 9.1μF, 4V, ±20%, 0402, X5R	NFM15PC915R0G3D	Murata	4
R_1	RES, 0Ω, 1%, 0.063W, 0402	RC0402FR-070RL	YAGEO	1
R_2, R_3	RES, 0.2Ω, 1%, 0.063W, 0402	RL0402FR-070R2L	YAGEO	2
U_1	SY20372 Synchronous Buck Regulator	SY20372QLQ	Silergy	1

PCB Design

The SY20372 is a high frequency switching regulator and proper PCB layout is critical for stable operation. For best results, refer to Figure 15 and follow the guidelines below.

- A four-layer PCB has its layers named layer 1, layer 2, layer 3 and layer 4 from top to bottom layer for easier description. Layer 2 should be a complete GND copper plane for shorten commutation path and noise immunity. The insulation thickness between layer 1 and layer 2 should be minimized to reduce input loop parasitic inductance, 75um is recommended for 1oz copper.
- Place VIN copper planes on layer 1 (top) and layer 4 (bottom) for form sandwich structure with the inner GND plane, to reduce parasitic impedance from the input MLCC to the SY20372. The VIN copper should be symmetrical for SY20372 VIN pins on both-sides, which can help the device to reduce EMI.
- Place as many PGND vias as possible underneath the package and close to the C_{IN} and C_{OUT} capacitors' pads to minimize both parasitic impedance and thermal resistance.
- Place input capacitors with small ESL as close as possible to the PVIN and PGND pins to reduce the parasitic PCB inductance, which can adversely affect operation. Place the major MLCC capacitors on the same layer as the SY20372.
- The VOS and RTN lines are used to sense the output voltage and should be routed directly to the load. Keep the VOS and RTN traces away from switching nodes or high-speed digital signals. Use same via in both traces to compensate for the delay between the traces.
- Avoid right-angle bends in a trace and try to route them at least with two 45° corners to minimize any VOS/RTN impedance change. Differential traces should be routed as close as possible to get a high coupling factor.

Place the BST cap and VCC/VCCFILT decoupling cap as close to the SY20372 pins as possible. Minimum the via number for the BST driving path. It's recommended to use a bootstrap cap of 0.22μF up to 1μF.

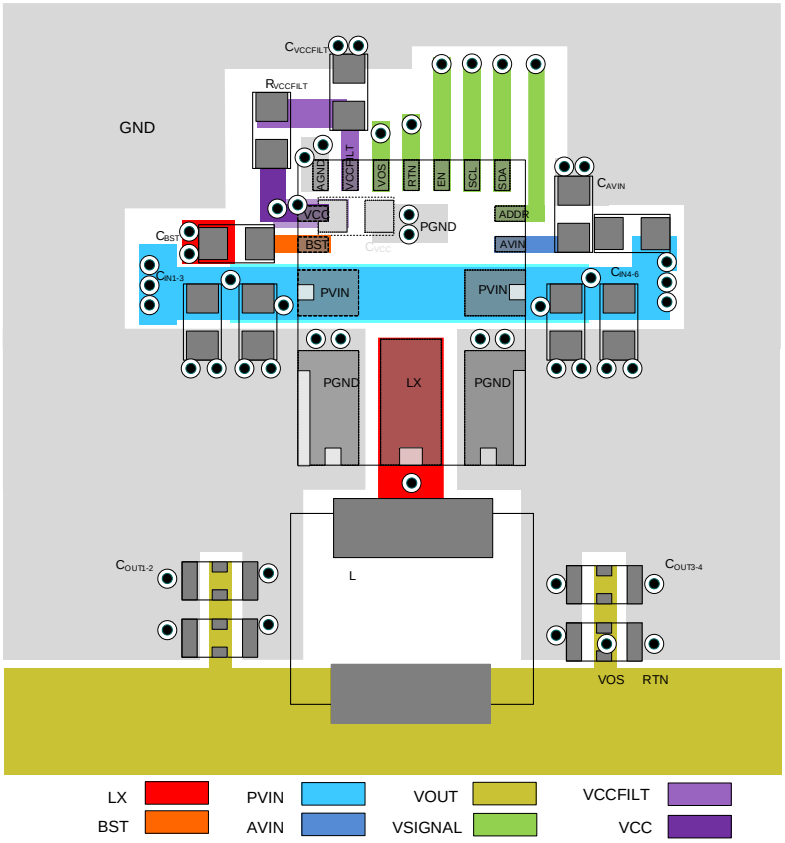


Figure 15. Recommended PCB Layout (top layer view)

I²C Compatible Interface

The SY20372 features an I²C interface that allows the HOST to set certain parameters and read out fault conditions. The I²C interface supports clock speed up to 3.4Mbps and uses standard I²C commands. Its I²C Device address is programmed by ADDR pin. The SY20372 always operates as a slave device, and is addressed using a 7-bit slave address followed by an 8th bit, which indicates whether the transaction is a read-operation or a write-operation. The I²C interface is fully functional after VIN is above V_{PORR} threshold, and EN pin pull high.

Table 4. I²C Device Address Configuration

ADDR Pin	I²C Device address
0Ω to GND	0x31
49.9kΩ to GND	0x32
200kΩ to GND	0x33
Floating or connect to VCC	0x34

START and STOP Conditions

The START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition. The I²C master always generates the START and STOP conditions.

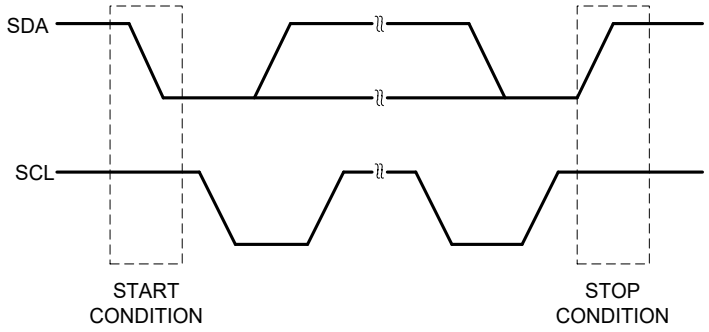


Figure 16. I²C START and STOP Conditions

Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

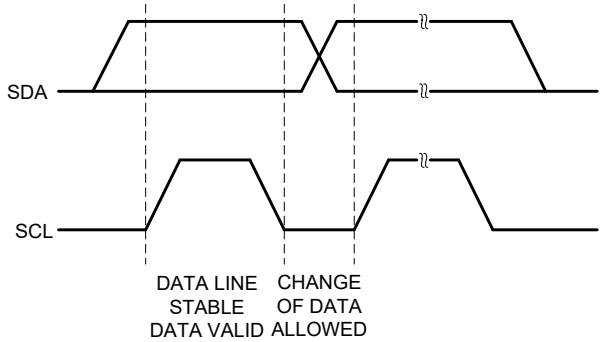


Figure 17. I²C Data Validity Condition

Acknowledge

Each address and data transmission uses 9-clock pulses. The ninth pulse is the acknowledge bit (ACK). After the START condition, the master sends 7-slave address bits and an R/$\overline{W}$ bit during the next 8-clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge. The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data.

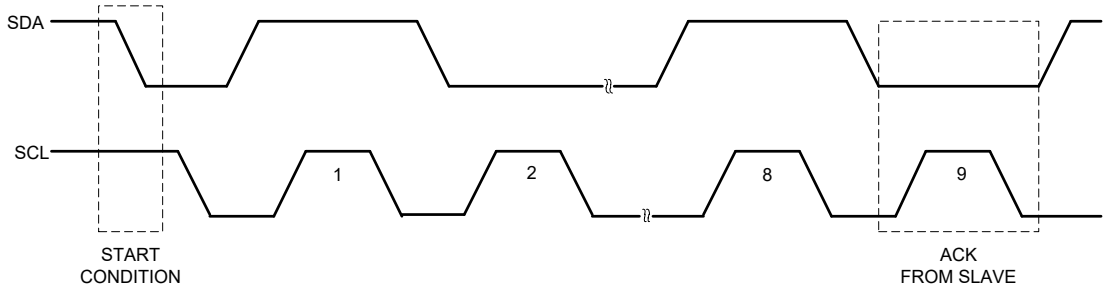


Figure 18. I²C Acknowledge Condition

Data Transactions

All transactions start with a control byte sent from the I²C master device. The control byte begins with a START condition, followed by 7-bits of slave address for the SY20372 (this address can be changed if necessary), followed by the 8th bit, R/$\overline{W}$ bit. The R/$\overline{W}$ bit is 0 for a write or 1 for a read. If any slave devices on the I²C bus recognize their address, they will acknowledge by pulling the SDA line low for the last clock cycle in the control byte. If no slaves exist at that address or are not ready to communicate, the data line will be 1, indicating a Not Acknowledge (NACK) condition. Once the control byte is sent, and the SY20372 acknowledges it, the 2nd byte sent by the master must be a register address byte. The register address byte tells the SY20372 which register the master will write or read. Once SY20372 receives a register address byte it responds with an acknowledge (ACK).

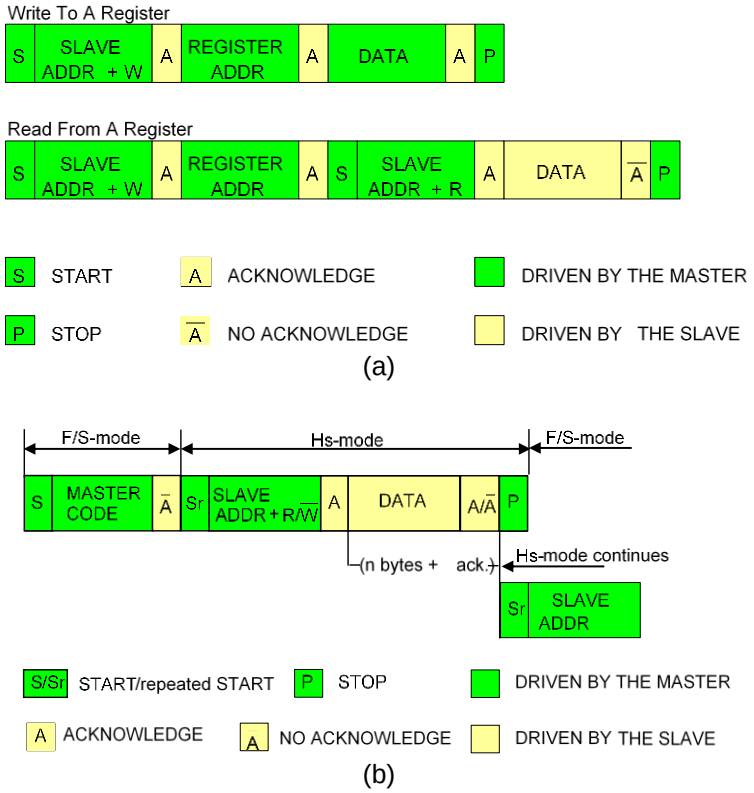


Figure 19. Data Transfer Format (a) in Standard/Fast Mode (b) in Hs-Mode

I²C Interface Timing Diagram

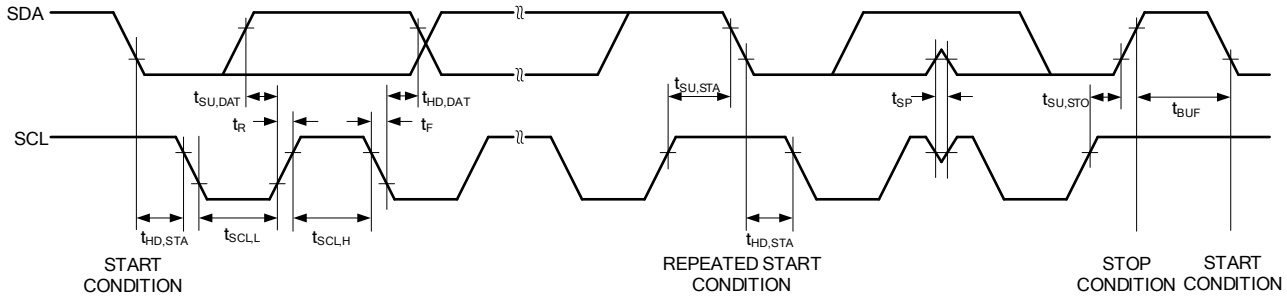


Table 5. I²C Specifications

Characteristics	Symbol	Units	Standard Mode		Fast Mode		High-Speed Mode	
			Min	Max	Min	Max	Min	Max
SCL Clock Frequency	f_{SCL}	kHz	0	100	0	400	0	3400
Hold Time (repeated) START Condition. (After this period, the first clock pulse is generated.)	$t_{HD;STA}$	μs	4		0.6		0.16	
LOW Period of the SCL Clock	t_{LOW}	μs	4.7		1.3		0.16	
HIGH Period of the SCL Clock	t_{HIGH}	μs	4		0.6		0.06	
Set-up Time for a Repeated START Condition	$t_{SU;STA}$	μs	4.7		0.6		0.16	
DATA in Hold Time	$t_{HD;DAT}$	ns	0	900	0	900	0	70
DATA out Hold Time	$t_{HD;DAT}$	ns		900		900		70
Data set-up Time	$t_{SU;DAT}$	ns	250		100		10	
Rise Time of both SDA and SCL Signals	t_r	ns		1000	5	300	5	40
Fall Time of both SDA and SCL Signals	t_f	ns		300	5	300	5	40
Set-up Time for STOP Condition	$t_{SU;STO}$	μs	4		0.6		0.16	
Bus Free Time between STOP and START Conditions	t_{BUF}	μs	4.7		1.3			
Capacitive Load for Each Bus Line	C_b	pF		400		400		100

Register Map

Table 6 Register Map

Address	Register
0x00	MTP_CTRL
0x01	FUNCTION_SETTING
0x02	VO_CTRL
0x04	LOOP_CTRL
0x05	FLT_RECORD

Register Settings

Table 7

MTP_CTRL (Address=0x00, default=00h)				
Bits	**Default**	**Name**	**R/W**	**Description**
7	0	MTP_R_EN	R/W	MTP read enable 0 disable 1 enable, MTP data can be read by I^2C This bit will auto reset to '0' when MTP read is finished
6	0	MTP_W_EN	R/W	MTP write enable 0 disable 1 enable This bit will auto reset to '0' when MTP write is finished
5	0	MTP EN	R/W	MTP write and read enable 0=MTP read/write disable, MTP block consume<1μA 1=MTP read/write enable, MTP block consume 260μA ~360μA when no R/W request from MTP. When programming "Reg 0x00" [5] = 1 to enable MTP, wait at least 100μs to enable MTP read or write bit.
4:0	000	Reserved	R/W	-

Table 8

FUNCTION_SETTING (Address=0x01, default=60h)				
Bits	**Default**	**Name**	**R/W**	**Description**
7	0	FB_RATIO	R/W	Feedback ratio 0 $V_{OUT}=V_{FB}$ 1 $V_{OUT}=1.5*V_{FB}$
6	1	ENABLE	R/W	Enable control 0 Disable 1 Enable
5	1	DISCHARGE	R/W	Discharge control 0 Disable discharge 1 Auto discharge
4:3	00	FRE_CTRL	R/W	Switching frequency setting 00=10MHz 01=5MHz 10=3.3MHz 11=3.3MHz
2	0	PFM	R/W	Light load operation 0 Forced PWM 1 Automatic PFM/PWM
1	0	DVS_SR	R/W	DVS slew rate select

				0 17.5mV/μs(when“Reg0x01”[7]=0) 25mV/μs(when“Reg0x01”[7]=1) 1 2.5mV/μs (when“Reg0x01”[7]=0) 3.7mV/μs(when“Reg0x01”[7]=1)
0	0	VCC_CTRL	R/W	VCC voltage control 0 3.3V 1 3.0V

Note: FB_RATIO/ FRE_CTRL/ PFM function is disable when EN pin high &REG0x01<6>=1.

Table 9

VO_CTRL (Address=0x02, default=78h)				
Bits	**Default**	**Name**	**R/W**	**Description**
7	0	-	R/W	
6:1	111100	VO_CTRL	R/W	When “Reg0x01”[7]=0, Feedback Reference Voltage range is 0.4V~1.0V, LSB = 10mV VO_CTRL = 400mV + DAC_DC_CTRL×10mV Ex: REF = 1V = 400mV + 60×10mV

Table 10

LOOP_CTRL (Address=0x04, default=08h)				
Bits	**Default**	**Name**	**R/W**	**Description**
7:4	00	Reserved	R/W	
3:1	100	KP_CTRL	R/W	Trim bits to set Verror ratio-gain compensation factor Verror=KP_CTRL*(Vref-Vo) 8(111): Vout drop 10mV, loop Vc see 80mV drop 7(110): Vout drop 10mV, loop Vc see 70mV drop 6(101): Vout drop 10mV, loop Vc see 60mV drop 5(100): Vout drop 10mV, loop Vc see 50mV drop 4(011): Vout drop 10mV, loop Vc see 40mV drop 3(010): Vout drop 10mV, loop Vc see 30mV drop 2(001): Vout drop 10mV, loop Vc see 20mV drop 1(000): Vout drop 10mV, loop Vc see 10mV drop
0	0	Reserved	R/W	

Note: LOOP_CTRL register is disable when EN pin high &REG0x01<6>=1.

Table 11

FLT_RECORD (Address=0x05, default=00h)				
Bits	**Default**	**Name**	**R/W**	**Description**
7	0	FLT_VO_SCP	R	Output Short Current (SCP) 0 No fault 1 Fault
6	0	FLT_VO_OVP	R	Output Over Voltage (OVP) 0 No fault 1 Fault
5	0	FLT_TEMP_SD	R	Over temperature shutdown (160℃) 0 No fault 1 Fault, greater than threshold
4	0	FLT_TEMP_DIE	R	Thermal warning (110℃) 0 No fault

				1 Fault, greater than threshold
3	0	FLT_VO_UVP	R	Output Under Voltage (UVP) 0 No fault 1 Fault
2	0	FLT_AVIN_OVP	R	Analog Input Over Voltage(OVP) 0 No fault 1 Fault
1	0	FLT_PVIN_OVP	R	Power Input Over Voltage(OVP) 0 No fault 1 Fault
0	0	FLT_BOOT	R	0 MTP data load is finished 1 MTP data load fail

Note: FLT_RECORD bit can be cleared by read 0x05 register.

Output Voltage Setting

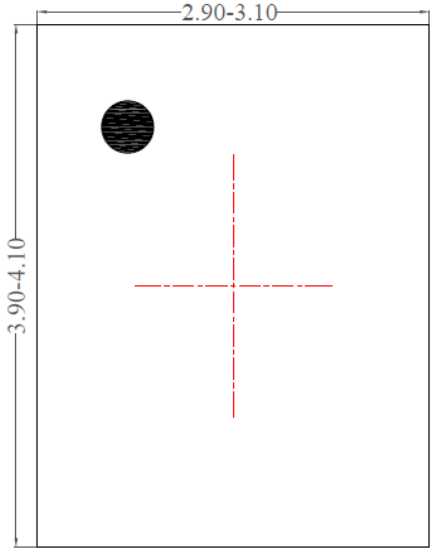
The output voltage can be programmed by writing a 6-bit register VO_CTRL. The feedback divider can be programmed by FB_RATIO. The corresponding output voltage setting is shown below.

Table 12. Output Voltage Setting

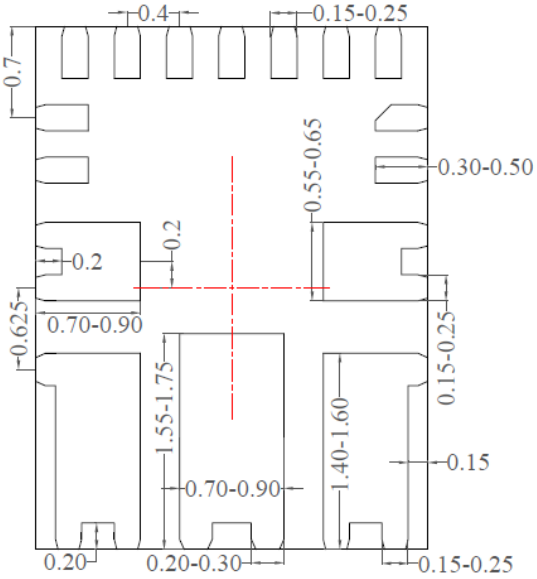
	$V_{OUT}=V_{FB}$	$V_{OUT}=1.5*V_{FB}$		$V_{OUT}=V_{FB}$	$V_{OUT}=1.5*V_{FB}$
0x02 Bit[6-1]	V_{OUT} (V)	V_{OUT} (V)	0x02 Bit[6-1]	V_{OUT} (V)	V_{OUT} (V)
000000	0.4	0.6	100000	0.72	1.08
000001	0.41	0.615	100001	0.73	1.095
000010	0.42	0.63	100010	0.74	1.11
000011	0.43	0.645	100011	0.75	1.125
000100	0.44	0.66	100100	0.76	1.14
000101	0.45	0.675	100101	0.77	1.155
000110	0.46	0.69	100110	0.78	1.17
000111	0.47	0.705	100111	0.79	1.185
001000	0.48	0.72	101000	0.8	1.2
001001	0.49	0.735	101001	0.81	1.215
001010	0.5	0.75	101010	0.82	1.23
001011	0.51	0.765	101011	0.83	1.245
001100	0.52	0.78	101100	0.84	1.26
001101	0.53	0.795	101101	0.85	1.275
001110	0.54	0.81	101110	0.86	1.29
001111	0.55	0.825	101111	0.87	1.305
010000	0.56	0.84	110000	0.88	1.32
010001	0.57	0.855	110001	0.89	1.335
010010	0.58	0.87	110010	0.9	1.35
010011	0.59	0.885	110011	0.91	1.365
010100	0.6	0.9	110100	0.92	1.38

010101	0.61	0.915	110101	0.93	1.395
010110	0.62	0.93	110110	0.94	1.41
010111	0.63	0.945	110111	0.95	1.425
011000	0.64	0.96	111000	0.96	1.44
011001	0.65	0.975	111001	0.97	1.455
011010	0.66	0.99	111010	0.98	1.47
011011	0.67	1.005	111011	0.99	1.485
011100	0.68	1.02	**111100**	**1 (default)**	**1.5**
011101	0.69	1.035	111101	1.01	1.515
011110	0.7	1.05	111110	1.02	1.53
011111	0.71	1.065	111111	1.03	1.545

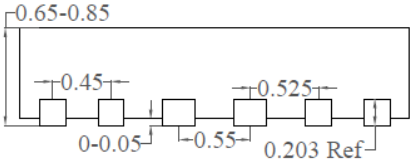
QFN3×4-16 Package Outline Drawing



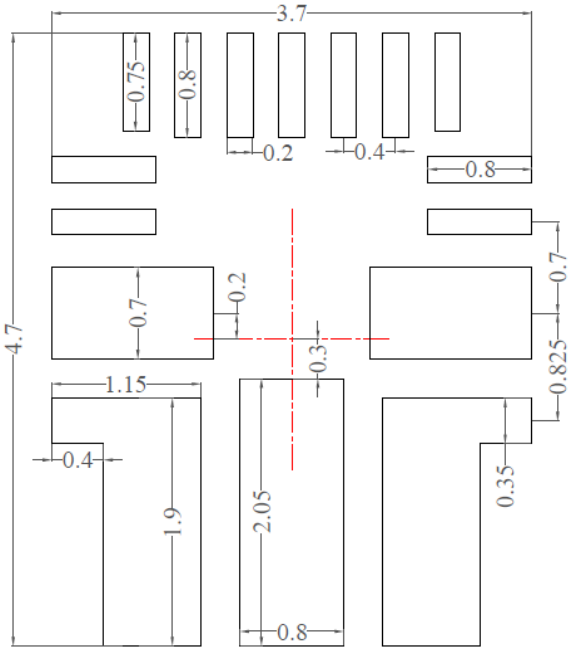
Top View



Bottom View



Side View



Recommended PCB layout
(Reference only)

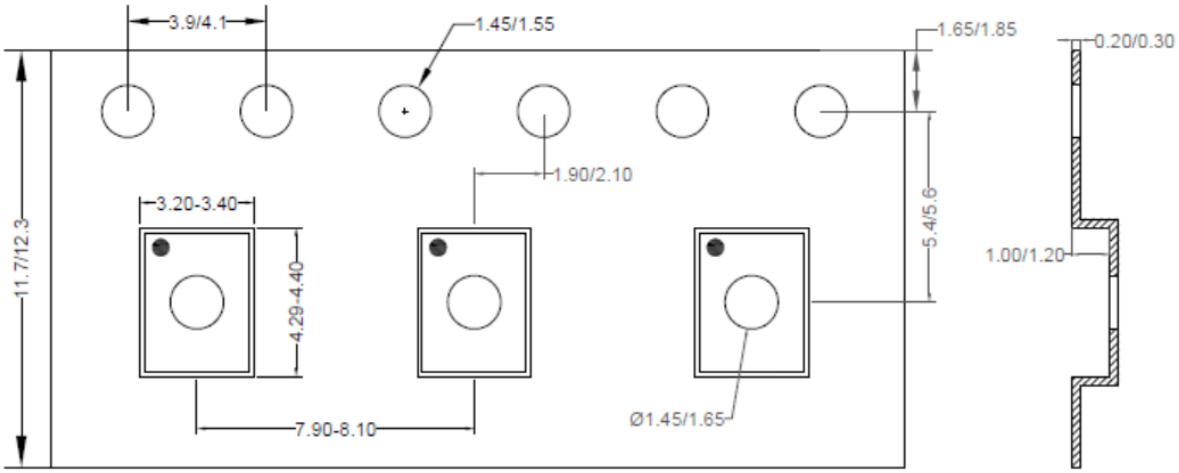
Notes:

1, All dimension in millimeter and exclude mold flash & metal burr.

2, Center of PCB refers the chip body Center.

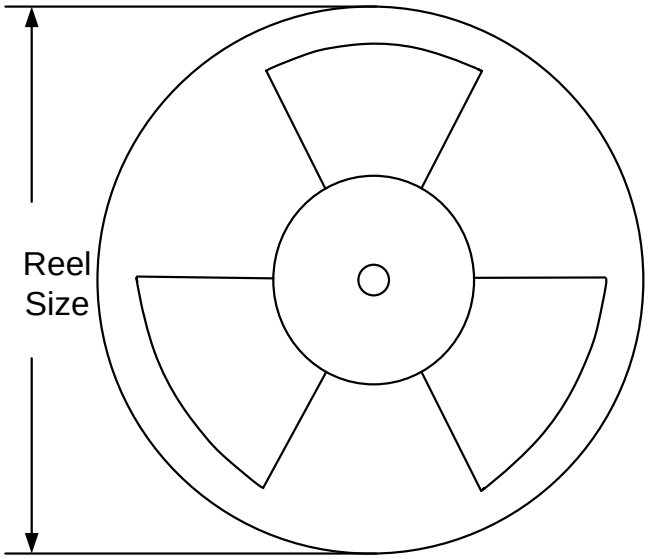
Taping & Reel Specification

Taping Orientation



Feeding Direction ⟶

Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
QFN3×4	12	8	13"	400	400	5000

Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Dec. 27, 2023	Revision 1.0	Initial Release.
Jan. 18, 2024	Revision 1.0A	1. Correct switching frequency from 3MHz to 3.3MHz. 2. Add notes for DVS slew rate accuracy in Electrical Characteristics Table (Page 5). 3. Refine the specific actions of EN control (Page 31).

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