SQ82968

Octal, 16-Bit, SPI, Voltage Output DAC with Internal Reference

General Description

The SQ82968 is an octal, 16-bit, buffered voltage-output DAC with low power consumption. The device is a highly efficient and accurate digital-to-analog converter designed for applications requiring the conversion of digital signals into analog voltages. Operating within a voltage supply range of 2.7V to 5.5V, this device is suitable for a wide range of electronic systems. The SQ82968 includes an on-chip 1.25V/2.5V, 8 ppm/°C reference with an internal gain of two, providing full-scale output voltage range of 2.5V or 5V. The internal reference is turned off at power-up, and an external reference is enabled by default. The internal reference can be selected and enabled using a SPI write.

The SQ82968 power-on reset output voltages are set to 0V or midscale and remain at this level until a valid write occurs. The device has a power-down feature, which can significantly reduce current consumption to as low as 0.1µA at 3V (0.2µA at 5V), offering software selectable output load for individual or multiple DAC channels during power-down mode and optimizing power efficiency. The SQ82968 also offers a simultaneous update LDAC_N input pin, enabling the simultaneous update of all DAC outputs. This feature is further enhanced by the capability to select specific DAC channels for the simultaneous update, providing precise control over the output voltages. The device features an asynchronous CLR_N input pin that allows all DAC outputs to be updated to a user-programmable zero, midscale, or full scale.

The versatile 3-wire serial interface operates at clock rates of up to 50MHz and is compatible with standard SPI®, QSPI™, MICROWIRE™, and DSP interface standards. The on-chip precision output amplifiers facilitates rail-to-rail output swing.

The SQ82968 is available in a 2.605mm x 2.605mm 16-ball CSP package.

Features

- Low Power, Small Footprint, Octal, 16-bit DAC
- 2.7V to 5.5V Power Supply
- Power-down Capability
- Shutdown Current: 0.1µA at 3V and 0.2µA at 5V(typ.)
- On-chip 1.25V/2.5V, 8 ppm/°C Reference
- Power-on Reset to 0V or Midscale
- Configurable Power-down DAC Outputs
- Hardware/Software LDAC_N and LDAC_N Controls
- Software Configurable DAC Output Reset to 0V, Mid-Scale or Full Scale
- Rail-to-rail Operation
- Available in 16-ball CSP Package

Applications

- Optical Networking
- Battery Test Equipment
- Industrial Automation
- Data Acquisition Systems

Typical Application

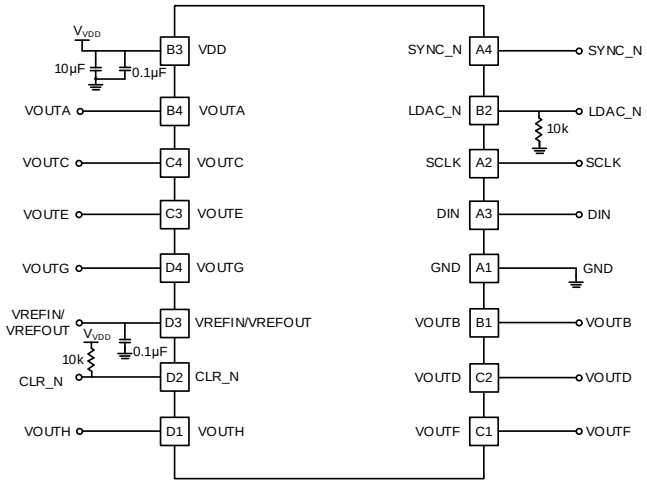


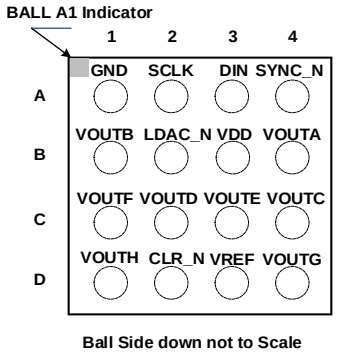
Figure 1. Typical Application Circuit

Ordering Information

Ordering Part Number	Package Type	Top Mark	Note
SQ82968VZS	CSP2.605 ×2.605-16	**FMW*xyz***	16-bit, 1.25V internal reference, power-on reset to 0V
SQ82968CVZS	CSP2.605 ×2.605-16	**GWQ*xyz***	16-bit, 2.5V internal reference, power-on reset to 0V
SQ82928VZS	CSP2.605 ×2.605-16	**GWT*xyz***	12-bit, 1.25V internal reference, power-on reset to 0V

Note: ***x = year code, y = week code, z = lot number code.***

Pinout (Top View)



(CSP2.605×2.605-16)

Pin Description

Pin No.	Pin Name	Pin Description
B3	VDD	Power Supply Input (2.7 to 5.5V).
B4	VOUTA	Analog Output Voltage from DAC A.
C4	VOUTC	Analog Output Voltage from DAC C.
C3	VOUTE	Analog Output Voltage from DAC E.
D4	VOUTG	Analog Output Voltage from DAC G.
D3	VREFIN/ VREFOUT	The device has a common pin for reference input and reference output. When using the internal reference, this is the reference output pin. When using an external reference, this is the reference input pin. The default for this pin is as a reference input.
D2	CLR_N	Asynchronous Clear Input. The CLR_N input is falling edge sensitive. When CLR_N is low, all LDAC_N pulses are ignored. When CLR_N is activated, the input register and the DAC registers are updated with the data contained in the CLR_N code register-zero, midscale, or full scale. Default setting is 0V for all the outputs.
D1	VOUTH	Analog Output Voltage from DAC H.
C1	VOUTF	Analog Output Voltage from DAC F.
C2	VOUTD	Analog Output Voltage from DAC D.
B1	VOUTB	Analog Output Voltage from DAC B.
A1	GND	Ground reference level for all circuitry.
A3	DIN	Serial Data Input. This device has a 32-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
A2	SCLK	Serial Clock Input. The interface supports clock rates up to 50MHz.
B2	LDAC_N	Pulsing this pin low allows any or all DAC registers to be simultaneously updated if the input registers have new data. Alternatively, this pin can be tied permanently low.
A4	SYNC_N	Active Low Control Input. This serves as the frame synchronization signal for the input data. Upon its transition to a low state, it activates the SCLK and DIN buffers, enabling the input shift register. The subsequent data transfer occurs during the falling edges of the next 32 clocks. If the signal returns to a high state prior to the 32nd falling edge, The next rising edge functions as an interrupt and the write sequence is disregarded.

Block Diagram

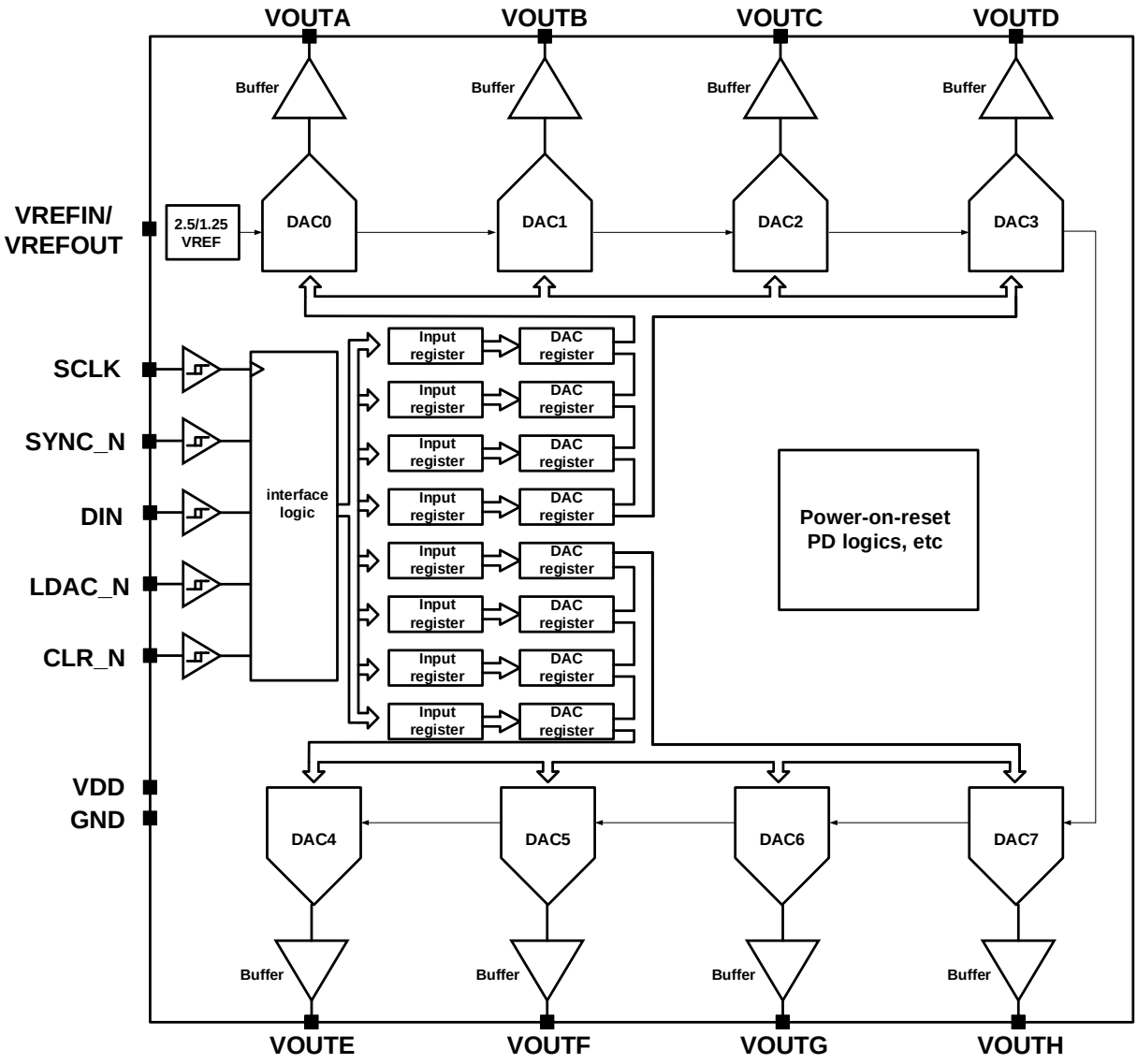


Figure 2. Functional Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VDD	-0.3	6.5	V
DIN, SCLK, SYNC_N, LDAC_N, CLR_N (Digital Inputs)	-0.3	V_{VDD}+0.3	
VOUTA ~ VOUTH	-0.3	V_{VDD}+0.3	
VREFIN/VREFOUT	-0.3	V_{VDD}+0.3	
Junction Temperature	-40	150	°C
Storage Temperature	-65	150	
Reflow Soldering Peak Temperature		260	
ESD: HBM (Human Body Model)	± 3000		V
ESD: CDM (Charged Device Model)	± 750		V

Thermal Information

Parameter (Note 2)	Value	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	55	°C/W
θ_{JC} Junction-to-Case (Top) Thermal Resistance	3.8	
θ_{JB} Junction-to-Board Thermal Resistance	30	

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
Operation Ambient Temperature Range	-40	125	°C
Operation Junction Temperature Range	-40	135	°C
VDD	2.7	5.5	V
Digital Inputs	0	V_{VDD}	V

Electrical Characteristics

V_{VDD}= 2.7V to 5.5V, R_L = 2kΩ to GND, C_L = 200pF to GND, V_{REFIN} = V_{VDD}. T_A = -40°C to 125°C, typical values are T_A = 25°C, unless otherwise noted (Note 4).

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static Performance						
Resolution	RES		16			LSB
Integral Nonlinearity	INL	Code range of 512 to 65024, Output unloaded		+1.3/ -2.7	±13.8	LSB
Differential Nonlinearity	DNL	Code range of 512 to 65024, Output unloaded		+2.6/ -1.0	±13.5	LSB
Zero Code Error (Refer to 错误!未找到引用源。)				1.8	12.5	mV
Zero Code Error Drift (Note 5)		V_{VDD} = 5V		±8.0		μV/°C
		V_{VDD} = 3V		±8.0		μV/°C
Full Scale Error	FSE			±0.05	±0.35	%FSR
Gain Error	GE	V_{VDD} = 4.5V – 5.5V		±0.02	±0.15	%FSR
		V_{VDD} = 2.7V – 3.6V		±0.02	±0.25	%FSR
Gain Temperature Coefficient (Note 5)		Of FSR/°C, V_{VDD} = 5V		±1.6		ppm
		Of FSR/°C, V_{VDD} = 3V		±1.6		ppm
Offset Error	OFE			±1.2	±12.5	mV
DC Power Supply Rejection Ratio (Note 5)	DC_PSRR	V_{VDD} ± 10%, V_{VDD} = 5V		-78		dB
		V_{VDD} ± 10%, V_{VDD} = 3V		-78		dB
DC Crosstalk (External Reference) (Note 5) (Refer to 错误!未找到引用源。)		Full-scale change, R_L = 2kΩ to GND or V_{VDD}, V_{VDD} = 5V		±38		μV
		Full-scale output change, R_L = 2kΩ to GND or V_{VDD}, V_{VDD} = 3V		±18		μV
		Load current change, V_{VDD} = 5V		±21		μV/mA
		Load current change, V_{VDD} = 3V		±27		μV/mA
		Powering down, V_{VDD} = 5V		±24		μV
		Powering down, V_{VDD} = 3V		±17		μV
DC Crosstalk (Internal Reference) (Note 5) (Refer to 错误!未找到引用源。)		Full-scale change, R_L = 2kΩ to GND or V_{VDD}, V_{VDD} = 5V		±31		μV
		Full-scale change, R_L = 2kΩ to GND or V_{VDD}, V_{VDD} = 3V		±34		μV
		Load current change, V_{VDD} = 5V		±27		μV/mA
		Load current change, V_{VDD} = 3V		±55		μV/mA
Output Characteristics						
Output Voltage Range (Note 5)	V_{OUT}		0		V_{VDD}	V
Capacitive Load Stability (Note 5)	C_L	R_L = ∞		2		nF
		R_L = 2 kΩ		10		nF
DC Output Impedance (Note 5)	R_{OUT}			0.05		Ω
Short-Circuit Current (Note 5)	I_{SHORT}	V_{VDD} = 5 V		81		mA
		V_{VDD} = 3V		81		mA

Output Current (Note 5)	I_{OUT}	Headroom = 0.2V.	30			mA
Output Headroom		Single channel output current = 30mA, V_{VDD} = 4.5V – 5.5V		90	200	mV
		Single channel output current = 30mA, V_{VDD} = 2.7V – 3.6V		150	300	mV
Power-up Time (Note 5)		Coming out of power-down mode, V_{VDD} = 5 V		3.5		µs
		Coming out of power-down mode, V_{VDD} = 3 V		3.0		µs
Reference Inputs						
Reference Current	I_{REFIN}	V_{REF} = V_{VDD} = 5.5 V (per DAC channel)		55		µA
Reference Input Range	V_{REFIN}		0		V_{VDD}	V
Reference Input Impedance	R_{FEFIN}			100		kΩ
Reference Output						
Output Voltage	V_{REFOUT}	V_{VDD} = 4.5V – 5.5V		2.5		V
		V_{VDD} = 2.7V – 3.6V		1.25		V
Reference TC (Note 5)				8		ppm/°C
Reference Output Impedance (Note 5)	R_{REFOUT}	V_{VDD} = 5V		0.04		Ω
		V_{VDD} = 3V		0.20		Ω
Logic Inputs (Note 5)						
Input Current		All digital inputs			±0.1	µA
Input Low Voltage	V_{INL}	V_{VDD} = 4.5V – 5.5V			0.8	V
		V_{VDD} = 2.7V – 3.6V			0.6	V
Input High Voltage	V_{INH}	V_{VDD} = 4.5V – 5.5V	2.9			V
		V_{VDD} = 2.7V – 3.6V	2.0			
Pin Capacitance				3		pF
Power Requirements						
Power Supply Voltage	V_{VDD}	All digital inputs at 0 or V_{VDD}, DAC active, excludes load current, V_{VDD} = 4.5V – 5.5V	4.5	5	5.5	V
		All digital inputs at 0 or V_{VDD}, DAC active, excludes load current, V_{VDD} = 2.7V – 3.6V	2.7	3	3.6	V
VDD Current (Normal Mode)	I_{DD}	Interface inactive. All DACs active. DAC outputs unloaded. V_{IH} = V_{VDD} and V_{IL} = GND, Internal reference off, V_{VDD} = 4.5V – 5.5V		4.5	8.1	mA
		Interface inactive. All DACs active. DAC outputs unloaded. V_{IH} = V_{VDD} and V_{IL} = GND, Internal reference off, V_{VDD} = 2.7V – 3.6V		4.0	7.3	mA
		Interface inactive. All DACs active. DAC outputs unloaded. V_{IH} = V_{VDD} and V_{IL} = GND, Internal reference on, V_{VDD} = 4.5V – 5.5V		4.9	8.9	mA
		Interface inactive. All DACs active. DAC outputs unloaded. V_{IH}		4.6	8.2	mA

		= V_{VDD} and V_{IL} = GND, Internal reference on, V_{VDD} = 2.7V – 3.6V				
VDD Current (All Power-Down Modes)	I_{DD}	All eight DACs powered down, V_{IH} = V_{VDD} and V_{IL} = GND, V_{VDD} = 4.5V – 5.5V		0.2	4.5	μA
		All eight DACs powered down, V_{IH} = V_{VDD} and V_{IL} = GND, V_{VDD} = 2.7V – 3.6V		0.1	3.0	μA
AC Characteristics (Each output)						
Output Voltage Settling Time		¼ to ¾ scale settling to ±2 LSB		3.0		μs
Slew Rate	SR			1.5		V/μs
Multiplying Bandwidth (Refer to 错误!未找到引用源。)		V_{REF} = 2 V ± 0.2Vpp		400		kHz
Total Harmonic Distortion (Refer to 错误!未找到引用源。)	THD	V_{REF} = 2 V ± 0.2Vpp, frequency = 10kHz		-78		dB
Output Noise Spectral Density	NSD	DAC code = 0x8400, 10kHz		113		nV/√Hz
Output Noise		0.1Hz to 10Hz, DAC code = 0x0000		71		μV p-p

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

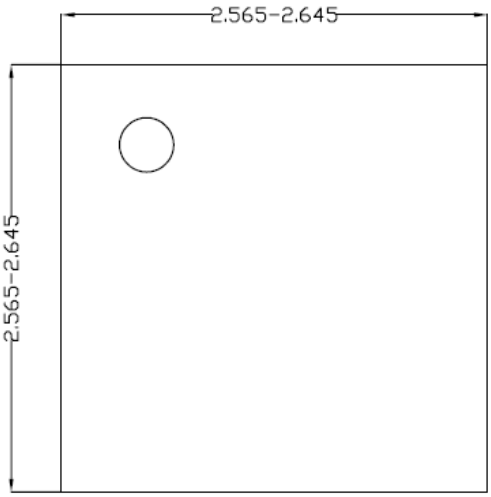
Note 2: Package thermal resistance is measured in the natural convection at T_A = 25˚C on an 8.5cm×8.5cm four-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

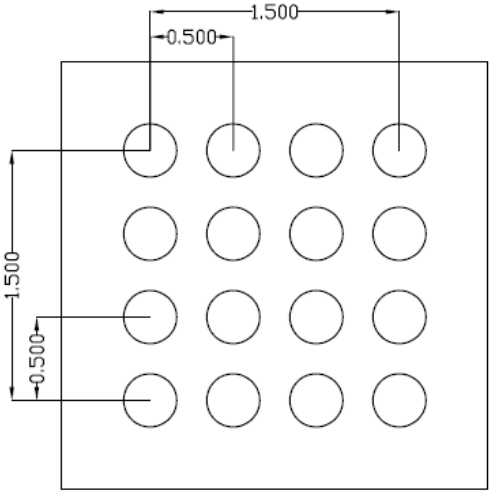
Note 4: Production tested at 25°C. Limits are guaranteed by design, test or statistical correlation.

Note 5: Guaranteed by design and characterization; not production tested.

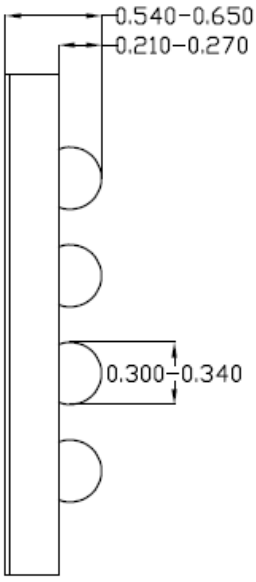
CSP2.605x2.605-16 Package Outline Drawing



Top view



Bottom view

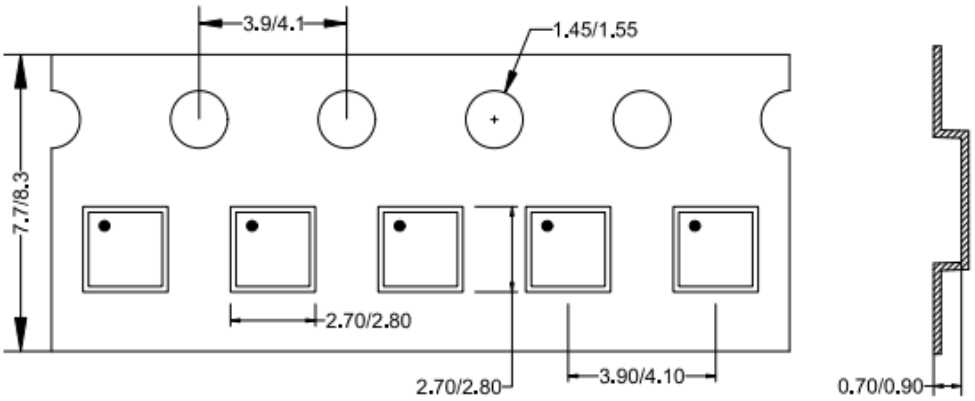


Side view

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

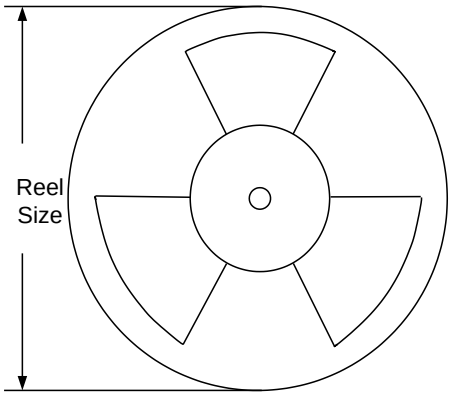
Taping & Reel Specification

CSP 2.605x2.605-16 taping orientation



Feeding direction →

Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
CSP2.605x2.605-16	8	4	7"	280	160	3000

Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Dec. 27, 2023	Revision 1.0	Initial Release
Mar. 28, 2024	Revision 1.0A	1. Recommended Operating Conditions: (1) Delete “Operation Junction Temperature Range: -40°C to 150°C” 2. 5V Electrical Characteristics Table (1) Input Current: change Max value from ±3 to ±0.1 (2) Input High Voltage: change Min value from 2.8 to 2.9 (3) The current of VDD (All Power-Down Modes): add the Max value 4.5 3. 3V Electrical Characteristics Table (1) Input Current: change Max value from ±3 to ±0.1 (2) Input Low Voltage: change Max value from 0.8 to 0.6 (3) The current of VDD (All Power-Down Modes): add the Max value 3 4. AC Electrical Characteristics Table (1) Output Noise: change Typ value from 33 to 71 5. Add specification of SQ82968C in datasheet.

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