SY2A58152

Twelve Half -bridge Driver with SPI Control

General Description

The SY2A58152 is a twelve half-bridge motor driver solution for automotive, industrial and other mechatronic applications. The half-bridges are fully controllable to achieve a forward, reverse, coasting and braking operation of motor. All the functions can be programmed through serial peripheral interface (SPI).

The SY2A58152 provides internal shutdown functions with an nFAULT output pin to alert the system when a fault occurs. Such as over current protection, open load detection, under voltage lockout, over voltage lockout and thermal shutdown. The device is packaged in QFN5×5-24 with exposed pad.

Ordering Information

SY2A58152 □(□□□)

Package Code

Optional Spec Code

Ordering Number	Package type	Note
SY2A58152VAQ	QFN5×5-24	

Features

- 12 Half-bridge Outputs
- 4.5V to 32V Operating Voltage
- Up to 1A RMS Output Current for Each Output
- Low-power Sleep Mode
- Compatible with 5V/3.3V System
- Serial Peripheral Interface, up to 5MHz;
- Daisy Chain Functionality
- PWM Capable Output for Frequency 80Hz, 100Hz, 200Hz and 2kHz with 8-Bit Duty Cycle Resolution
- Integrated Protection: Overcurrent Protection (OCP), Short Circuit Protection (SCP), Open Load Detection (OLD), Under Voltage Lockout (UVLO), Over Voltage Protection (OVP) and Thermal Shutdown (TSD)
- nFAULT Pin Output
- AEC-Q100 Qualified

Applications

- Automotive
- HVAC
- DC brushed motors
- LED

Typical Application

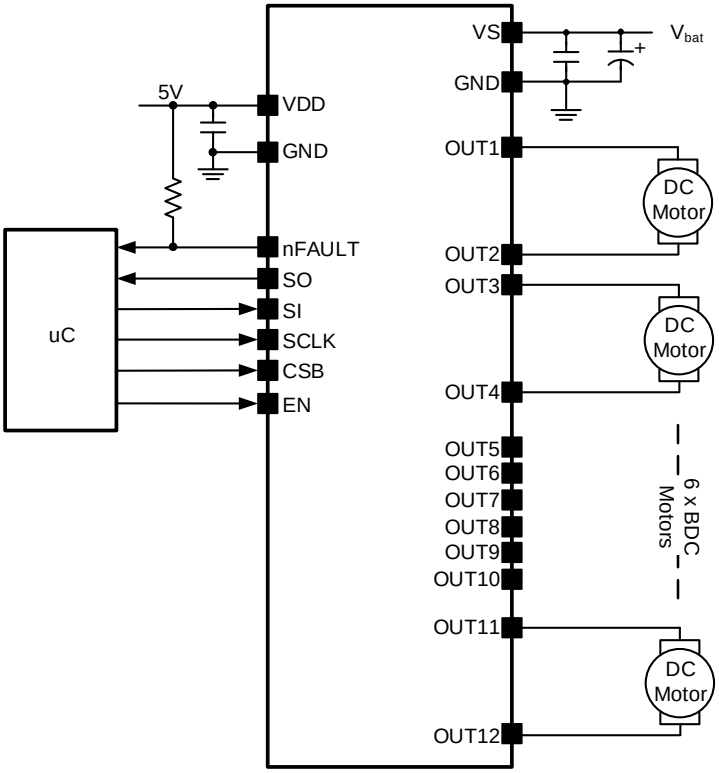
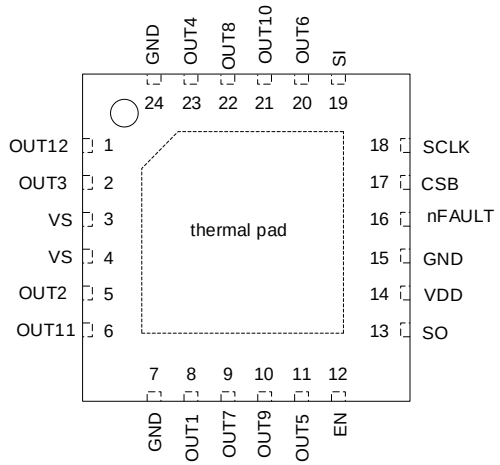


Figure 1. Typical Application Circuit

Pinout (Top View)



(QFN5×5-24)

Top Mark: FWW*xyz* (device code: **FWW**, ***x=year code, y=week code, z= lot number code)***

Pin Name	Pin No.	Pin Description
OUT12	1	Half-bridge Output 12.
OUT3	2	Half-bridge Output 3.
VS	3,4	Power supply for internal high side output drivers.
OUT2	5	Half-bridge Output 2.
OUT11	6	Half-bridge Output 11.
OUT1	8	Half-bridge Output 1.
OUT7	9	Half-bridge Output 7.
OUT9	10	Half-bridge Output 9.
OUT5	11	Half-bridge Output 5.
EN	12	Enable. Logic high enables the IC. Internal pull down.
SO	13	Serial data output. 16-bit serial communications output.
VDD	14	Power supply for internal logic.
GND	7,15,24	Ground. Internal connection to lead frame.
CSB	17	Chip select Bar. Active low serial port operation.
SCLK	18	Serial Clock. Clock input for use with SPI communication.
SI	19	Serial input. 16-bit serial communications input.
OUT6	20	Half-bridge Output 6.
OUT10	21	Half-bridge Output 10.
OUT8	22	Half-bridge Output 8.
OUT4	23	Half-bridge Output 4.
nFAULT	16	Fault indicator output. This pin is pulled logic low during a fault condition and requires an external pull-up resistor.

Function Block

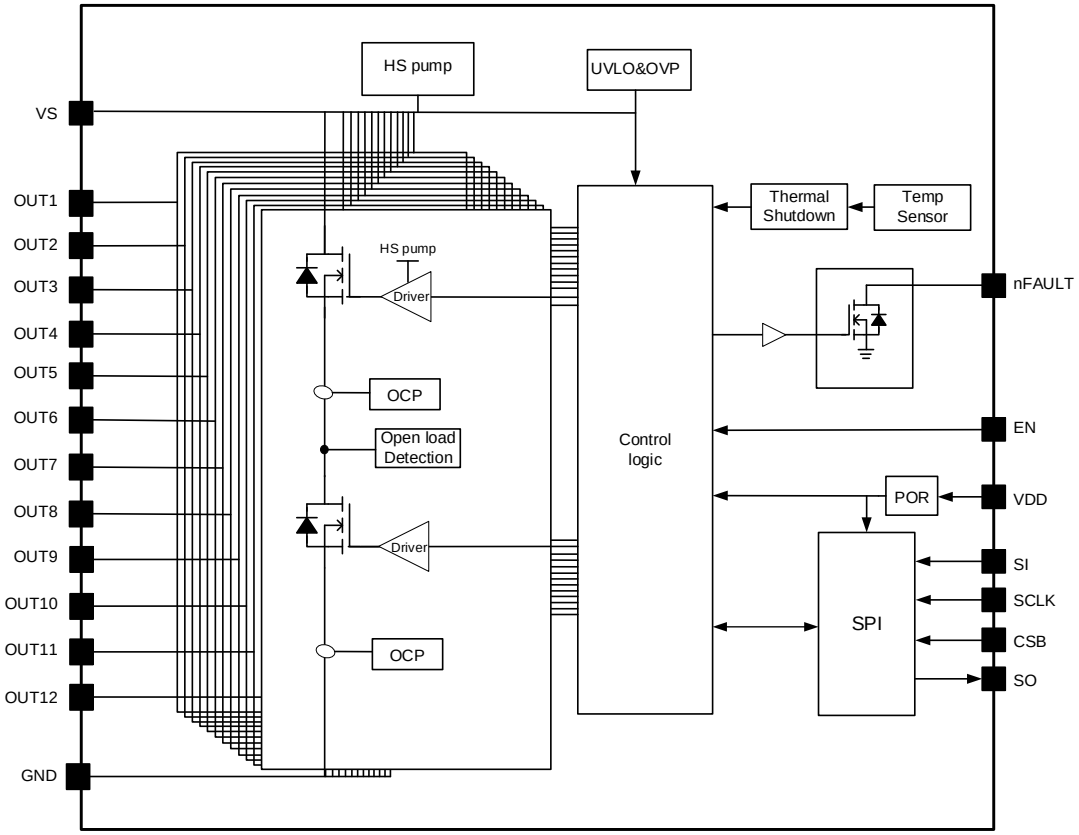


Figure 2. SY2A58152 Function Block Diagram

Absolute Maximum Ratings (Note 1)

VS (DC) ---------- -0.3V to 40V
OUTx (DC) ---------- -0.3V to VS+0.7V
Digital pin (SI, SCLK, CS, SO, EN, nFAULT) ---------- -0.3V to VDD+0.3V
VDD---------- -0.3V to 5.75 V
Continuous supply current (VS pins) (Note 2) ----------0A to 6A
Continuous sink current (GND pins) (Note 2) ----------0A to 6A
Junction Temperature (T_J) ---------- -40°C to 150°C
Storage Temperature ---------- -65°C to 150°C
QFN5×5-24 Package Thermal Resistance (Note 3)

θ_{JA} ---------- 22°C/W

$\theta_{JC\ TOP}$ ---------- 12°C/W

Recommended Operating Conditions

VS ---------- 4.5V to 32V
VDD ---------- 3.15V to 5.5V
Digital pin ---------- 0V to 5.5V
nFAULT pullup voltage---------- 0V to 5.5V
nFAULT output current---------- 0V to 5mA
Operating Temperature (T_A) ---------- -40°C to 125°C
Junction Temperature (T_J) ---------- -40°C to 150°C

Electrical Characteristics

(-40°C <T_A < 125°C, 4.5V< VS <32V, 3.15V<VDD<5.5V, EN=VDD, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supplies						
VS Sleep Mode Current	I_{VS_sleep}	VS =13.5V, EN=L, T_A=25°C		0.35	1	μA
		VS =13.5V, EN=L, T_A=125°C			4.5	μA
VS Standby Mode Current	$I_{VS\_standby}$	VS=13.5V, EN=H, Driver=OFF,T_A=25°C		0.5	0.7	mA
		VS=13.5V, EN=H, Driver=OFF,T_A=125°C			0.7	mA
VS Operating Mode Current	I_{VS}	VS=13.5V, EN=H, All High-Side FETs=ON, T_A=25°C		2.6	4	mA
		VS=13.5V, EN=H, All High-Side FETs=ON, T_A=125°C			4	mA
VS Undervoltage Lockout Voltage	V_{UVLO_FALL}	VS falling	3.8		4.3	V
	V_{UVLO_RISE}	VS rising	4		4.5	V
	V_{UVLO_HYS}			200		mV
VS Undervoltage Lockout Deglitch Time	t_{UVLO}			10		μs
VS Overvoltage Protection	V_{OVP}	VS rising, EXT_OVP=0b	21		25	V
		VS falling, EXT_OVP=0b	20		24	V
		VS rising, EXT_OVP=1b	32.6		35.1	V
		VS falling, EXT_OVP=1b	32		34.5	V
	V_{OVP_HYS}	Rising to falling threshold, EXT_OVP=0b		1		V
		Rising to falling threshold, EXT_OVP=1b		0.7		V
VS Overvoltage Protection Deglitch Time	t_{OVP}			10		μs
VDD Power On Reset Threshold	V_{POR_ON}	Supply rising	2.75		3.05	V
VDD Power Off Reset Threshold	V_{POR_OFF}	Supply falling	2.6		2.9	V
POR Undervoltage Hysteresis	V_{POR_HYS}	Rising to falling threshold		150		mV
VDD Operating Supply Current	I_{VDD}	VS=13.5V, VDD=3.3V, EN=H, all low-side FETs=ON, SPI=ON, T_A=25°C		3.5	5	mA
		VS =13.5V, VDD=3.3V, EN=H, all low-side FETs=ON, SPI=ON, T_A=125°C			5	mA
VDD Standby Mode Current	$I_{VDD\_standby}$	VS=13.5V, VDD=3.3V, EN=H,SPI=OFF, T_A=25°C		2	3	mA
		VS=13.5V, VDD=3.3V, EN=H,SPI=OFF, T_A=125°C			3	mA
VDD Sleep Mode Current	I_{VDD_sleep}	VS=13.5V, VDD=3.3V, EN=L, T_A=25°C		1.1	2	μA
		VS=13.5V, VDD=3.3V, EN=L, T_A=125°C			2	μA
Logic Level Input (EN, SI, SCLK, CSB)						
Input Low Voltage	V_{IL}		0		0.6	V
Input High Voltage	V_{IH}		2			
Input Logic Hysteresis	V_{HYS}		200			mV
Input Low Current	I_{IL}	VIN=0V	-1		1	μA
Input High Current	I_{IH}	VIN=VDD		60	100	μA
Input Capacitance	C_{CAPINX}	(Note 4)		-	15	pF
Open-Drain Output(nFAULT)						
Output Low Voltage	V_{OL}	I_{sink}=5mA	0		0.4	V
Output High Current	I_{OH}	V_{OD}=5V	-1		1	μA
Output Capacitance	C_{OD}	(Note 4)	-	-	15	pF
Push-pull Output (SO) (Note 4)						
Output Low Voltage	V_{OL}	I_{out}= -5mA (Note 4)	0		0.4	V
Output High Voltage	V_{OH}	I_{out}= 5mA (Note 4)	VDD-0.6		VDD	V
Output Capacitance	C_{OD}	(Note 4)			30	pF
Output Low Current	I_{OL}	V_{SO}=0V	-1		1	μA
Output High Current	I_{OH}	V_{SO}=VDD	-1		1	μA
Power MOSFETs						
High Side FETs on Resistance	R_{DSON}	I_{out}=500mA VS=13.5V		0.75	1.6	Ω
Low Side FETs on Resistance		I_{out}=500mA VS=13.5V		0.75	1.6	

Output Rise and Fall Time (HS&LS)	$SL_{rise\ and\ fall}$	VS=13.5V,10-90% R_{LOAD}=27Ω, HBx_SR=0b		1		V/μs
		VS=13.5V,10-90% R_{LOAD}=27Ω, HBx_SR=1b		3.7		V/μs
Output Dead Time (High to Low / Low to High)	t_{DEAD}	VS =13.5V, SR=0, HS/LS driver OFF to LS/HS driver ON	6	15	25	μs
		VS =13.5V, SR=1, HS/LS driver OFF to LS/HS driver ON	2	5	15	μs
Propagation Delay (Hide-side and Low-side ON/OFF)	t_{PD}	High-side ON or low-side ON command (SPI last transition) to OUTx transition from Hi-Z state, SR=0	3	6	15	μs
		High-side ON or low-side ON command (SPI last transition) to OUTx transition from Hi-Z state, SR=1	1	3	8	μs
Source Leakage Current	I_{source_LC}	OUTx=0V, EN=1		6	10	μA
		OUTx=0V, EN=0			2	μA
Sink Leakage Current	I_{sink_LC}	OUTx=13.5V, EN=1, SR=0b		13.5	20	μA
		OUTx=13.5V, EN=1, SR=1b		13.5	20	μA
		OUTx=13.5V, EN=0, SR=0b			2	μA
PWM Mode						
PWM Switching Frequency	f_{PWM}	PWM_CHx_FREQ=00b	56	80	104	Hz
		PWM_CHx_FREQ=01b	70	100	130	Hz
		PWM_CHx_FREQ=10b	140	200	260	Hz
		PWM_CHx_FREQ=11b	1400	2000	2600	Hz
Protections						
Thermal Warning Temperature	T_{WARN}	(Note 4)	120	140	170	°C
Thermal Warning Hysteresis	T_{WARN_HYS}	(Note 4)		20		°C
Thermal Shutdown Temperature	T_{SD}	(Note 4)	150	165	185	°C
Thermal Shutdown Hysteresis	T_{HYS}	(Note 4)		20		°C
Over Current Shutdown Threshold (Source)	I_{OCSO}	VDD=5V, VS=13.5V	-2.3	-1.8	-1.3	A
Over Current Shutdown Threshold (Sink)	I_{OCSI}	VDD=5V, VS=13.5V	1.3	1.8	2.3	A
Over Current Shutdown Delay Time	t_{oc}	OCP_DEG=000b	6	10	14.5	μs
		OCP_DEG=001b(Note 4)	2.6	5	7.9	μs
		OCP_DEG=010b(Note 4)	0.4	2.5	5.9	μs
		OCP_DEG=011b	0.1	1	3.4	μs
		OCP_DEG=100b	38.2	60	80	μs
		OCP_DEG=101b(Note 4)	23.1	40	51.9	μs
		OCP_DEG=110b(Note 4)	18.5	30	41.5	μs
		OCP_DEG=111b(Note 4)	8.4	20	31.6	μs
Open Load Detection Current	I_{OLD}	High-side or Low side	2	9	18	mA
Open Load Detection Current in Low Current OLD Mode	I_{OLD_LOW}	Low side	0.2	0.8	2	mA
Open Load Detection Delay Time	t_{OLD}	Continuous Mode	2.2	3	3.8	ms
		PWM Mode	150	200	300	μs

Serial Peripheral Interface

(-40°C <T_A < 125°C, 4.5V< VS <32V, 3.15V<VDD<5.5V, EN=VDD, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}	(Note 4)			5	MHz
SCLK High Time	t_{CLKH}	(Note 4)	100			ns
SCLK Low Time	t_{CLKL}	(Note 4)	100			ns
SI Setup Time	t_{SU_SI}	(Note 4)	40			ns
SI Hold Time	t_{HD_SI}	(Note 4)	60			ns
SO Output Data Delay Time	t_{DLY_SO}	SCLK high to SO valid(Note 4)			60	ns
CSB Setup Time	t_{SU_CSB}	(Note 4)	100			ns
CSB Hold Time	t_{HD_CSB}	(Note 4)	100			ns
CSB Disable Delay Time	t_{DIS_CSB}	CSB high to SO High-Z (Note 4)		30		ns
CSB Minimum High Time before Active Low	t_{HI_CSB}	(Note 4)	600			ns
EN Low Valid Time	t_{ENL}	VDD=5V, EN going low 50% to OUTx turning off 50% (Note 4)	10			μs
EN High to SPI Valid	t_{ENH_SPIV}	(Note 4)			100	μs

Note 1: Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied.

Note 2: Power dissipation and thermal limits must be observed.

Note 3: θ_{JA} are measured under the natural convention at T_A = 25°C on a highly effective four layer thermal conductivity test board with thermal via.

Note 4: Guaranteed by design.

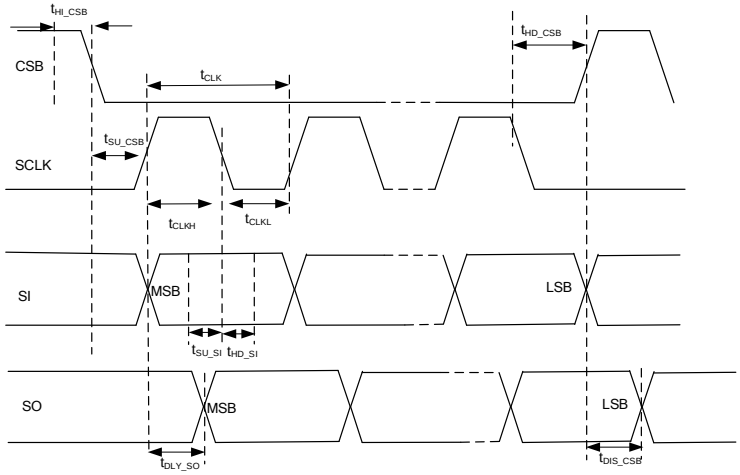
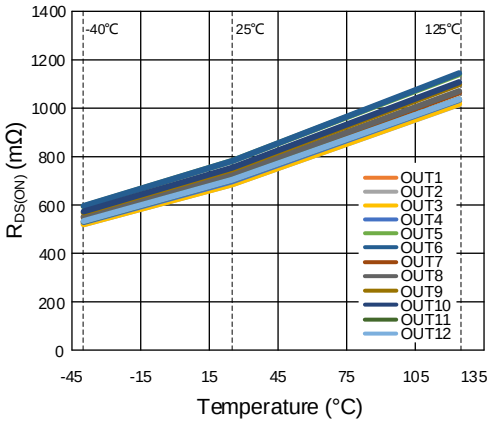


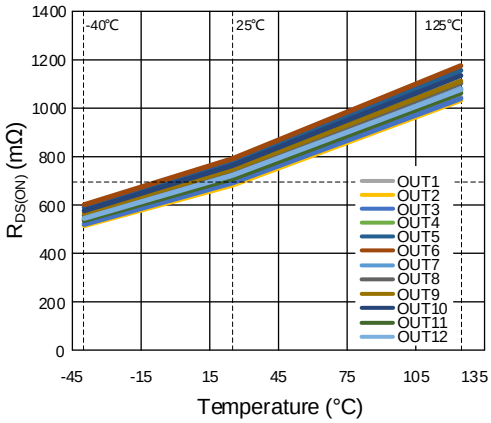
Figure 3. SPI Timing

Typical Performance Characteristics

High Side MOSFETs on Resistance

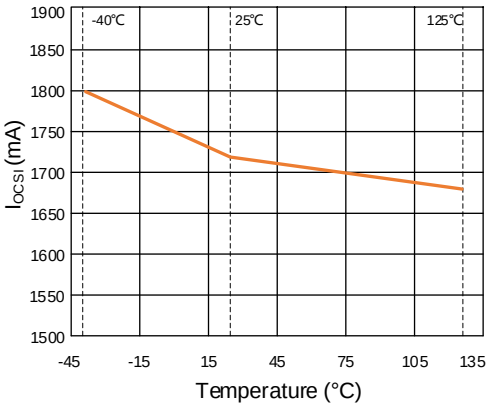


Low Side MOSFETs on Resistance



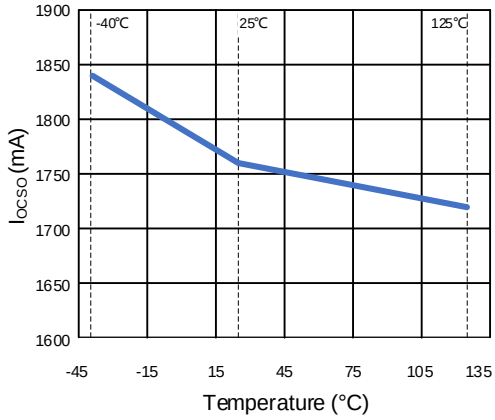
Low Side MOSFETs Over Current Limit

(VS=13.5V)



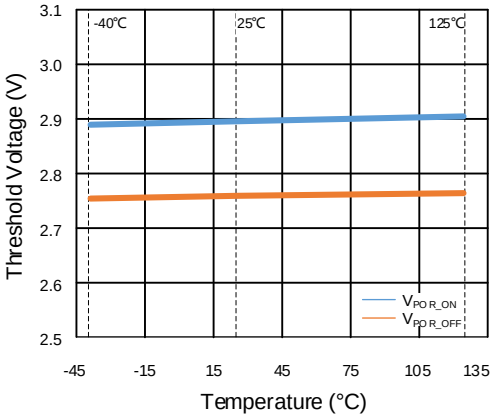
High Side MOSFETs Over Current Limit

(VS=13.5V)



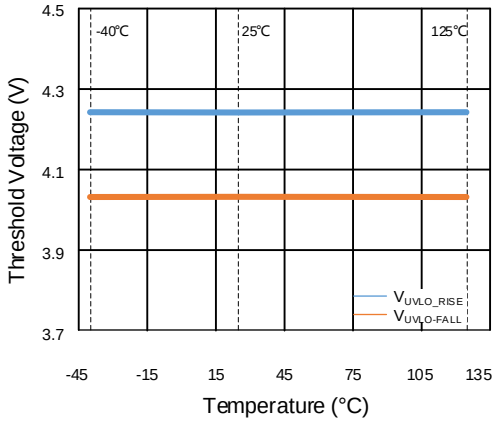
VDD Power On Reset and Power Off Reset

(VS=13.5V)

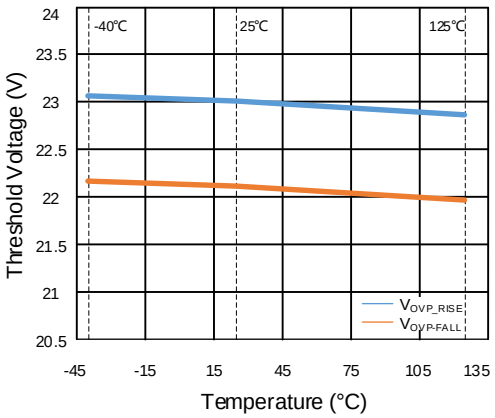


VS Undervoltage Lockout Voltage

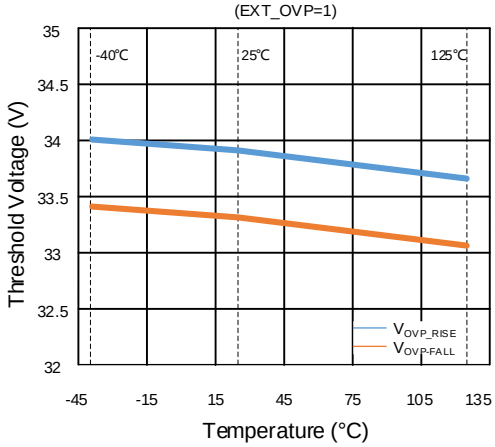
(VDD=5V)



VS Overvoltage Protection Voltage
(EXT_OVP=0)

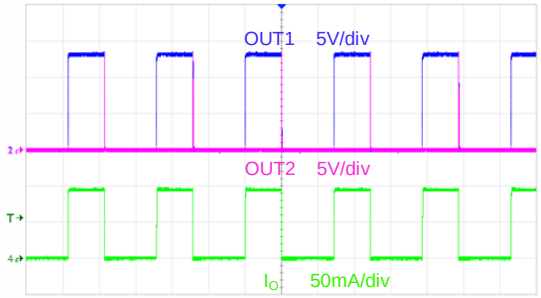


VS Overvoltage Protection Voltage
(EXT_OVP=1)



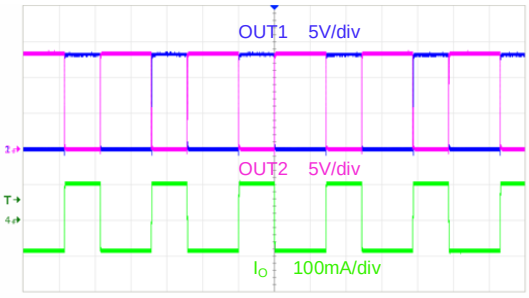
Operation Waveform

Passive Free-wheeling
(VS=13.5V Io=100mA Duty=25% Frequency=80Hz)



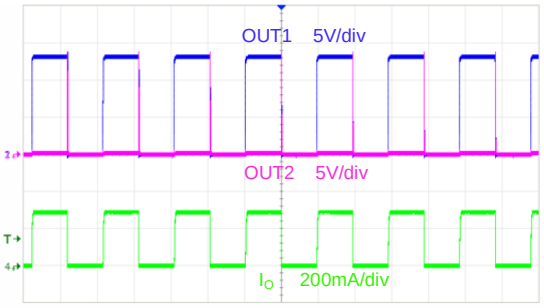
Time (5ms/div)

Active Free-wheeling
(VS=13.5V Io=100mA Duty=25% Frequency=80Hz)



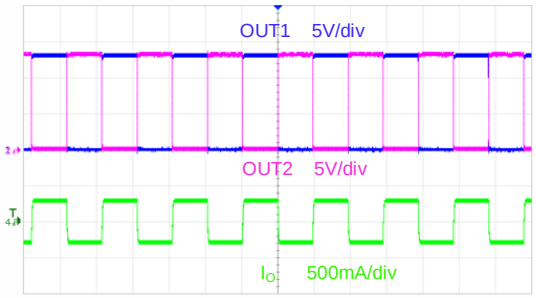
Time (5ms/div)

Passive Free-wheeling
(VS=13.5V Io=300mA Duty=50% Frequency=100Hz)



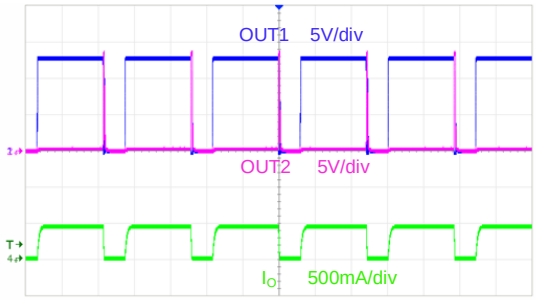
Time (5ms/div)

Active Free-wheeling
(VS=13.5V Io=300mA Duty=50% Frequency=100Hz)



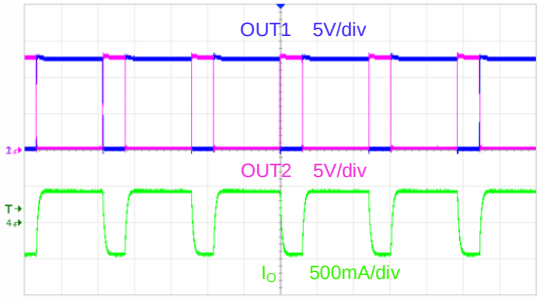
Time (5ms/div)

Passive Free-wheeling
(VS=13.5V Io=500mA Duty=75% Frequency=200Hz)



Time (2ms/div)

Active Free-wheeling
(VS=13.5V Io=500mA Duty=75% Frequency=200Hz)



Time (2ms/div)

Function Description

The SY2A58152 is a twelve half-bridge motor driver solution for automotive, industrial and other mechatronic applications. It can be configured as 6 independent H-bridges. The half-bridges are designed to support 1-A per half-bridge.

The device supports a standard 16-bit, 5-MHz serial peripheral interface (SPI). The device is also equipped with a daisy-chain functionality which allows connecting multiple devices using a single CSB line and saving on multiple resources.

Power Supply

VS powers the MOSFETs, and VDD powers the logic circuits. After the VS power up, the drivers are allowed to turn on. All the drivers are initialized in the off condition, and remain off regardless of VDD status. VDD power up resets all the internal logic. All the internal registers are cleared on VDD POR.

Driving Control

The device can be configured as H-bridge, high-side or low-side driver. The half-bridge outputs of the device are intended to drive motor or LEDs loads. The half-bridge drivers can be programmed to drive loads continuously (without PWM) or in chopping mode (with PWM) and in parallel operation for driving high current.

Continuous Mode (Without PWM)

The half-bridge drivers can be programmed to drive loads continuously (without PWM). The device can set the high-side enable bits (HBx_HS_EN) and low-side enable bits (HBx_LS_EN) in operation control registers (OP_CTRL_1, OP_CTRL_2) to turn on/off high-side or low-side MOSFETs individually. In addition, the device will stay in Hi-Z mode if high-side and low-side switch are set high of a half-bridge. An illustration is shown in Figure 4 and Figure 5, OUT1 and OUT2 driving a DC brush motor. With this configuration. The motor will work in forward direction with high-side FET of OUT1 and low-side FET of OUT2, and the motor current will flow from OUT1 into OUT2. Similarly, if turn on the high-side FET of OUT2 and low-side FET of OUT1, the motor will work in reverse, the motor current will flow from OUT2 into OUT1.

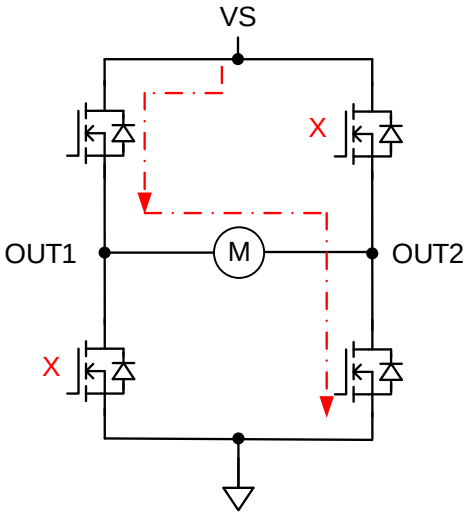


Figure 4. Continuous Mode (Forward)

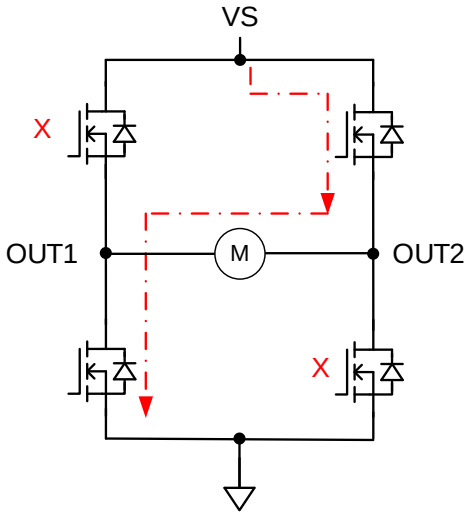


Figure 5. Continuous Mode (Reverse)

If the motor initially running in forward or reverse direction, then switch high-side and low-side off, the H-bridge will operation in coast mode. Because of the inductance energy, the current will continue to flow in motor and take the path flow through the body diodes of FETs, shown in Figure 6 and Figure 7.

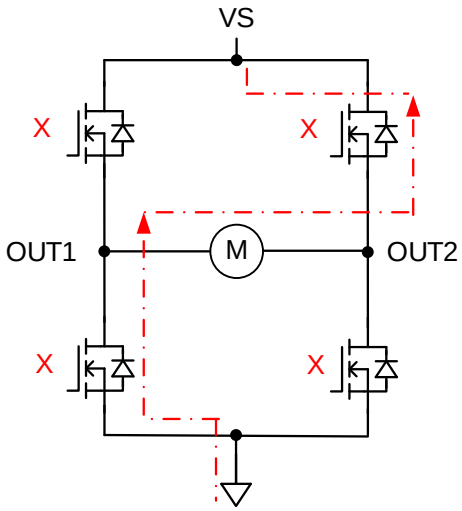


Figure 6. Coast-From Forward

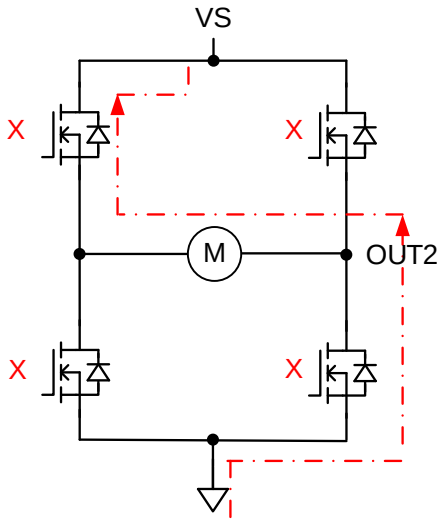


Figure 7. Coast-From Reverse

If the motor initially running in forward or reverse direction, then switch both high-side or low-side on, the H-bridge will operation in brake mode. For the low-side braking, both low-side FETs of the driver are turned on. Similarly, both high-side FETs of the driver are turned on for the high-side braking, shown in Figure 8 and Figure 9.

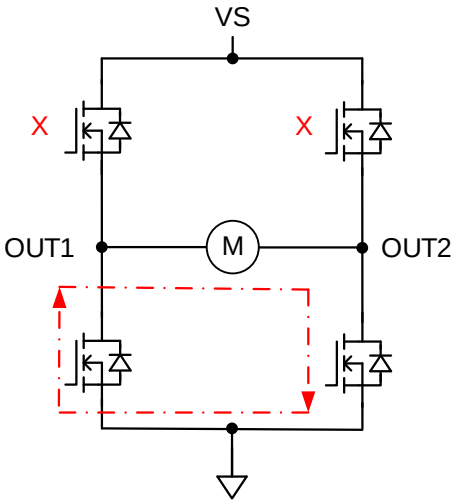


Figure 8. Brake-Low-Side

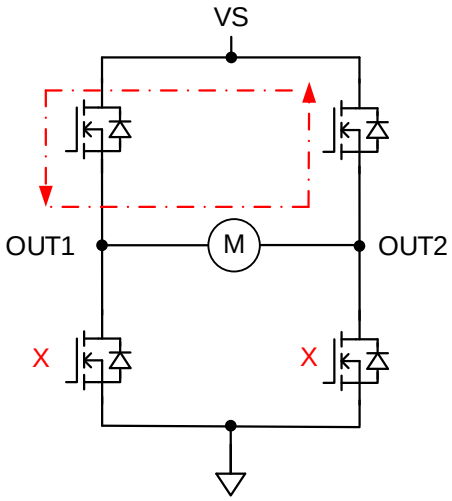


Figure 9. Brake-High-Side

Chopping Mode (With PWM)

Each half-bridge can be configured into PWM mode to drive an inductive load (e.g., DC brush motor), and has been allocated four PWM channels with individual duty cycle settings with 8-bit resolution. The device has four PWM frequency 80-Hz, 100-Hz, 200-Hz and 2-kHz for different application.

The PWM chopping mode operation is configured in five steps as follows:

1. PWM Configuration
2. Free-wheeling Mode (Synchronous Rectification) Disable/Enable
3. PWM Channels Mapping
4. PWM Channels Configuration (PWM Frequency and PWM Duty)
5. Half-bridge Enable

PWM Configuration

Half-bridge can be configured into continuous mode or chopping mode (PWM mode) by using the PWM control register (PWM_CTRL_1 and PWM_CTRL_2). The HBx_PWM bit = 1 is set to enable the PWM switching mode, otherwise it will operate in continuous mode. The PWM_CHx_DIS bit in PWM control register (PWM_CTRL_2) is set to enable the PWM generator.

Free-Wheeling Mode (Synchronous Rectification) Disable/Enable

The device support to select the synchronous rectification mode by setting the HBx_FW bit in free-wheeling control registers (FW_CTRL_1 and FW_CTRL_2). Figure 10 shows when the HBx_FW is disable, the current path will go through the high-side diode during the PWM off time. If the HBx_FW is enabled, it will open the FET to create a current path. Figure 11 shows example of the synchronous rectification, where the high-side FET of OUT2 half-bridge is turned on when the low-side FET of same half-bridge is turned off in a PWM cycle.

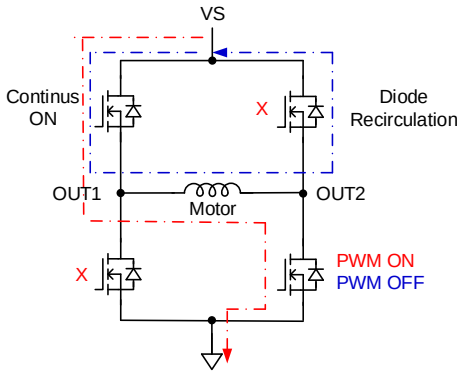


Figure 10. PWM Mode (Synchronous Rectification =OFF)

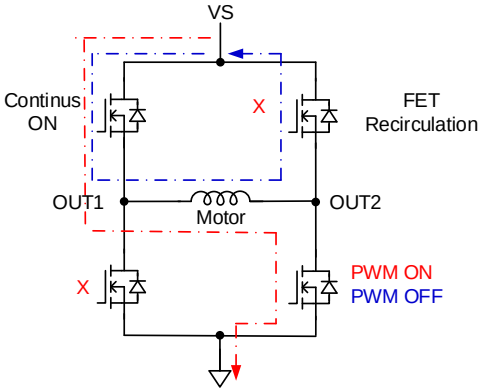


Figure 11. PWM Mode (Synchronous Rectification =ON)

PWM Channels Mapping

By configuring the PWM map control registers (PWM_MAP_CTRL_x), the any of the OUTx half bridge outputs can map different PWM generator, because the device includes 4 PWM generators. The HBx_PWM_MAP bits are used to map any of the 12 channels, as shown in Table 1.

Table 1. PWM Mapping

HBx_PWM MAP BITS	PWM CHANNEL
HBx_PWM_MAP=00b	Channel 1 selected for OUTx
HBx_PWM_MAP=01b	Channel 2 selected for OUTx
HBx_PWM_MAP=10b	Channel 3 selected for OUTx
HBx_PWM_MAP=11b	Channel 4 selected for OUTx

PWM Channels Configuration (PWM Frequency and PWM Duty)

Each PWM generator can be configured different frequency and duty independently. The PWM frequency of each channel is controlled by the PWM frequency control register (PWM_FREQ_CTRL). The PWM_DUTY_CHx bit of the PWM duty control register (PWM_DUTY_CTRL_x) is used to control PWM duty output, detailed shown in Table 2.

Table 2. PWM Frequency

HBX_PWM MAP BITS	PWM CHANNEL
PWM_CHx_FREQ=00b	80Hz
PWM_CHx_FREQ =01b	100Hz
PWM_CHx_FREQ =10b	200Hz
PWM_CHx_FREQ =11b	2000Hz

Table 3. PWM Duty Control Channelx Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PWM_DUTY_CHx	R/W	00000000b	00000000b = 0 % PWM Duty 11111111b = 100 % PWM Duty Calculate duty as decimal (xxxxxxxxb) × 1/255

Half-Bridge Enable

After the four steps, the last step is set high-side or low-side enable. Once the half-bridge is configured for the PWM generation, the half-bridge is enabled by enabling either of the high-side or low-side switch. The HBx_HS_EN bit is used to set the high-side enable, and the HBx_LS_EN bit is used to set the low-side enable in operation control registers (OP_CTRL_1, OP_CTRL_2, OP_CTRL_3).

Protection Circuits

This device has embedded protective functions such as undervoltage, overvoltage, overcurrent, power on reset, open load, thermal shutdown.

Undervoltage Lockout (UVLO)

When voltage VS drops below V_{UVLO_FALL}, all output stages are switched off. However, the logic information remains intact and uncorrupted. The VS under-voltage error bit is also latched high in the IC status register (IC_START), the nFAULT pin is driven low. If VS voltage rises again and reaches the switch on voltage V_{UVLO_RISE} threshold, the power stages will automatically be activated and the nFAULT pin is released. The UVLO error bit remains set until cleared through the CLR_FLT bit.

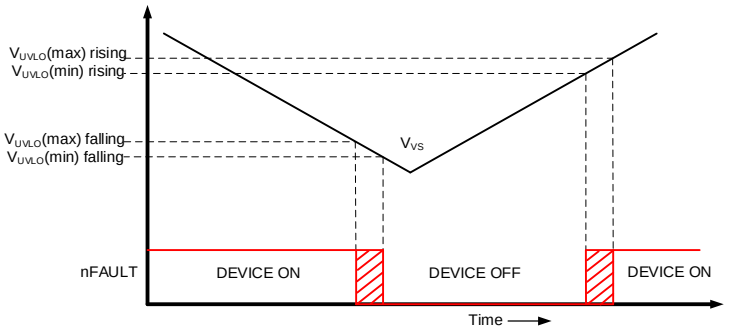


Figure 12. VS UVLO Operation

Overvoltage Protection (OVP)

In the event the supply voltage VS rises above the switch off voltage V_{OVP}, all output stages are switched off. The VS overvoltage error bit is also latched high in the IC status register (IC_START), the nFAULT pin is driven low. If VS falls again and reaches the switch-on voltage threshold (V_{OVP} -V_{OVP_HYS}), the power stages will automatically be activated and the nFAULT pin is released. The OVP error bit remains set until cleared through the CLR_FLT bit. The device supports an extended overvoltage operation for higher over-voltage range up to 33V by enabling the EXT_OVP bit in CONFIG_CTRL register.

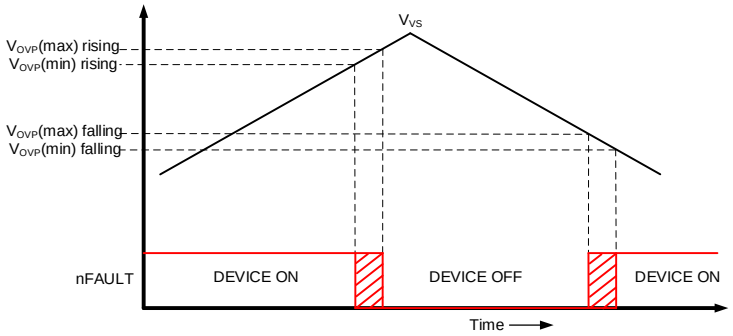


Figure 13. VS OVP Operation

VDD Power on Reset (POR)

In the event the VDD logic supply decreases below the undervoltage threshold, V_{POR_FALL}, the SPI interfaces no longer be functional and the device will enter reset mode. The digital block will be initialized and the output stages are switched off to high impedance. The undervoltage reset is released once VDD voltage levels are above the undervoltage threshold, V_{POR_ON}. The reset event is reported in CONFIG_CTRL register by the NPOR bit. The NPOR error bit remains reset and latched low until cleared through the CLR_FLT bit.

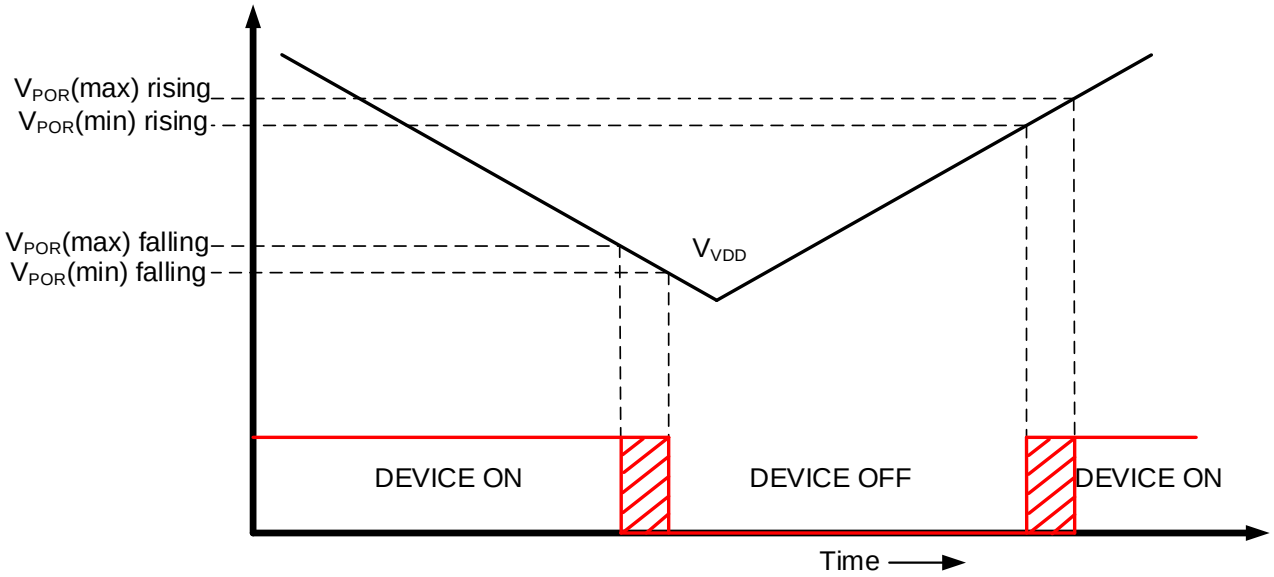


Figure 14. VDD UVLO Operation

Overcurrent Protection (OCP)

The device offers over current protection. Monitoring the current on the high side and low side drivers at any time, once the current exceeds the overcurrent shutdown threshold, the corresponding HS or LS driver is latched off and the corresponding error bit, HBx_HS_OCP or HBx_LS_OCP is set and latched after the specified shutdown time, t_{OC}. To resume normal functionality of the power switch (in the event the overcurrent condition disappears or to verify if the failure still exists), user could disable the OCP fault on the nFAULT pin by setting the OCP_REP bit in the CONFIG_CTRL register.

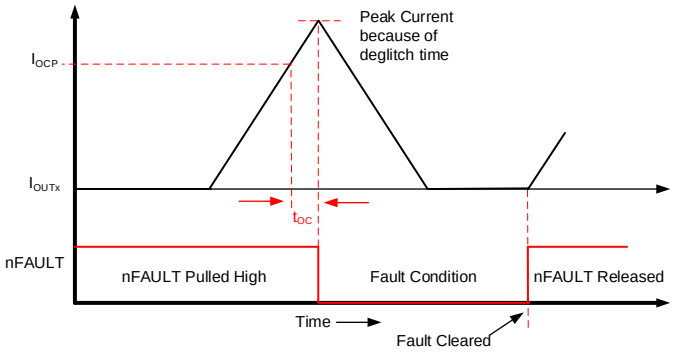


Figure 15. Over Current Protection

Open Load Detection (OLD)

The open-load detection (OLD) function ensures the proper load connection. The device support active OLD and low-current OLD.

Active OLD

Active OLD can identify an open-load condition on the OUTx pins while driving a load. As shown in Figure 16, open-load fault would be detected if the motor current I_{OUTx} is lower than the open-load current threshold (I_{OLD}) and the duration of fault condition longer than the open-load deglitch time (t_{OLD}). If the active OLD happen, the nFAULT pin will go down. When the open-load condition is removed and set the CLR_FLT bit to 1, the nFAULT pin be released. The controller also can read the register to know whether there is an open-load condition. The OLD bit in the IC status (IC_STAT) register will be set to 1 and HBx_HS_OLD or HBx_LS_OLD bit in the open-load status register (OLD_STAT_x) will be set to 1. There are two OLD control registers (OLD_CTRL_1 and OLD_CTRL_2) are used to configure OLD function. The HBx_OLD_DIS bit in OLD_CTRL_1 register allows the user to disable OLD on the OUTx pins, OLD on the devices is enabled by default. The OLD_REP bit in the OLD_CTRL_2 register determines whether report on the nFAULT pin. The OLD_OP bit determines the response of the device to an active OLD fault. If OLD_OP = 0, the OUTx pins go to the Hi-Z state to stop driving the outputs. Otherwise, the OUTx pins will stay in their previous state and do not react to the OLD fault unless the controller takes action.

Low-Current OLD

The device also includes a low-current OLD mode which is similar with active open-load detection. The difference between low-current open-load and active open-load is the current detection threshold. The current detection threshold is around 10x lower than the active open-load detection scheme. In addition, the low-current open-load only work in the low-side MOSFET. Enable the low-current OLD mode will also disable the high-side OLD for the particular half-bridge. As shown in Figure 17, If the motor current I_{OUTx} is lower than the open-load current threshold (I_{OLD_LOW}) and the duration of fault condition longer than the open-load deglitch time (t_{OLD}). The device will identify a low-current open-load fault condition. If the low-current OLD happen, the nFAULT pin will go down. When the open-load condition is removed and set the CLR_FLT bit to 1, the nFAULT pin release. The controller also can read the register to know whether there is an open-load fault. The OLD bit in the IC status (IC_STAT) register will be set to 1 and HBx_LS_OLD bit in the open-load status register (OLD_STAT_x) will be set to 1.

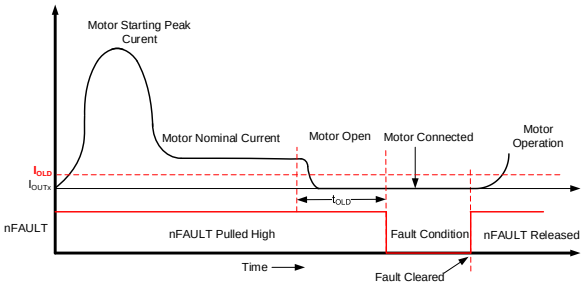


Figure 16. Active Open-load Detection

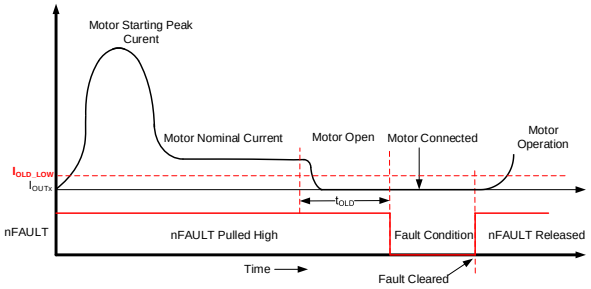


Figure 17. Low-current OLD

Thermal Warning (OTW)

The device offers temperature warning protection. If one or more temperature sensors reach the warning temperature, the temperature pre-warning bit, OTW is set in the IC status (IC_START) register. This bit is latched and can only be cleared via SPI, but the outputs stages remain activated. The reporting of OTW on the nFAULT pin can be enabled by setting the over-temperature warning reporting (OTW_REP) bit in the configuration control (CONFIG_CTRL) register. The nFAULT pin releases when the die temperature decreases below the hysteresis point of the thermal warning (T_{WARN_HYS})

Thermal Shutdown (TSD)

If one or more temperature sensors reach the shut-down temperature threshold, all outputs are latched off and the nFAULT pin is driven low. The OTSD bit is set in the IC status (IC_START) register. All outputs will be activated and the nFAULT pin is released when the overtemperature shutdown condition is removed and die temperature decreases below the hysteresis point of the thermal warning (T_{HYS}). The OTSD bit remains latched high indicating that a thermal event occurred until a clear fault command is issued through the CLR_FLT bit. This protection feature cannot be disabled.

Programming Configuration

SPI

The device supports standard 16-bit SPI to be controlled. The commutation is performed by MSB clocked in first. The SPI interface is a synchronous serial interface for address and data transfer at bit rates of up to 5MHz. It is configured in 8-bit bytes designed to interface with a standard SPI bus. Four pins are used to communicate on the SPI: SCLK (synchronous clock), CSB (chip select, active low), SI (data input to the device for write operations,) and SO (data output from the device for read operations). As shown in Figure 18.

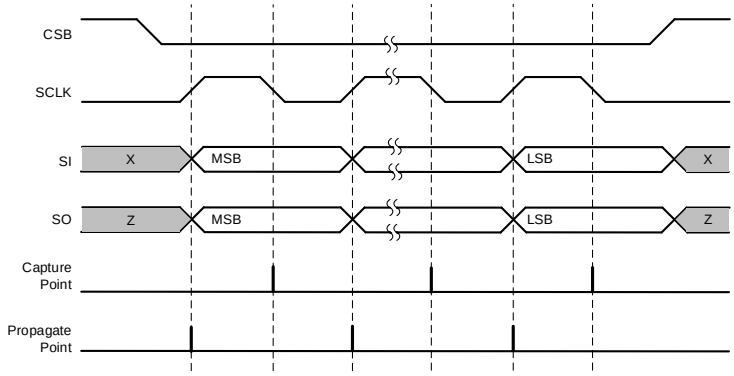


Figure 18. SPI Data Frame

A valid frame must meet the following conditions:

1). When the CSB pin is pulled high, any signals at the SCLK and SI pins are ignored and the SO pin is placed in the Hi-Z state

2). Data is captured on the falling edge of SCLK and data is propagated on the rising edge of SCLK

3). The most significant bit (MSB) is shifted in and out first

4). A full 16 SCLK cycles must occur for transaction to be valid

5). Data word sent to the SI pin should not be less than or more than 16 bits

6). For a write command, the existing data in the register being written to is shifted out on the SO pin following the 8-bit command data

SPI Format

Each SPI communication starts with one address byte followed by one data byte. The SPI function of the device has 1 R/W bit in bit14, 6 address bits and 8 data bits. The control registers are READ/WRITE registers. To set the control register to READ, bit 14 of the address must be programmed to '1', otherwise '0' for WRITE. While the microcontroller sends the address byte on SI, SO shifts out the IC Status Register data. A further data byte (bit7-bit0) is allocated to either configure the half-bridges or retrieve status information of the device. The SPI Registers have been mapped as shown in Table 6 respectively.

Table 4. SI Input Data Word Format

		R/W	Address						Data							
Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data	0	W0	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

Table 5. SO Output Data Word Format

			Address						Data							
Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data	1	1	OTSD	OLD	OCP	UVLO	OVP	NPOR	D7	D6	D5	D4	D3	D2	D1	D0

Daisy Chain

The device supports daisy chain operation with devices with the same SPI protocol shown in Figure 20. The master output (MO) is connected to a slave SI and the first slave SO is connected to the next slave SI to form a chain. The SO of the final slave in the chain will be connected to the master input (MI) to close the loop of the SPI communication frame. In daisy chain configuration, a single chip selects, CSB, and clock signal, SCLK, connected in parallel to each slave device, are used by the microcontroller to control or access the SPI devices. Figure 19 shows the topology when 3 devices are connected in series with waveforms.

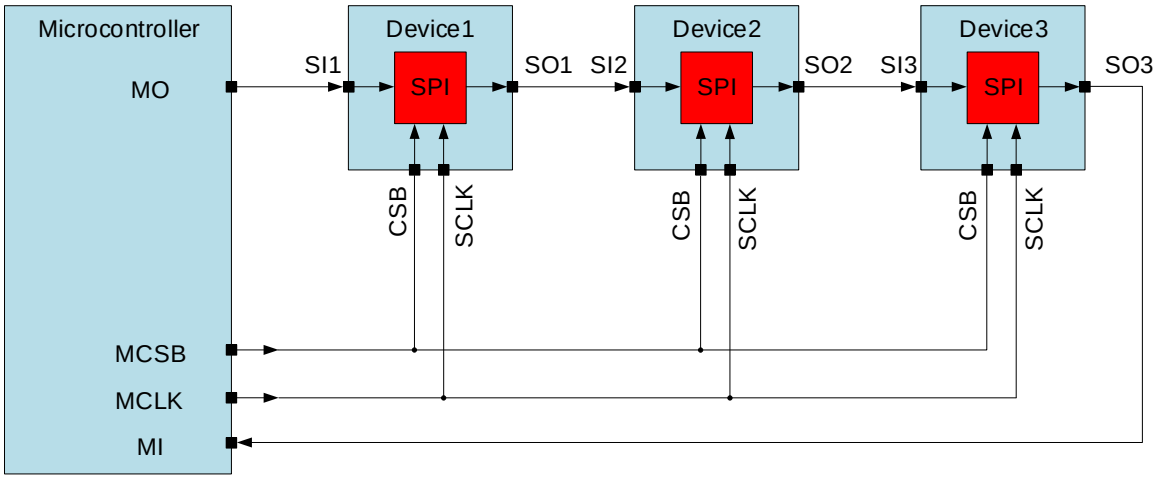


Figure 19. SPI Daisy Chain

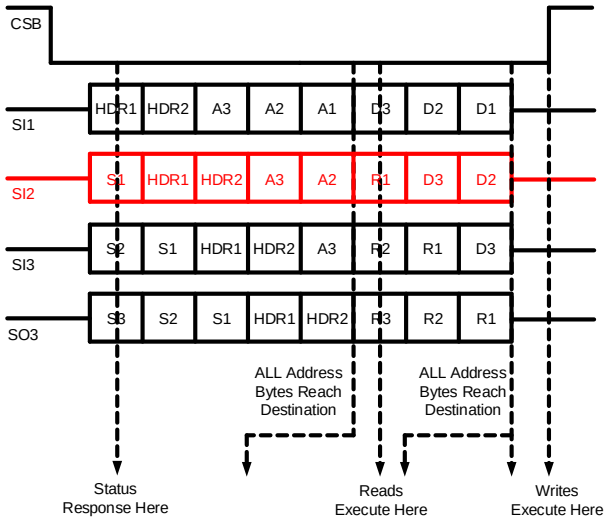


Figure 20. Daisy Chain SPI Operation

The first device in the chain shown above receives data from the master controller in the following format. See SI1 in Figure 20.

1). 2 bytes of Header
2). 3 bytes of Address
3). 3 bytes of Data

After the data has been transmitted through the chain, the master controller receives it in the following format. See SO3 in Figure 20.

1). 3 bytes of Status
2). 2 bytes of Header (should be identical to the information controller sent)
3). 3 bytes of Report

There are two Header bytes contain information of the number of devices and a global clear fault. The N5 to N0 in Header1 shows up to 2^6-1 devices can be connected in series per daisy chain connection. The CLR bit in Header2 is a global clear fault command that will clear the fault registers of all the devices. Both two Header bytes must start with 1 and 0.

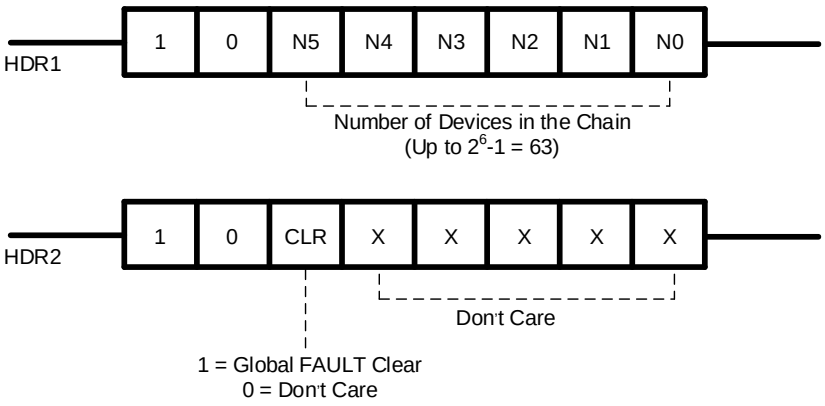


Figure 21. Header Bits

All the device will feedback fault status register in the status byte shown in Figure 21.It will be very convenient for the controller to read fault status and for the device to work efficiently.

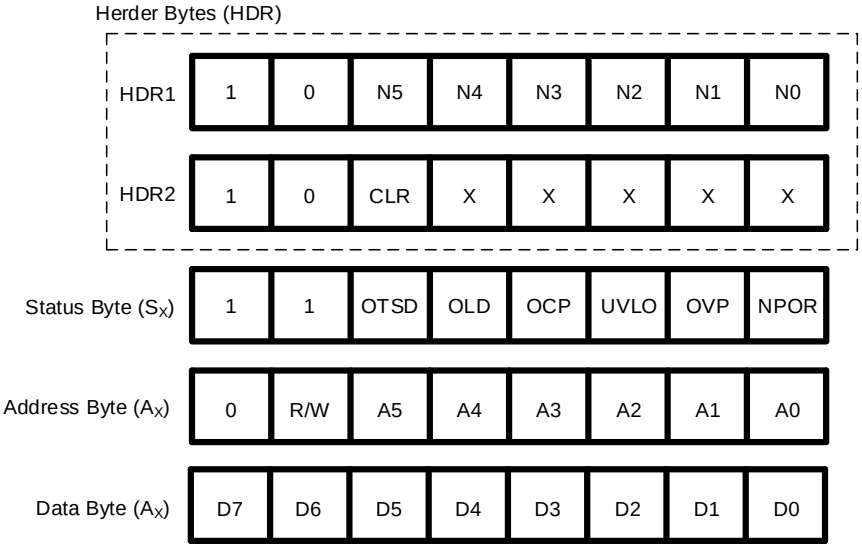


Figure 22. Daisy Chain Read Registers

The device can count the number of Status bytes behind the Header byte to recognize its position. As shown in Figure 20, the device 2 has One Status bytes (S1) behind the Header byte and the device 3 has Two Status bytes (S1, S2) behind the Header byte. When the device knows its position and the number of devices connected in the chain, the device could load the relevant address and data byte in its buffer and bypasses the other bits. In this way, even the chain has 63 devices, the device still works fleetly.

Table 6. SY2A58152 Register Map

Name	7	6	5	4	3	2	1	0	Type	Address
IC_STAT	Reserved	OTSD	OTW	OLD	OCP	UVLO	OVP	NPOR	R	00h
OCP_STAT_1	HB4_HS_OCP	HB4_LS_OCP	HB3_HS_OCP	HB3_LS_OCP	HB2_HS_OCP	HB2_LS_OCP	HB1_HS_OCP	HB1_LS_OCP	R	01h
OCP_STAT_2	HB8_HS_OCP	HB8_LS_OCP	HB7_HS_OCP	HB7_LS_OCP	HB6_HS_OCP	HB6_LS_OCP	HB5_HS_OCP	HB5_LS_OCP	R	02h
OCP_STAT_3	HB12_HS_OCP	HB12_LS_OCP	HB11_HS_OCP	HB11_LS_OCP	HB10_HS_OCP	HB10_LS_OCP	HB9_HS_OCP	HB9_LS_OCP	R	03h
OLD_STAT_1	HB4_HS_OLD	HB4_LS_OLD	HB3_HS_OLD	HB3_LS_OLD	HB2_HS_OLD	HB2_LS_OLD	HB1_HS_OLD	HB1_LS_OLD	R	04h
OLD_STAT_2	HB8_HS_OLD	HB8_LS_OLD	HB7_HS_OLD	HB7_LS_OLD	HB6_HS_OLD	HB6_LS_OLD	HB5_HS_OLD	HB5_LS_OLD	R	05h
OLD_STAT_3	HB12_HS_OLD	HB12_LS_OLD	HB11_HS_OLD	HB11_LS_OLD	HB10_HS_OLD	HB10_LS_OLD	HB9_HS_OLD	HB9_LS_OLD	R	06h
CONFIG_CTRL	Reserved				OCP_REP		EXT_OVP	CLR_FLT	RW	07h
OP_CTRL_1	HB4_HS_EN	HB4_LS_EN	HB3_HS_EN	HB3_LS_EN	HB2_HS_EN	HB2_LS_EN	HB1_HS_EN	HB1_LS_EN	RW	08h
OP_CTRL_2	HB8_HS_EN	HB8_LS_EN	HB7_HS_EN	HB7_LS_EN	HB6_HS_EN	HB6_LS_EN	HB5_HS_EN	HB5_LS_EN	RW	09h
OP_CTRL_3	HB12_HS_EN	HB12_LS_EN	HB11_HS_EN	HB11_LS_EN	HB10_HS_EN	HB10_LS_EN	HB9_HS_EN	HB9_LS_EN	RW	0Ah
PWM_CTRL_1	HB8_PWM	HB7_PWM	HB6_PWM	HB5_PWM	HB4_PWM	HB3_PWM	HB2_PWM	HB1_PWM	RW	0Bh
PWM_CTRL_2	PWM_CH4_DIS	PWM_CH3_DIS	PWM_CH2_DIS	PWM_CH1_DIS	HB12_PWM	HB11_PWM	HB10_PWM	HB9_PWM	RW	0Ch
FW_CTRL_1	HB8_FW	HB7_FW	HB6_FW	HB5_FW	HB4_FW	HB3_FW	HB2_FW	HB1_FW	RW	0Dh
FW_CTRL_2	Reserved				HB12_FW	HB11_FW	HB10_FW	HB9_FW	RW	0Eh
PWM_MAP_CTRL_1	HB4_PWM_MAP		HB3_PWM_MAP		HB2_PWM_MAP		HB1_PWM_MAP		RW	0Fh
PWM_MAP_CTRL_2	HB8_PWM_MAP		HB7_PWM_MAP		HB6_PWM_MAP		HB5_PWM_MAP		RW	10h
PWM_MAP_CTRL_3	HB12_PWM_MAP		HB11_PWM_MAP		HB10_PWM_MAP		HB9_PWM_MAP		RW	11h
PWM_FREQ_CTRL	PWM_CH4_FREQ		PWM_CH3_FREQ		PWM_CH2_FREQ		PWM_CH1_FREQ		RW	12h
PWM_DUTY_CTRL_1	PWM_DUTY_CH1								RW	13h
PWM_DUTY_CTRL_2	PWM_DUTY_CH2								RW	14h
PWM_DUTY_CTRL_3	PWM_DUTY_CH3								RW	15h
PWM_DUTY_CTRL_4	PWM_DUTY_CH4								RW	16h
SR_CTRL_1	HB8_SR	HB7_SR	HB6_SR	HB5_SR	HB4_SR	HB3_SR	HB2_SR	HB1_SR	RW	17h
SR_CTRL_2	Reserved				HB12_SR	HB11_SR	HB10_SR	HB9_SR	RW	18h
OLD_CTRL_1	HB8_OLD_DIS	HB7_OLD_DIS	HB6_OLD_DIS	HB5_OLD_DIS	HB4_OLD_DIS	HB3_OLD_DIS	HB2_OLD_DIS	HB1_OLD_DIS	RW	19h
OLD_CTRL_2	OLD_REP	OLD_OP	Reserved		HB12_OLD_DIS	HB11_OLD_DIS	HB10_OLD_DIS	HB9_OLD_DIS	RW	1Ah
OLD_CTRL_3	OCP_DEG		Reserved		HB12_LOLD_EN	HB11_LOLD_EN	HB10_LOLD_EN	HB9_LOLD_EN	RW	1Bh
OLD_CTRL_4	HB8_LOLD_EN	HB7_LOLD_EN	HB6_LOLD_EN	HB5_LOLD_EN	HB4_LOLD_EN	HB3_LOLD_EN	HB2_LOLD_EN	HB1_LOLD_EN	RW	24h

SPI Status Registers

The Status Register are used to report warning and fault conditions. The status registers are read-only registers.

IC_STAT

IC_Status Register (Address =0x00) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	OTSD	OTW	OLD	OCP	UVLO	OVP	NPOR
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
Reserved	D7	r	
OTSD	D6	r	Temperature shutdown error detection 0_B Junction temperature below temperature shutdown threshold 1_B Junction temperature has reached temperature shutdown threshold
OTW	D5	r	Temperature pre-warning error detection 0_B Junction temperature below temperature pre-warning threshold 1_B Junction temperature has reached temperature pre-warning threshold.
OLD	D4	r	Open Load error detection 0_B No Open Load 1_B Open load
OCP	D3	r	Over current error detection 0_B No Over current 1_B Over current
UVLO	D2	r	VS Undervoltage error detection 0_B No undervoltage on VS detected 1_B Undervoltage on VS detected
OVP	D1	r	VS Overvoltage error detection 0_B No overvoltage on VS detected 1_B Overvoltage on VS detected
NPOR	D0	r	Not Power on Reset (NPOR) detection 0_B POR on EN or VDD supply rail 1_B No POR

OCP_STAT_1

Overcurrent Error Status of Half-bridge Outputs 1-4 (Address =0x01) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB4_HS_OC	HB4_LS_OC	HB3_HS_OC	HB3_LS_OC	HB2_HS_OC	HB2_LS_OC	HB1_HS_OC	HB1_LS_OC
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
HB4_HS_OC	D7	r	High-side (HS) switch of half-bridge 4 overcurrent detection 0_B No error on HS4 switch 1_B Overcurrent detected on HS4 switch
HB4_LS_OC	D6	r	Low-side (LS) switch of half-bridge 4 overcurrent detection 0_B No error on LS4 switch 1_B Overcurrent detected on LS4 switch
HB3_HS_OC	D5	r	High-side (HS) switch of half-bridge 3 overcurrent detection 0_B No error on HS3 switch 1_B Overcurrent detected on HS3 switch
HB3_LS_OC	D4	r	Low-side (LS) switch of half-bridge 3 overcurrent detection 0_B No error on LS3 switch 1_B Overcurrent detected on LS3 switch

HB2_HS_OC	D3	r	High-side (HS) switch of half-bridge 2 overcurrent detection 0_B No error on HS2 switch 1_B Overcurrent detected on HS2 switch
HB2_LS_OC	D2	r	Low-side (LS) switch of half-bridge 2 overcurrent detection 0_B No error on LS2 switch 1_B Overcurrent detected on LS2 switch
HB1_HS_OC	D1	r	High-side (HS) switch of half-bridge 1 overcurrent detection 0_B No error on HS1 switch 1_B Overcurrent detected on HS1 switch
HB1_LS_OC	D0	r	Low-side (LS) switch of half-bridge 1 overcurrent detection 0_B No error on LS1 switch 1_B Overcurrent detected on LS1 switch

OCP_STAT_2

Overcurrent Error Status of Half-bridge Outputs 5-8 (Address =0x02) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_HS_OC	HB8_LS_OC	HB7_HS_OC	HB7_LS_OC	HB6_HS_OC	HB6_LS_OC	HB5_HS_OC	HB5_LS_OC
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
HB8_HS_OC	D7	r	High-side (HS) switch of half-bridge 8 overcurrent detection 0_B No error on HS8 switch 1_B Overcurrent detected on HS8 switch
HB8_LS_OC	D6	r	Low-side (LS) switch of half-bridge 8 overcurrent detection 0_B No error on LS8 switch 1_B Overcurrent detected on LS8 switch
HB7_HS_OC	D5	r	High-side (HS) switch of half-bridge 7 overcurrent detection 0_B No error on HS7 switch 1_B Overcurrent detected on HS7 switch
HB7_LS_OC	D4	r	Low-side (LS) switch of half-bridge 7 overcurrent detection 0_B No error on LS7 switch 1_B Overcurrent detected on LS7 switch
HB6_HS_OC	D3	r	High-side (HS) switch of half-bridge 6 overcurrent detection 0_B No error on HS6 switch 1_B Overcurrent detected on HS6 switch
HB6_LS_OC	D2	r	Low-side (LS) switch of half-bridge 6 overcurrent detection 0_B No error on LS6 switch 1_B Overcurrent detected on LS6 switch
HB5_HS_OC	D1	r	High-side (HS) switch of half-bridge 5 overcurrent detection 0_B No error on HS5 switch 1_B Overcurrent detected on HS5 switch
HB5_LS_OC	D0	r	Low-side (LS) switch of half-bridge 5 overcurrent detection 0_B No error on LS5 switch 1_B Overcurrent detected on LS5 switch

OCP_STAT_3

Overcurrent Error Status of Half-bridge Outputs 9-12 (Address =0x03) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB12_HS_OC	HB12_LS_OC	HB11_HS_OC	HB11_LS_OC	HB10_HS_OC	HB10_LS_OC	HB9_HS_OC	HB9_LS_OC
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
HB12_HS_OC	D7	r	High-side (HS) switch of half-bridge 12 overcurrent detection 0_B No error on HS12 switch 1_B Overcurrent detected on HS12 switch
HB12_LS_OC	D6	r	Low-side (LS) switch of half-bridge 12 overcurrent detection

			0_B No error on LS12 switch 1_B Overcurrent detected on LS12 switch
HB11_HS_OC	D5	r	High-side (HS) switch of half-bridge 11 overcurrent detection 0_B No error on HS11 switch 1_B Overcurrent detected on HS11 switch
HB11_LS_OC	D4	r	Low-side (LS) switch of half-bridge 11 overcurrent detection 0_B No error on LS11 switch 1_B Overcurrent detected on LS11 switch
HB10_HS_OC	D3	r	High-side (HS) switch of half-bridge 10 overcurrent detection 0_B No error on HS10 switch 1_B Overcurrent detected on HS10 switch
HB10_LS_OC	D2	r	Low-side (LS) switch of half-bridge 10 overcurrent detection 0_B No error on LS10 switch 1_B Overcurrent detected on LS10 switch
HB9_HS_OC	D1	r	High-side (HS) switch of half-bridge 9 overcurrent detection 0_B No error on HS9 switch 1_B Overcurrent detected on HS9 switch
HB9_LS_OC	D0	r	Low-side (LS) switch of half-bridge 9 overcurrent detection 0_B No error on LS9 switch 1_B Overcurrent detected on LS9 switch

OLD_STAT_1

Open Load Error Status of Half-bridge Outputs 1-4 (Address =0x04) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB4_HS_OL	HB4_LS_OL	HB3_HS_OL	HB3_LS_OL	HB2_HS_OL	HB2_LS_OL	HB1_HS_OL	HB1_LS_OL
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
HB4_HS_OL	D7	r	High-side (HS) switch of half-bridge 4 open load detection 0_B No error on HS4 switch (default value) 1_B Open load detected on HS4 switch
HB4_LS_OL	D6	r	Low-side (LS) switch of half-bridge 4 open load detection 0_B No error on LS4 switch (default value) 1_B Open load detected on LS4 switch
HB3_HS_OL	D5	r	High-side (HS) switch of half-bridge 3 open load detection 0_B No error on HS3 switch (default value) 1_B Open load detected on HS3 switch
HB3_LS_OL	D4	r	Low-side (LS) switch of half-bridge 3 open load detection 0_B No error on LS3 switch (default value) 1_B Open load detected on LS3 switch
HB2_HS_OL	D3	r	High-side (HS) switch of half-bridge 2 open load detection 0_B No error on HS2 switch (default value) 1_B Open load detected on HS2 switch
HB2_LS_OL	D2	r	Low-side (LS) switch of half-bridge 2 open loadt detection 0_B No error on LS2 switch (default value) 1_B Open load detected on LS2 switch
HB1_HS_OL	D1	r	High-side (HS) switch of half-bridge 1 open load detection 0_B No error on HS1 switch (default value) 1_B Open load detected on HS1 switch
HB1_LS_OL	D0	r	Low-side (LS) switch of half-bridge 1 open load detection 0_B No error on LS1 switch (default value) 1_B Open load detected on LS1 switch

OLD_STAT_2

Open Load Error Status of Half-bridge Outputs 5-8 (Address =0x05) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_HS_OL	HB8_LS_OL	HB7_HS_OL	HB7_LS_OL	HB6_HS_OL	HB6_LS_OL	HB5_HS_OL	HB5_LS_OL
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
HB8_HS_OL	D7	r	High-side (HS) switch of half-bridge 8 open load detection 0_B No error on HS8 switch 1_B Open load detected on HS8 switch
HB8_LS_OL	D6	r	Low-side (LS) switch of half-bridge 8 open load detection 0_B No error on LS8 switch 1_B Open load detected on LS8 switch
HB7_HS_OL	D5	r	High-side (HS) switch of half-bridge 7 open load detection 0_B No error on HS7 switch 1_B Open load detected on HS7 switch
HB7_LS_OL	D4	r	Low-side (LS) switch of half-bridge 7 open load detection 0_B No error on LS7 switch 1_B Open load detected on LS7 switch
HB6_HS_OL	D3	r	High-side (HS) switch of half-bridge 6 open load detection 0_B No error on HS6 switch 1_B Open load detected on HS6 switch
HB6_LS_OL	D2	r	Low-side (LS) switch of half-bridge 6 open load detection 0_B No error on LS6 switch 1_B Open load detected on LS6 switch
HB5_HS_OL	D1	r	High-side (HS) switch of half-bridge 5 open load detection 0_B No error on HS5 switch 1_B Open load detected on HS5 switch
HB5_LS_OL	D0	r	Low-side (LS) switch of half-bridge 5 open load detection 0_B No error on LS5 switch 1_B Open load detected on LS5 switch

OLD_STAT_3

Open Load Error Status of Half-bridge Outputs 9-12 (Address =0x06) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB12_HS_OL	HB12_LS_OL	HB11_HS_OL	HB11_LS_OL	HB10_HS_OL	HB10_LS_OL	HB9_HS_OL	HB9_LS_OL
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
HB12_HS_OL	D7	r	High-side (HS) switch of half-bridge 12 open load detection 0_B No error on HS12 switch 1_B Open load detected on HS12 switch
HB12_LS_OL	D6	r	Low-side (LS) switch of half-bridge 12 open load detection 0_B No error on LS12 switch 1_B Open load detected on LS12 switch
HB11_HS_OL	D5	r	High-side (HS) switch of half-bridge 11 open load detection 0_B No error on HS11 switch 1_B Open load detected on HS11 switch
HB11_LS_OL	D4	r	Low-side (LS) switch of half-bridge 11 open load detection 0_B No error on LS11 switch 1_B Open load detected on LS11 switch
HB10_HS_OL	D3	r	High-side (HS) switch of half-bridge 10 open load detection 0_B No error on HS10 switch 1_B Open load detected on HS10 switch
HB10_LS_OL	D2	r	Low-side (LS) switch of half-bridge 10 open load detection 0_B No error on LS10 switch

			1_B Open load detected on LS10 switch
HB9_HS_OL	D1	r	High-side (HS) switch of half-bridge 9 open load detection 0_B No error on HS9 switch 1_B Open load detected on HS9 switch
HB9_LS_OL	D0	r	Low-side (LS) switch of half-bridge 9 open load detection 0_B No error on LS9 switch 1_B Open load detected on LS9 switch

SPI Control Registers

The Control Register are used to configure the device. The control registers are read and write capable.

CONFIG_CTRL

Configuration Register (Address =0x07) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	OCP_REG	OTW_REG	EXT_OVP	CLR_FLT
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
Reserved	D7	r/w	Bit reserved. Always reads ‘0’.
Reserved	D6	r/w	Bit reserved. Always reads ‘0’.
Reserved	D5	r/w	Bit reserved. Always reads ‘0’.
Reserved	D4	r/w	Bit reserved. Always reads ‘0’.
OCP_REG	D3	r/w	0_B Overcurrent condition is reported in nFAULT pin 1_B Overcurrent condition warning is not reported in nFAULT pin
OTW_REG	D2	r/w	0_B Overtemperature warning is not reported in nFAULT pin 1_B Overtemperature warning is reported in nFAULT pin
EXT_OVP	D1	r/w	0_B Overvoltage protection threshold is at 21V min. 1_B Overvoltage protection threshold is at 32.7V min.
CLR_FLT	D0	r/w	0_B Faults not cleared 1_B Clear all faults

OP_CTRL_1

Half-bridge Output Control 1(Address =0x08) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB4_HS_EN	HB4_LS_EN	HB3_HS_EN	HB3_LS_EN	HB2_HS_EN	HB2_LS_EN	HB1_HS_EN	HB1_LS_EN
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
HB4_HS_EN	D7	r/w	Half-bridge output 4 High side switch enable 0_B HS4 OFF 1_B HS4 ON
HB4_LS_EN	D6	r/w	Half-bridge output 4 Low side switch enable 0_B LS4 OFF 1_B LS4 ON
HB3_HS_EN	D5	r/w	Half-bridge output 3 High side switch enable 0_B HS3 OFF 1_B HS3 ON
HB3_LS_EN	D4	r/w	Half-bridge output 3 Low side switch enable 0_B LS3 OFF 1_B LS3 ON
HB2_HS_EN	D3	r/w	Half-bridge output 2 High side switch enable 0_B HS2 OFF 1_B HS2 ON
HB2_LS_EN	D2	r/w	Half-bridge output 2 Low side switch enable 0_B LS2 OFF 1_B LS2 ON

HB1_HS_EN	D1	r/w	Half-bridge output 1 High side switch enable 0_B HS1 OFF 1_B HS1 ON
HB1_LS_EN	D0	r/w	Half-bridge output 1 Low side switch enable 0B LS1 OFF 1B LS1 ON

OP_CTRL_2
Half-bridge output control 2 (Address =0x09) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_HS_EN	HB8_LS_EN	HB7_HS_EN	HB7_LS_EN	HB6_HS_EN	HB6_LS_EN	HB5_HS_EN	HB5_LS_EN
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
HB8_HS_EN	D7	r/w	Half-bridge output 8 High side switch enable 0_B HS8 OFF 1_B HS8 ON
HB8_LS_EN	D6	r/w	Half-bridge output 8 Low side switch enable 0_B LS8 OFF 1_B LS8 ON
HB7_HS_EN	D5	r/w	Half-bridge output 7 High side switch enable 0_B HS7 OFF 1_B HS7 ON
HB7_LS_EN	D4	r/w	Half-bridge output 7 Low side switch enable 0_B LS7 OFF 1_B LS7 ON
HB6_HS_EN	D3	r/w	Half-bridge output 6 High side switch enable 0_B HS6 OFF 1_B HS6 ON
HB6_LS_EN	D2	r/w	Half-bridge output 6 Low side switch enable 0_B LS6 OFF 1_B LS6 ON
HB5_HS_EN	D1	r/w	Half-bridge output 5 High side switch enable 0_B HS5 OFF 1_B HS5 ON
HB5_LS_EN	D0	r/w	Half-bridge output 5 Low side switch enable 0_B LS5 OFF 1_B LS5 ON

OP_CTRL_3
Half-bridge output control 3 (Address =0x0A) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB12_HS_EN	HB12_LS_EN	HB11_HS_EN	HB11_LS_EN	HB10_HS_EN	HB10_LS_EN	HB9_HS_EN	HB9_LS_EN
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
HB12_HS_EN	D7	r/w	Half-bridge output 12 High side switch enable 0_B HS12 OFF 1_B HS12 ON
HB12_LS_EN	D6	r/w	Half-bridge output 12 Low side switch enable 0_B LS12 OFF 1_B LS12 ON
HB11_HS_EN	D5	r/w	Half-bridge output 11 High side switch enable 0_B HS11 OFF 1_B HS11 ON
HB11_LS_EN	D4	r/w	Half-bridge output 11 Low side switch enable

			0_B LS11 OFF 1_B LS11 ON
HB10_HS_EN	D3	r/w	Half-bridge output 10 High side switch enable 0_B HS10 OFF 1_B HS10 ON
HB10_LS_EN	D2	r/w	Half-bridge output 10 Low side switch enable 0_B LS10 OFF 1_B LS10 ON
HB9_HS_EN	D1	r/w	Half-bridge output 9 High side switch enable 0_B HS9 OFF 1_B HS9 ON
HB9_LS_EN	D0	r/w	Half-bridge output 9 Low side switch enable 0_B LS9 OFF 1_B LS9 ON

PWM_CTRL_1
Half-bridge PWM Control 1 (Address =0x0B) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_PWM	HB7_PWM	HB6_PWM	HB5_PWM	HB4_PWM	HB3_PWM	HB2_PWM	HB1_PWM
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
HB8_PWM	D7	r/w	0_B Half-bridge 8 is operating in continuous mode 1_B Half-bridge 8 is operating in PWM mode
HB7_PWM	D6	r/w	0_B Half-bridge 7 is operating in continuous mode 1_B Half-bridge 7 is operating in PWM mode
HB6_PWM	D5	r/w	0_B Half-bridge 6 is operating in continuous mode 1_B Half-bridge 6 is operating in PWM mode
HB5_PWM	D4	r/w	0_B Half-bridge 5 is operating in continuous mode 1_B Half-bridge 5 is operating in PWM mode
HB4_PWM	D3	r/w	0_B Half-bridge 4 is operating in continuous mode 1_B Half-bridge 4 is operating in PWM mode
HB3_PWM	D2	r/w	0_B Half-bridge 3 is operating in continuous mode 1_B Half-bridge 3 is operating in PWM mode
HB2_PWM	D1	r/w	0_B Half-bridge 2 is operating in continuous mode 1_B Half-bridge 2 is operating in PWM mode
HB1_PWM	D0	r/w	0_B Half-bridge 1 is operating in continuous mode 1_B Half-bridge 1 is operating in PWM mode

PWM_CTRL_2
Half-bridge PWM Control 2 (Address =0x0C) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_CH4_DIS	PWM_CH3_DIS	PWM_CH2_DIS	PWM_CH1_DIS	HB12_PWM	HB11_PWM	HB10_PWM	HB9_PWM
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
PWM_CH4_DIS	D7	r/w	0_B PWM Generator-4 is enabled 1_B PWM Generator-4 is disabled
PWM_CH3_DIS	D6	r/w	0_B PWM Generator-3 is enabled 1_B PWM Generator-3 is disabled
PWM_CH2_DIS	D5	r/w	0_B PWM Generator-2 is enabled 1_B PWM Generator-2 is disabled
PWM_CH1_DIS	D4	r/w	0_B PWM Generator-1 is enabled 1_B PWM Generator-1 is disabled
HB12_PWM	D3	r/w	0_B Half-bridge 12 is operating in continuous mode 1_B Half-bridge 12 is operating in PWM mode

HB11_PWM	D2	r/w	0_B Half-bridge 11 is operating in continuous mode 1_B Half-bridge 11 is operating in PWM mode
HB10_PWM	D1	r/w	0_B Half-bridge 10 is operating in continuous mode 1_B Half-bridge 10 is operating in PWM mode
HB9_PWM	D0	r/w	0_B Half-bridge 9 is operating in continuous mode 1_B Half-bridge 9 is operating in PWM mode

FW _CTRL_1
Free-wheeling Configuration 1 (Address =0x0D) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
FW_HB8	FW_HB7	FW_HB6	FW_HB5	FW_HB4	FW_HB3	FW_HB2	FW_HB1
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
FW_HB8	D7	r/w	HB8 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling
FW_HB7	D6	r/w	HB7 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling
FW_HB6	D5	r/w	HB6 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling
FW_HB5	D4	r/w	HB5 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling
FW_HB4	D3	r/w	HB4 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling
FW_HB3	D2	r/w	HB3 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling
FW_HB2	D1	r/w	HB2 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling
FW_HB1	D0	r/w	HB1 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling

FW _CTRL_2
Free-wheeling Configuration 2 (Address =0x0E) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	FW_HB12	FW_HB11	FW_HB10	FW_HB9
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
Reserved	D7	r/w	Reserved. Always reads as ‘0’
Reserved	D6	r/w	Reserved. Always reads as ‘0’
Reserved	D5	r/w	Reserved. Always reads as ‘0’
Reserved	D4	r/w	Reserved. Always reads as ‘0’
FW_HB12	D3	r/w	HB12 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling
FW_HB11	D2	r/w	HB11 free-wheeling configuration 0_B Passive free-wheeling

			1_B Active free-wheeling
FW_HB10	D1	r/w	HB10 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling
FW_HB9	D0	r/w	HB9 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling

PWM_MAP_CTRL_1
Half-bridge Output PWM Map Control 1 (Address =0x0F) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB4_PWM_MAP		HB3_PWM_MAP		HB2_PWM_MAP		HB1_PWM_MAP	
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
HB4_PWM_MAP	D7:D6	r/w	Half-bridge output 4 mode select 00_B PWM control with PWM Channel 1 01_B PWM control with PWM Channel 2 10_B PWM control with PWM Channel 3 11_B PWM control with PWM Channel 4
HB3_PWM_MAP	D5:D4	r/w	Half-bridge output 3 mode select 00_B PWM control with PWM Channel 1 01_B PWM control with PWM Channel 2 10_B PWM control with PWM Channel 3 11_B PWM control with PWM Channel 4
HB2_PWM_MAP	D3:D2	r/w	Half-bridge output 2 mode select 00_B PWM control with PWM Channel 1 01_B PWM control with PWM Channel 2 10_B PWM control with PWM Channel 3 11_B PWM control with PWM Channel 4
HB1_PWM_MAP	D1:D0	r/w	Half-bridge output 1 mode select 00_B PWM control with PWM Channel 1 01_B PWM control with PWM Channel 2 10_B PWM control with PWM Channel 3 11_B PWM control with PWM Channel 4

PWM_MAP_CTRL_2
Half-bridge Output PWM Map Control 2 (Address =0x10) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_PWM_MAP		HB7_PWM_MAP		HB6_PWM_MAP		HB5_PWM_MAP	
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
HB8_PWM_MAP	D7:D6	r/w	Half-bridge output 8 mode select 00_B PWM control with PWM Channel 1 01_B PWM control with PWM Channel 2 10_B PWM control with PWM Channel 3 11_B PWM control with PWM Channel 4
HB7_PWM_MAP	D5:D4	r/w	Half-bridge output 7 mode select 00_B PWM control with PWM Channel 1 01_B PWM control with PWM Channel 2 10_B PWM control with PWM Channel 3 11_B PWM control with PWM Channel 4
HB6_PWM_MAP	D3:D2	r/w	Half-bridge output 6 mode select 00_B PWM control with PWM Channel 1 01_B PWM control with PWM Channel 2

			10_B PWM control with PWM Channel 3 11_B PWM control with PWM Channel 4
HB5_PWM_MAP	D1:D0	r/w	Half-bridge output 5 mode select 00_B PWM control with PWM Channel 1 01_B PWM control with PWM Channel 2 10_B PWM control with PWM Channel 3 11_B PWM control with PWM Channel 4

PWM_MAP_CTRL_3

Half-bridge Output PWM Map Control 3 (Address =0x11) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB12_PWM_MAP		HB11_PWM_MAP		HB10_PWM_MAP		HB9_PWM_MAP	
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
HB12_PWM_MAP	D7:D6	r/w	Half-bridge output 12 mode select 00_B PWM control with PWM Channel 1 01_B PWM control with PWM Channel 2 10_B PWM control with PWM Channel 3 11_B PWM control with PWM Channel 4
HB11_PWM_MAP	D5:D4	r/w	Half-bridge output 11 mode select 00_B PWM control with PWM Channel 1 01_B PWM control with PWM Channel 2 10_B PWM control with PWM Channel 3 11_B PWM control with PWM Channel 4
HB10_PWM_MAP	D3:D2	r/w	Half-bridge output 10 mode select 00_B PWM control with PWM Channel 1 01_B PWM control with PWM Channel 2 10_B PWM control with PWM Channel 3 11_B PWM control with PWM Channel 4
HB9_PWM_MAP	D1:D0	r/w	Half-bridge output 9 mode select 00_B PWM control with PWM Channel 1 01_B PWM control with PWM Channel 2 10_B PWM control with PWM Channel 3 11_B PWM control with PWM Channel 4

PWM_ FREQ_CTRL

PWM Channel Frequency Select (Address =0x12) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_CH4_FREQ		PWM_CH3_FREQ		PWM_CH2_FREQ		PWM_CH1_FREQ	
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
PWM_CH4_FREQ	D7:D6	r/w	PWM Channel 4 frequency select 00_B PWM frequency: 80Hz 01_B PWM frequency: 100Hz 10_B PWM frequency: 200Hz 11_B PWM frequency: 2000Hz
PWM_CH3_FREQ	D5:D4	r/w	PWM Channel 3 frequency select 00_B PWM frequency: 80Hz 01_B PWM frequency: 100Hz 10_B PWM frequency: 200Hz 11_B PWM frequency: 2000Hz
PWM_CH2_FREQ	D3:D2	r/w	PWM Channel 2 frequency select 00_B PWM frequency: 80Hz 01_B PWM frequency: 100Hz

			10_B PWM frequency: 200Hz 11_B PWM frequency: 2000Hz
PWM_CH1_FREQ	D1:D0	r/w	PWM Channel 1 frequency select 00_B PWM frequency: 80Hz 01_B PWM frequency: 100Hz 10_B PWM frequency: 200Hz 11_B PWM frequency: 2000Hz

PWM_DUTY_CTRL_1

PWM Channel 1 Duty Cycle Configuration (Address =0x13) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH1							
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
PWM_DUTY_CH1	D7:D0	r/w	PWM Channel 1 Duty Cycle configuration 0000 0000_B 100% OFF xxxx $xxxx_B$ parts of 255 ON 1111 1111_B 100% ON

PWM1_DUTY_CTRL_2

PWM Channel 2 Duty Cycle Configuration (Address =0x14) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH2							
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
PWM_DUTY_CH2	D7:D0	r/w	PWM Channel 2 Duty Cycle configuration 0000 0000_B 100% OFF xxxx $xxxx_B$ parts of 255 ON 1111 1111_B 100% ON

PWM1_DUTY_CTRL_3

PWM Channel 3 Duty Cycle Configuration (Address =0x15) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH3							
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
PWM_DUTY_CH3	D7:D0	r/w	PWM Channel 3 Duty Cycle configuration 0000 0000_B 100% OFF xxxx $xxxx_B$ parts of 255 ON 1111 1111_B 100% ON

PWM1_DUTY_CTRL_4

PWM Channel 4 Duty Cycle Configuration (Address =0x16) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH4							
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
PWM_DUTY_CH4	D7:D0	r/w	PWM Channel 4 Duty Cycle configuration 0000 0000_B 100% OFF xxxx $xxxx_B$ parts of 255 ON 1111 1111_B 100% ON

SR _CTRL_1

The Slew Rate Configuration 1 (Address =0x17) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_SR	HB7_SR	HB6_SR	HB5_SR	HB4_SR	HB3_SR	HB2_SR	HB1_SR
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
HB8_SR	D7	r/w	HB8 slew rate configuration 0_B 1V/μs 1_B 3.7V/μs
HB7_SR	D6	r/w	HB7 slew rate configuration 0_B 1V/μs 1_B 3.7V/μs
HB6_SR	D5	r/w	HB6 slew rate configuration 0_B 1V/μs 1_B 3.7V/μs
HB5_SR	D4	r/w	HB5 slew rate configuration 0_B 1V/μs 1_B 3.7V/μs
HB4_SR	D3	r/w	HB4 slew rate configuration 0_B 1V/μs 1_B 3.7V/μs
HB3_SR	D2	r/w	HB3 slew rate configuration 0_B 1V/μs 1_B 3.7V/μs
HB2_SR	D1	r/w	HB2 slew rate configuration 0_B 1V/μs 1_B 3.7V/μs
HB1_SR	D0	r/w	HB1 slew rate configuration 0_B 1V/μs 1_B 3.7V/μs

SR _CTRL_2

The Slew Rate Configuration 2 (Address =0x18) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_SR	HB7_SR	HB6_SR	HB5_SR	HB4_SR	HB3_SR	HB2_SR	HB1_SR
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
Reserved	D7	r/w	Reserved. Always reads as ‘0’
Reserved	D6	r/w	Reserved. Always reads as ‘0’
Reserved	D5	r/w	Reserved. Always reads as ‘0’
Reserved	D4	r/w	Reserved. Always reads as ‘0’
HB12_SR	D3	r/w	HB12 slew rate configuration 0_B 1V/μs 1_B 3.7V/μs
HB11_SR	D2	r/w	HB11 slew rate configuration 0_B 1V/μs 1_B 3.7V/μs
HB10_SR	D1	r/w	HB10 slew rate configuration 0_B 1V/μs 1_B 3.7V/μs
HB9_SR	D0	r/w	HB9 slew rate configuration 0_B 1V/μs 1_B 3.7V/μs

OLD _CTRL_1

The Open Load Detect Control 1 (Address =0x19) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_OLD_DIS	HB7_OLD_DIS	HB6_OLD_DIS	HB5_OLD_DIS	HB4_OLD_DIS	HB3_OLD_DIS	HB2_OLD_DIS	HB1_OLD_DIS
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
HB8_OLD_DIS	D7	r/w	HB8 open load detect configuration 0_B Open-load detection on half-bridge 8 is enable 1_B Open-load detection on half-bridge 8 is disable
HB7_OLD_DIS	D6	r/w	HB7 open load detect configuration 0_B Open-load detection on half-bridge 7 is enable 1_B Open-load detection on half-bridge 7 is disable
HB6_OLD_DIS	D5	r/w	HB6 open load detect configuration 0_B Open-load detection on half-bridge 6 is enable 1_B Open-load detection on half-bridge 6 is disable
HB5_OLD_DIS	D4	r/w	HB5 open load detect configuration 0_B Open-load detection on half-bridge 5 is enable 1_B Open-load detection on half-bridge 5 is disable
HB4_OLD_DIS	D3	r/w	HB4 open load detect configuration 0_B Open-load detection on half-bridge 4 is enable 1_B Open-load detection on half-bridge 4 is disable
HB3_OLD_DIS	D2	r/w	HB3 open load detect configuration 0_B Open-load detection on half-bridge 3 is enable 1_B Open-load detection on half-bridge 3 is disable
HB2_OLD_DIS	D1	r/w	HB2 open load detect configuration 0_B Open-load detection on half-bridge 2 is enable 1_B Open-load detection on half-bridge 2 is disable
HB1_OLD_DIS	D0	r/w	HB1 open load detect configuration 0_B Open-load detection on half-bridge 1 is enable 1_B Open-load detection on half-bridge 1 is disable

OLD _CTRL_2

The Open Load Detect Control 2 (Address =0x1A) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
OLD_REP	OLD_OP	Reserved		HB12_OLD_DIS	HB11_OLD_DIS	HB10_OLD_DIS	HB9_OLD_DIS
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
OLD_REP	D7	r/w	0_B Report on nFAULT pin during OLD condition 1_B No report on nFAULT pin during OLD condition
OLD_OP	D6	r/w	0_B Half-bridge are not active after OLD condition detect 1_B Half-bridge are active after OLD condition detect
Reserved	D5	r/w	Reserved. Always reads as ‘0’
Reserved	D4	r/w	Reserved. Always reads as ‘0’
HB12_OLD_DIS	D3	r/w	HB12 open load detect configuration 0_B Open-load detection on half-bridge 12 is enable 1_B Open-load detection on half-bridge 12 is disable
HB11_OLD_DIS	D2	r/w	HB11 open load detect configuration 0_B Open-load detection on half-bridge 11 is enable 1_B Open-load detection on half-bridge 11 is disable
HB10_OLD_DIS	D1	r/w	HB10 open load detect configuration 0_B Open-load detection on half-bridge 10 is enable 1_B Open-load detection on half-bridge 10 is disable

HB9_OLD_DIS	D0	r/w	HB9 open load detect configuration 0_B Open-load detection on half-bridge 9 is enable 1_B Open-load detection on half-bridge 9 is disable

OLD _CTRL_3
The Open Load Detect Control 3 (Address =0x1B) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
OCP_DEG			Reserved	HB12_OLD_EN	HB11_OLD_EN	HB10_OLD_EN	HB9_OLD_EN
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
OCP_DEG	D7:D5	r/w	000_B OCP deglitch time is 10μs 001_B OCP deglitch time is 5μs 010_B OCP deglitch time is 2.5μs 011_B OCP deglitch time is 1μs 100_B OCP deglitch time is 60μs 101_B OCP deglitch time is 40μs 110_B OCP deglitch time is 30μs 111_B OCP deglitch time is 20μs
Reserved	D4	r/w	Reserved. Always reads as '0'
HB12_OLD_EN	D3	r/w	HB12 low-current OLD detect configuration 0_B Low-current OLD detection on half-bridge 12 is disable 1_B Low-current OLD detection on half-bridge 12 is enable
HB11_OLD_ EN	D2	r/w	HB11 low-current OLD detect configuration 0_B Low-current OLD detection on half-bridge 11 is disable 1_B Low-current OLD detection on half-bridge 11 is enable
HB10_OLD_ EN	D1	r/w	HB10 low-current OLD detect configuration 0_B Low-current OLD detection on half-bridge 10 is disable 1_B Low-current OLD detection on half-bridge 10 is enable
HB9_OLD_ EN	D0	r/w	HB9 low-current OLD detect configuration 0_B Low-current OLD detection on half-bridge 9 is disable 1_B Low-current OLD detection on half-bridge 9 is enable

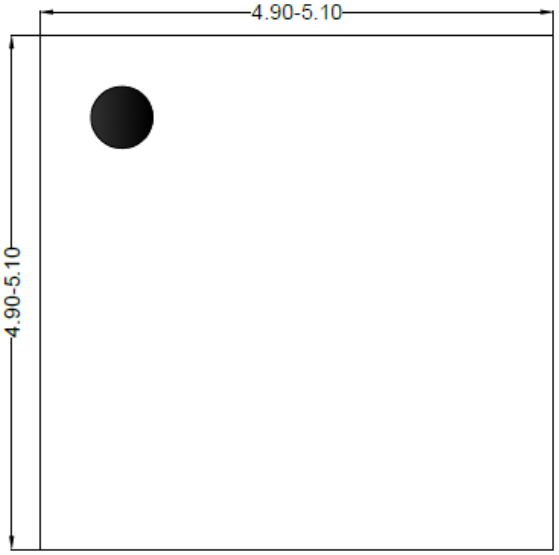
OLD _CTRL_4
The Open Load Detect Control 4 (Address =0x24) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_OLD_EN	HB7_OLD_EN	HB6_OLD_EN	HB5_OLD_EN	HB4_OLD_EN	HB3_OLD_EN	HB2_OLD_EN	HB1_OLD_EN
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

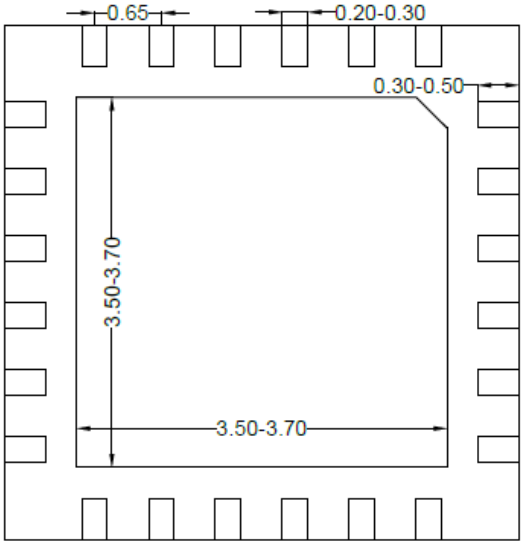
Field	Bits	Type	Description
HB8_OLD_ EN	D7	r/w	HB8 low-current OLD detect configuration 0_B Low-current OLD detection on half-bridge 8 is disable 1_B Low-current OLD detection on half-bridge 8 is enable
HB7_OLD_ EN	D6	r/w	HB7 low-current OLD detect configuration 0_B Low-current OLD detection on half-bridge 7 is disable 1_B Low-current OLD detection on half-bridge 7 is enable
HB6_OLD_EN	D5	r/w	HB6 low-current OLD detect configuration 0_B Low-current OLD detection on half-bridge 6 is disable 1_B Low-current OLD detection on half-bridge 6 is enable
HB5_OLD_ EN	D4	r/w	HB5 low-current OLD detect configuration 0_B Low-current OLD detection on half-bridge 5 is disable 1_B Low-current OLD detection on half-bridge 5 is enable
HB4_OLD_ EN	D3	r/w	HB4 low-current OLD detect configuration 0_B Low-current OLD detection on half-bridge 4 is disable 1_B Low-current OLD detection on half-bridge 4 is enable
HB3_OLD_ EN	D2	r/w	HB3 low-current OLD detect configuration 0_B Low-current OLD detection on half-bridge 3 is disable

			1_B Low-current OLD detection on half-bridge 3 is enable
HB2_OLD_ EN	D1	r/w	HB2 low-current OLD detect configuration 0_B Low-current OLD detection on half-bridge 2 is disable 1_B Low-current OLD detection on half-bridge 2 is enable
HB1_OLD_ EN	D0	r/w	HB1 low-current OLD detect configuration 0_B Low-current OLD detection on half-bridge 1 is disable 1_B Low-current OLD detection on half-bridge 1 is enable

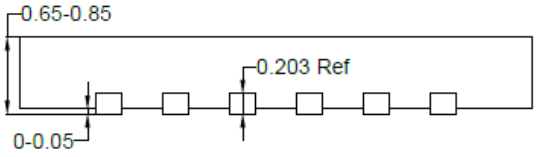
QFN5×5-24 Package Outline Drawing



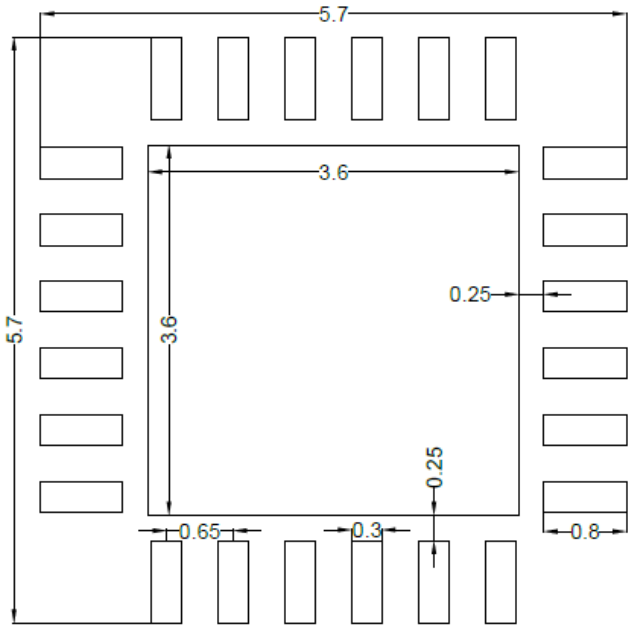
Top View



Bottom View



Front View



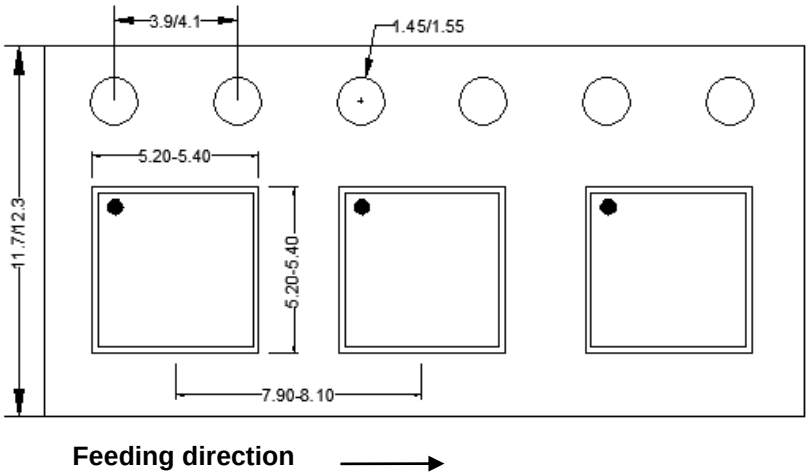
Recommended PCB Layout
(Reference Only)

Notes: All dimension in millimeter and exclude mold flash & metal burr

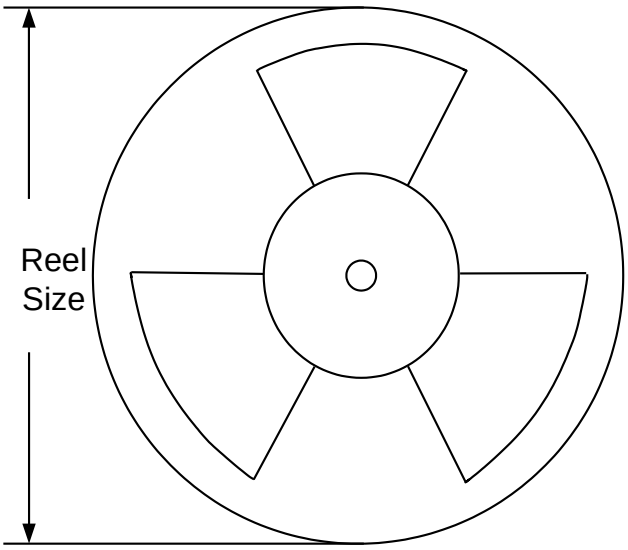
Taping & Reel Specification

1. Taping Orientation

QFN5×5



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN5×5	12	8	13"	400	400	5000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description
1.0	Nov 30, 2023	Initial Release

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