SA32B16 / SA32B14 / SA32B12

ARM® Cortex® M4F Automotive MCU with Functional Safety Features

1. General Description

The SA32B1x series MCUs are based on the popular ARM Cortex-M4F core, designed for high reliability and functional safety to meet the requirements of the automotive market. They comply with ISO26262 ASIL-B level functional safety requirements and meet AEC-Q100 G1 grade reliability standards. The SA32B1x series offers an optimal balance of performance and cost, making it ideal for automotive body, comfort, and telematics applications.

2. Features

- **CPU:**
  - ARM Cortex-M4F CPU
  - Max Frequency: 120MHz
  - Supports DSP, FPU, MPU, and NVIC
  - Supports JTAG and SWD Debug Interfaces
- **Memory:**
  - Code Flash: 512KB, 256KB, or 128KB
  - Dedicated Data Flash: 128KB
  - Fast Access to Code Flash
  - High Endurance Data Flash: Capable of 100K-Cycling, Supports FEE Emulation
  - System SRAM: 64KB
  - Instruction Cache: 8KB
- **System:**
  - On-Chip Boot ROM for FOTA Upgrade with UDS Protocol
  - Dual DMA Engines with 16 Channels for Efficient Paralleled Data Transmissions
  - Flexible Module Interconnection Matrix
  - SysTick and RTC Timer
- **Safety:**
  - Supports ISO26262 ASIL-B Level
  - Flash and SRAM with ECC Check
  - On-Chip Clock Monitor for Safety
  - On-Chip Power Monitor for Safety
  - On-Chip Temperature Monitor for Safety
  - 3xCRC for Safety and Data Integrity Check
  - Dual Watchdogs with Independent Clock Sources, Supports Windows Mode
- **Security:**
  - SSE Security Engine for Encryption and Decryption
  - Supports AES128, SHA256, TRNG, Secured Key Storage and Unique ID
  - Supports Secure Boot and MAC Authentication
  - Compliant with AUTOSAR SHE Standards
  - Meets EVITA Light HSM Requirements
- **Analog:**
  - Crystal Oscillator Frequency Range: From 8MHz to 40MHz
  - High Accuracy HIRC: On-Chip, 24MHz
  - Low Power LIRC: On-Chip, 131.072KHz
  - PLL: On-Chip for System Clock Generation
  - SAR ADC: Dual 16-Channel, 12-Bit, 1Msps, Optimized for Automotive Applications
  - Built-in 2.5V ADC Reference
  - Analog Comparators: Two Fast Comparators with Dedicated 8-Bit DAC for Reference
  - Built-in Temperature Monitor
- **Peripherals:**
  - 3x CAN Modules: Supports CAN 2.0 and FD
  - 4x UART/LIN Modules: Compliant with LIN2.2 and SAE J2602
  - 4x SPI Modules: Each with Four Chip Selects
  - 2x I^2C Modules: Supports SMBUS and 4-Wire Modes
  - 1x SENT Module: Features Two SENT Channels
  - 4x 16-Bit Advanced PWM Timers: Each PWM Supports up to eight channels; Supports complementary outputs with programmable dead-time; Supports Input capture and output compare with Edge and Center-Aligned Mode
  - 2x 32-Bit Flexible Trigger Timers (TRGT): Each with Four Channels
  - 2x 16-Bit General Purpose Timer (GPT)
- **Others:**
  - AEC-Q100 G1 Grade (T_A：-40 to 125°C)
  - Packages Available: LQFP100, LQFP64, LQFP48, and QFN32

3. Applications

- Automotive Body and Comfort (BCM, HVAC, Seats, Doors, Roof, Lights, etc.)
- Electric Vehicle Applications (OBC, BMS, PDU, PTC Heaters, Heat Management Systems, etc.)
- Automotive Telematics (T-Box, UWB, etc.)
- Automotive Safety (Airbag, Seatbelt, EPB, etc.)
- Industrial Applications

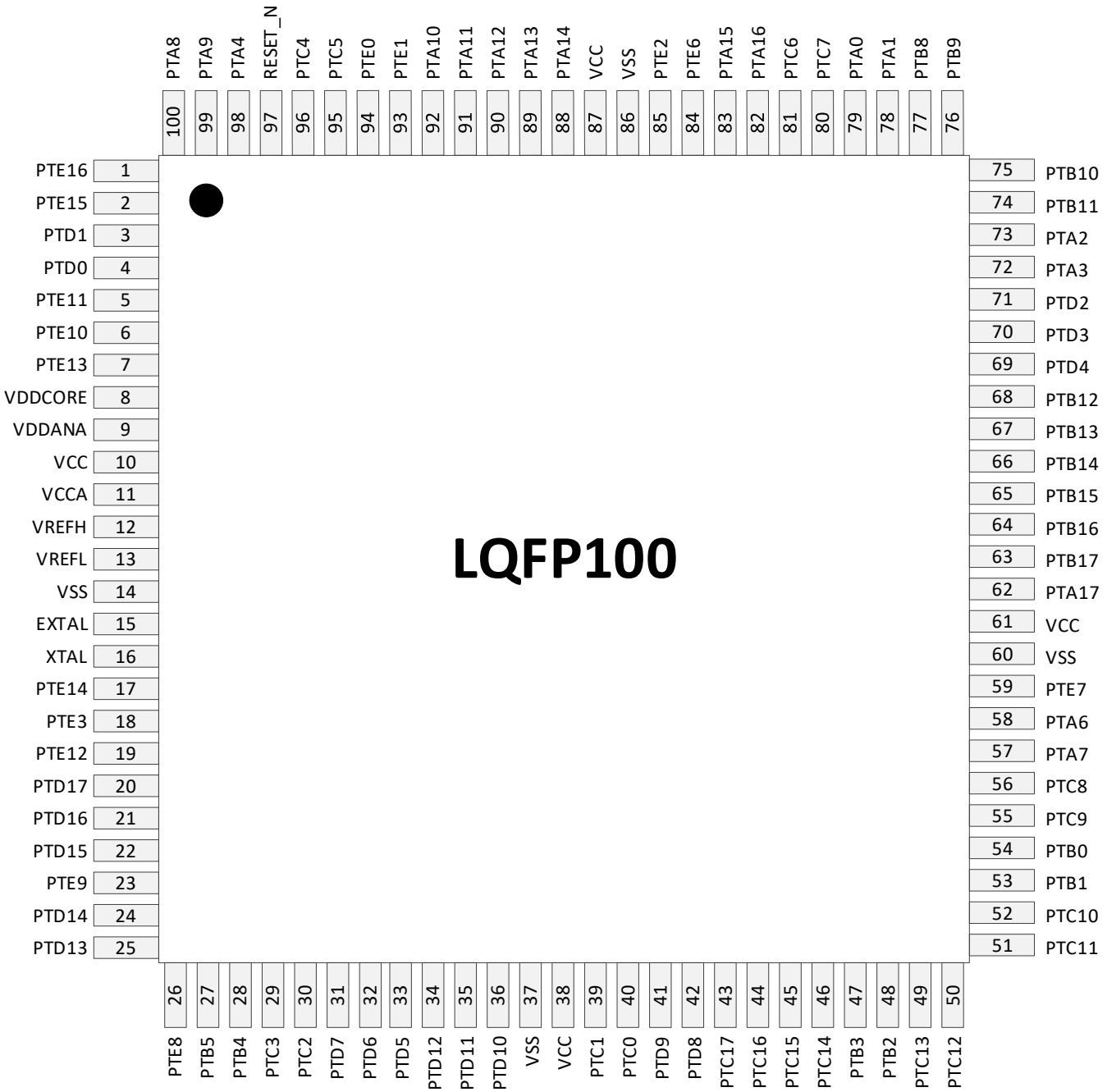
4. Ordering Information

Part Number	CPU Freq (MHz)	Code Flash (KB)	Data Flash (KB)	SRAM (KB)	Package	Carrier Type	MOQ	Top Mark
SA32B16GEF	120	512	128	64	LQFP14×14-100	Tape and Reel	1000	FNGxyz
SA32B16GEF-T	120	512	128	64	LQFP14×14-100	Tray	360	FNGxyz
SA32B16GDF	120	512	128	64	LQFP10×10-64	Tape and Reel	1500	FNHxyz
SA32B16GDF-T	120	512	128	64	LQFP10×10-64	Tray	640	FNHxyz
SA32B16GFF	120	512	128	64	LQFP7×7-48	Tape and Reel	2000	HCDxyz
SA32B16GFF-T	120	512	128	64	LQFP7×7-48	Tray	1000	HCDxyz
SA32B14GDF	120	256	128	64	LQFP10×10-64	Tape and Reel	1500	FRKxyz
SA32B14GDF-T	120	256	128	64	LQFP10×10-64	Tray	640	FRKxyz
SA32B14GFF	120	256	128	64	LQFP7×7-48	Tape and Reel	2000	FRYxyz
SA32B14GFF-T	120	256	128	64	LQFP7×7-48	Tray	1000	FRYxyz
SA32B12GFF	120	128	128	64	LQFP7×7-48	Tape and Reel	2000	FTBxyz
SA32B12GFF-T	120	128	128	64	LQFP7×7-48	Tray	1000	FTBxyz
SA32B12QEQ	120	128	128	64	QFN5×5-32	Tape and Reel	5000	HCCxyz
SA32B12QEQ-T	120	128	128	64	QFN5×5-32	Tray	1960	HCCxyz
SA32B12AQEQ	120	128	128	64	QFN5×5-32	Tape and Reel	5000	HKDxyz
SA32B12AQEQ-T	120	128	128	64	QFN5×5-32	Tray	1960	HKDxyz

Device codes: FNG, FNH, HCD, FRK, FRY, FTB, HCC, HKD
x=year code, y=week code, z= lot number code
* Future product, Specifications subject to change.

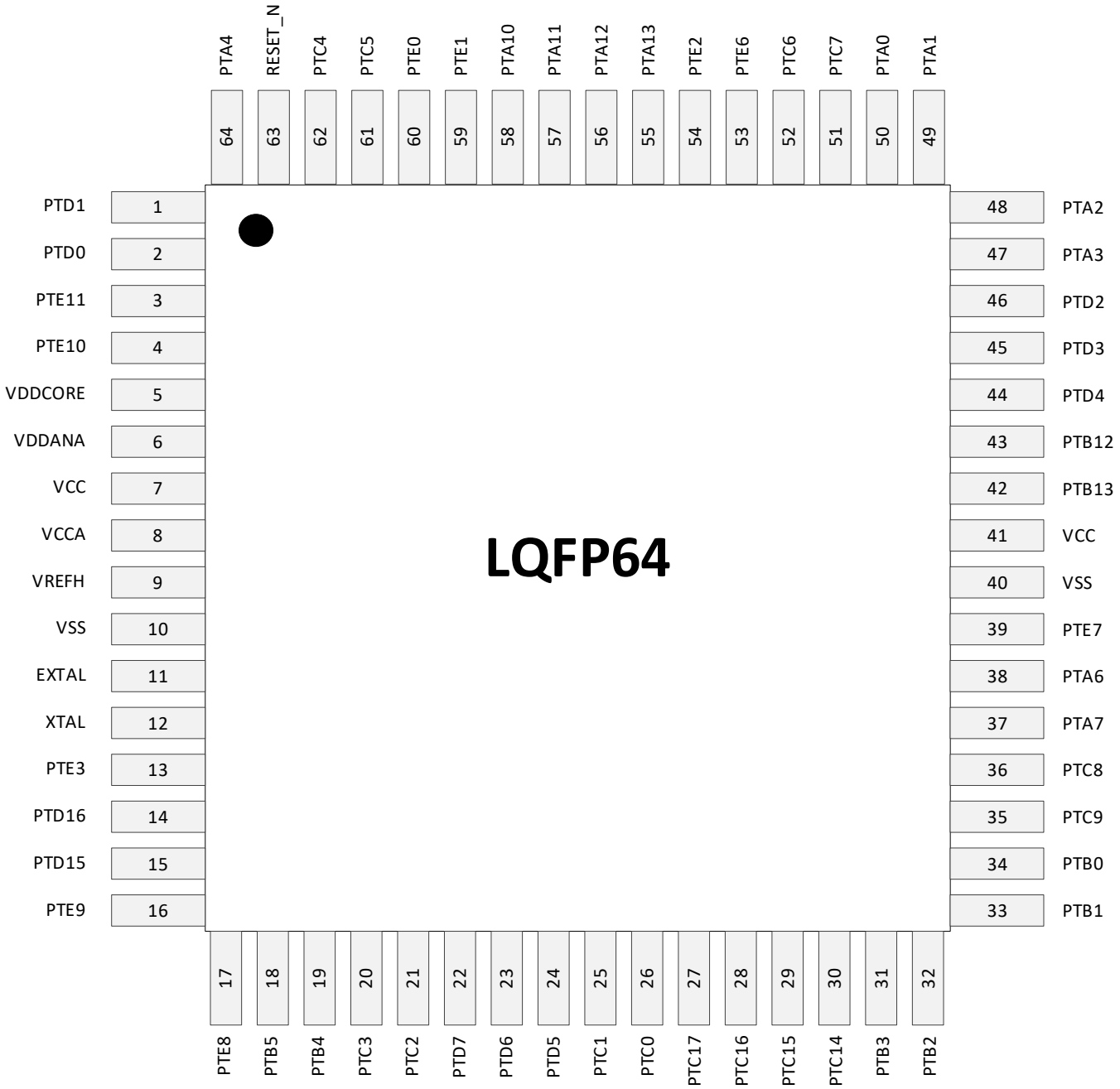
5. Packages

5.1 100-Pin LQFP (14 x 14 x 1.4 mm, Pitch 0.5mm)



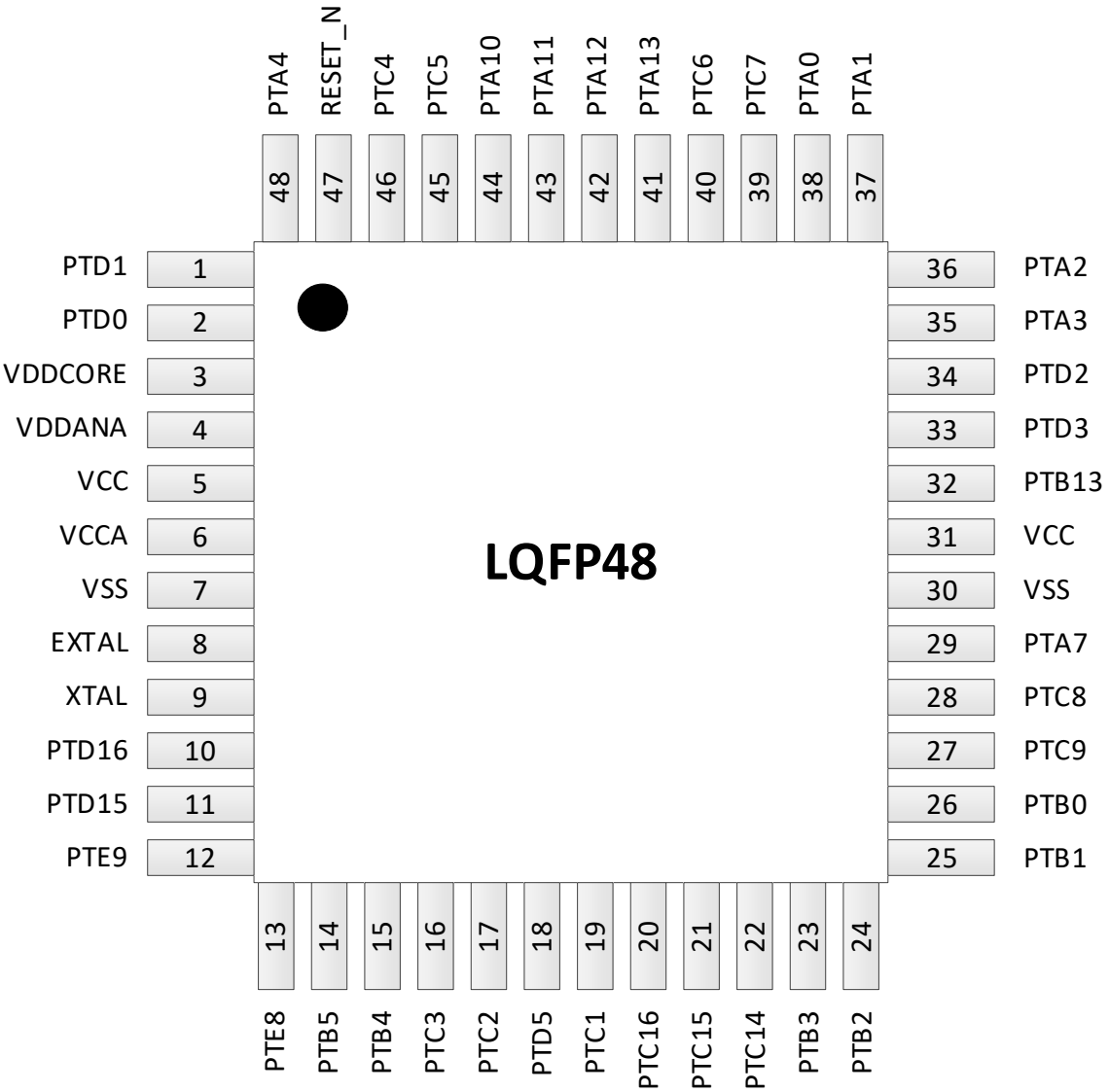
(LQFP14×14-100)

5.2 64-pin LQFP (10 x 10 x 1.4 mm, Pitch 0.5mm)



(LQFP10×10-64)

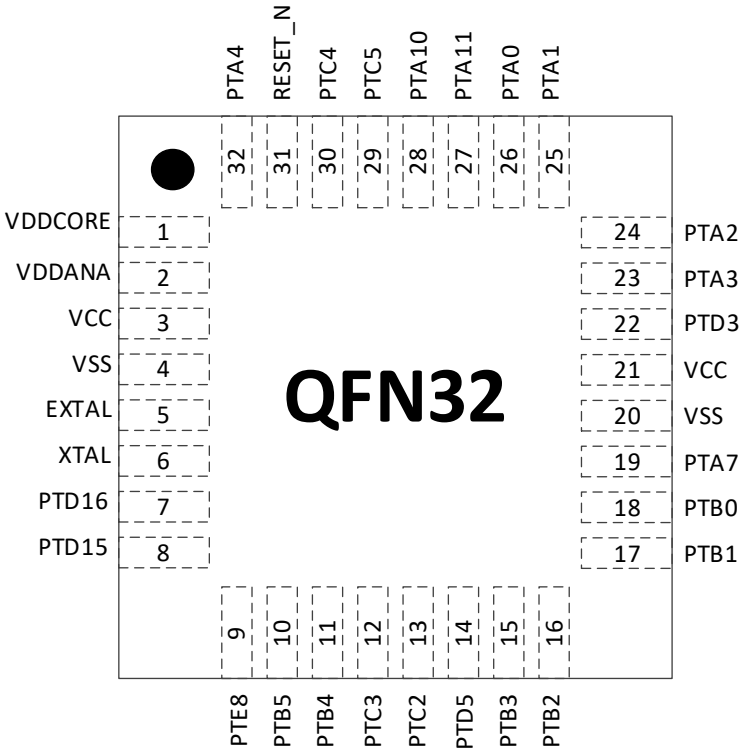
5.3 48-pin LQFP (7 x 7 x 1.4 mm, Pitch 0.5mm)



(LQFP7×7-48)

5.4 32-pin QFN (5 x 5 x 0.85 mm, Pitch 0.5mm)

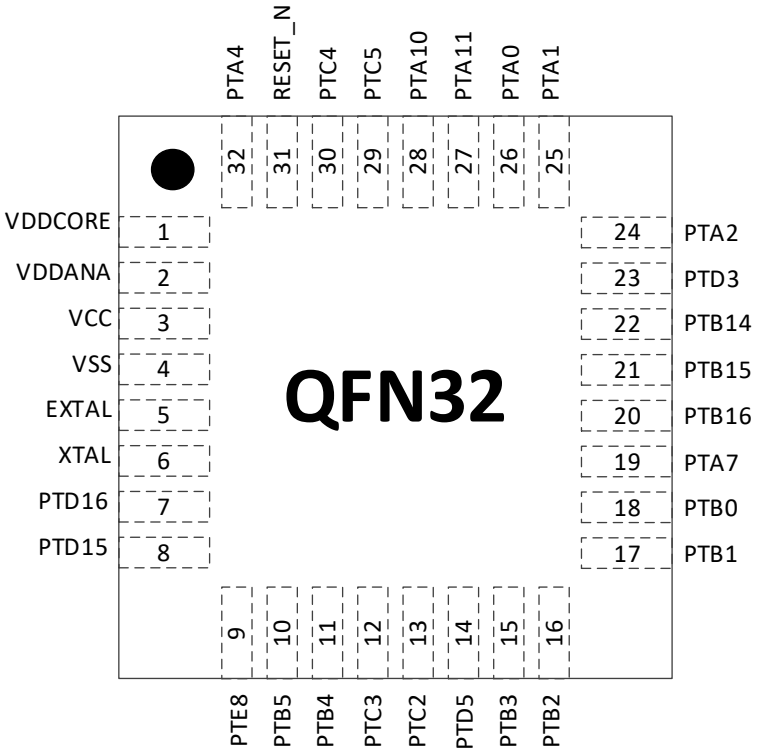
SA32B12QEQ



(QFN5×5-32)

5.5 32-pin QFN (5 x 5 x 0.85 mm, Pitch 0.5mm)

SA32B12AQEQ



(QFN5×5-32)

6. Pin Description

LQFP 100	LQFP 64	LQFP 48	QFN 32	QFN 32_A	Pin_Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1					PTE16	DISABLED		PTE16	UART1_RTS	SPI2_SDI	PWM2_CH7	UART3_TX		TRGMUX_OUT2
2					PTE15	DISABLED		PTE15	UART1_CTS	SPI2_SCK	PWM2_CH6	UART3_RX		TRGMUX_OUT3
3	1	1			PTD1	DISABLED		PTD1	PWM0_CH3	SPI1_SDI	PWM2_CH1	UART3_RTS		TRGMUX_OUT2
4	2	2			PTD0	DISABLED		PTD0	PWM0_CH2	SPI1_SCK	PWM2_CH0	UART3_CTS		TRGMUX_OUT1
5	3				PTE11	DISABLED		PTE11	SPI2_PCS0	GPT0_ALT1	PWM2_CH5	UART3_TX		TRGMUX_OUT0
6	4				PTE10	DISABLED		PTE10	CLKOUT	SPI2_PCS1	PWM2_CH4	UART3_RX		TRGMUX_OUT1
7					PTE13	DISABLED		PTE13		SPI2_PCS2	PWM2_FLT0			
8	5	3	1	1	VDDCORE	VDDCORE	VDDCORE							
9	6	4	2	2	VDDANA	VDDANA	VDDANA							
10	7	5	3	3	VCC	VCC	VCC							
11	8	6			VCCA	VCCA	VCCA							
12	9				VREFH	VREFH	VREFH							
13					VREFL	VREFL	VREFL							
14	10	7	4	4	VSS	VSS	VSS							
15	11	8	5	5	EXTAL	EXTAL	EXTAL	PTB7	I2C0_SCL					
16	12	9	6	6	XTAL	XTAL	XTAL	PTB6	I2C0_SDA					
17					PTE14	DISABLED		PTE14	PWM0_FLT1		PWM2_FLT1			
18	13				PTE3	DISABLED		PTE3	PWM0_FLT0	UART2_RTS	PWM2_FLT0		TRGMUX_IN2	CMP0_OUT
19					PTE12	DISABLED		PTE12	PWM0_FLT3	UART2_TX		SPI3_SDO		
20					PTD17	DISABLED		PTD17	PWM0_FLT2	UART2_RX		SPI3_SDI		
21	14	10	7	7	PTD16	DISABLED		PTD16	PWM0_CH1		SPI0_SDI	CMP0_RRT		
22	15	11	8	8	PTD15	DISABLED		PTD15	PWM0_CH0		SPI0_SCK			
23	16	12			PTE9	DISABLED		PTE9	PWM0_CH7	UART2_CTS		SPI3_SCK		
24					PTD14	DISABLED		PTD14	PWM2_CH5	UART1_TX		SPI3_PCS3		CLKOUT
25					PTD13	DISABLED		PTD13	PWM2_CH4	UART1_RX				RTC_CLKOUT
26	17	13	9	9	PTE8	CMP0_IN3	CMP0_IN3	PTE8	PWM0_CH6	GPT1_ALT1				
27	18	14	10	10	PTB5	DISABLED		PTB5	PWM0_CH5	SPI0_PCS1	SENT0_RX0	CLKOUT	TRGMUX_IN0	CMP1_OUT
28	19	15	11	11	PTB4	CMP1_IN0	CMP1_IN0	PTB4	PWM0_CH4	SPI0_SDO	SENT0_RX1		TRGMUX_IN1	
29	20	16	12	12	PTC3	ADC0_SE11/CMP0_IN4 /CMP1_IN4	ADC0_SE11/CMP0_IN4/ CMP1_IN4	PTC3	PWM0_CH3	CAN0_TX	UART0_TX			
30	21	17	13	13	PTC2	ADC0_SE10/CMP0_IN5 /CMP1_IN5	ADC0_SE10/CMP0_IN5/ CMP1_IN5	PTC2	PWM0_CH2	CAN0_RX	UART0_RX			
31	22				PTD7	CMP0_IN6/CMP1_IN6	CMP0_IN6/CMP1_IN6	PTD7	UART2_TX		PWM2_FLT3			
32	23				PTD6	CMP0_IN7/CMP1_IN7	CMP0_IN7/CMP1_IN7	PTD6	UART2_RX		PWM2_FLT2			
33	24	18	14	14	PTD5	DISABLED		PTD5	PWM2_CH3	GPT0_ALT2	PWM2_FLT1	I2C1_SCL	TRGMUX_IN3	
34					PTD12	DISABLED		PTD12	PWM2_CH2	I2C1_HREQ		SPI3_PCS0	UART2_RTS	
35					PTD11	DISABLED		PTD11	PWM2_CH1	PWM2_QD_PHA		SPI3_PCS1	UART2_CTS	
36					PTD10	DISABLED		PTD10	PWM2_CH0	PWM2_QD_PHB		SPI3_PCS2		
37					VSS	VSS	VSS							
38					VCC	VCC	VCC							
39	25	19			PTC1	CMP1_IN1	CMP1_IN1	PTC1	PWM0_CH1	SPI2_SDO		I2C1_SDA	PWM1_CH7	
40	26				PTC0	CMP1_IN2	CMP1_IN2	PTC0	PWM0_CH0	SPI2_SDI			PWM1_CH6	
41					PTD9	DISABLED		PTD9	I2C1_SCL		PWM2_FLT3		PWM1_CH5	
42					PTD8	DISABLED		PTD8	I2C1_SDA		PWM2_FLT2		PWM1_CH4	
43	27				PTC17	ADC0_SE15	ADC0_SE15	PTC17	PWM1_FLT3	CAN2_TX		I2C1_SCLS		
44	28	20			PTC16	ADC0_SE14	ADC0_SE14	PTC16	PWM1_FLT2	CAN2_RX	SPI2_SDI	I2C1_SDAS		
45	29	21			PTC15	ADC0_SE13	ADC0_SE13	PTC15	PWM1_CH3	SPI2_SCK			TRGMUX_IN3	
46	30	22			PTC14	ADC0_SE12	ADC0_SE12	PTC14	PWM1_CH2	SPI2_PCS0			TRGMUX_IN2	
47	31	23	15	15	PTB3	ADC0_SE7	ADC0_SE7	PTB3	PWM1_CH1	SPI0_SDI	PWM1_QD_PHA			
48	32	24	16	16	PTB2	ADC0_SE6	ADC0_SE6	PTB2	PWM1_CH0	SPI0_SCK	PWM1_QD_PHB			
49					PTC13	DISABLED		PTC13	PWM3_CH7	PWM2_CH7	UART2_RTS	UART3_RTS		
50					PTC12	DISABLED		PTC12	PWM3_CH6	PWM2_CH6	UART2_CTS	UART3_CTS		
51					PTC11	DISABLED		PTC11	PWM3_CH5			UART3_TX	TRGMUX_IN1	
52					PTC10	DISABLED		PTC10	PWM3_CH4			UART3_RX	TRGMUX_IN0	
53	33	25	17	17	PTB1	ADC0_SE5/ADC1_SE15	ADC0_SE5/ADC1_SE15	PTB1	UART0_TX	SPI0_SDO		CAN0_TX		
54	34	26	18	18	PTB0	ADC0_SE4/ADC1_SE14	ADC0_SE4/ADC1_SE14	PTB0	UART0_RX	SPI0_PCS0	GPT0_ALT3	CAN0_RX		
55	35	27			PTC9	DISABLED		PTC9	UART1_TX	PWM1_FLT1		CAN0_TX	UART0_RTS	
56	36	28			PTC8	DISABLED		PTC8	UART1_RX	PWM1_FLT0		CAN0_RX	UART0_CTS	
57	37	29	19	19	PTA7	ADC0_SE3	ADC0_SE3	PTA7	PWM0_FLT2		RTC_CLKIN		UART1_RTS	
58	38				PTA6	ADC0_SE2/CMP1_IN3	ADC0_SE2/CMP1_IN3	PTA6	PWM0_FLT1	SPI1_PCS1			UART1_CTS	
59	39				PTE7	DISABLED		PTE7	PWM0_CH7	PWM3_FLT0				
60	40	30	20		VSS	VSS	VSS							
61	41	31	21		VCC	VCC	VCC							
62					PTA17	DISABLED		PTA17	PWM0_CH6	PWM3_FLT0	EWDOG_OUT_b			
63					PTB17	DISABLED		PTB17	PWM0_CH5	SPI1_PCS3				
64				20	PTB16	DISABLED		PTB16	PWM0_CH4	SPI1_SDO				
65				21	PTB15	DISABLED		PTB15	PWM0_CH3	SPI1_SDI				
66				22	PTB14	ADC1_SE9/ADC0_SE9	ADC1_SE9/ADC0_SE9	PTB14	PWM0_CH2	SPI1_SCK				
67	42	32			PTB13	ADC1_SE8/ADC0_SE8	ADC1_SE8/ADC0_SE8	PTB13	PWM0_CH1	PWM3_FLT1	CAN2_TX			

68	43				PTB12	ADC1_SE7	ADC1_SE7	PTB12	PWM0_CH0	PWM3_FLT2	CAN2_RX				
69	44				PTD4	ADC1_SE6	ADC1_SE6	PTD4	PWM0_FLT3	PWM3_FLT3					
70	45	33	22	23	PTD3	ADC1_SE3	ADC1_SE3	PTD3	PWM3_CH5	SPI1_PCS0					NMI_b
71	46	34			PTD2	ADC1_SE2	ADC1_SE2	PTD2	PWM3_CH4	SPI1_SDO					
72	47	35	23		PTA3	ADC1_SE1	ADC1_SE1	PTA3	PWM3_CH1	I2C0_SCL	EWDOG_IN			UART0_TX	
73	48	36	24	24	PTA2	ADC1_SE0	ADC1_SE0	PTA2	PWM3_CH0	I2C0_SDA	EWDOG_OUT_b			UART0_RX	
74					PTB11	DISABLED		PTB11	PWM3_CH3	I2C0_HREQ	EWDOG_IN			SENT0_RX0	
75					PTB10	DISABLED		PTB10	PWM3_CH2	I2C0_SDAS				SENT0_RX1	
76					PTB9	DISABLED		PTB9	PWM3_CH1	I2C0_SCLS					
77					PTB8	DISABLED		PTB8	PWM3_CH0		EWDOG_OUT_b				
78	49	37	25	25	PTA1	ADC0_SE1/CMP0_IN1	ADC0_SE1/CMP0_IN1	PTA1	PWM1_CH1	I2C0_SDAS		PWM1_QD_PHA		UART0_RTS	TRGMUX_OUT0
79	50	38	26	26	PTA0	ADC0_SE0/CMP0_IN0	ADC0_SE0/CMP0_IN0	PTA0	PWM2_CH1	I2C0_SCLS		PWM2_QD_PHA		UART0_CTS	TRGMUX_OUT3
80	51	39			PTC7	ADC1_SE5	ADC1_SE5	PTC7	UART1_TX	CAN1_TX	PWM3_CH3			PWM1_QD_PHA	
81	52	40			PTC6	ADC1_SE4	ADC1_SE4	PTC6	UART1_RX	CAN1_RX	PWM3_CH2			PWM1_QD_PHB	
82					PTA16	ADC1_SE13	ADC1_SE13	PTA16	PWM1_CH3	SPI1_PCS2					
83					PTA15	ADC1_SE12	ADC1_SE12	PTA15	PWM1_CH2	SPI0_PCS3	SPI2_PCS3				
84	53				PTE6	ADC1_SE11	ADC1_SE11	PTE6	SPI0_PCS2	GPT1_ALT2	PWM3_CH7			UART1_RTS	
85	54				PTE2	ADC1_SE10	ADC1_SE10	PTE2	SPI0_SDO	GPT0_ALT3	PWM3_CH6			UART1_CTS	
86					VSS	VSS	VSS								
87					VCC	VCC	VCC								
88					PTA14	DISABLED		PTA14	PWM0_FLT0	PWM3_FLT1	EWDOG_IN			PWM1_FLT0	
89	55	41			PTA13	DISABLED		PTA13	PWM1_CH7	CAN1_TX	I2C1_SCLS			PWM2_QD_PHA	
90	56	42			PTA12	DISABLED		PTA12	PWM1_CH6	CAN1_RX	I2C1_SDAS			PWM2_QD_PHB	
91	57	43	27	27	PTA11	DISABLED		PTA11	PWM1_CH5	UART2_TX		CMP0_RRT			
92	58	44	28	28	PTA10	JTAG_TDO/TRACE_SWO		PTA10	PWM1_CH4	UART2_RX					JTAG_TDO/ TRACE_SWO
93	59				PTE1	DISABLED		PTE1	SPI0_SDI	I2C0_HREQ	I2C1_SCL	SPI1_PCS0		PWM1_FLT1	
94	60				PTE0	DISABLED		PTE0	SPI0_SCK	GPT1_ALT3	I2C1_SDA	SPI1_SDO		PWM1_FLT2	
95	61	45	29	29	PTC5	JTAG_TDI		PTC5	PWM2_CH0	RTC_CLKOUT	I2C1_HREQ	PBTN_RST_N		PWM2_QD_PHB	JTAG_TDI
96	62	46	30	30	PTC4	SWD_CLK	CMP0_IN2	PTC4	PWM1_CH0	RTC_CLKOUT		EWDOG_IN		PWM1_QD_PHB	JTAG_TCLK/ SWD_CLK
97	63	47	31	31	RESET_N	RESET_N		PTA5							RESET_N
98	64	48	32	32	PTA4	SWD_DIO		PTA4			CMP0_OUT	EWDOG_OUT_b			JTAG_TMS/ SWD_DIO
99					PTA9	DISABLED		PTA9	UART2_TX	SPI2_PCS0	PWM2_CH3	PWM3_FLT2		PWM1_FLT3	
100					PTA8	DISABLED		PTA8	UART2_RX	SPI2_SDO	PWM2_CH2	PWM3_FLT3			

Note: “DISABLED” refers to a high-impedance state

7. Block Diagram

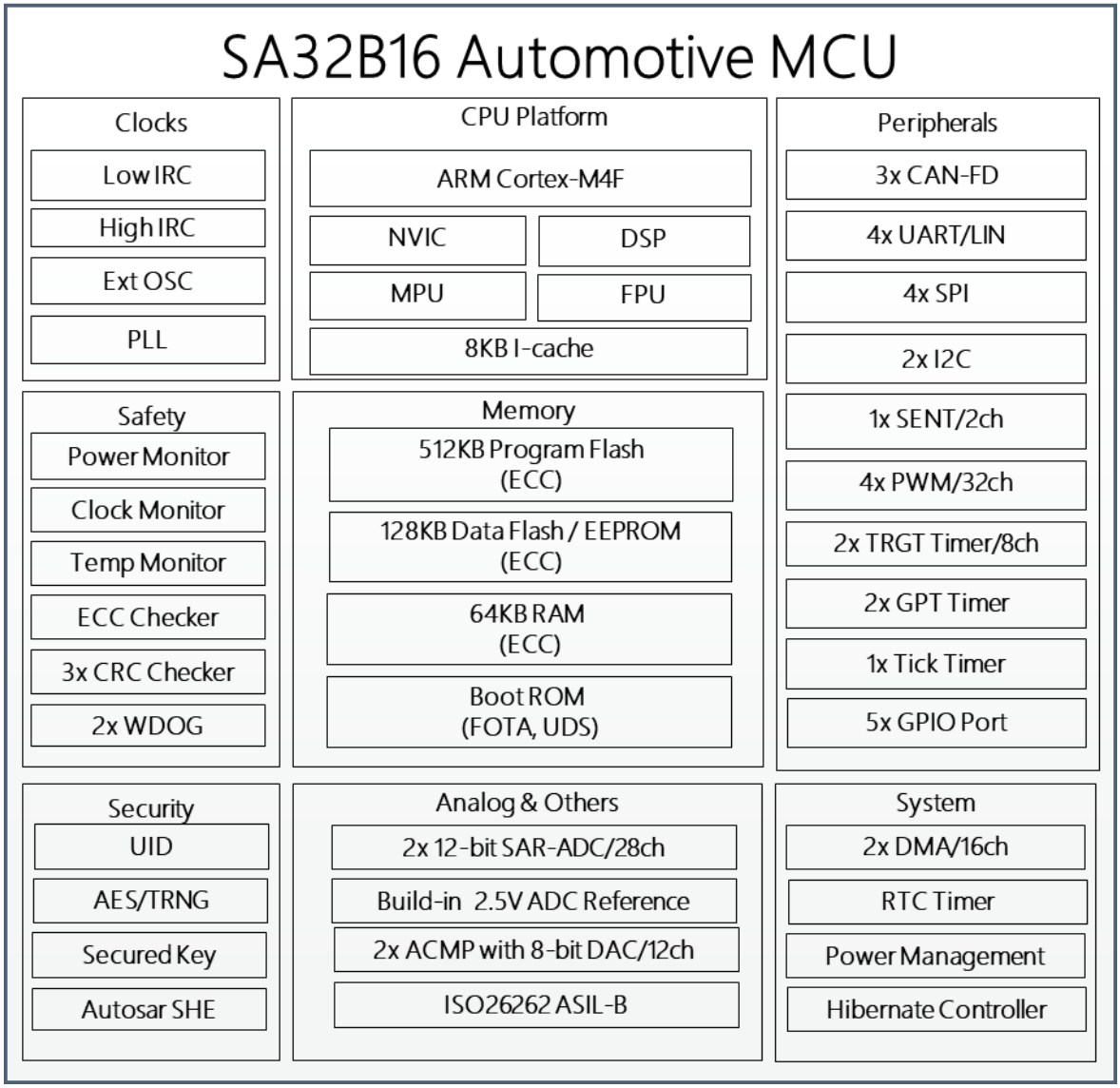


Figure 1. SA32B16 Block Diagram

8. Absolute Maximum Ratings

Parameter (Note 1)		Min	Max	Unit
VCC, VCCA		-0.3	6	V
PTA_X, PTB_X, PTC_X, PTD_X, PTE_X, EXTAL, XTAL		GND-0.3	V_{VCC}	V
VDDCORE		GND-0.3	1.32	
VDDANA		GND-0.3	2.75	
VSS, VREFL		GND-0.3	GND+0.3	
VREFH (Note 2)		2.8	V_{VCCA}	
Maximum Input Current on All Pins		-	30	mA
Latch-up		-	±250	
Ambient Temperature Range		-40	125	°C
Storage Temperature T_J Range		-55	165	
V_{ESD} Electrostatic Discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001	±4000		V
	Charged-device model (CDM), per JEDEC JESD22-C101	±750		V
MCU Supply Ramp Rate		0.5 V/min	500 V/ms	-

9. Thermal Information

Parameter (Note 3)	Package				Unit
	LQFP100	LQFP64	LQFP48	QFN32	
Power Dissipation, PD at T_A = 125°C	0.387	0.325	0.286	1.121	W
θ_{JA} Junction-to-Ambient Thermal Resistance	64.5	77	87.47	22.3	°C/W
θ_{JC} Junction-to-Case (Top) Thermal Resistance	10.3	10.9	11.8	14.8	
θ_{JB} Junction-to-board Thermal Resistance	33.1	33.9	37.8	8.4	

10. Recommended Operating Conditions

Parameter (Note 4)	Min	Max	Unit
VCC, VCCA Supply Voltage	2.8	5.5	V
Digital Input	0	V_{VCC}	V
Analog Input	0	V_{VCC}	V
Junction Temperature	-40	150	°C
Ambient Temperature	-40	125	°C

11. Electrical Characteristics

VCC = VCCA = 5V, T_J = -40ºC to 125ºC, typical values are at T_J = 25ºC, unless otherwise specified (Note 5)

11.1 Power and Operation Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power and Operation Conditions						
VCC Supply Voltage Range	V_{VCC}, V_{VCCA}	-	2.8	-	5.5	V
VDDCORE Supply Voltage Range	$V_{VDDCORE}$	-	1.08	1.2	1.32	V
Ground Voltage Range	V_{VSS}, V_{VSSA}	-	-0.1	-	0.1	V
Supply Voltage POR Threshold	V_{POR}	VCC	2.4	2.55	2.8	V
		VDDCORE	-	1.1	-	V
Supply Voltage LVR Threshold (Note 7)	V_{LVR}	VCC	2.38	2.5	2.52	V
		VDDCORE	-	1.05	-	V
Supply Voltage LVD Threshold (Note 7)	V_{CC_LVD}	VCC=3.3V	2.6	2.7	2.75	V
		VCC=5V	3.8	4.0	4.1	V
Supply Voltage LVW Threshold	V_{CC_LVW}	VCC=5V	4.3	4.5	4.6	V
POR, LVR, LVD, LVW Hysteresis	$V_{CC\_UVLO\_HYS}$	-	-	50	-	mV
Default Idle Current	I_{IDLE}	POR IDLE current without running code	2.0	4	8.5	mA
Run Mode Current	I_{RUN}	All peripheral clock disabled with system clock = 120MHz	-	30	-	mA
Deepsleep Mode (Note 7)	$I_{DSLEEP0}$	Chip enters Stop mode with all optional modules on	-	10	-	mA
	$I_{DSLEEP1}$	Chip enters Stop mode with all optional modules off	-	700	-	µA
Hibernation Mode Current	I_{DHIB}	Chip enters Hibernation mode	-	50	150	µA

11.2 I/O Specs 5V Power Supply Mode

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Supply Voltage Range	V_{VCC}	-		4	5.0	5.5	V
Input High Voltage	V_{IH}	-		V_{VCC} x 0.7	-	-	V
Input Low Voltage	V_{IL}	-		-	-	V_{VCC} x 0.3	V
Schmitt Triger Hysteresis	V_{HYS}	-		V_{VCC} x 0.06	-	-	V
Output High Voltage for Normal Mode	V_{OH_NORMAL}	1mA current		V_{VCC}– 0.5	-	-	V
		3mA current		V_{VCC}– 1.0	-		V
Output Low Voltage for Normal Mode	V_{OL_NORMAL}	1mA current		-	-	0.5	V
		3mA current		-	-	1	V
Output High Voltage for Fast Mode	V_{OH_FAST}	5mA current		V_{VCC}– 0.5	-	-	V
		10mA current		V_{VCC}– 1.0	-	-	V
Output Low Voltage for Fast Mode	V_{OL_FAST}	5mA current		-	-	0.5	V
		10mA current		-	-	1	V
Pull up Resistance	R_{PU}	-		20	-	40	kΩ
Pull down Resistance	R_{PD}	-		20	-	40	kΩ
Rise Time (Note 8)	t_{RISE_TIME}	Driving strength = Normal mode	C_{LOAD} = 25pF	-	4.96	-	ns
			C_{LOAD} = 50pF	-	6.04	-	ns
			C_{LOAD} = 200pF	-	36.7	-	ns
		Driving strength = Fast mode	C_{LOAD} = 25pF	-	2.96	-	ns
			C_{LOAD} = 50pF	-	3.28	-	ns

			C_{LOAD} = 200pF	-	7.56	-	ns
Fall Time (Note 8)	t_{FALL_TIME}	Driving strength = Normal mode	C_{LOAD} = 25pF	-	4.68	-	ns
			C_{LOAD} = 50pF	-	5.84	-	ns
			C_{LOAD} = 200pF	-	30.6	-	ns
		Driving strength = Fast mode	C_{LOAD} = 25pF	-	2.68	-	ns
			C_{LOAD} = 50pF	-	2.96	-	ns
			C_{LOAD} = 200pF	-	12.64	-	ns

11.3 I/O Specs 3.3V Power Supply Mode

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Supply Voltage Range	V_{VCC}	-		2.8	3.3	4	V
Input High Voltage	V_{IH}	-		V_{VCC} x 0.7	-	-	V
Input Low Voltage	V_{IL}	-		-	-	V_{VCC} x 0.3	V
Schmitt Triger Hysteresis	V_{HYS}	-		V_{VCC}x0.06	-	-	V
Output High Voltage for Normal Mode	V_{OH_NORMAL}	1mA current		V_{VCC} - 0.5	-	-	V
		3mA current		V_{VCC} - 1.0	-	-	V
Output Low Voltage for Normal Mode	V_{OL_NORMAL}	1mA current		-	-	0.5	V
		3mA current		-	-	1	V
Output High Voltage for Fast mode	V_{OH_FAST}	5mA current		V_{VCC} - 0.5	-	-	V
		10mA current		V_{VCC} -1.0	-	-	V
Output Low Voltage for Fast Mode	V_{OL_FAST}	5mA current		-	-	0.5	V
		10mA current		-	-	1	V
Pull Up Resistance	R_{PU}	-		25	-	45	kΩ
Pull Down Resistance	R_{PD}	-		25	-	45	kΩ
Rise Time (Note 8)	t_{RISE_TIME}	Driving strength = Normal mode	C_{LOAD} = 25pF	-	6.34	-	ns
			C_{LOAD} = 50pF	-	20.2	-	ns
			C_{LOAD} = 200pF	-	67.2	-	ns
		Driving strength = Fast mode	C_{LOAD} = 25pF	-	5.54	-	ns
			C_{LOAD} = 50pF	-	7.66	-	ns
			C_{LOAD} = 200pF	-	36	-	ns
Fall Time (Note 8)	t_{FALL_TIME}	Driving strength = Normal mode	C_{LOAD} = 25pF	-	3.52	-	ns
			C_{LOAD} = 50pF	-	3.92	-	ns
			C_{LOAD} = 200pF	-	10.4	-	ns
		Driving strength = Fast mode	C_{LOAD} = 25pF	-	3.2	-	ns
			C_{LOAD} = 50pF	-	3.5	-	ns
			C_{LOAD} = 200pF	-	8.2	-	ns

11.4 Clock Specs

Parameter (Note 6)	Symbol	Test Conditions	Min	Typ	Max	Unit
Oscillator Specification (OSC)						
OSC Crystal or Resonator Frequency	f_{OSC}	-	8	24	40	MHz
OSC Startup Time	-	-	-	2	-	ms
OSC Loading Capacitor	-	-	-	8	-	pF
OSC Power Consumption	-	With full voltage and frequency range	-	-	2	mA
High Frequency RC Oscillator (HIRC)						
HIRC Frequency	f_{HIRC}	-	-	24	-	MHz
HIRC Frequency Drift	-	T_J =-40°C to 125°C	-3	-	3	%
HIRC Startup Time	-	-	-	-	5	μs
HIRC Power Consumption	-	With full voltage range	-	-	<150	μA
Low Frequency RC Oscillator (LIRC)						
LIRC Frequency	f_{LIRC}	-	-	131.072	-	kHz

LIRC Frequency Drift	-	T_J =-40°C to 125°C	-6	-	6	%
LIRC Startup Time	-	-	-	-	20	µs
LIRC Power Consumption	-	With full voltage range	-	-	<50	µA
PLL Specification						
PLL Reference Clock Frequency	-	-	8	-	40	MHz
VCO Output Frequency	-	-	144	240	400	MHz
PLL Output Frequency	-	-	80	120	180	MHz
PLL Period Jitter (Note 6)	-	-	-	120	-	ps
PLL Accumulated Jitter over 1us(Note 6)	-	-	-	1000	-	ps

11.5 Flash Memory Specs

Parameter	Symbol	Test Conditions	Min	Typ.	Max	Unit
Flash Memory Specs						
Program Time (72bits) (Note 6)	-	-	-	9	-	µs
Sector Erase Time (512 X 72bits) (Note 6)	-	-	-	3.6	-	ms
Read Time (72bits) (Note 6)	-	-	-	50	-	ns
Chip Erase Time (512KB) (Note 6)	-	-	-	18	-	ms

11.6 ADC Specs

Parameter	Symbol	Test Conditions	Min	Typ.	Max	Unit
ADC Specs with 12-bit Mode						
Adc Resolution	-	-	-	12	-	bit
ADC Input Voltage	-	-	V_{VSS}	-	V_{VCCA}	V
ADC Conversion Frequency	-	-	-	-	1	Msps
ADC sampling capacitance	C_{IN}	-	-	5.6	-	pF
ADC sampling switch resistance	R_{IN}	-	-	463	-	Ω
Total Overall Error	TOE	V_{VCC}=V_{VCCA}=5V; V_{REFH}=5V	-	±4	-	LSB
Differential Non-Linearity	DNL	V_{VCC}=V_{VCCA}=5V; V_{REFH}=5V	-	±1	-	LSB
Integral Non-Linearity	INL	V_{VCC}=V_{VCCA}=5V; V_{REFH}=5V	-	±2	-	LSB
Build-in 2.5V ADC Reference	-	T_J =-40°C to 125°C	-3	-	3	%

11.7 CMP Specs

Parameter (Note 7)	Symbol	Test Conditions	Min	Typ	Max	Unit
Analog Comparator (CMP) Specs with 8-bit DAC						
CMP Input Voltage Range	V_{CMP_IN}	-	V_{VSS}	-	V_{VCCA}	V
CMP Input Overall Offset	V_{OFFSET}	DAC with VCCA reference,	-10	±1	15	mV
		DAC with V2P5 reference,	-30	±4	30	mV
CMP Hysteresis	V_{HYS0}	T_J= 25°C, V_{HYS} = 25mV	10	25	35	mV
	V_{HYS1}	T_J= 25°C, V_{HYS} = 50mV	30	50	60	mV
	V_{HYS2}	T_J= 25°C, V_{HYS} = 200mV	170	200	240	mV
CMP Propagation Delay	t_{PD}	-	10	50	70	nS
CMP Power Consumption	I_{CMP}	-	-	-	200	µA
8-bit DAC Reference Voltage	V_{DAC}	V_{VCCA}	-	V_{VCCA}	-	V
		V2P5	-	V2P5	-	V
8-bit DAC INL	INL_{DAC}	-	-0.75	-	0.75	LSB
8-bit DAC DNL	DNL_{DAC}	-	-0.5	-	0.5	LSB
8-bit DAC Initialization and Switching Setting Time	t_{DDAC}	-	-	-	30	µs

11.8 I²C Specs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
I²C Interface-100kHz						
Clock Operation Frequency	f_{SCL}	SCL Duty=50%	-	-	100	kHz
START Condition Hold Time	$t_{HD:STA}$	-	4.0	-	-	μs
Low Period of the SCL Clock	t_{LOW}	-	4.7	-	-	μs
High Period of the SCL Clock	t_{HIGH}	-	4.0	-	-	μs
SETUP Condition Hold Time	$t_{SU:STA}$	-	4.7	-	-	μs
DATA Hold Time (SDA Input)	$t_{HD:DAT}$	-	0	-	-	ns
DATA Setup Time (SDA Input)	$t_{SU:DAT}$	-	250	-	-	ns
Clock Rise Time	t_r	30%-70%	-	-	1000	ns
Clock Fall Time	t_f	70%-30%	-	-	300	ns
Setup Time STOP Condition	$t_{SU:STO}$	-	4.0	-	-	μs
BUS Free Time Stop to Start	t_{BUF}	-	4.7	-	-	μs
I²C Interface-400kHz						
Clock Operation Frequency	f_{SCL}	SCL Duty=50%	-	-	400	kHz
START Condition Hold Time	$t_{HD:STA}$	-	0.6	-	-	μs
Low Period of the SCL Clock	t_{LOW}	-	1.3	-	-	μs
High Period of the SCL Clock	t_{HIGH}	-	600	-	-	ns
SETUP Condition Hold Time	$t_{SU:STA}$	-	600	-	-	ns
DATA Hold Time (SDA Input)	$t_{HD:DAT}$	-	0	-	-	ns
DATA Setup Time (SDA Input)	$t_{SU:DAT}$	-	100	-	-	ns
Clock Rise Time	t_r	30%-70%	-	-	300	ns
Clock Fall Time	t_f	70%-30%	-	-	300	ns
Setup Time STOP Condition	$t_{SU:STO}$	-	0.6	-	-	μs
BUS Free Time Stop to Start	t_{BUF}	-	1.3	-	-	μs

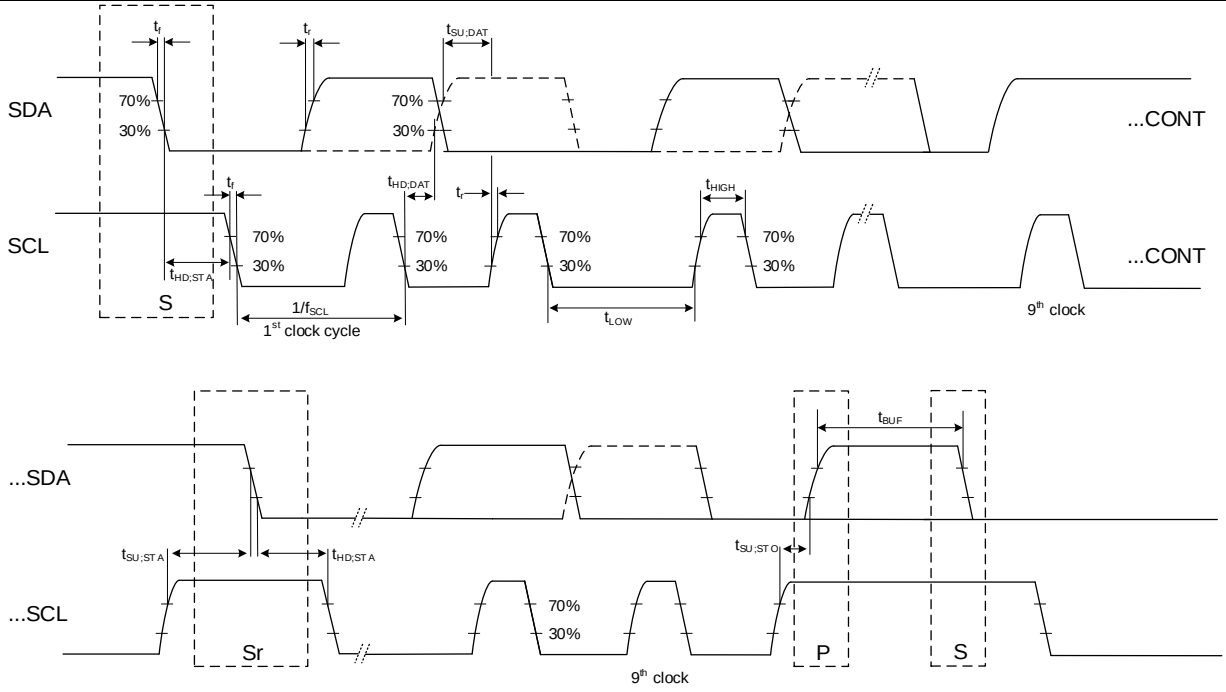


Figure 2. Definition of Timing for F/S-Mode Devices on the I²C-Bus

11.9 CAN Specs

Refer to “I/O Specs” for more details.

11.10 UART Specs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Baud Rate	-	-	300	-	926800	bps

Refer to “I/O Specs” for more details.

11.11 SPI Specs

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with controller and peripheral operations. Many of the transfer attributes are programmable. The following tables offer timing characteristics for classic SPI timing modes.

• All timing is shown with respect to 20% V_{VCC} and 80% V_{VCC} thresholds.

• Maximum output load of 25pF, and the drive strength of the GPIO is set to 10mA.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Internal Peripheral Frequency	f_{periph}	-	-	-	120	MHz
Frequency of Operation	f_{op}	-	-	-	20	MHz
Peripheral Clock Period	t_1	-	8.3	-	-	ns
SCK Period	t_2	-	50	-	-	ns
PCS to SCK Delay (Note 7)	t_3	Master	25	(PCS2SCK+1)*t_1	-	ns
SCK to PCS Delay (Note 7)	t_4	Master	25	(SCK2PCS+1)*t_1	-	ns
SCK High/Low Time	t_5	Master	t_2/2-5	t2/2	t_2/2+5	ns
Data Input Setup Time	t_6	Master	12	-	-	ns
		Slave	4	-	-	ns
Data Input Hold Time	t_7	Master	3	-	-	ns
		Slave	4	-	-	ns
Data Output Valid Time	t_8	Master	-	-	10	ns
		Slave	-	-	28	ns
Data Output Hold Time	t_9	Master	0	-	-	ns
		Slave	6	-	-	ns
Rise/Fall Time Input	t_{10}	-	-	-	11	ns
Rise/Fall Time Output	t_{11}	-	-	-	12	ns

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: When V_{VCCA} is between 2.8V and 3.0V, the ADC ENOB may be downgraded.

Note 3: θ_{JA} of LQFP100, LQFP64, and LQFP48 are measured in natural convection at T_A = 125°C on a low effective single-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. θ_{JA} of QFN32 is measured in natural convection at T_A = 125°C on a four-layer highly effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on “2x2” FR-4 substrate PCB, 2oz copper, with a minimum recommended pad on the top layer and thermal vias to the bottom layer ground plane.

Note 4: The device is not guaranteed to function outside its operating conditions.

Note 5: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that T_A T_J = 25°C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 6: Guaranteed by design or statistical correlation and not production tested.

Note 7: For details, please see SA32B16/14/12 Reference Manual

Note 8: All timing is shown with respect to 20% V_{VCC} and 80% V_{VCC} thresholds.

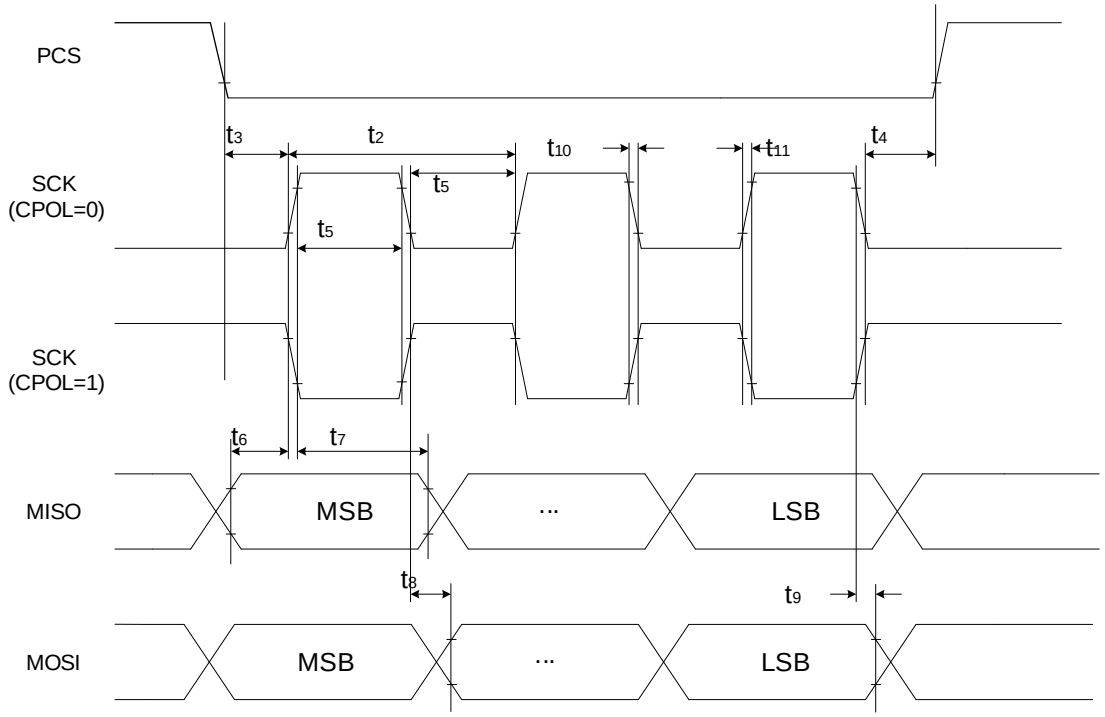


Figure 3. SPI Controller Mode Timing (CPHA = 0)

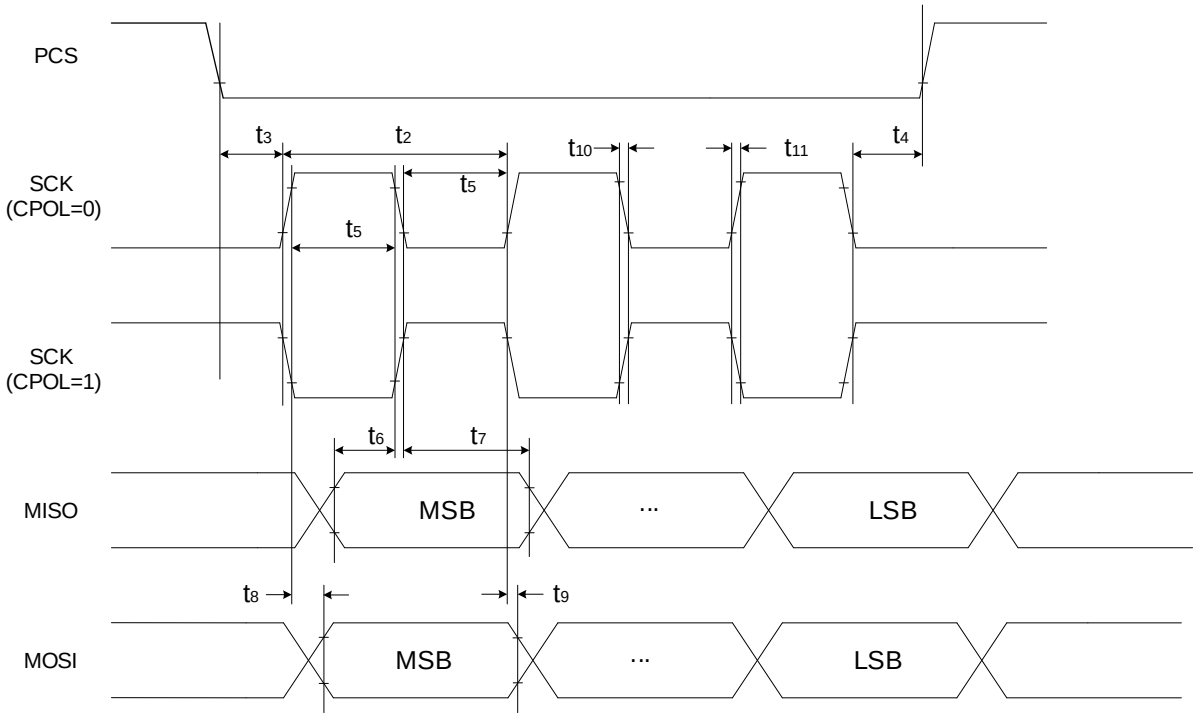


Figure 4. SPI Controller Mode Timing (CPHA = 1)

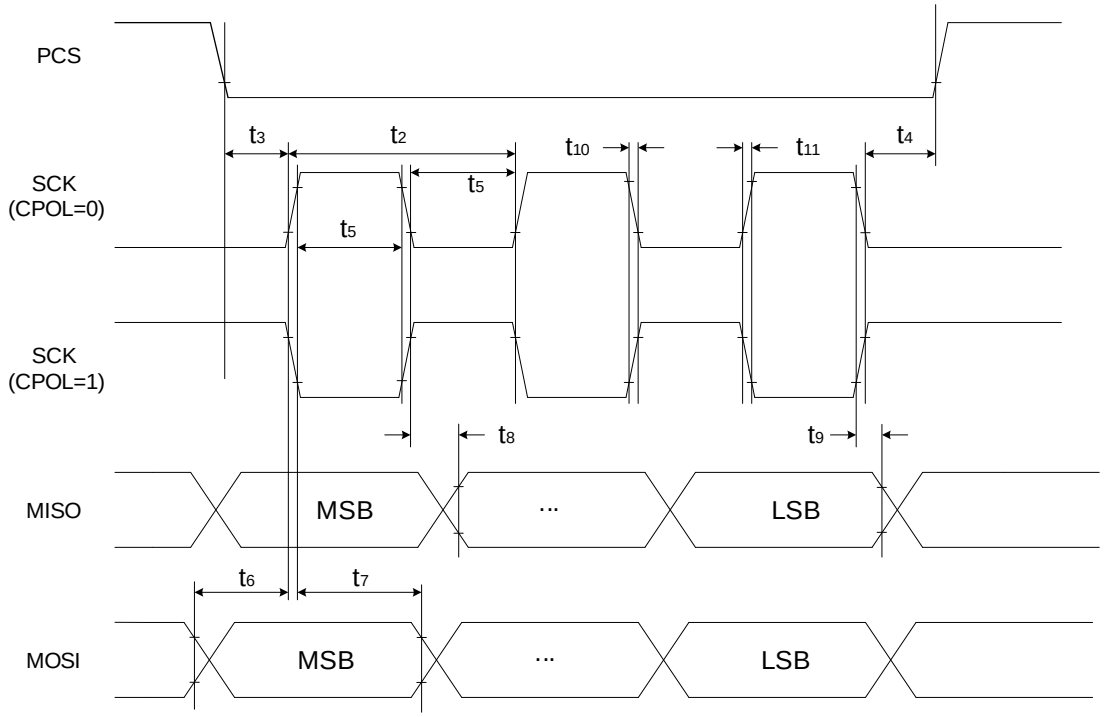


Figure 5. SPI Peripheral Mode Timing (CPHA = 0)

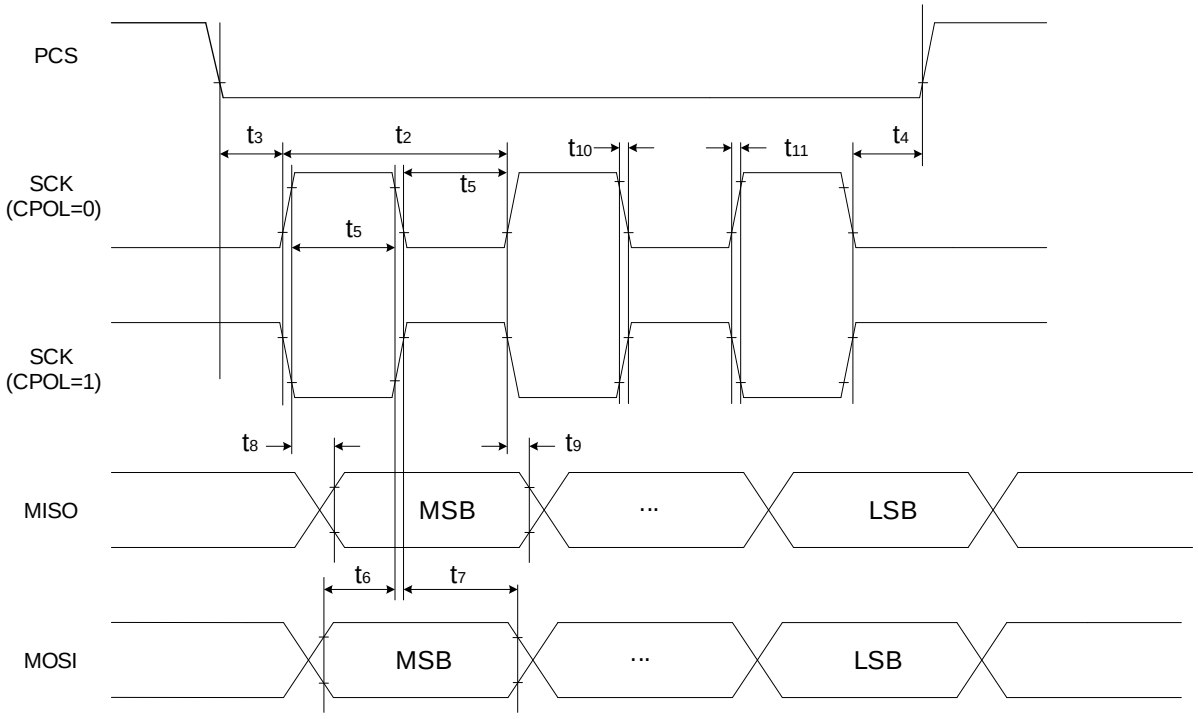


Figure 6. SPI Peripheral Mode Timing (CPHA = 1)

12. Function Overviews

12.1 CPU Core

This chip integrates an ARM Cortex®-M4F core with the following features:

- Max 120MHz frequency with 1.25DMIPS/MHz performance
- Integrated digital signal processing (DSP)
- Single precision floating point unit (FPU)
- Supports a 16-region memory protection unit (MPU)
- Supports SWD and JTAG debug interfaces

12.2 Interrupt Controller

This chip integrates a Nested Vector Interrupt Controller (NVIC) and a Wakeup Interrupt Controller (WIC). The NVIC manages all interrupts, including the core exceptions. The WIC is primarily used in deep sleep mode when the NVIC is disabled.

The NVIC controller handles interrupts during the Normal Run mode and wakes the core in Sleep mode.

The WIC controller is used to wake up the core in DeepSleep mode and to resume system clocking.

The NVIC and the core interface are closely coupled, which enables low-latency interrupt processing and efficient processing of late-arriving interrupts.

12.3 Code Flash

This chip integrates a fast access code flash macro with a 72-bit width interface (including 8-bit ECC code). This guarantees high performance of CPU instruction fetch to achieve zero wait access.

Each device may incorporate different sizes of code flash macros. The detailed code flash size is listed in the following table.

The code flash contains multiple sectors which can be erased individually. Each sector size is 512 x 72 bits.

Table 1: Code Flash Memory Size

Part Number	Main Size(KB)	Sectors	Address
SA32B16x	512	128	0x0000_0000~0x0007_FFFF
SA32B14x	256	64	0x0000_0000~0x0003_FFFF
SA32B12x	128	32	0x0000_0000~0x0001_FFFF

12.4 Data Flash

This chip integrates a dedicated data flash macro for user data. This data flash supports 100K-cycling high endurance. It can also be used as EEPROM emulation (FEE function) to achieve higher endurance. With separated data flash macro, this chip can support the read-while-write function during user data program.

The data flash size is listed in the following table.

The data flash contains 32 sectors which can be erased individually, and the last two sectors are only for SHE module. Each sector size is 512x72 bits.

Table 2: Data Flash Memory Size

Part Number	Main Size(KB)	Sectors	Address
SA32B16x	128	32	0x2002_0000~0x2003_DFFF
SA32B14x	128	32	0x2002_0000~0x2003_DFFF
SA32B12x	128	32	0x2002_0000~0x2003_DFFF

12.5 TCMs and System RAM

This chip integrates two tightly coupled local SRAMs (TCM: SRAM0 and SRAM1) and one system SRAM (SRAM2).

- SRAM0 is working as Instruction TCM (ITCM)
- SRAM1 is working as Data TCM (DTCM)
- SRAM2 is working as System RAM

The TCM (Tightly Coupled Memory) units provide zero wait-time access for both instruction fetch and data access, optimizing core efficiency. Additionally, DMAs can access TCM memories through an AHB peripheral port on the bus matrix. When accessed by a DMA module, TCM operates similarly to system RAM.

- The core and the DMAs can both access the System RAM memory.
- The SRAM bus width is 32-bits. The size of each SRAM is listed in the following table:

Table 3: SRAM Memory Size

Name	Size (KB)	Start Address	End Address	Note
SRAM0	16	0x1FFF_C000	0x1FFF_FFFF	ITCM
SRAM1	16	0x2000_0000	0x2000_3FFF	DTCM
SRAM2	32	0x2000_4000	0x2000_BFFF	System RAM

12.6 Boot ROM

This chip integrates a Boot ROM. The ROM is factory-programmed with the Silergy proprietary bootloader. The bootloader uses UDS protocol and provides a variety of ways for users to update code. It also supports a flash code integrity check service during chip POR.

This chip supports FOTA updates with the CAN interface using the ROM Bootloader or Flash Bootloader.

12.7 Power Modes

The chip supports four power modes:

1. Normal Run Mode:
   - All analog and digital modules are active and functioning normally. Peripherals can be optionally activated or deactivated by software.
2. Sleep Mode:
   - The core enters Sleep mode via WFI (Wait for Interrupt) or WFE (Wait for Event) instructions. While in this mode, the NVIC (Nested Vectored Interrupt Controller) and SysTick remain active. The NVIC can wake the CPU from Sleep mode when an enabled interrupt is received.
3. DeepSleep Mode:
   - Initiated by the WFI or WFE instruction with the SLEEPDEEP control bit set in the ARM System Control Register. In this mode, NVIC and SysTick are disabled. Components such as the PLL, Flash, DMA, TCMC, peripherals, and analog modules can be selectively turned on or off. The Wakeup Interrupt Controller (WIC) is responsible for waking up the CPU from DeepSleep mode upon receiving an enabled interrupt. This mode is sometimes referred to as "Stop mode" in some device documentation.
4. Hibernate Mode:
   - Designed to achieve the lowest possible power consumption. In this mode, regulators, along with all peripherals and memories (except for the HIB Controller, RSTGEN module, RTC module, and a wakeup timer), can be optionally turned off. The system can be awakened from Hibernate mode by the wakeup timer, the Reset pin, a push-button event (PBTN), or GPIO wakeup pins (either edge or pulse triggered).

12.8 DMA

This chip integrates two DMA modules, each with eight channels (2x 8ch DMA), but can support up to 64 DMA requests.

The DMA controller module enables fast data transfer and provides an efficient way to move data without CPU interaction.

The DMA supports 8-bit, 16-bit, or 32-bit data transfers. DMA data transfers can be explicitly initiated by software or peripheral hardware requests.

12.9 TRGMUX

This chip features a TRGMUX module that facilitates event cross-triggers and interconnections among components such as Timers, Peripherals, ADCs, and CMPs. This module enables the triggering of other modules via specific events using a purely hardware-based scheme, eliminating the need for CPU interrupts. Additionally, the TRGMUX offers software trigger capabilities for added flexibility when required.

The following peripherals are capable of providing trigger events:

- GPIO Ports
- TRGT Timers
- GPT Timers
- PWM Timers
- CMPs
- ADCs
- RTC
- Software Triggers

12.10 WDOG

The watchdog (WDOG) is a 16-bit safety timer used to detect and recover from software or hardware failures. The WDOG works with independent clock sources to avoid common failures within the system.

To prevent an unintended system reset, the CPU must periodically refresh the WDOG within this interval. The WDOG employs a robust write sequence to refresh its counter and also supports a window mode for counter refresh, enhancing system security and reliability.

The WDOG module is enabled by default, but its reset functionality is initially disabled. The reset function can be activated via software during the MCU's Power-On Reset (POR) initialization. The configuration bits for enabling the WDOG reset function are write-once only post-reset to prevent accidental modification.

12.11 EWDG

The redundant external watchdog (EWDG) provides a backup mechanism to the internal watchdog (WDOG) to reset the MCU or external circuits/chips into a safe mode.

The critical difference between the External Watchdog Timer (EWDG) and the internal watchdog (WDOG) is that the EWDG does not directly reset the MCU. Instead, it relies on external circuits or chips, such as a Power Management Integrated Circuit (PMIC), to initiate the reset process.

The EWDG will generate an alert signal if the CPU does not refresh the EWDG within the programmed window. An optional external input is also provided to control the assertion of an EWDG alert when an external event (such as a failure or request) occurs.

12.12 CRC

This chip integrates three Cyclic Redundancy Check (CRC) modules for parallel error detection. The CRC module usually calculates 16/32-bit CRC codes to detect error information. In addition, CRC-based technology verifies the integrity of the transmission or storage of data information.

The CRC module supports configurable polynomial and initial seed values to achieve 16-bit or 32-bit CRC calculations. It also allows input data or CRC results to be transposed by bit or byte and inverse the final CRC result.

12.13 ADC

The ADC on this chip is a successive approximation analog-to-digital converter (SAR-ADC) with rail-to-rail inputs (up to V_{VCC}). This chip integrates two ADCs, each supporting 16 external channels (32ch totally).

The ADC supports configurable 12-bit, 10-bit, and 8-bit resolutions and a maximum sample rate of up to 1Msps with 12-bit mode. It has three conversion groups, one regular group, and two injected groups. The groups and channels support configurable priority.

The conversion of each channel can be performed in single, scan, or continuous mode. The conversion results are stored in dedicated data registers with a programmable threshold monitor. The ADC also supports selectable software conversion triggers and hardware triggers.

This ADC is specially designed and optimized for automotive applications.

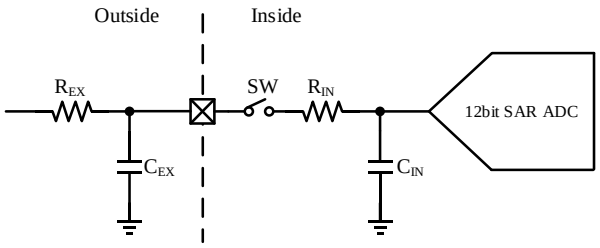


Figure 7. ADC Input Network

1. Refer to 11.6 ADC spec in Electrical Characteristics for the values of R_{IN} and C_{IN}.
2. R_{EX} and C_{EX} are the equivalent resistance and capacitance outside the chip.
3. The sample time(t_s) of 12bit SAR ADC need meet the follow condition:
   a) $t_s \geq N \times \tau$
   b) $N = \ln(2^{12}/error) - \ln(C_{EX}/C_{IN})$
   c) $\tau = R_{EX} \times C_{EX} + (R_{EX} + R_{IN}) \times C_{IN}$
   d) error is the settling error, for example: if the expected settling error is 0.5LSB, error = 0.5
4. Default value of t_s is 250ns.

12.14 CMP

The comparator (CMP) module provides a circuit for comparing two input analog signals or an input signal with an internal reference. An 8-bit DAC, a 256-tap resistor ladder network with a selectable Vin supply, can generate the reference.

The comparator is designed to operate across the full supply voltage range (rail-to-rail) with fast response. It supports programmable hysteresis control, output polarity, window mode, and digital filter on comparator output. It also supports selectable interrupt on rising-edge, falling-edge, or both rising and falling edges of the comparator output.

12.15 CAN

The chip includes three CAN modules compatible with the CAN 2.0 Specification and supports the Flexible Data-rate (CAN-FD) functionality. These modules can handle standard and extended frames, transmitting up to 64 bytes of data and facilitating higher-speed communication. Message buffers are stored in dedicated RAM for CAN.

The CAN module includes the following features:

- Compliant with CAN protocol specification, Version 2.0 B
- Compliant with the ISO 11898-1 standard
- Supports Flexible Data Rate (CAN FD) protocol specification
- Supports up to 32 message buffers
- Supports standard or extended data frames
- Supports programmable bit rate

- Programmable 0 to 64 bytes mailbox data length
- Programmable transmission priority scheme
- Support normal mode, listen-only mode and loop-back mode
- Supports global network time synchronization
- Supports transceiver delay compensation
- Supports Rx FIFO ID filtering mechanism
- Supports Pretended Networking

12.16 UART/LIN

The chip integrates four UART/LIN modules. The UART (Universal Asynchronous Receiver/Transmitter) is a serial data bus used for asynchronous communication, allowing bidirectional communication that supports full duplex transmission and reception. The LIN protocol, which uses a similar mechanism for asynchronous communication, is implemented with the UART modules.

The UART/LIN module supports the following features:

- Full-duplex asynchronous communications
- NRZ standard format
- Programmable baud rate and oversampling rate
- Supports Autobaud mode
- Supports 7, 8, 9, or 10 bits data word length
- Supports optional parity bit and 1 or 2 stop bits
- Programmable data order with MSB-first or LSB-first shifting
- Supports single-wire Half-duplex communications
- Supports wakeup with idle detect, bit mark, and address match
- Configurable break character generation/detection
- Support hardware flow control with RTS and CTS
- Support IrDA RZI format with programmable pulse width
- Supports transmit and receive FIFO
- Complies with LIN2.2 and SAE J2602

12.17 SPI

The chip integrates four SPI modules, each supporting four chip selects. The SPI is a synchronous communication protocol that supports simplex, half-duplex, and full-duplex synchronous communication as a controller or peripheral.

The SPI module has the following features:

- Supports controller mode or peripheral mode
- Programmable data frame size
- Programmable baud rate by eight divider options
- Programmable clock polarity and phase
- Programmable data width (up to 4 bits parallel transmission)
- Optional data order with MSB-first or LSB-first shifting
- Supports four words: Transmit and Receive FIFOs
- Supports multi-peripheral broadcasting mode
- Supports 1-bit data transfer in full or half duplex mode
- Support 2-bit, 4-bit data transfer in half-duplex mode
- Programmable match function of received data and wakeup interrupt generation
- Optional sample clock of receiving data (controller only)

12.18 I²C

The chip integrates two I²C modules. The I²C module supports controller mode and peripheral mode. It supports the System Management Bus (SMBus) Specification, version 2. The SMBus is a single-ended, simple two-wire bus for low-bandwidth communications.

The I²C module has the following features:

- Supports Controller or Peripheral modes
- Controller mode supports up to Ultra Fast mode (5Mbps)
- Peripheral mode supports up to High Speed mode (3.4Mbps)
- Supports multi-controllers, including synchronization and arbitration
- Supports configurable bus idle timeout and pin-stuck-low timeout
- Supports 7-bit or 10-bit addressing, address range, SMBus alert, and general call address
- Programmable match function of received data and interrupt generation
- Software-controllable ACK or NACK, optional clock stretching
- Supports 2-wire mode and 4-wire mode
- Supports FIFO and DMA modes

12.19 SENT

The Single Edge Nibble Transmission (SENT) module is designed to receive serial data frames from sensors that use the SENT encoding scheme, facilitating data presentation and processing to the CPU. The SENT protocol suits applications requiring high-resolution data from a sensor to the Electronic Control Unit (ECU). It aims to provide a straightforward, low-cost alternative to traditional methods such as 10-bit A/D converters, PWM, and other communication protocols like CAN or LIN.

This chip features two independent SENT channels that operate in parallel.

12.20 PWM Timer

The chip integrates four PWM timers, each supporting up to eight PWM channels (32 channels total). The PWM Timer is an advanced timer block that can generate flexible and complicated PWM signals for specific applications such as Motor Control or Digital Power Control.

The PWM Timer has the following features:

- 16-bit counter with up counting mode or up/down counting mode
- Each module includes eight independent channels for:
  - Input capture
  - Output compare
  - PWM generation (Edge and Center-Aligned Mode)
  - Single-shot mode output
- Supports complementary outputs with programmable dead-time
- Supports software control of PWM outputs
- Supports fault protection and control
- Support Quadrature decoder with input filters
- Shadow register and write protection for critical registers
- Hardware counter synchronization between PWM Timers

12.21 Trigger Timer

The Trigger Timer (TRGT) is a versatile device capable of hardware trigger generation, periodic PWM or pulse generation, pulse counting, and capture. The chip includes two TRGT timer modules, each supporting four timer channels. Each timer channel generates trigger output signals or interrupts when it reaches the programmed count value. These trigger output signals can serve as hardware events to activate other modules within the chip.

- **32-bit Periodic Counter Mode:** The counter is loaded with a value and begins counting down. An interrupt and trigger are generated when the counter reaches zero.
- **Dual 16-bit Periodic Counter Mode:** The counter is loaded with a value, with the lower 16 bits counting down to zero to assert a trigger signal. Subsequently, the upper 16 bits count down to zero, de-asserting the trigger signal and generating an interrupt.
- **32-bit Trigger Accumulator:** The counter is loaded with a value and decreases to zero with each rising edge of the trigger input. Upon reaching zero, it generates an interrupt and a trigger output signal.
- **32-bit Trigger Input Capture:** The counter starts counting down from 0xFFFFFFFF to 0. The inverse of the current counter value is stored in the counter register with each rising edge of the trigger input signal, leading to the generation of an interrupt and a trigger output signal.

12.22 GPT Timer

The general purpose timer (GPT) supports two modes. It can operate as a general timer or pulse counter with an optional glitch filter.

The features of the GPT module include:

- 16-bit counter with free-running mode or reset on compare
- Support general timer mode or pulse counter mode
- Supports asynchronous wakeup from DeepSleep mode
- Supports interrupt and hardware trigger outputs
- Configurable clock source for prescaler/glitch filter
- Configurable rising-edge or falling-edge input for pulse counter

12.23 RTC

The real-time clock (RTC) is an independent timer with BCD coding.

The RTC module has the following characteristics:

- 32-bit seconds register with roll-over protection and 32-bit alarm register
- 16-bit prescaler register with compensation function to correct errors between 0.12 ppm and 3906 ppm
- Configurable 1, 2, 4, 8, 16, 32, 64, or 128Hz square wave output with optional interrupt feature

12.24 SHE Security Engine

The chip integrates a SHE Security Engine (SSE). The security engine complies with the Secure Hardware Extension (SHE) R19-11 specification AUTOSAR defines. The SHE standard is intended to move the control over cryptographic keys from the software domain into the hardware domain, protecting keys from software attacks.

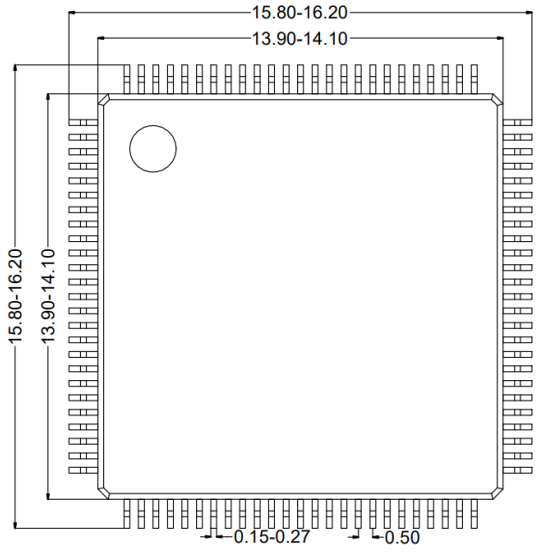
The SSE module implements all of the requirements of the SHE standard, including AES128, secure zone, secure cryptographic key storage, and CMD communication. In addition, the SSE also integrates a secure hash engine for SHA256/SHA224 and a True Random Number Generator (TRNG) that meets the SP800-22 random number test standard.

The SSE engine supports the following functions or algorithms:

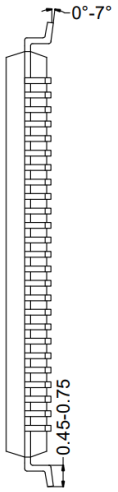
- Data encryption and decryption with ECB and CBC modes
- MAC generation and verification
- Compression function with AES
- Secure Booting
- In addition to meeting AUTOSAR SHE standards, the SSE engine complies with the HSM up to the EVITA Light Level.

13. Package Outline Drawing

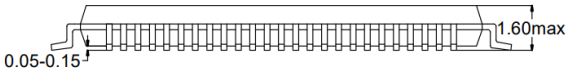
13.1 LQFP14x14-100 Package Outline Drawing



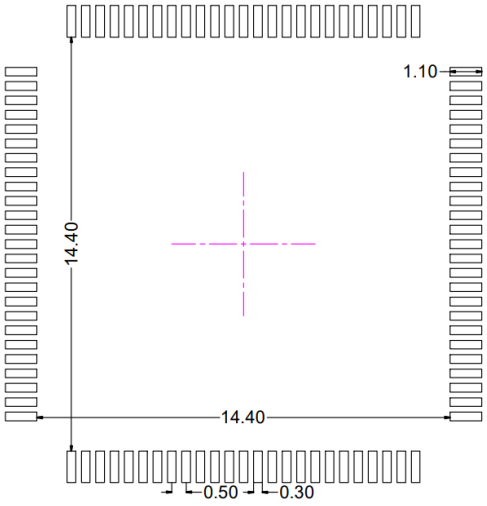
Top View



Side View



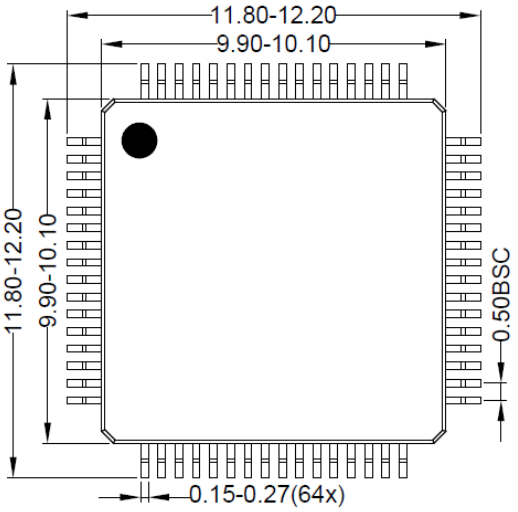
Front View



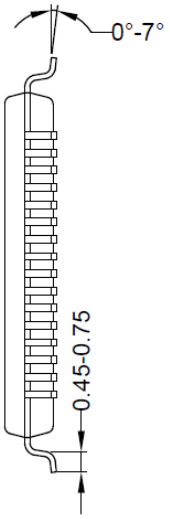
Recommended PCB Layout (Reference Only)

Note: All dimensions are in millimeters and don't include mold flash and metal burr.

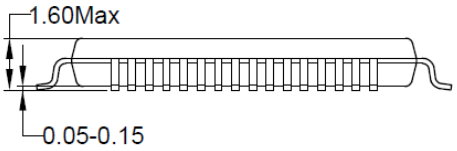
13.2 LQFP10x10-64 Package Outline Drawing



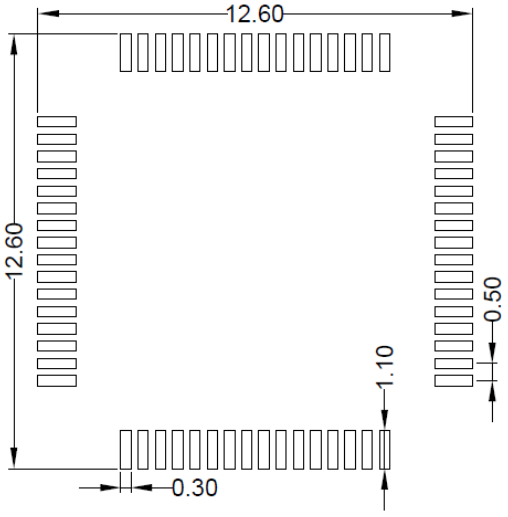
Top View



Side View



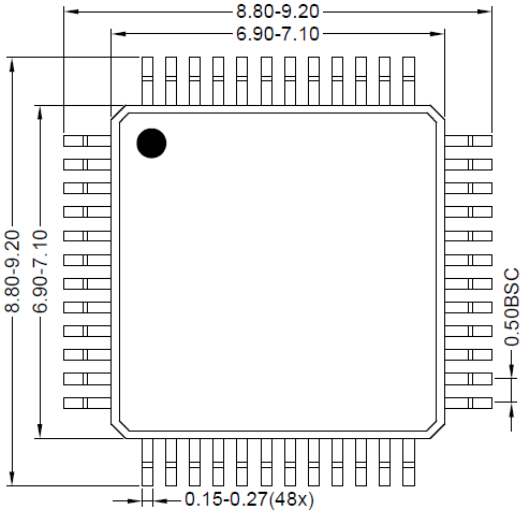
Front View



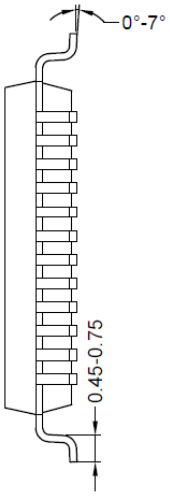
Recommended PCB Layout (Reference only)

Note: All dimensions are in millimeters and don't include mold flash and metal burr.

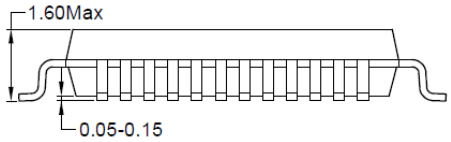
13.3 LQFP7x7-48 Package Outline Drawing



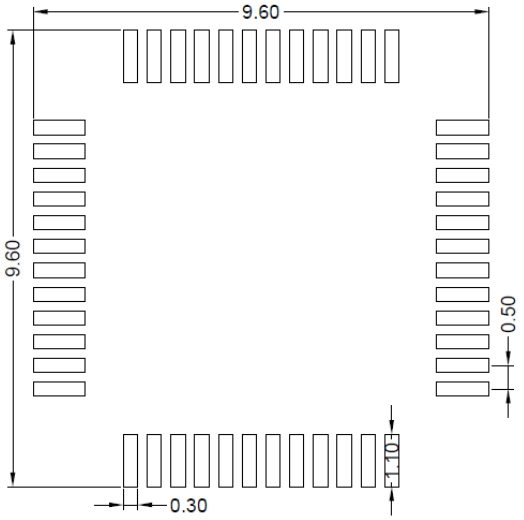
Top View



Side View



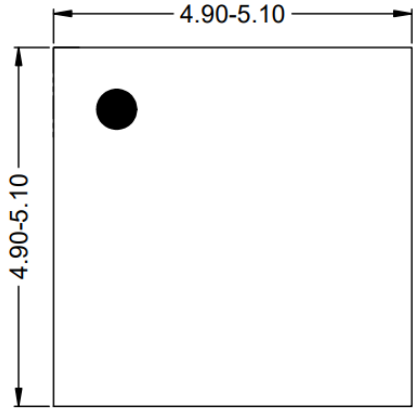
Front View



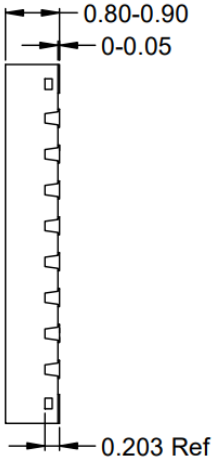
Recommended PCB Layout (Reference only)

Note: All dimensions are in millimeters and don't include mold flash and metal burr.

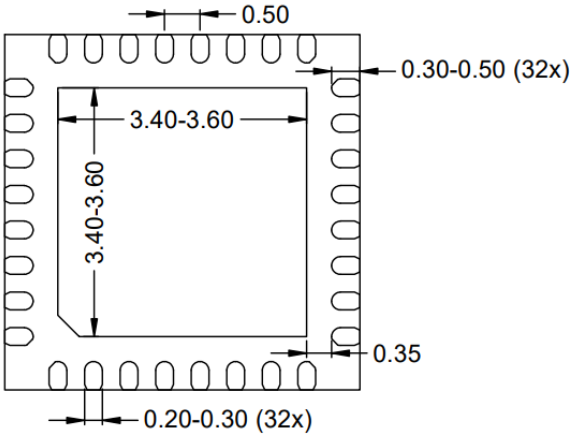
13.4 QFN5x5-32 Package Outline Drawing



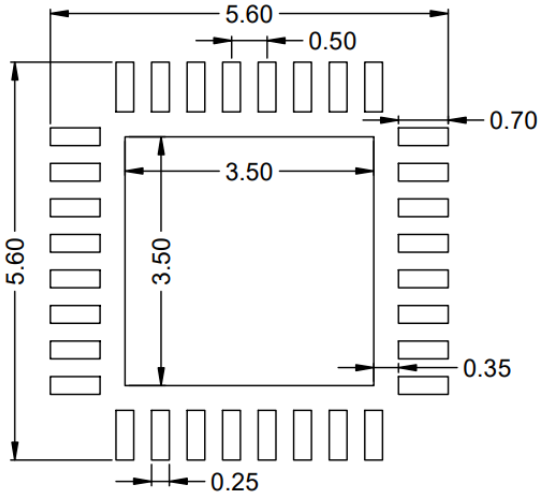
Top View



Side View



Bottom View



Recommended PCB Layout (Reference Only)

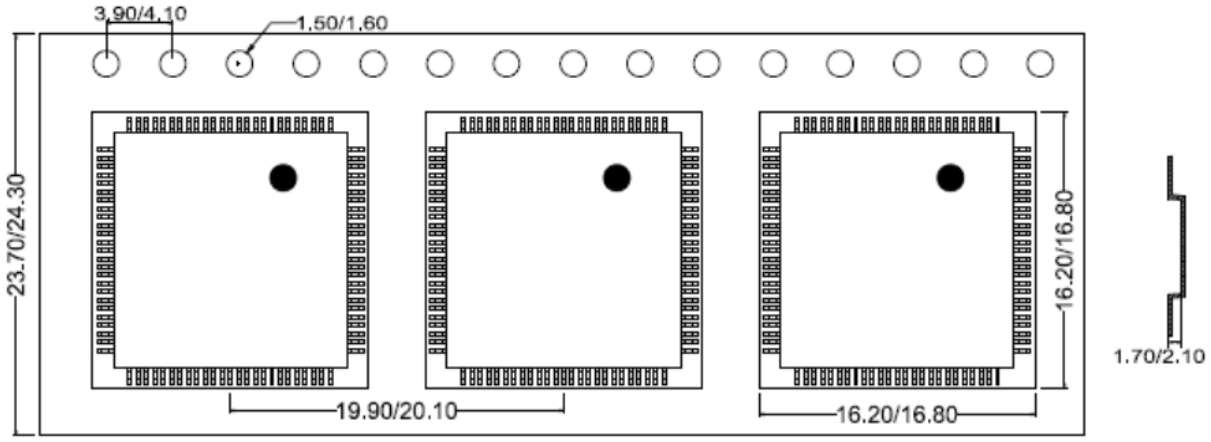
Note: All dimensions are in millimeters and don't include mold flash and metal burr.

14. Tape and Reel Information

14.1 LQFP14x14-100 Tape and Reel Information

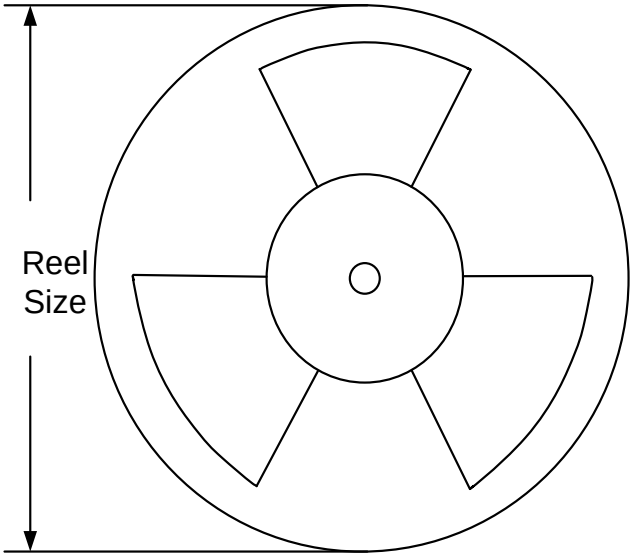
1. Tape Dimensions and Pin 1 Orientation

LQFP14x14-100



Feeding Direction ⟶

2. Reel Dimensions

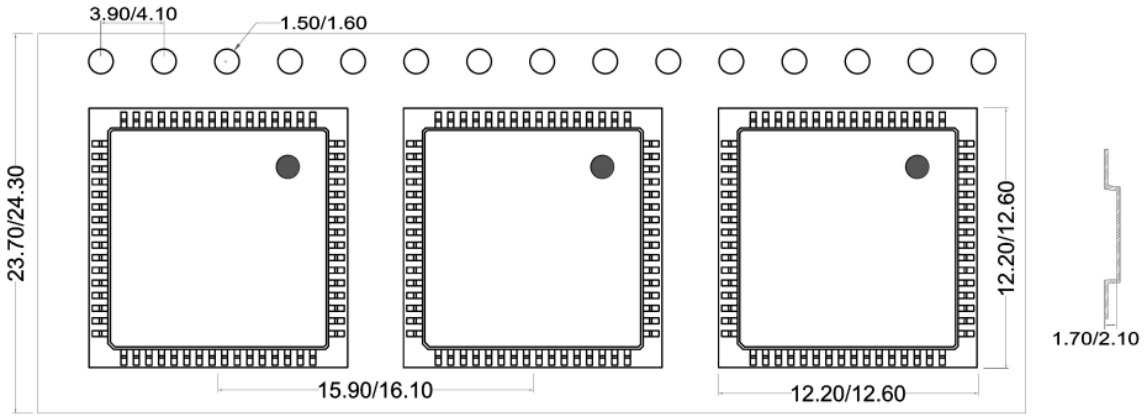


Part number	Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
SA32B16GEF	LQFP14x14-100	24	20	13"	1400	1400	1000

14.2 LQFP10x10-64 Tape and Reel Information

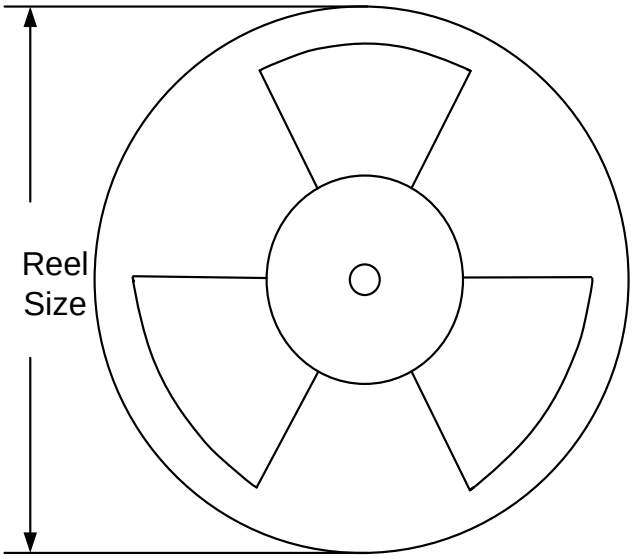
1. Tape Dimensions and Pin 1 Orientation

LQFP10x10-64



Feeding Direction ⟶

2. Reel Dimensions

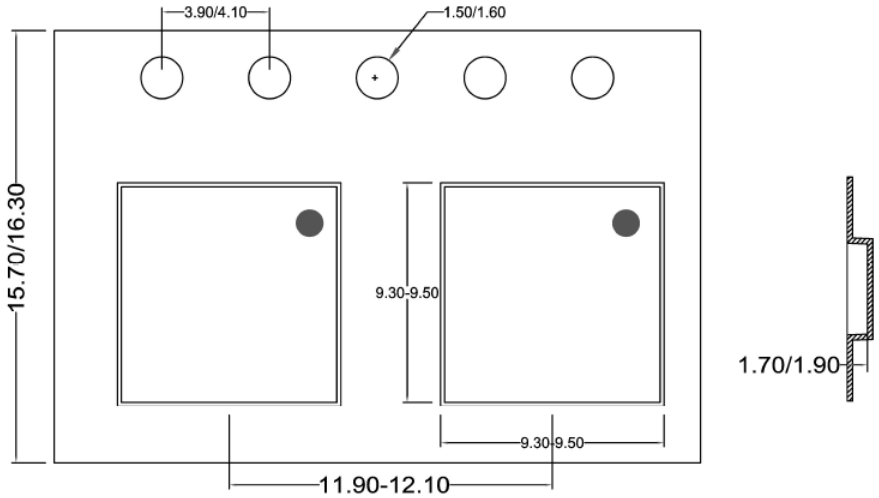


Part number	Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
SA32B16GDF	LQFP10x10-64	24	16	13"	1400	1400	1500
SA32B14GDF							

14.3 LQFP7x7-48 Tape and Reel Information

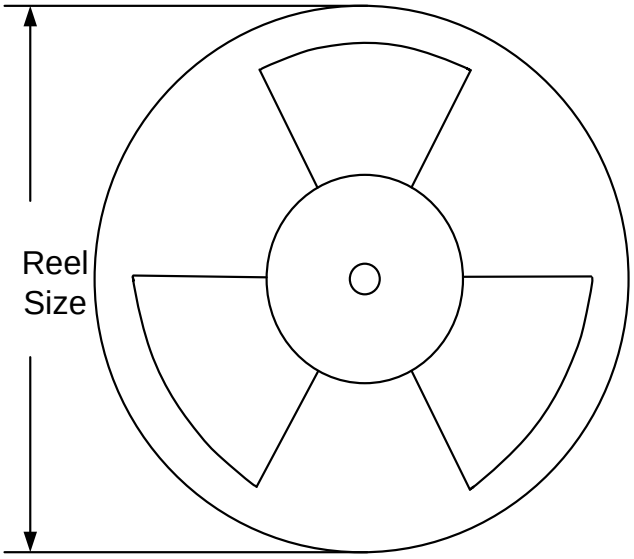
1. Tape Dimensions and Pin 1 Orientation

LQFP7x7-48



Feeding Direction ⟶

2. Reel Dimensions

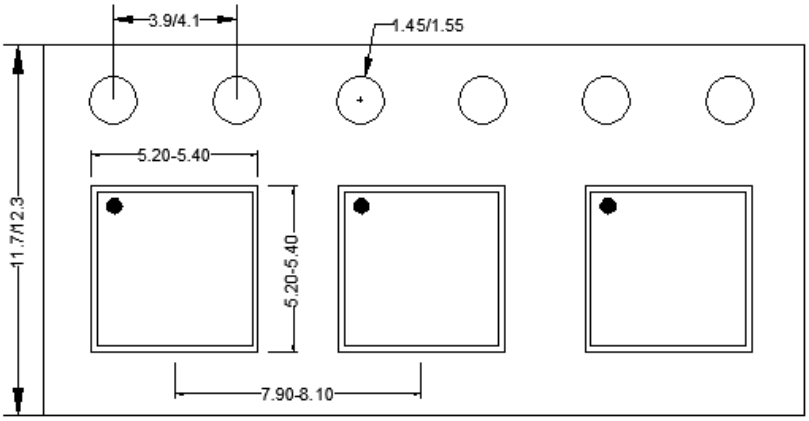


Part number	Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
SA32B16GFF	LQFP7x7-48	16	12	13"	400	400	2000
SA32B14GFF							
SA32B12GFF							

14.4 QFN5x5-32 Tape and Reel Information

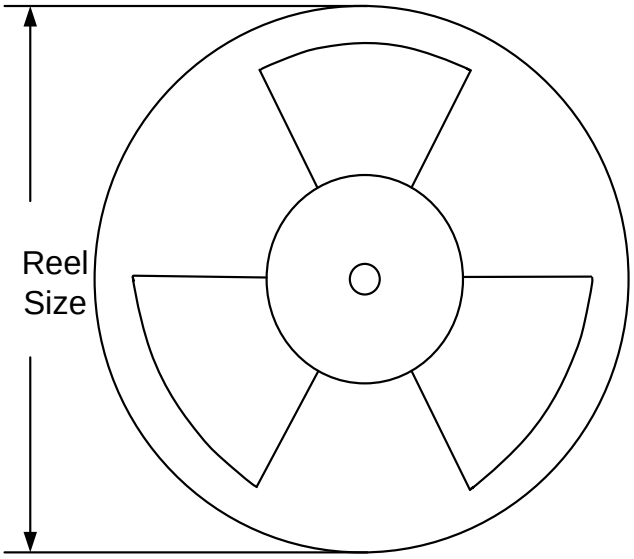
1. Tape Dimensions and Pin 1 Orientation

QFN5x5



Feeding Direction ⟶

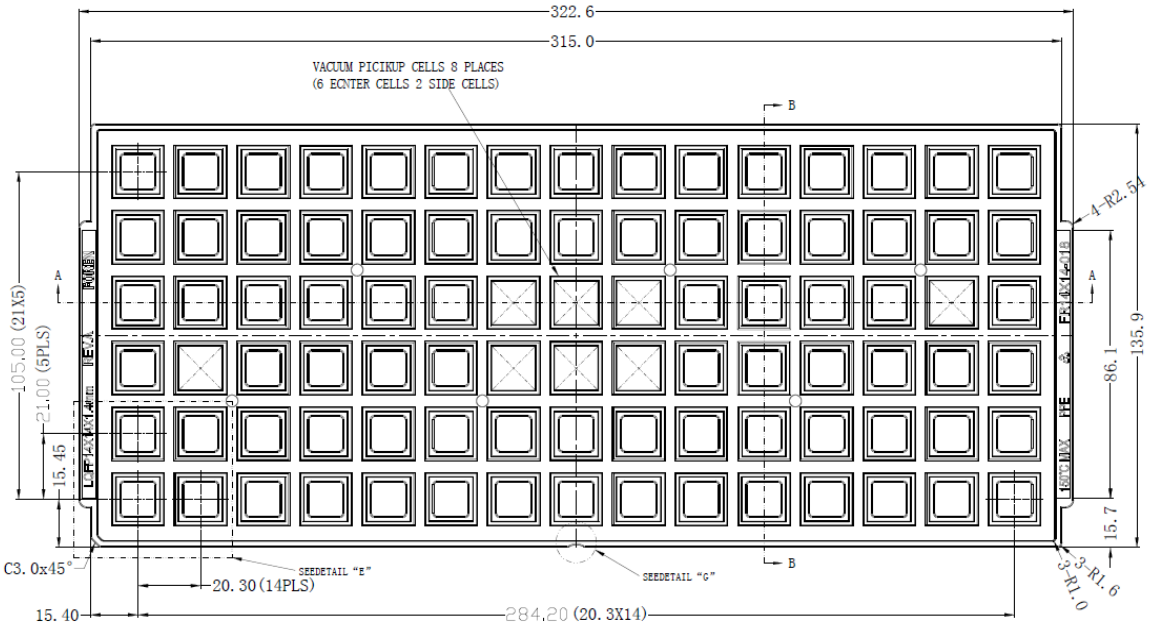
2. Reel Dimensions



Part number	Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
SA32B12QEQ SA32B12AQEQ	QFN5x5-32	12	8	13"	400	400	5000

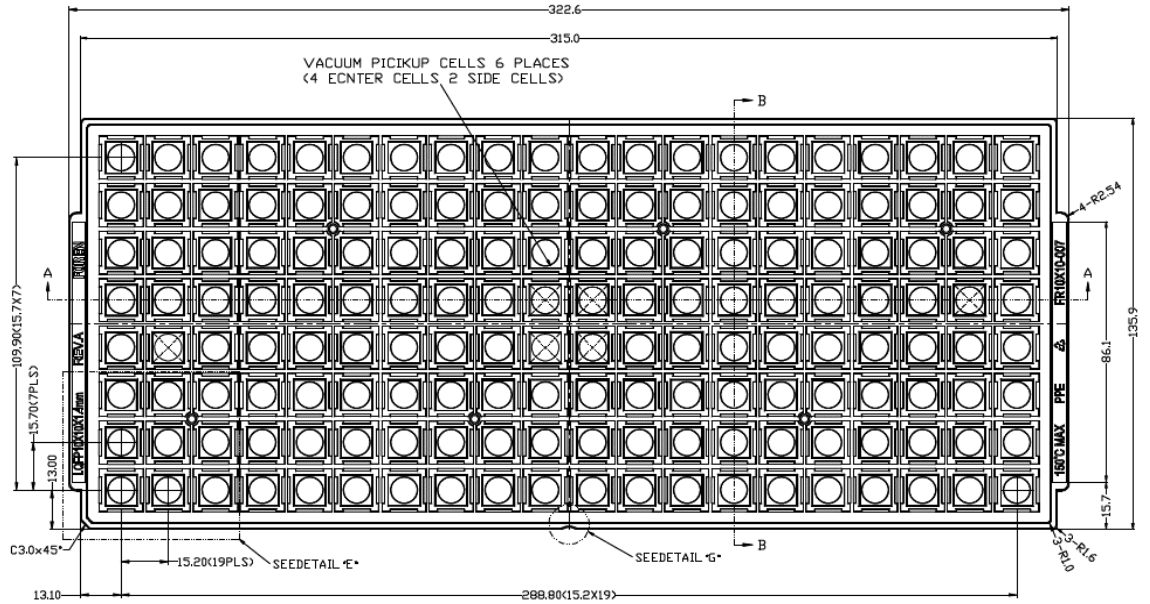
15. Tray Information

15.1 LQFP14x14-100 Tray Information



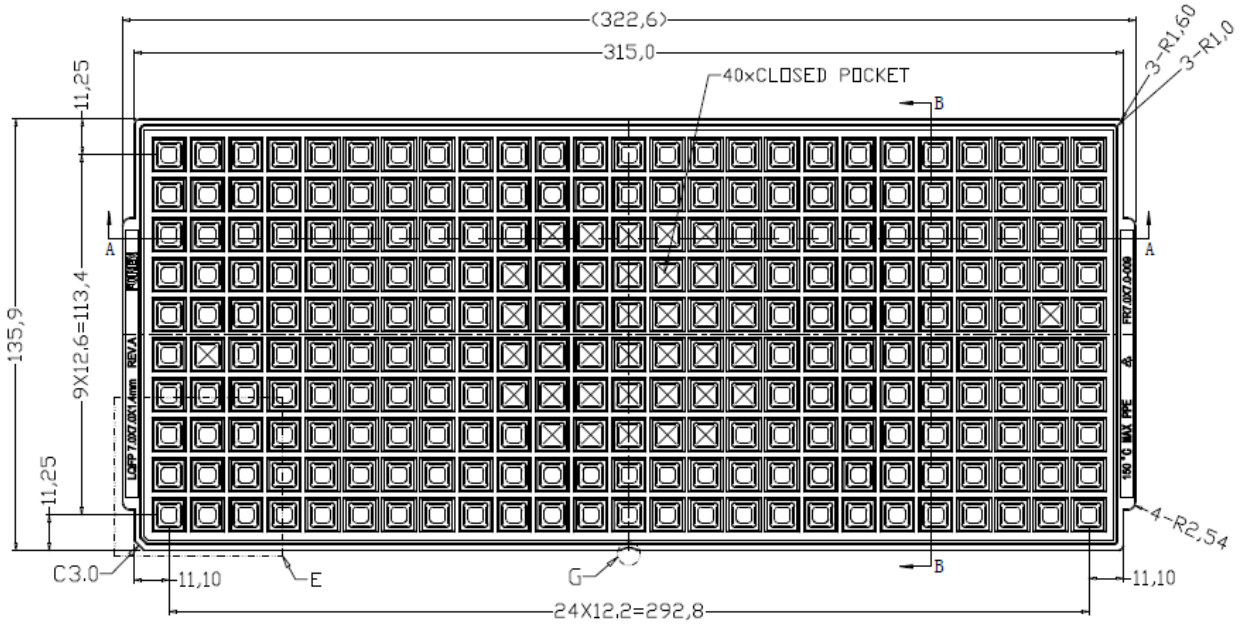
Part number	Package types	Qty per tray (pcs)	trays per box	Qty per box (pcs)
SA32B16GEF-T	LQFP14×14-100	90	4	360

15.2 LQFP10x10-64 Tray Information



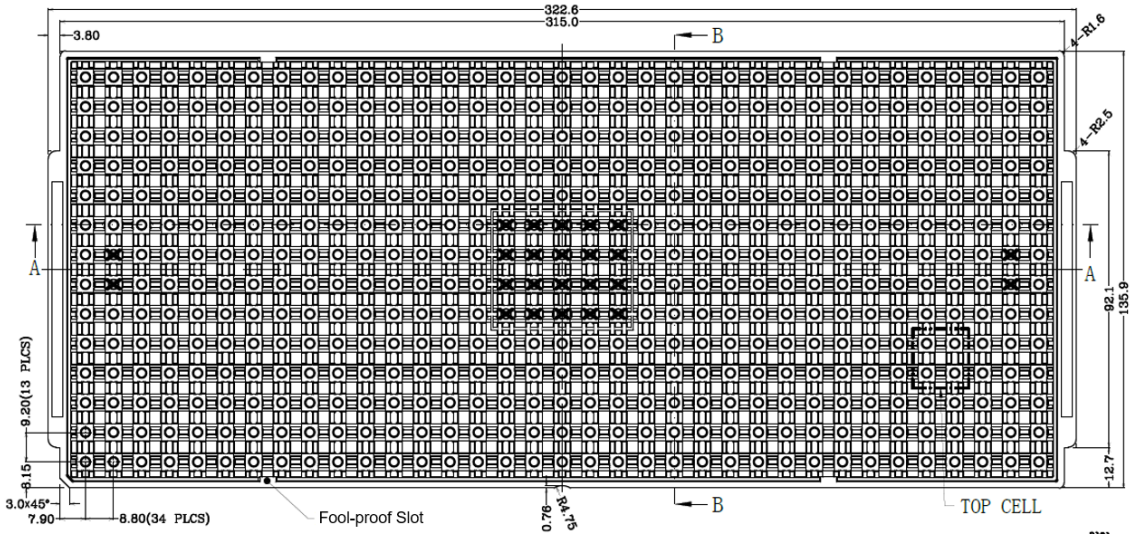
Part number	Package types	Qty per tray (pcs)	trays per box	Qty per box (pcs)
SA32B16GDF-T	LQFP10×10-64	160	4	640
SA32B14GDF-T				

15.3 LQFP7x7-48 Tray Information



Part number	Package types	Qty per tray (pcs)	trays per box	Qty per box (pcs)
SA32B16GFF-T	LQFP7×7-48	250	4	1000
SA32B14GFF-T				
SA32B12GFF-T				

15.4 QFN5x5-32 Tray Information



Part number	Package types	Qty per tray (pcs)	trays per box	Qty per box (pcs)
SA32B12QEQ-T	QFN5x5-32	490	4	1960
SA32B12AQEQ-T				

16. Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
May. 27, 2024	Revision 1.0	SA32B16GEF Initial Release
Dec. 30,2024	Revision 1.0A	1. SA32B12QEQ/ SA32B12AQEQ/ SA32B12GFF/ SA32B14GFF/ SA32B14GDF/ SA32B16GFF/ SA32B16GDF Initial Production Release. 2. Page1: Delete 12ns Access Time in Memory part and delete 12ns at page 19 in 12.3 Code Flash. Add Built-in 2.5V ADC Reference and Built-in temperature monitor in Memory part. Add Supports complementary outputs with programmable dead-time； Supports Input capture and output compare with Edge and Center-Aligned Mode in Peripherals Part in *2.Features*. 3. Page2: Add products SA32B1x-T which Carrier Type is tray in *4. Ordering Information* and add *15. Tray Information* at Page34. 4. Page8-9: Delete SSE_UART_TX/SSE_UART_RX/SSE_SWD_CLK SSE_SWD_DIO and add Note: “DISABLED” refers to a high-impedance state at Page9 in the *6. Pin Description*. 5. Page10: Modify TRND to TRNG and Modify Support OTA Upgrate to Build-in 2.5V ADC Reference in *7. Block Diagram*. 6. Page11: **Update Electrostatic Discharge of Human-body model for all package from ±6000V to ±4000V; Modify Min value of VREFH from GND-0.3 to 2.8V and add Note 2: When V_{VCCA} is between 2.8V and 3.0V, the ADC ENOB may be downgraded to explain the updated VREFH value**; add new spec MCU Supply Ramp Rate in *8. Absolute Maximum Ratings*. 7. Page11-13: **Modify Min value of VCC, VCCA Supply Voltage from 2.7 to 2.8** in *10. Recommended Operating Conditions*. **Modify Min value of VCC Supply Voltage Range from 2.7 to 2.8** at Page12 in *11.1 Power and Operation Conditions*. **Modify Min value of Supply Voltage Range from 2.7 to 2.8** at Page13 in *11.3 I/O Specs 3.3V Power Supply Mode*. 8. Page12: Add test condition of Supply Voltage LVD Threshold and Supply Voltage LVW Threshold; **Update max value of Supply Voltage LVD Threshold (VCC=3.3V) from 2.73 to 2.75; Update Min value of Default Idle Current Min from 2.7 to 2.0**; update the test condition of Run Mode Current from “All peripheral clock disabled” to “All peripheral clock disabled with system clock = 120MHz”; add note 6 for Deepsleep Mode and **Modify Typ value of Deepsleep Mode from 1mA to 700μA** in *11.1 Power and Operation Conditions*. 9. Page12-13: Modify the title of 11.2 from “I/O Specs VCC=5.0V” to “I/O Specs 5V Power Supply Mode”; add Note 8: All timing is shown with respect to 20% V_{VCC} and 80% VVCC thresholds for Rise Time and Fall Time. Change Symbol of Rise Time from T_{RISE_TIME} to t_{RISE_TIME}; **Modify Min value of Pull up Resistance and Pull down Resistance from 24 to 20 and Max value from 37 to 40** in *11.2 I/O Specs 5V Power Supply Mode*. 10. Page13: Modify the title of 11.2 from “I/O Specs VCC=3.3V” to “I/O Specs 3.3V Power Supply Mode”; add Note 8: All timing is shown with respect to 20% V_{VCC} and 80% VVCC thresholds for Rise Time and Fall Time. **Modify Min value of Pull up Resistance and Pull down Resistance from 27 to 25 and Max value from 43 to 45** in *11.3 I/O Specs 3.3V Power Supply Mode*. 11. Page13: Change Symbol of Frequency from F to f in *11.4 Clock Specs*. 12. Page14: **Remove Min / Max value and add Typ value of Program Time, Sector Erase Time and Chip Erase Time** and add Note 6 for those specs; Add new spec Read Time in *11.5 Flash Memory Specs*.

		13. Page14: **Remove Typ value and add Max value of ADC Conversion Frequency;** Add TOE, INL, DNL test condition V_{VCC}=V_{VCCA}=5V; V_{REFH}=5V; Add new specs ADC sampling capacitance, ADC sampling switch resistance, Build-in 2.5V ADC Reference in *11.6 ADC Specs* 14. Page14: **Modify Min value of CMP Hysteresis, when V_{HYS} = 25mV, from 15 to 10, when V_{HYS} = 50mV, min value from 35 to 30; change Min value of CMP Propagation Delay from 15 to 10** in *11.7 CMP Specs*. 15. Page15: Correct test condition of Clock Rise Time from 10%-90% to 30%-70% and Clock Fall Time from 90%-10% to 70%-30% in *11.8 I2C Specs* 16. Page16: Modify Peripheral Frequency to Internal Peripheral Frequency; Move 8.3 from the Test Conditions to min value of SPI Peripheral Clock Period; Add Note 7 for PCS to SCK Delay and SCK to PCS Delay; Change test condition Controller to master; Change test condition peripheral to slave in *11.11 SPI Specs*. 17. Page19: Modify the data flash sectors number of B16/B14/B12 in *Table 2 Data Flash Memory Size* from 30 to 32. Update the description from “The data flash contains multiple sectors which can be erased individually.” to “The data flash contains 32 sectors which can be erased individually, and the last two sectors are only for SHE module.” in *12.4 Data Flash*. 18. Page20: delete the LIN update method in *12.6 Boot ROM*. 19. Page21: Add ADC input network and equivalent impedance calculation formula; Update the description from “This chip integrates two ADCs, each supporting 16 external channels (32ch).” to “This chip integrates two ADCs, each supporting 16 external channels (32ch totally).” in *12.13 ADC*. 20. Page27-28: Add Recommended PCB Layout in *13.2 LQFP10x10-64 Package Outline Drawing* and *13.3 LQFP7x7-48 Package Outline Drawing*

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