SY2A54560

Mono Audio Digital to Analog Converter

General Description

The SY2A54560 is a 32-bit high performance mono audio DAC with low distortion and low idle noise. It is comprised of a multibit sigma delta modulator, high performance digital interpolation filters, and continuous-time differential current steering DAC and IV converter. It supports a wide range of PCM sample rates from 8 kHz to 192 kHz and a 16, 20, 24, and 32-bit width digital audio input on the audio interface, which are suitable for high-resolution audio playback. The audio interface supports I²S, Left Justified, and Right Justified data formats.

The SY2A54560 offers two control modes: I²C interface and hardware. In I²C mode, all functions can be programmed by registers, while in hardware mode, only the audio format and de-emphasis function can be programmed through the two control pins.

The device is available in a TSSOP-24 package.

Features

- AEC-Q100 Grade 1 Qualified
- Power supply
  - 5 V for Analog and 3.3 V for Digital
- Large Differential Voltage Output
  - 8.6 V_{PP} at 0dBFS (default)
- Excellent Audio performance
  - –90dB THD+N at 0dBFS
  - 115 dB A-weighted SNR
  - 115 dB Dynamic Range
- Low power consumption
  - Power-Save Mode: 6.5uA AVDD quiescent current
  - Play mode: 1.7mA AVDD quiescent current at fs=48kHz MCLK=512*fs
- Flexible Audio Interface
  - Input Sampling Rates: 8 kHz to 192 kHz
  - I/F Format: I²S, Left/Right Justified
  - Input Data Length: 16, 20, 24, 32 Bits
- Flexible Mode Control
  - I²C mode with four Peripheral Addresses
  - Hardware Mode
- Comprehensive Error Detection and Protection
  - Zero Detection
  - Clock Error Detection
  - Supply Undervoltage Detection
  - Analog Mute Triggered By Detected Faults
- Output Current Limit Protection

Applications

- Car Audio
- Home Audio

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Typical Application

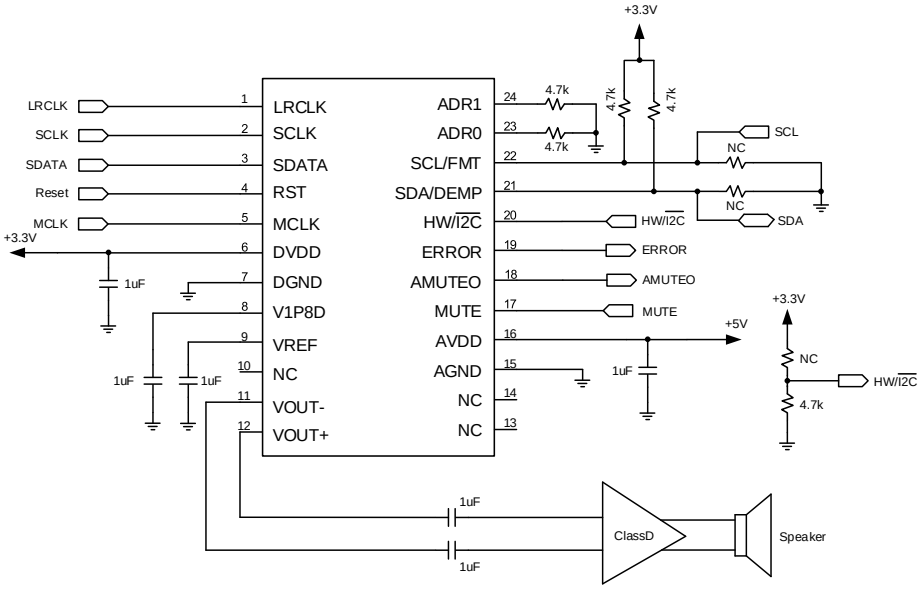

Figure 1. Typical Application Circuit

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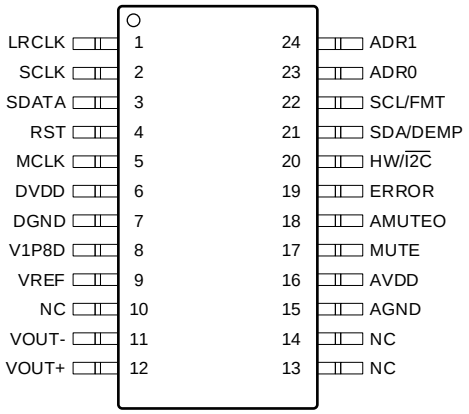
Ordering Information

Ordering Part Number	Package Type	Top Mark
SY2A54560HNP	TSSOP24 RoHS Compliant and Halogen Free	***GEGxyz***

Device code: GEG

x=year code, y=week code, z= lot number code

Pinout (Top View)



Pin Number	Pin Name	Type (Note 1)	Termination (Note 2)	Description
1	LRCLK	DI	Pull down	Serial audio frame clock.
2	SCLK	DI	Pull down	Serial audio clock.
3	SDATA	DI	Pull down	Serial audio data.
4	RST	DI	Pull down	Reset pin, active low.
5	MCLK	DI	Pull down	System clock input.
6	DVDD	P		Digital power supply.
7	DGND	P		Digital ground.
8	V1P8D	P		1.8V LDO decoupling pin. Connect a 1μF capacitor between this pin and GND.
9	VREF	P		Reference voltage decoupling pin.
10	NC			Not connected.
11	VOUT-	AO		DAC negative analog output.
12	VOUT+	AO		DAC positive analog output.
13	NC			Not connected.
14	NC			Not connected.
15	AGND	P		Analog ground.
16	AVDD	P		Analog power supply.
17	MUTE	DI	Pull down	Mute pin input, active low.
18	AMUTEO	DO		Analog mute control output, active low.
19	ERROR	DO		Error pin.
20	HW/ $\overline{\text{I2C}}$	DI	Pull up	Control mode selection. Pull low: I²C mode. Pull high: hardware mode.
21	SDA/DEMP	DIO (Note 3)	Pull up (Note 4)	I²C serial control data. De-emphasis control for hardware control mode.
22	SCL/FMT	DI	Pull up (Note 4)	I²C serial clock. Format select for hardware control mode.
23	ADR0	DI	Pull down	I²C slave address selection 0.
24	ADR1	DI	Pull down	I²C slave address selection 1.

Note 1: TYPE: A =analog; D =digital; P =power/ground/decoupling; I =input; O =output; IO=in/out.

Note 2: All pull-ups and pull-downs are weak.

Note 3: For hardware mode, pin 21 is digital input.

Note 4: For hardware mode, the terminations of pin 21 and pin 22 are pulled down.

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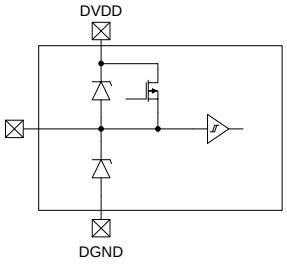
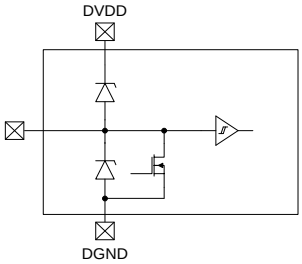
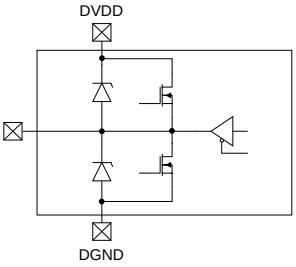
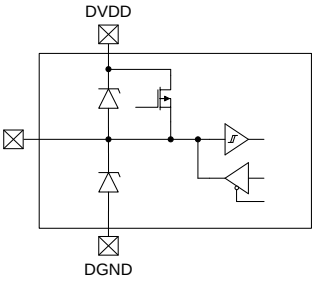
Digital IO Equivalent Circuits

Pin No.	Pin Name	Equivalent Circuit	IO Type
20 22	HW/ $\overline{\text{I2C}}$ SCL		Input with pull-up (87kΩ)
1 2 3 4 5 17 21 22 23 24	LRCLK SCLK SDATA RST MCLK MUTE DEMP FMT ADR0 ADR1		Input with pull-down (87kΩ)
18 19	AMUTEO ERROR		Push-pull output
21	SDA		Bidirectional IO with pull-up (87kΩ)

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Block Diagram

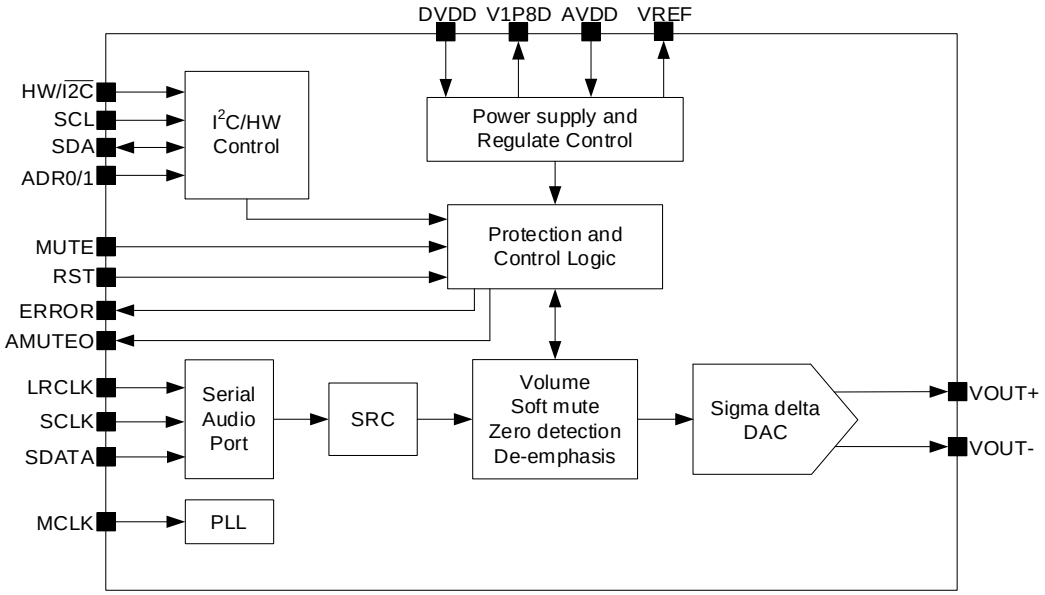

Figure 2. Block Diagram

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Absolute Maximum Ratings (Note 1)

Parameter	Min	Typ	Max	Unit
AVDD, Analog Supply Voltage	-0.3		6.5	V
DVDD, Digital Supply Voltage	-0.3		4	V
Digital Input (SDA, SCL, MCLK, LRCLK, SCLK, SDATA, MUTE, RST, ADR0, ADR1, HW/ $\overline{I2C}$)	-0.3		DVDD+0.3	V
Digital Output (ERROR, AMUTEO)	-0.3		5.5	V
Analog Output (VOUT+, VOUT-)	-0.3		AVDD+0.3	V
Junction Temperature Range	-40		150	°C
Storage Temperature Range	-55		150	°C

Recommended Operating Conditions

Parameter(Note 3)	Min	Typ	Max	Unit
AVDD, Analog Supply Voltage			5	V
DVDD, Digital Supply Voltage			3.3	V
Operating Ambient Temperature Range	-40		125	°C

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Electrical Characteristics

T_A=-40℃ to 125℃, AVDD=5V, DVDD=3.3V, f_S=48kHz, MCLK=512f_S, 24-bit data, sampling mode=auto, filter:20Hz~20kHz, typical values are tested at T_A=25℃, unless otherwise specified (Note 4)

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
Data Format	Sampling Frequency	f_S		8		192	kHz
	Master Clock Frequency	MCLK		2.048		36.864	MHz
Input Logic	Input Logic Level, High	V_{IH}	SCLK, LRCLK, SDATA, MCLK, MUTE, RST,SDA,SCL,ADR1,ADR0, HW/ $\overline{I2C}$	2.4			V
	Input Logic Level, Low	V_{IL}	SCLK, LRCLK, SDATA, MCLK, MUTE, RST,SDA,SCL,ADR1,ADR0, HW/ $\overline{I2C}$			0.8	V
Power Supply	Analog Supply Voltage	AVDD		4.5	5	5.5	V
	Digital Supply Voltage	DVDD		3	3.3	3.6	V
	Regulator Output for Digital Core	V1P8D		1.62	1.8	1.98	V
	Reference Voltage for DAC	V_{REF}	Default	1.02	1.1	1.18	V
	Analog Quiescent Current (Note 5)	I_{AVDD}	fs=8kHz, MCLK=512fs, Play mode with zero input		1.54		mA
			fs=48kHz, MCLK=128fs, Play mode with zero input		1.55		
			fs=48kHz, MCLK=512fs, Play mode with zero input		1.69		
			fs=192kHz, MCLK=128fs, Play mode with zero input		1.70		
			fs=48kHz, MCLK=512fs, RESET=high, MUTE=low		1.53		
			fs=48kHz, MCLK=512fs, RESET=low, MUTE=high		6.5		μA
			fs=48kHz, MCLK=512fs, shutdown (Note 6)		6.5		
			Full Power-down (Note 7)		6.5		
	Digital Quiescent Current (Note 5)	I_{DVDD}	fs=8kHz, MCLK=512fs, Play mode with zero input		0.43		mA
			fs=48kHz, MCLK=128fs, Play mode with zero input		0.91		
			fs=48kHz, MCLK=512fs, Play mode with zero input		1.84		
			fs=192kHz, MCLK=128fs, Play mode with zero input		3.17		
			fs=48kHz, MCLK=512fs, RESET=high, MUTE=low		0.46		
			fs=48kHz, MCLK=512fs, RESET=low, MUTE=high		0.40		
			fs=48kHz, MCLK=512fs, shutdown (Note 6)		0.43		
			Full Power-down (Note 7)		120		μA
DAC Output	Output Voltage		Default, differential		8.6		V_{pp}
	Gain Error					4.7	%FSR
	Load Impedance (Note 8)			1			kΩ
Digital Filter Performance with Sharp Roll-off	Passband (single, dual)		Except MCLK = 128 fs and 192 fs			0.454	fs
			MCLK = 128 fs and 192 fs			0.432	
	Passband (quad)					0.432	
	Stop Band (single, dual)		Except MCLK = 128 fs and 192 fs	0.546			
			MCLK = 128 fs and 192 fs	0.569			

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	Stop Band (quad)			0.569			
	Passband Ripple		< 0.454 × fs, 0.432 × fs			±0.0018	dB
	Stop Band Attenuation		> 0.546 × fs, 0.569 × fs	-75			dB
Digital Filter Performance with Slow Roll-off	Passband					0.328	fs
	Stop Band			0.673			
	Passband Ripple		< 0.328 × fs			±0.001	dB
	Stop Band Attenuation		> 0.673 × fs	-112			dB
Digital Filter Performance (Note 5)	Group Delay Time (single, dual)		Except MCLK = 128 fs and 192 fs		59/fs		sec
			MCLK = 128 fs and 192 fs		32/fs		sec
	Group Delay Time (quad)				32/fs		sec
	De-emphasis Error				±0.1		dB
Performance (Note 5)	Total Harmonics Distortion Pulse Noise	THD+N	fs=48kHz, MCLK=128fs, input 1kHz 0dBFS		0.0028		%
			fs=48kHz, MCLK=512fs, input 1kHz 0dBFS		0.004		
			fs=96kHz, MCLK=128fs, input 1kHz 0dBFS		0.0031		
			fs=192kHz, MCLK=128fs, input 1kHz 0dBFS		0.004		
	Signal to Noise Ratio	SNR	fs=48kHz, MCLK=128fs, A-weighted		115.8		dB
			fs=48kHz, MCLK=512fs, A-weighted		116.3		
			fs=96kHz, MCLK=128fs, A-weighted		116.4		
			fs=192kHz, MCLK=128fs, A-weighted		116.2		dB
	Dynamic Range	DR	fs=48kHz, MCLK=128fs, A-weighted		116.0		dB
			fs=48kHz, MCLK=512fs, A-weighted		116.2		
			fs=96kHz, MCLK=128fs, A-weighted		116.2		
			fs=192kHz, MCLK=128fs, A-weighted		116.3		
	Output Noise	V_n	Play mode, zero input, A-weighted		5.3		μVrms
			Mute mode, zero input, A-weighted		5		
Protection	AVDD V_{UVLO_FALL}	UVP	AVDD Falling to enter UVLO	3.8	4		V
	AVDD V_{UVLO_RISE}		AVDD Rising to exit UVLO		4.25	4.45	
	DVDD V_{UVLO_FALL}		DVDD Falling to enter UVLO	2.2	2.5		
	DVDD V_{UVLO_RISE}		DVDD Rising to exit UVLO		2.7	2.95	
	Output Current Limit	OCL	Default		40		mA

Note 1: Stresses beyond the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective four layers thermal conductivity test board of JEDEC 51-7.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 1: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \approx T_J$ = 25°C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Typical value tested on demonstration board is guaranteed by design.

Note 6: Shutdown: Write "0" to bit 7 of register 0x11 and write "1" to bit 4 of register 0x12.

Note 7: Full Power-down: Enter shutdown using registers 0x11 and 0x12 and remove I2S.

Note 8: The load lower than this value will result in derated of audio performance and reduced reliability.

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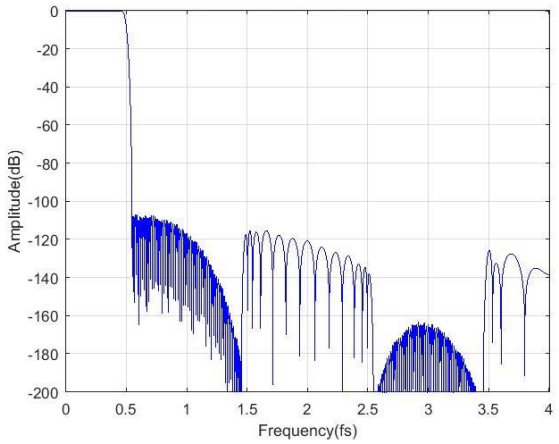
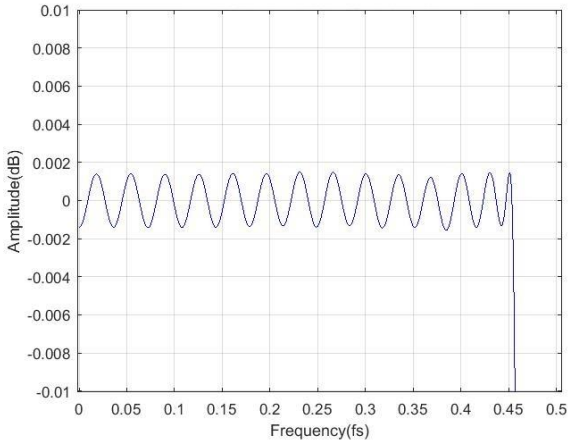
Typical Performance Characteristics

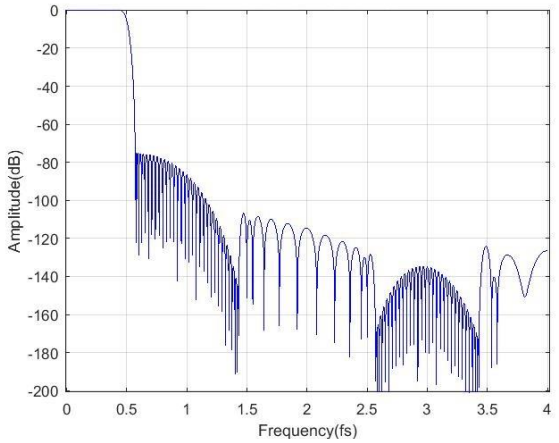
Digital Filter



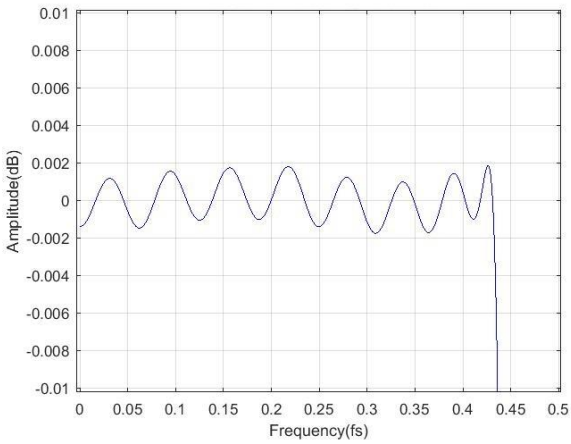
TPC F1. Frequency Response
Sharp roll-off, single and dual rate except MCLK = 128/192fs



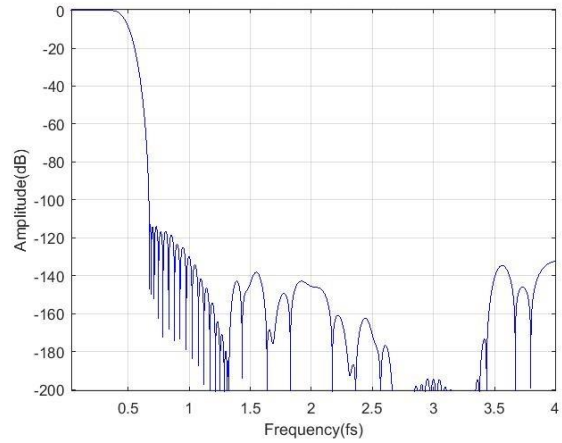
TPC F2. Passband Frequency Response
Sharp roll-off, single and dual rate except MCLK = 128/192fs



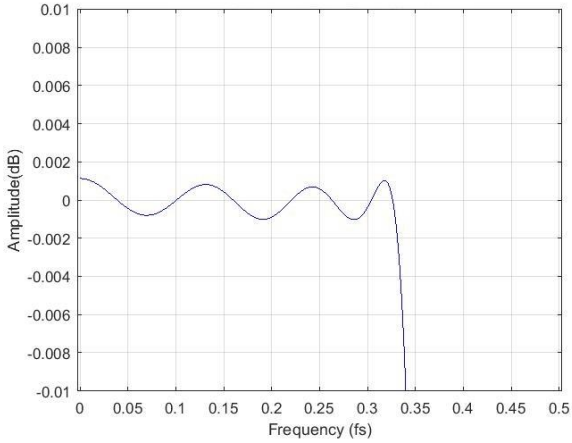
TPC F3. Frequency Response
Sharp roll-off, single and dual rate at MCLK=128/192fs and quad rate



TPC F4. Passband Frequency Response
Sharp roll-off, single and dual rate at MCLK=128/192fs and quad rate



TPC F5. Frequency Response
Slow roll-off



TPC F6. Passband Frequency Response
Slow roll-off

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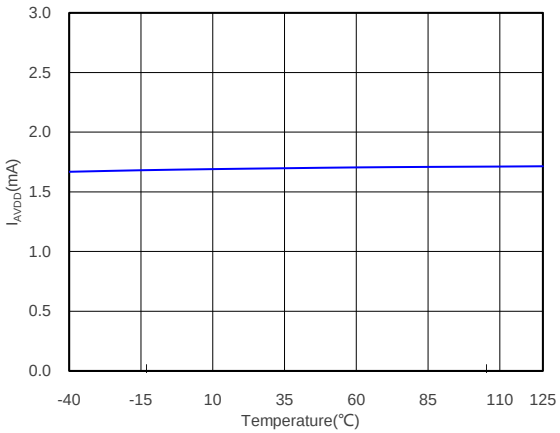
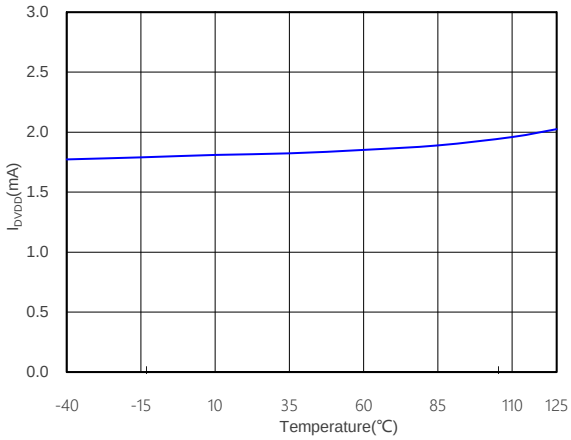
Dynamic Performance

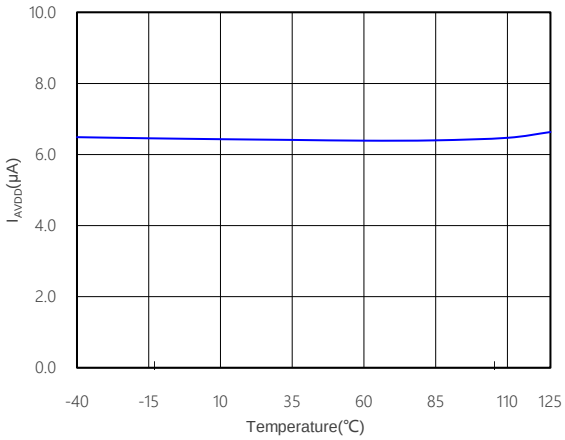
T_A = 25°C, AVDD = 5V, DVDD = 3.3V, f_S = 48 kHz, MCLK = 512f_S, 24-bit data, 0dBFS input, and sampling mode = auto, sharp roll-off, unless otherwise noted.



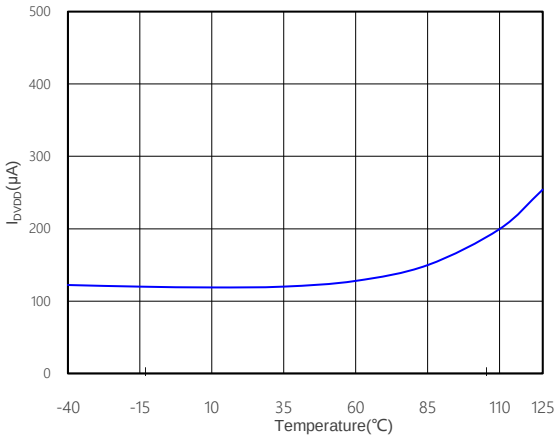
TPC F7. AVDD Quiescent Current vs Temperature
Normal operation mode



TPC F8. DVDD Quiescent Current vs Temperature
Normal operation mode



TPC F9. AVDD Quiescent Current vs Temperature
Full Power-down mode



TPC F10. DVDD Quiescent Current vs Temperature
Full Power-down mode

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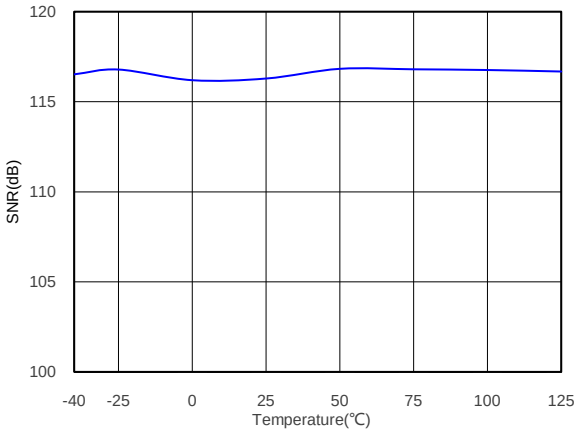
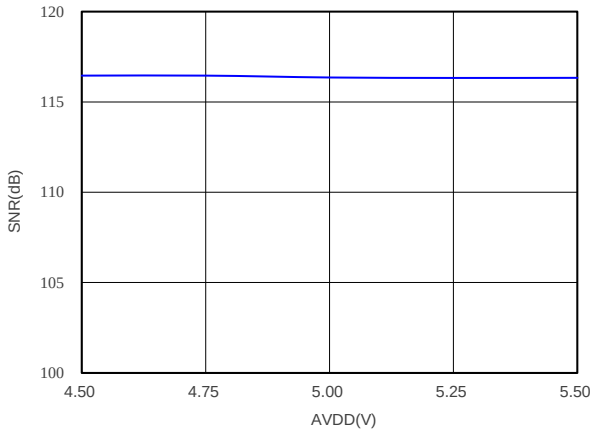
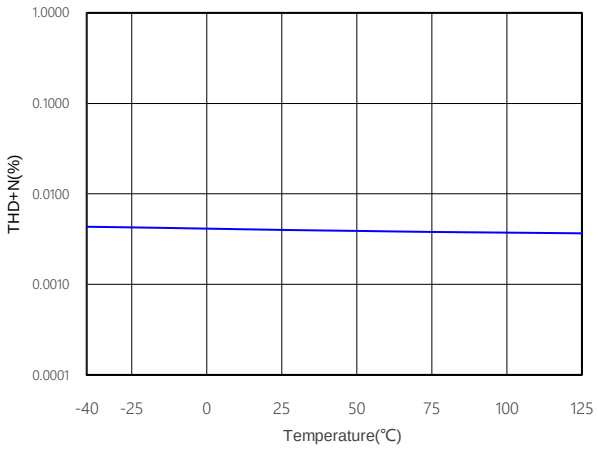


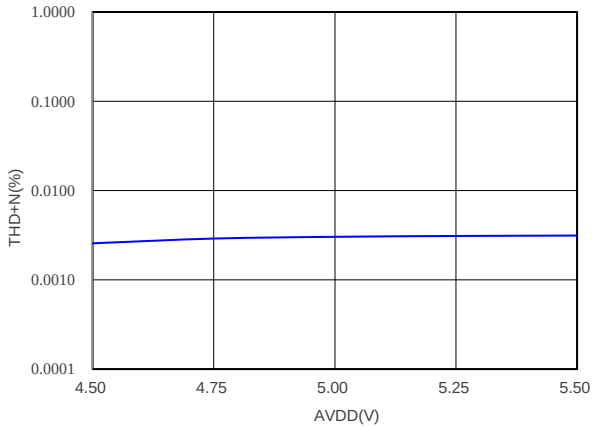
TPC F11. SNR vs Temperature
A-weighting



TPC F12. SNR vs AVDD Supply
A-weighting



TPC F13. THD+N vs Temperature



TPC F14. THD+N vs AVDD Supply

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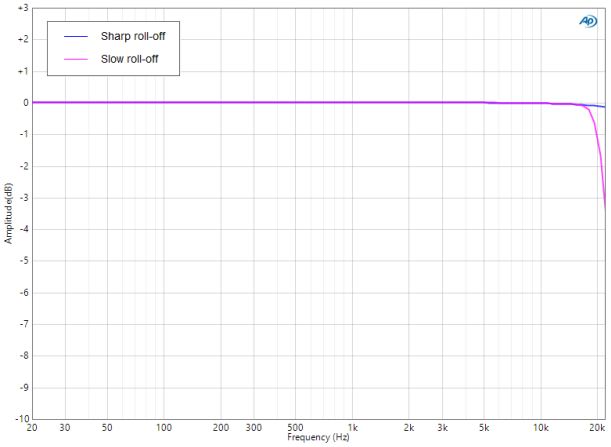
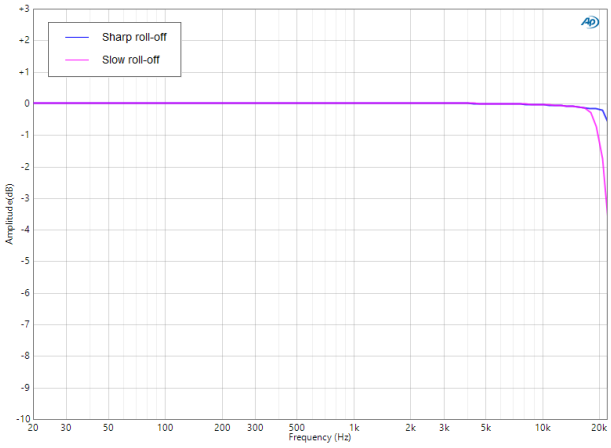
DAC Output Performance

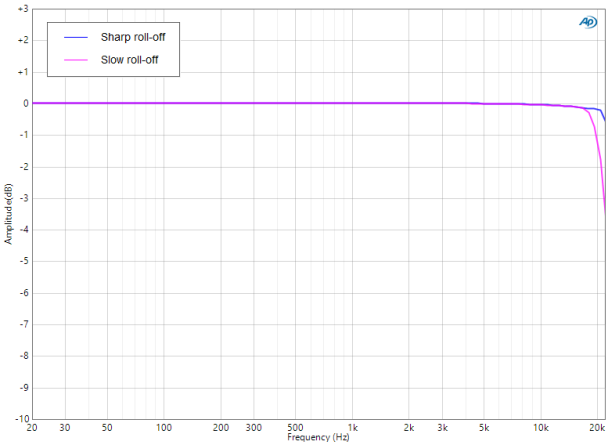
T_A = 25°C, AVDD = 5V, DVDD = 3.3V, f_S = 48 kHz, MCLK = 512f_S, 24-bit data, 0dBFS input, and sampling mode = auto, sharp roll-off, unless otherwise noted.



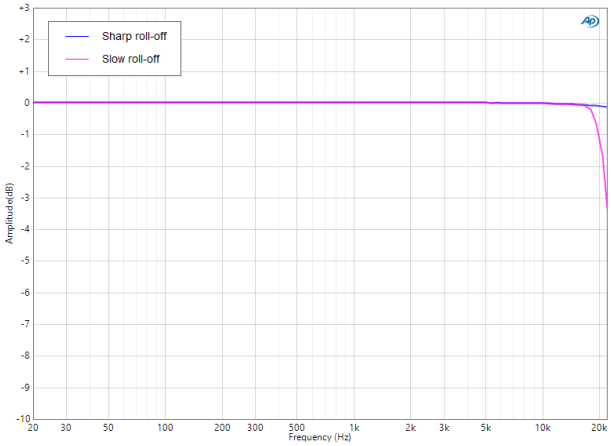
TPC F15. Frequency Response
fs=48kHz, MCLK=512fs, auto



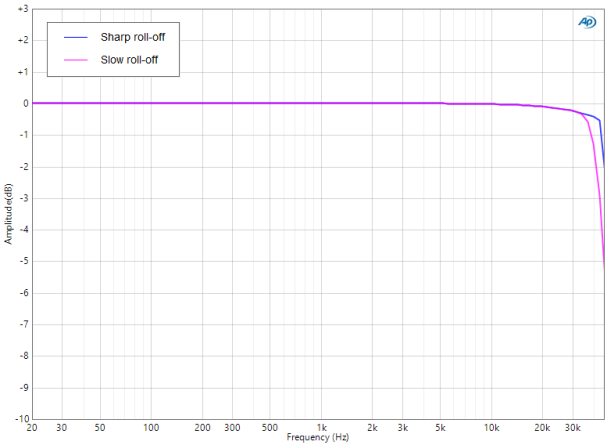
TPC F16. Frequency Response
fs=48kHz, MCLK=128fs, single rate



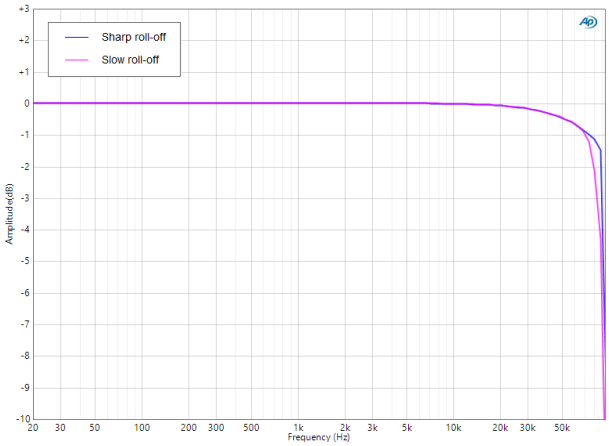
TPC F17. Frequency Response
fs=48kHz, MCLK=192fs, single rate



TPC F18. Frequency Response
fs=48kHz, MCLK=512fs, single rate



TPC F19. Frequency Response
fs=96kHz, MCLK=128fs, dual rate



TPC F20. Frequency Response
fs=192kHz, MCLK=128fs, quad rate

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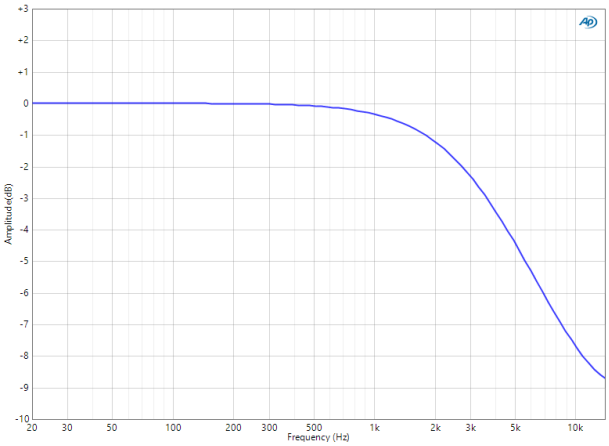
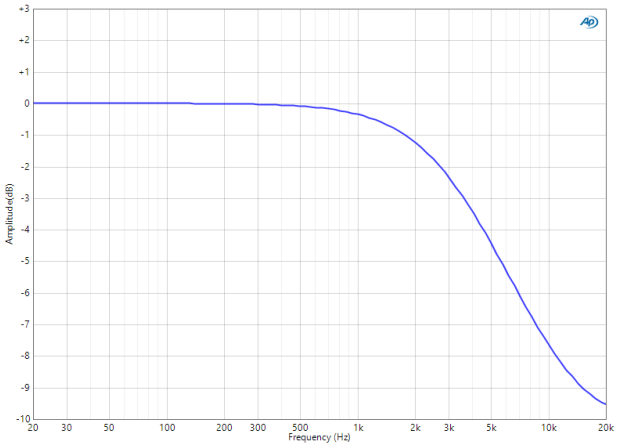
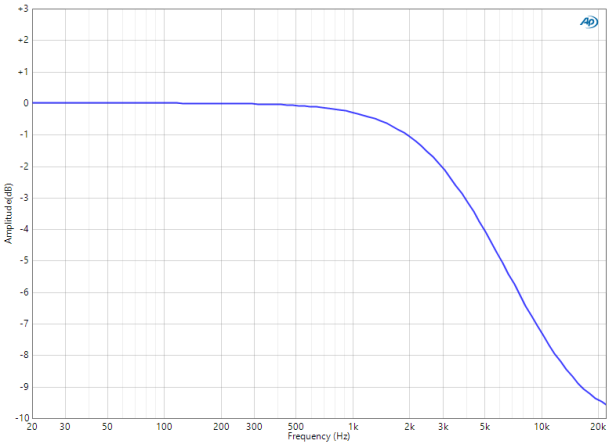


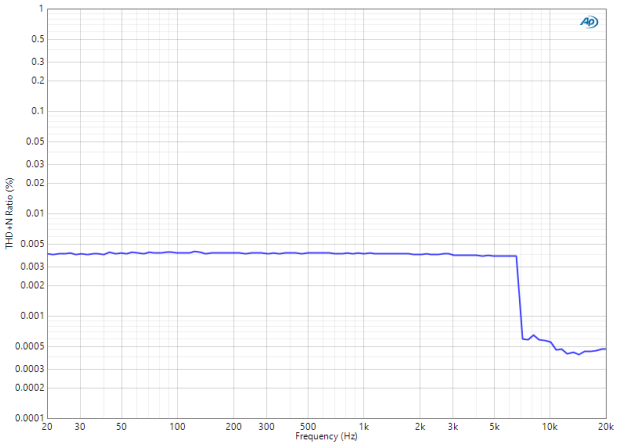
TPC F21. 32kHz De-emphasis Frequency Response
fs=32kHz



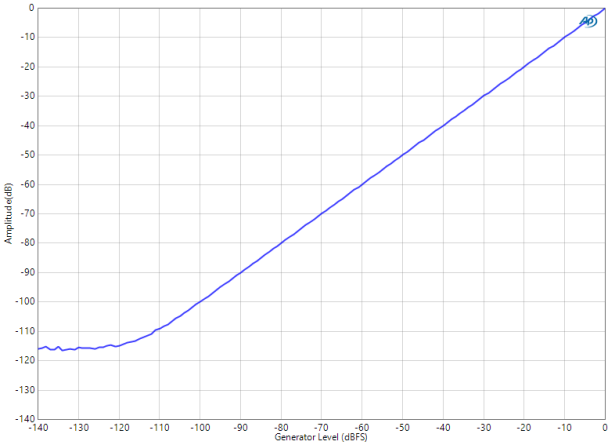
TPC F22. 44.1kHz De-emphasis Frequency Response
fs=44.1kHz



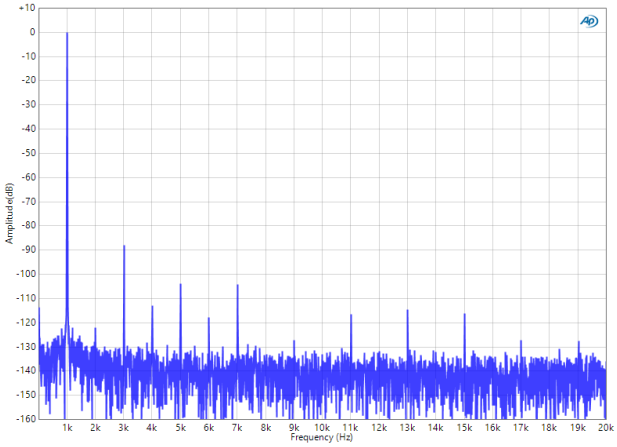
TPC F23. 48kHz De-emphasis Frequency Response
fs=48kHz



TPC F24. THD+N vs Frequency Sweep
fs=48kHz



TPC F25. Linearity
0dBFS to -140dBFS sweep at 1kHz, filter:20Hz ~ 20kHz, A-weighting



TPC F26. FFT Spectrum
0dBFS input at 1kHz, filter:20Hz ~ 20kHz

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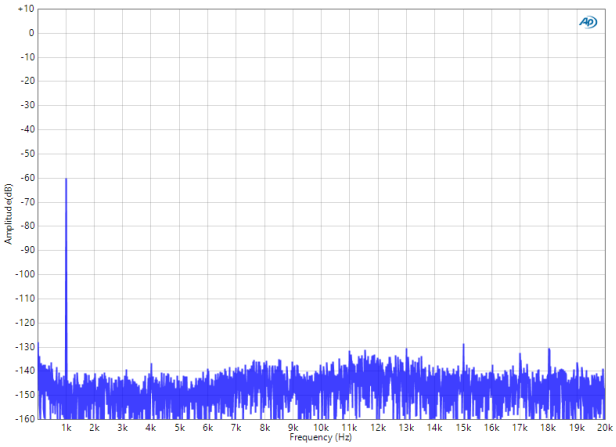
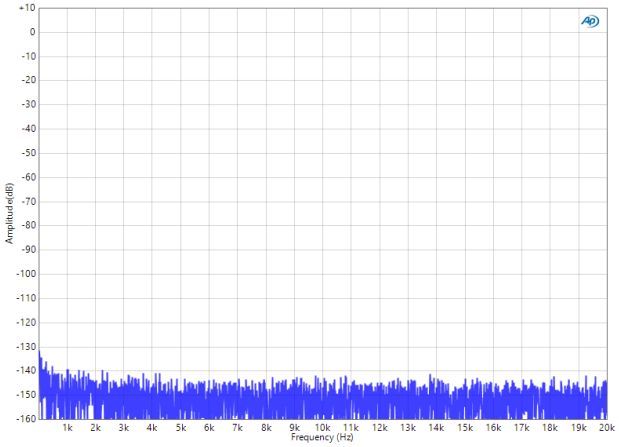


TPC F27. FFT Spectrum
-60dBFS input at 1kHz, filter:20Hz ~ 20kHz



TPC F28. FFT Spectrum
Zero input, filter:20Hz ~ 20kHz

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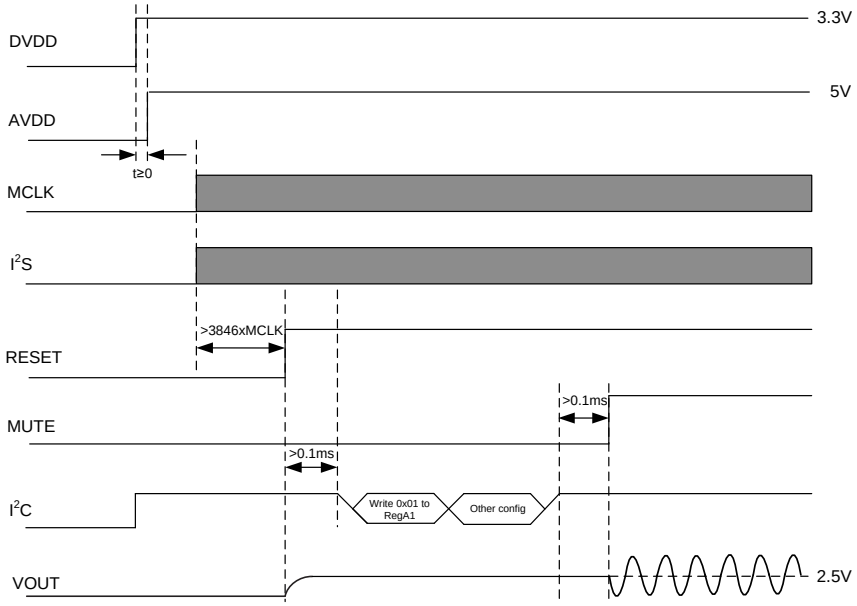
Recommended Power Up Timing

The recommended power up timing for I²C mode is shown in figure 3:

1) Provide 3.3V to DVDD and 5V AVDD.
2) Set RST=0, provide MCLK and I2S (LRCLK, SCLK, and SDATA), then set RST=1 after at least 3846 MCLK cycles.
3) Configure the SY2A54560 using I²C.
4) Set MUTE=1.

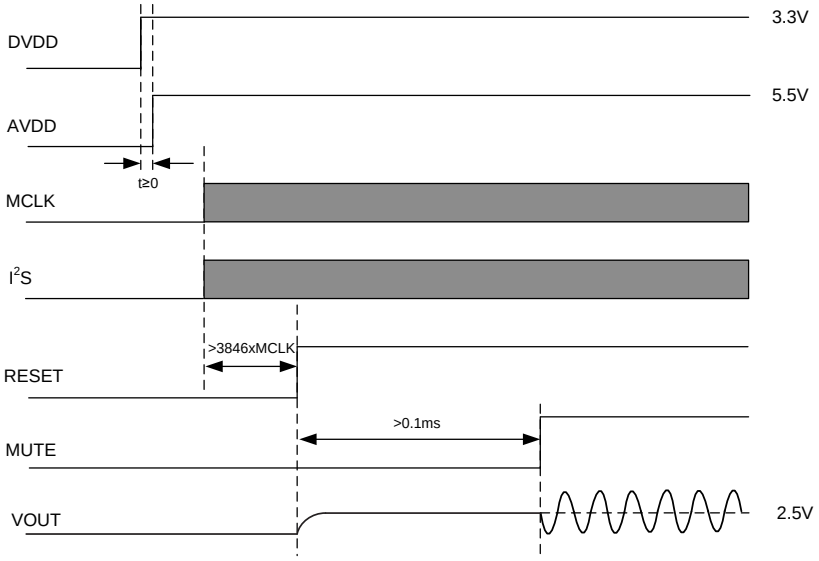


Note: The device uses an internal reset signal independent of the external RESET. Once the power supply rails are within the operating range, the internal reset signal will be released after 3846 MCLK cycles.

Figure 3. Recommended Power Up Timing for I²C mode

The recommended power up timing for hardware mode is shown in figure 4:

1) Provide 3.3V to DVDD and 5V to AVDD.
2) Set RST=0, provide MCLK and I2S (LRCLK, SCLK, and SDATA), then set RST=1 after at least 3846 MCLK cycles.
3) Set MUTE=1.



Note: The device uses an internal reset signal independent of the external RESET. Once the power supply rails are within the operating range, the internal reset signal will be released after 3846 MCLK cycles.

Figure 4. Recommended Power Up Timing for Hardware Mode

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Recommended Power Down Timing

The recommended power down timing is shown in figure 5:

1) The device is in normal operation.
2) Pull MUTE low.
3) Wait at least 1ms.
4) Pull RST low, stop MCLK, and ramp down DVDD and AVDD. There is no sequence requirement between DVDD and AVDD when ramping down.

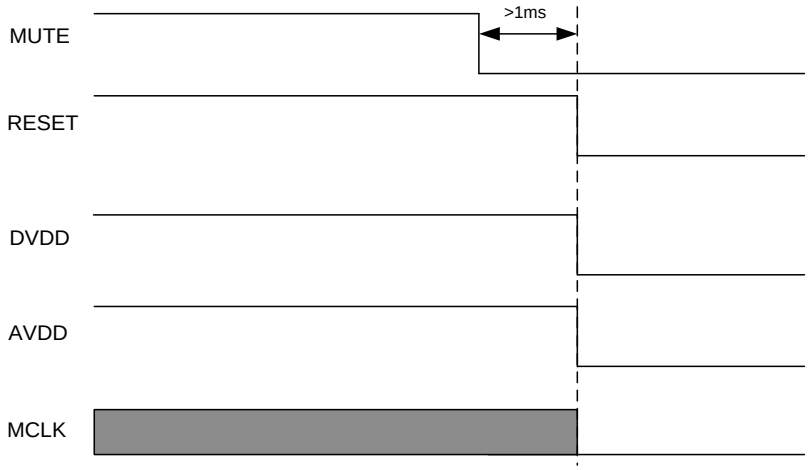

Figure 5. Recommended Power Down Timing

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Detailed Description and Theory of Operation

Analog Outputs

The analog outputs, VOUT+ and VOUT-, are biased to +2.5V. The differential output voltage is $8.6V_{PP}$ at 0dBFS input by default, which is related to VREF voltage.

Voltage Reference VREF

The SY2A54560 includes a VREF pin for the reference voltage of DAC output. VREF is 1.1V by default, which can be programmed by register 0x86. A 1μF capacitor is recommended to be placed between the VREF pin and ground.

System Clock Input

The SY2A54560 requires an external MCLK input. The MCLK should not be lower than 2.048MHz and higher than 36.864MHz, and its frequency should be selected as an integer coefficient of the sampling rate, fs. The coefficients used for DAC operation should be selected in the range from $128xf_S$ to $1152xf_S$.

Reset Operation

The SY2A54560 has an RST pin. When it is set to low, the whole chip will enter a device reset and power down state. VOUT is forced to the AGND level. When it is set to high, the device starts operation. After 1.54ms, the SY2A54560 will enter normal operation mode and DAC outputs become active. Figure 6 shows the timing of the external reset.

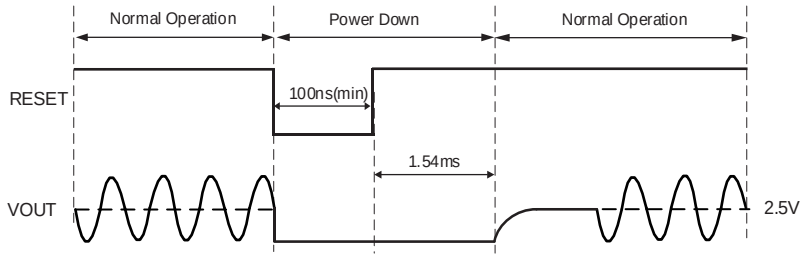

Figure 6. External Reset Timing

Error

The SY2A54560 has an error output pin, which is used to signal a zero detect result by default (see details below). The ERROR pin can also report other errors enabled using register 0x81, including clock error, AVDD undervoltage, DVDD undervoltage, and SRAM ECC error. The polarity of the flag can be set using bit 0 of register 0x16.

Zero Detect

If the input data remains at '0' for 21ms, the zero input signal state is detected. In such event, the ERROR pin will be set to high by default. The ERROR pin is set to low immediately if the input data read '1'. Zero data detection is supported for 16/20/24-bit data width only.

Clock Error Detection

The SY2A54560 has a clock error detection function, which includes MCLK error detection, SCLK error detection, and MCLK stop error detection. The clock detection result can be reported in register 0xA2 and the Error pin, which will be latched unless register 0xA1 is written 0x01. Each error can be enabled or disabled by register 0x82.

MCLK Error Detection

The clock error detection block will count the pulses of MCLK in each frame of LRCLK. If Cln≠Cln+1 or Cln+1≠Cln+2, MCLK error is reported.

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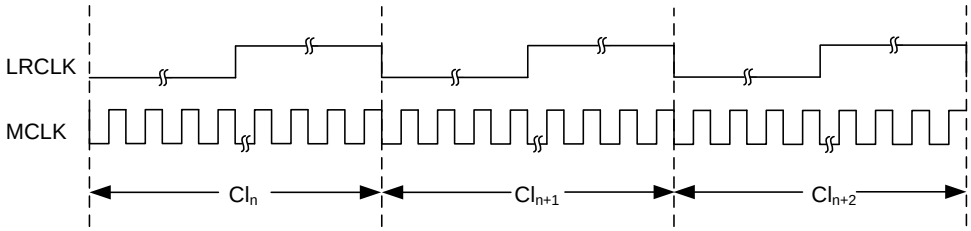

Figure 7. MCLK Error Detection

SCLK Error Detection

The clock error detection block will count the pulses of SCLK in each frame of LRCLK. If Csn≠Csn+1 or Csn+1≠Csn+2, SCLK error is reported.

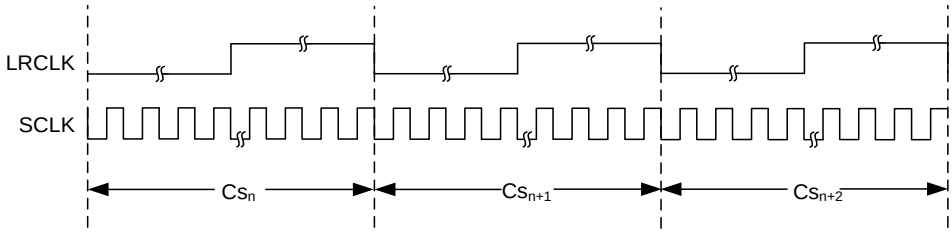

Figure 8. SCLK Error Detection

MCLK Stop Error Detection

There is a window in the clock error detection block for counting MCLK, If the counted value is 0, the logic will report a MCLK stop error.

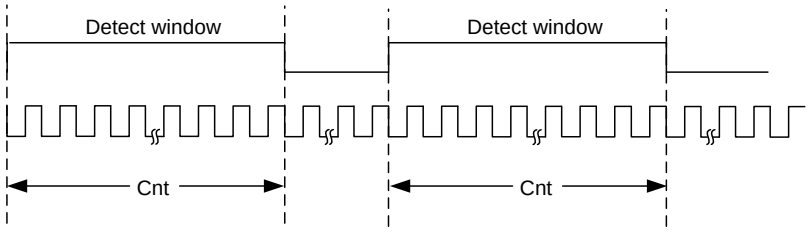

Figure 9. MCLK Stop Error Detection

Undervoltage Detection

The SY2A54560 has AVDD and DVDD undervoltage detection comparators. The undervoltage thresholds of AVDD and DVDD are 4V and 2.5V, respectively. The register 0xA2 reports the undervoltage fault when the power supply is lower than the corresponding threshold. Bit 4 of register 0x81 can enable or disable the ERROR pin to report undervoltage faults. Furthermore, the DAC output will be forced to 2.5V when the threshold is triggered if the AMUTE function of undervoltage is enabled in register 0x82.

Auto-correction of SRAM

The ECC (Error Correcting Code) is an algorithm developed based on the Single Error Correct-Double Error Detect (SECDED) algorithm using Hamming code. The ECC provides an automatic error detection and correction circuit. In the design, six parity bits are added to the data word upon a write to memory. With such parity bits, both single and double data errors can be detected when reading the word from memory. Single bit data error can be corrected while double bit error cannot. The double bit error can be reported in register 0xA2 and ERROR pin.

Output Current Limit

The SY2A54560 has an output stage current limit function. The output stage current is sensed and compared with the IREF limit (40mA default). The output current will be limited to IREF. With this function, if the output is shorted by mistake, the

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output current can be limited to protect the DAC output stage. The limited output current can be set by register 0x86. The output stage current limit function can be enabled using register 0x84, which is disabled by default.

Volume Control

The SY2A54560 has a volume control block. The volume step is configured using register 0x16.. The step is 0.5dB by default. The volume can be calculated using the following formula:

volume (dB) = step × (M– 255),

When step=0.5dB, M>128. When step=1dB, M>154. M is the decimal value in register 0x18. Table 1 shows the volume table.

Table 1. Volume table

Register 0x18 Value		Volume	
HEX	Decimal	Step=0.5dB	Step=1dB
FF	255	0 dB(default)	0 dB(default)
FE	254	–0.5 dB	-1 dB
FD	253	–1.0 dB	-2 dB
...	...	...	...
9C	156	-49.5 dB	-99 dB
9B	155	–50.0 dB	-100 dB
9A	154	–50.5 dB	Mute
...	...	...	...
82	130	–62.5 dB	Mute
81	129	–63.0 dB	Mute
80	128	Mute	Mute
...	...	...	...
00	0	Mute	Mute

MUTE Control

The SY2A54560 has a MUTE control pin. When the MUTE pin is set to low, the DAC output will be forced to 2.5V. The SY2A54560 also has a digital mute controlled by register 0x14. A fade process is implemented when the digital mute is enabled or disabled, with which improves the audio user experience. The fade process volume can be configured using register 0x18. The fade time can be calculated using the formula below:

Table 2. The Formula for Fade Time Calculating

Sampling Mode	Fade Time	
	Volume step=0.5dB	Volume step =1dB
Single rate	(255-129)/fs *4	(255-155)/fs *8
Dual rate	(255-129)/fs *8	(255-155)/fs *16
Quad rate	(255-129)/fs *16	(255-155)/fs *32

AMUTEO is the status output pin of the internal analog mute circuit. The following conditions can activate the analog mute control circuit: pulling down the MUTE pin, MCLK halt, asynchronous detect, zero detect, DAC disable command, AVDD and DVDD undervoltage. The behavior can be configured by register 0x10 and 0x82. AMUTEO low indicates the analog mute control circuit is active, and in this state the DAC output will be forced to 2.5V.

MODE Control

The SY2A54560 has two control modes which can be configured by the HW/ $\overline{\text{I2C}}$ pin. When the HW/ $\overline{\text{I2C}}$ pin is pulled low, I²C mode is selected. When the HW/ $\overline{\text{I2C}}$ is pulled high, hardware mode is selected. The HW/ $\overline{\text{I2C}}$ pin has an internal 87kΩ pullup to DVDD.

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I²C Control

When the HW/ $\overline{\text{I2C}}$ pin is pulled low, I²C mode is enabled. In this mode, the audio interface format can be selected by register 0x11, which includes I²S, Left-Justified, and Right-Justified. In I²C mode, digital de-emphasis is controlled by register 0x16, which can set different sampling rates, including 32 kHz, 44.1 kHz, and 48 kHz.

The ADR1 pin and ADR0 pin define the four I²C address. The following table shows the detailed device address configurations.

Table 3. Peripheral Address

I²C Peripheral Address		ADR1		
		Pull-down ('L')	Pull-up ('H')	No PD/PU (Default: 'L')
ADR0	Pull-down ('L')	0x98	0x9C	0x98
	Pull-up ('H')	0x9A	0x9E	0x9A

I²C Communication Protocol

The SY2A54560 has a bidirectional I²C interface which is compatible with the I²C BUS protocol and supports both 100 kHz and 400 kHz data transfer rates for writing and reading operations. The device does not support a multi-controller BUS or wait state insertion. The I²C control is used to program the registers and to read device status. The following figures show the detailed write and read transfer operations.

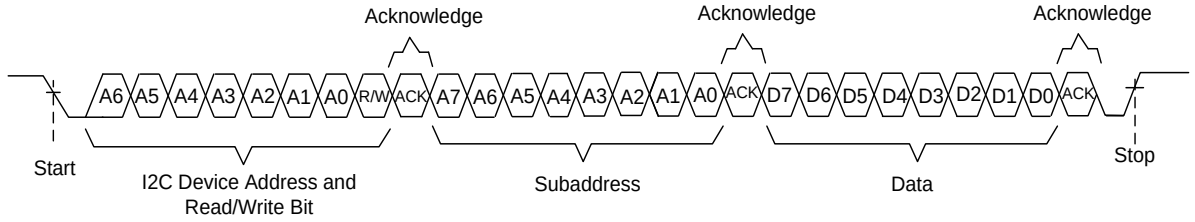

Figure 10. Write Transfer

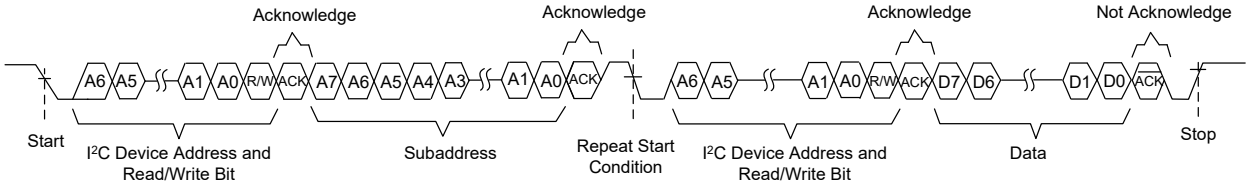

Figure 11. Read Transfer

I²C Timing

Parameter	Symbol	Conditions	Min	Max	Unit
SCL Frequency	f_{SCL}	No wait states		400	kHz
SCL and SDA Rise Time	t_r			300	ns
SCL and SDA Fall Time	t_f			300	ns
SCL High Duration Time	t_{WH}		0.6		μs
SCL Low Duration Time	t_{WL}		1.3		μs
SDA to SCL Setup Time	t_{S1}		100		ns
SCL to SDA Hold Time	t_{h1}	(Note 1)	0		ns
Free Time between Stop and Start Condition	t_{buf}		1.3		μs
SCL to Start Condition	t_{S2}		0.6		μs
Start Condition to SCL Hold Time	t_{h2}		0.6		μs
SCL to Stop Condition	t_{S3}		0.6		μs
Load Capacitor for Each Bus Line	C_{Load}			400	pF

Note 1: A device must internally provide a hold time of at least t_f for the SDA signal to bridge the undefined region of the falling edge of SCL.

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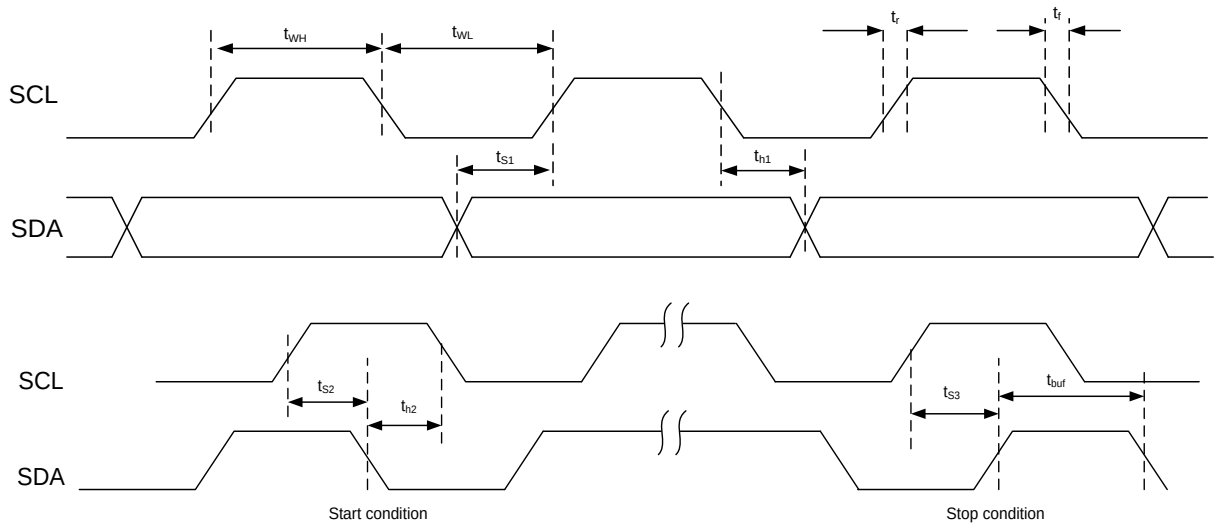

Figure 12. I²C Timing Diagram

Hardware Control

When the HW/ $\overline{\text{I2C}}$ pin is pulled high, hardware mode is enabled. In this mode, the FMT pin is used to set audio interface format. When the FMT pin is set to low, I²S format is enabled. When the FMT pin is set to high, Left Justified format is enabled. In hardware mode, the DEMP pin controls the 44.1kHz digital de-emphasis function. When the DEMP pin is set to low, the de-emphasis function is disabled. When the DEMP pin is set to high, 44.1 kHz de-emphasis is enabled.

Sampling Mode

Four sampling modes are available in the SY2A54560, including single rate, dual rate, quad rate and auto, which can be selected using register 0x10. Table 4 shows the oversampling rates of the digital filter and ΔΣ modulator in each sampling mode. The coefficients between the MCLK and f_S are limited by MCLK frequency. Table 4 also shows the common audio sampling rates in each sampling mode.

Table 4. Digital Filter and ΔΣ Modulator OSR in each Sampling Mode

Sampling Mode	Sampling rate (fs)	MCLK (xfs)	Digital Filter OSR	ΔΣ Modulator OSR
Auto	8~32kHz	1152	x8	x128
	8~48kHz	512, 768	x8	x128
	8~96kHz	256, 384	x8	x64
	16~192kHz	128, 192	x4	x32
Single	8~32kHz	1152	x8	x128
	8~48kHz	512, 768	x8	x128
	8~48kHz	256, 384	x8	x128
	16~48kHz	128, 192	x4	x64
Dual	88.2~96kHz	256, 384	x8	x64
		128, 192	x4	x64
Quad	176.4~192kHz	128, 192	x4	x32

In auto mode, the sampling mode is automatically set according to the coefficient between the MCLK and f_S. SY2A54560 operates in Auto Sampling Mode when hardware mode is selected. Table 5 shows the actual sampling mode under various coefficients in auto mode.

Table 5. The Actual Sampling Mode for Auto Sampling Mode

MCLK/fs	128	192	256	384	512	768	1152
Sampling mode	Quad rate		Dual rate		Single rate		

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Audio Serial Interface

The SY2A54560 audio serial interface consists of three signals, SCLK, LRCLK, and SDATA. SCLK is the bit clock input. LRCLK is the left/right word clock or frame synchronization clock input. SDATA is the audio data input.

The SY2A54560 supports three audio interface formats. In I²C mode, audio interface format can be configured using register 0x11, which includes I²S, Left Justified, and Right Justified. In hardware mode, the FMT pin sets the audio interface format. When the FMT pin is set to low, I²S format is enabled. When the FMT pin is set to high, Left Justified format is enabled. Table 7 shows the supported audio data depth and word width in all formats.

Table 7. Supported Audio Data Depth and Word Width in All Formats

Control Mode	Format	Data Bits	SCLK Rate (xf_S)
Software control	I²S / Left Justified	16/20/24	64, 48
		32	64
	Right Justified	24,16	64, 48
		16	32
Hardware control	I²S / Left Justified	16/20/24	64, 48
		32	64

I²S

In I²S mode, LRCLK defines which channel data is transmitted to. LRCLK is set to low for the left channel and high for the right channel. SCLK clocks in data at 48fs / 64fs. There is a one-cycle delay from the time LRCLK changes state to the first data bit. The data is written to the MSB first and is valid on the rising edge of the clock. The DAP masks the unused trailing data bit positions.

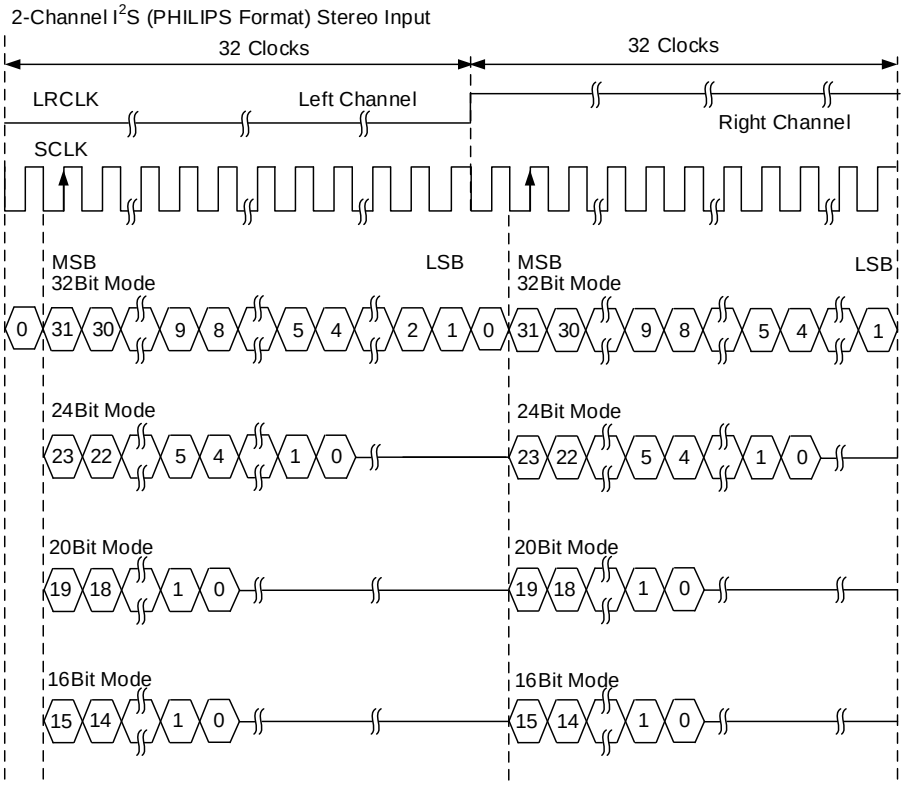

Figure 13. I²S 64fs Format

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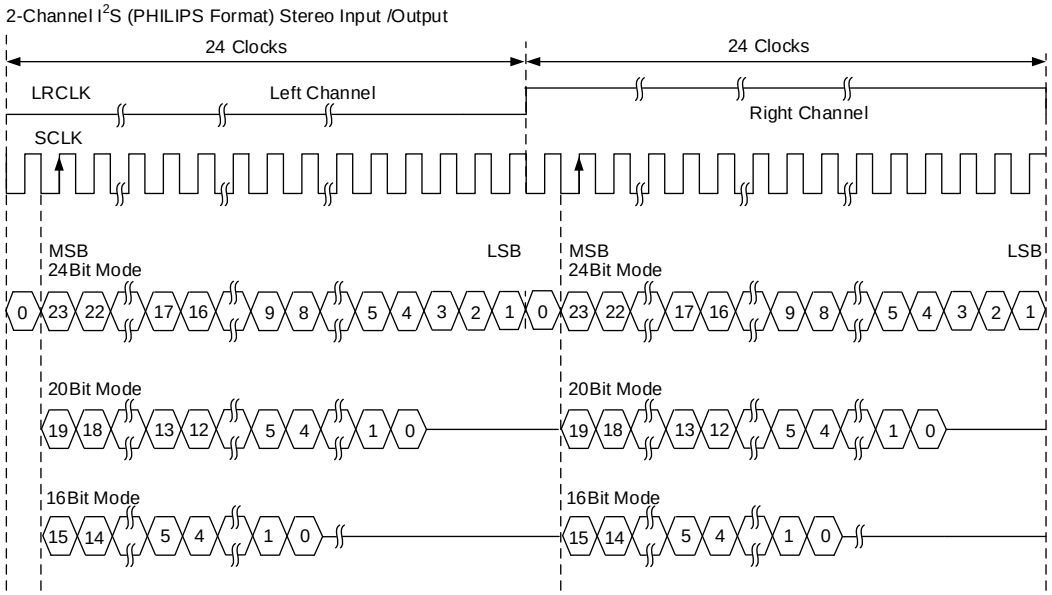

Figure 14. I²S 48fs Format

Left Justified

In Left Justified (LJ) timing mode, LRCLK defines which channel data is transmitted to. LRCLK is set to high for the left channel and low for the right channel. SCLK clocks in data at 48fs / 64fs. LRCLK toggling starts the first bit data transmission.. The data is written to the MSB first and is valid on the rising edge of the clock. The DAP masks the unused trailing data bit positions.

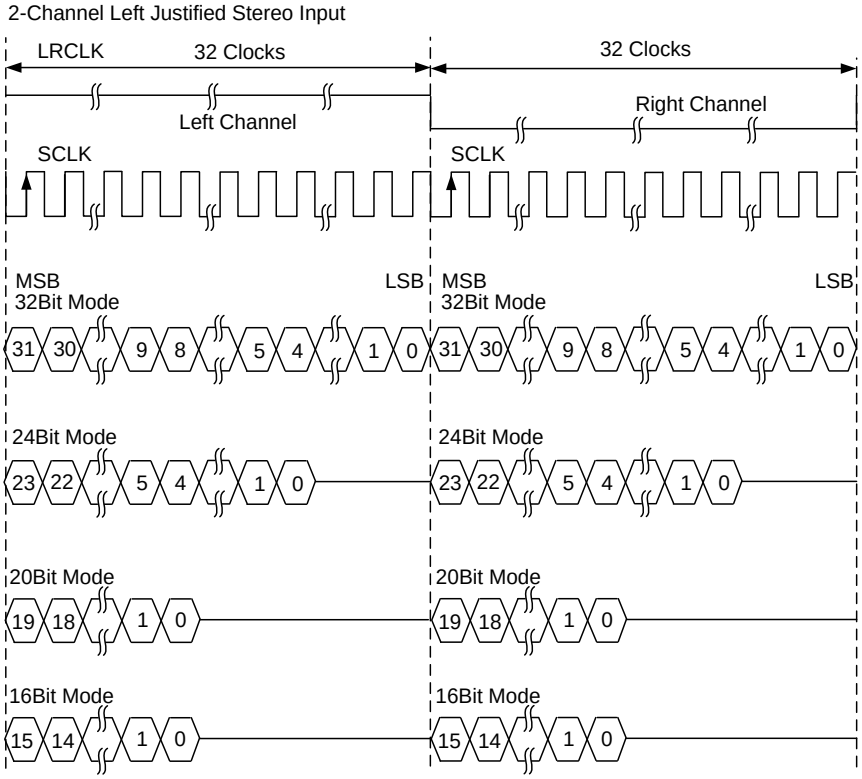

Figure 15. Left Justified 64fs Format

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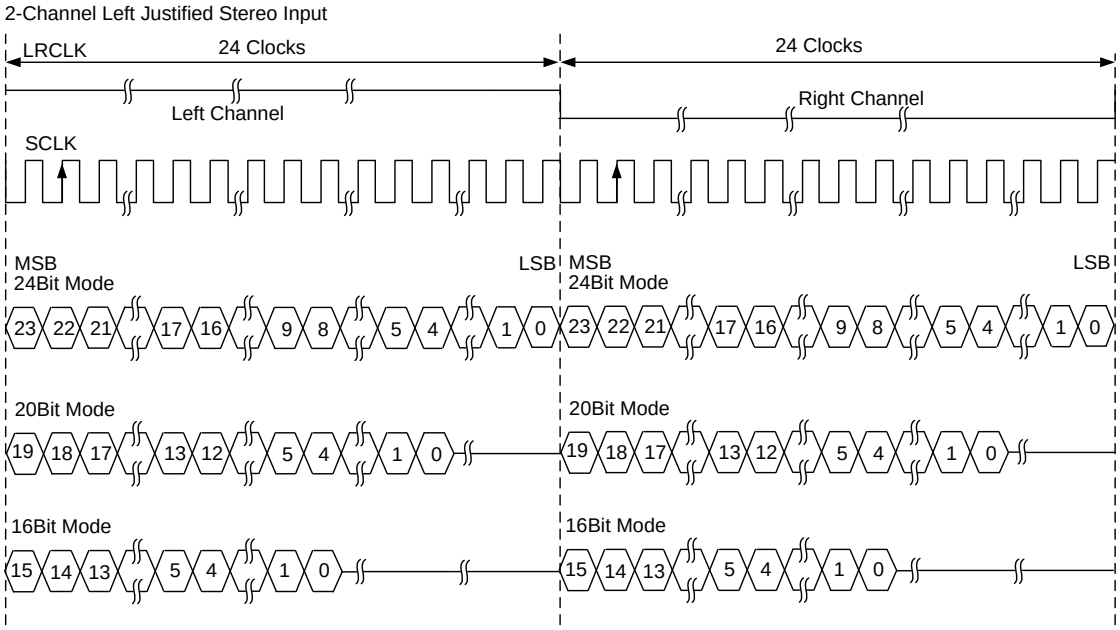

Figure 16. Left Justified 48fs Format

Right Justified

In Right Justified (RJ) timing mode, LRCLK defines which channel data is transmitted to. LRCLK is set to high for the left channel and low for the right channel. SCLK clocks in data at 32fs/48fs/64fs. The data is written to the MSB first and is valid on the rising edge of clock. The DAP masks the unused trailing data bit positions.

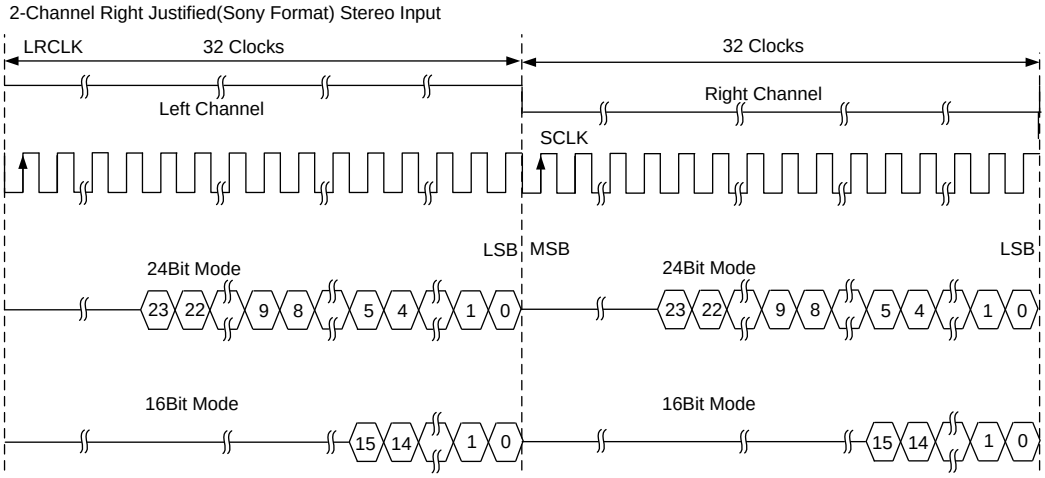

Figure 17. Right Justified 64fs Format

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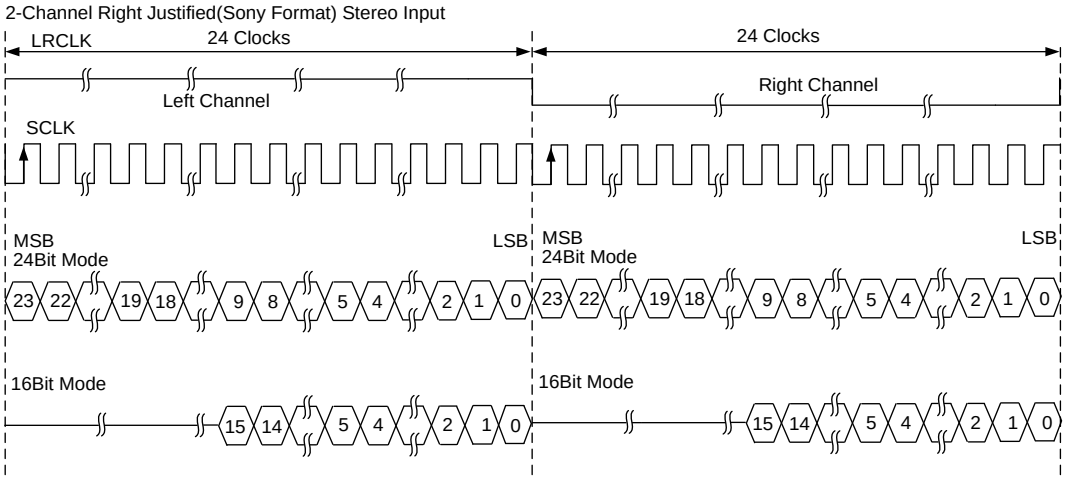

Figure 18. Right Justified 48fs Format

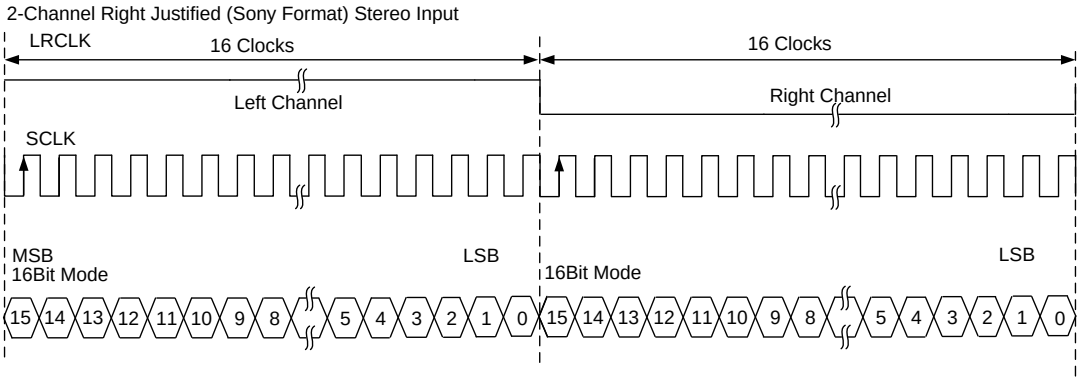

Figure 19. Right Justified 32fs Format

Serial Audio Interface Timing Requirements

Parameter	Symbol	Condition	Min	Typ	Max	Unit
LRCLK Frequency	F_{LRCLK}		8		192	kHz
SCLK Frequency	F_{SCLK}		0.256		12.288	MHz
LRCLK to SCLK Rising Edge Setup Time	t_{S1}		10			ns
LRCLK from SCLK Rising Edge Hold Time	t_{h1}		10			ns
SDATA to SCLK Rising Edge Setup Time	t_{S2}		10			ns
SDATA from SCLK Rising Edge Hold Time	t_{h2}		10			ns
SCLK Duty Cycle			40%	50%	60%	
LRCLK Duty Cycle			40%	50%	60%	
LRCLK Edge with Respect to the Falling Edge of SCLK	t_{edge}		-1/4		1/4	SCLK period
Rise/Fall Time for SCLK/LRCLK	t_{rs}/ t_{fs}	(Note 1)			1/8	SCLK period

Note 1: Rise /Fall time refers to the time the device takes for the leading edge of a pulse to transition from its minimum to its maximum value. Rise / Fall time is typically measured from 10% to 90% of the value.

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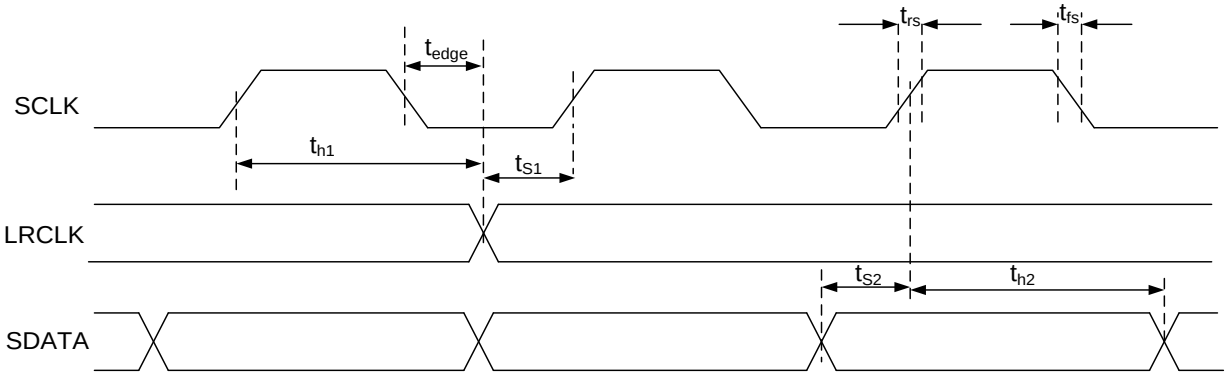

Figure 20. I²S timing Diagram

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Register Map

Address	Functions
0x10	Reset all register, reset signal path, analog mute control, and sampling mode selection
0x11	Power-save selection and audio format configuration
0x12	Shutdown control and digital filter selection
0x13	DAC out invert control
0x14	Soft mute control
0x15	Zero Detection
0x16	Volume mode selection, de-emphasis control, error flag polarity selection
0x17	Reserved
0x18	Volume setting
0x80	Monitor enable, bist mode selection, bist enable
0x81	Enable error out to ERROR pin, enable zero detection result to ERROR pin, enter mute when SRAM ECC multi-bit error occurs, enable anti-pop, AMUTE control for ECC error
0x82	Enable AVDD/DVDD under voltage detection, AMUTE control for AVDD/DVDD undervoltage, clock error control, bist fail shutdown enable
0x83	For factory inspection only
0x84	Enable output current limit, enable fast charge for VREF
0x85	For factory inspection only
0x86	Enable DAC analog gain control, VREF voltage configuration, output current limit configuration
0x87	DAC analog gain control
0x88	For factory inspection only
0x89	For factory inspection only
0x8A	For factory inspection only
0x8F	Monitor configuration
0x90	For factory inspection only
0x91	For factory inspection only
0x92	For factory inspection only
0x93	For factory inspection only
0x94	For factory inspection only
0xA0	Chip ID
0xA1	Clear all the fault flags of register 0xA2
0xA2	Clock error detection result, AVDD/DVDD undervoltage detection result
0xA3	For factory inspection only
0xA4	For factory inspection only
0xA5	For factory inspection only
0xA6	For factory inspection only
0xA7	For factory inspection only
0xA8	For factory inspection only
0xA9	For factory inspection only
0xAA	For factory inspection only
0xAB	For factory inspection only
0xB0	I²C_dly_en, I²C_sda_timeout_en, I²S_SCLK and LRCLK invert
0xB1	DSP fade force enable, I²S selection
0xB2	For factory inspection only

Register Definitions

Address	Bit	Label	Access	Default	Description
0x10	7	all_reg_reset	RW	1'b1	Register reset: 1'b0: reset all registers to default value 1'b1: normal operation
	6	sig_path_reset	RW	1'b1	Signal path reset: 1'b0: reset the whole signal path 1'b1: normal operation
	5	analog_mute_ctrl	RW	1'b0	Analog mute control3:

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					1’b0: disable analog mute control by DAC disable command 1’b1: enable analog mute control by DAC disable command
	4		RW	1’b0	Analog mute control2: 1’b0: disable analog mute control by zero detect 1’b1: enable analog mute control by zero detect
	3		RW	1’b0	Analog mute control1: 1’b0: disable analog mute control by asynchronous detect 1’b1: enable analog mute control by asynchronous detect
	2		RW	1’b0	Analog mute control0: 1’b0: disable analog mute control by MCLK halt 1’b1: enable analog mute control by MCLK halt
	1:0	samp_ mode_sel	RW	2’b00	Sampling mode selection: 2’b00: auto 2’b01: single rate 2’b10: dual rate 2’b11: quad rate

Address	Bit	Label	Access	Default	Description
0x11	7	power saving mode selection	RW	1’b0	1’b0: enable power-save mode 1’b1: disable Power-save mode
	6:3	N/A	R	4’d0	Reserved
	2:0	I²S_fmt	RW	3’d0	3’b000: 16-/20-/24-/32-bit I²S format 3’b001: 16-/20-/24-/32-bit left-justified format 3’b010: 24-bit right-justified format 3’b011: 16-bit right-justified format 3’b100: 16-/20-/24-/32-bit I²S format 3’b101: 16-/20-/24-/32-bit left-justified format Others: reserved

Address	Bit	Label	Access	Default	Description
0x12	7:5	N/A	R	3’d0	Reserved
	4	DAC shutdown	RW	1’b0	1’b0: normal operation 1’b1: DAC shutdown
	3:1	N/A	R	3’d0	Reserved
	0	digital filter selection	RW	1’b0	1’b0: sharp roll-off 1’b1: slow roll-off

Address	Bit	Label	Access	Default	Description
0x13	7:1	N/A	R	7’d0	Reserved
	0	DAC out invert	RW	1’b0	1’b0: DAC out normal 1’b1: DAC out inverted

Address	Bit	Label	Access	Default	Description
0x14	7:1	N/A	R	7’d0	Reserved
	0	soft mute control	RW	1’b0	1’b0: DAC output mute disable 1’b1: DAC output mute enable

Address	Bit	Label	Access	Default	Description
0x15	7:1	N/A	R	7’d0	Reserved
	0	zero flag	R	1’b0	1’b0: zero input not detected 1’b1: zero input detected

Address	Bit	Label	Access	Default	Description
0x16	7	volume mode	RW	1’b0	1'b0: step=0.5dB, volume range: -63dB to 0dB 1'b1: step=1dB, volume range: -100dB to 0dB
	6	N/A	R	1’b0	Reserved
	5:4	de-emphasis control	RW	2’b00	2’b00: Disable 2’b01: 48 kHz enable

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					2'b10: 44.1 kHz enable 2'b11: 32 kHz enable
	3:1	N/A	R	3'd0	Reserved
	0	error flag polarity	RW	1'b0	1'b0: high for error occur 1'b1: low for error occur

Address	Bit	Label	Access	Default	Description
0x18	7:0	DSP_volume_set	RW	8'hff	When step is 0.5dB, 8'h00~8'h80: mute; 8'h81: -63dB; 8'hFF: 0dB; When step is 1dB, 8'h00~8'h9A: mute; 8'h9B: -100dB; 8'hFF: 0dB; volume step is configured by register 0x16

Address	Bit	Label	Access	Default	Description
0x80	7:6	N/A	R	3'd0	Reserved
	5	monitor0_en	RW	1'b0	1'b0: disable Reg8F mon0_cfg 1'b1: enable Reg8F mon0_cfg
	4	monitor1_en	RW	1'b0	1'b0: disable Reg8F mon1_cfg 1'b1: enable Reg8F mon1_cfg
	3:2	N/A	R	2'd0	Reserved
	1	bist_mode	RW	1'b0	For factory inspection only
	0	bist_en	RW	1'b0	For factory inspection only

Address	Bit	Label	Access	Default	Description
0x81	7:5	N/A	R	3'd0	Reserved
	4	error_out_en	RW	1'b0	1'b0: disable error result to ERROR pin 1'b1: enable error result to ERROR pin
	3	zero_out_en	RW	1'b1	1'b0: disable zero result to ERROR pin 1'b1: enable zero result to ERROR pin
	2	sram_err_mute_en	RW	1'b1	1'b0: normal 1'b1: enter mute when SRAM ECC multi-bit error occurs
	1	dac_ana_fade_en	RW	1'b0	1'b0: disable anti_pop 1'b1: enable anti_pop
	0	ecc_err_amute_en	RW	1'b0	1'b0: normal 1'b1: enter amute when ECC error occurs

Address	Bit	Label	Access	Default	Description
0x82	7	avdd_uvdet_en	RW	1'b1	1'b0: disable AVDD undervoltage detection 1'b1: enable AVDD undervoltage detection
	6	dvdd_uvdet_en	RW	1'b1	1'b0: disable DVDD undervoltage detection 1'b1: enable DVDD undervoltage detection
	5	avdd_uv_amute_en	RW	1'b0	1'b0: normal 1'b1: enter amute when avdd_uv occurs
	4	dvdd_uv_amute_en	RW	1'b0	1'b0: normal 1'b1: enter amute when dvdd_uv occurs
	3	mclk_stop_err_en	RW	1'b1	1'b0: disable mclk_stop error 1'b1: enable mclk_stop error
	2	sclk_err_en	RW	1'b1	1'b0: disable SCLK error 1'b1: enable SCLK error
	1	mclk_err_en	RW	1'b1	1'b0: disable MCLK error 1'b1: enable MCLK error
	0	bist_fail_shutdown_en	RW	1'b1	For factory inspection only

Address	Bit	Label	Access	Default	Description
0x84	7	drv_ilimit_en	RW	1'b0	1'b0: disable output current limit 1'b1: enable output current limit
	6	fastchg_force_high	RW	1'b0	1'b0: disable fast charge for VREF 1'b1: enable fast charge for VREF
	5:4	ldo_ilimit_ctrl	RW	2'b00	For factory inspection only
	3	clk_hold_sel	RW	1'b1	For factory inspection only

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	2:0	dac_bg_tc_sel	RW	3'd0	For factory inspection only

Address	Bit	Label	Access	Default	Description
0x86	7	dac_ana_gain_ctl_en	RW	1'b0	1'b0: disable DAC analog gain control 1'b1: enable DAC analog gain control
	6:4	VREF_ level_setting	RW	3'b011	VREF level setting: 3'b000: 975mV 3'b001: 1020 mV 3'b010: 1060 mV 3'b011: 1100 mV 3'b100: 1140 mV 3'b101: 1180 mV 3'b110: 1220 mV 3'b111: 1260 mV
	3:2	drv_ilimit_sel	RW	2'b00	Output current limit selection: 2'b00: 40mA 2'b01: 60mA 2'b10: 60mA 2'b11: 120mA
	1:0	drv_ilimit_mul_sel	RW	2'b01	Multiple of output current limit selection based on drv_ilimit_sel: 2'b00: 0.5 2'b01: 1 2'b10: 1.5 2'b11: 2

Address	Bit	Label	Access	Default	Description
0x87	7:0	dac_ana_gain_ctl	RW	8'h40	Control analog gain 8'bxxxx 1000: -18dB 8'bxxx1 0000: -12dB 8'bxx10 0000: -6dB 8'bx100 0000: 0dB 8'b1000 0000: 6dB others reserved

Address	Bit	Label	Access	Default	Description
0x8F	7:4	mon0_cfg	RW	4'd0	PIN19 reuse, to monitor the internal signal 4'd0: for factory inspection only 4'd1: a2d_avdd_uvdet_out 4'd2: dsp_1bit_data_out 4'd3: d2a_ref_en 4'd4: d2a_bg_fastchg 4'd5: d2a_sw_ampbias_fsm 4'd6: d2a_drv_ampout_en_fsm 4'd7: d2a_en_vcm_tied_fsm 4'd8: d2a_drv_gain_sw_fsm[1] 4'd9: d2a_drv_gain_sw_fsm[3] 4'd10: d2a_drv_gain_sw_fsm[5] 4'd11: d2a_drv_gain_sw_fsm[7] 4'd12: I²S_frame_pulse 4'd13: dsp_frame_begin others reserved
	3:0	mon1_cfg	RW	4'd0	PIN18 reuse, to monitor the internal signal 4'd0: for factory inspection only 4'd1: a2d_osc_clk 4'd2: a2d_dvdd3p3_uvdet_out 4'd3: d2a_dac_en 4'd4: d2a_dac_reset 4'd5: d2a_drv_ampin_en_fsm 4'd6: d2a_dac_sw_fsm 4'd7: d2a_en_gnd_tied_fsm 4'd8: d2a_drv_gain_sw_fsm[0]

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					4'd9: d2a_drv_gain_sw_fsm[2] 4'd10: d2a_drv_gain_sw_fsm[4] 4'd11: d2a_drv_gain_sw_fsm[6] 4'd12: ~dsp_1bit_data_out 4'd13: I²S_dout_mix[23:0] 4'd14: dsp_run 4'd15: dac_clk

Address	Bit	Label	Access	Default	Description
0xA0	7:0	dig_chip_id	RO	8'h07	chip ID

Address	Bit	Label	Access	Default	Description
0xA1	7:4	N/A	R	4'd0	Reserved
	3:0	fault_clr_key	WO	4'd0	write 4'd1 will clear all the fault flags of register 0xA2.

Address	Bit	Label	Access	Default	Description
0xA2	7	sram_ecc_multi_err	RO	1'd0	1'd0: normal 1'd1: SRAM ECC multi error
	6	mclk_err_fault	RO	1'd0	1'd0: normal 1'd1: MCLK error
	5	sclk_err_fault	RO	1'd0	1'd0: normal 1'd1: SCLK error
	4	mclk_stop_fault	RO	1'd0	1'd0: normal 1'd1: MCLK stop error
	3:2	N/A	R	2'd0	Reserved
	1	avdd_uv_fault	RO	1'd0	1'd0: normal 1'd1: AVDD undervoltage detected
	0	dvdd_uv_fault	RO	1'd0	1'd0: normal 1'd1: DVDD undervoltage detected

Address	Bit	Label	Access	Default	Description
0xB0	7:4	N/A	R	4'd0	Reserved
	3	I²C_dly_en	RW	1'b1	1'b0: disable 1'b1: enable
	2	I²C_sda_timeout_en	RW	1'b1	1'b0: disable 1'b1: enable
	1	I²S_sclk_inv	RW	1'b0	1'b0: not invert SCLK 1'b1: invert SCLK
	0	I²S_lr_polarity	RW	1'b0	1'b0: not invert LRCLK 1'b1: invert LRCLK

Address	Bit	Label	Access	Default	Description
0xB1	7:5	N/A	R	3'd0	Reserved
	4	dsp_fade_force_en	RW	1'b0	1'b0: fade disable 1'b1: fade enable
	3:2	I²S selection	RW	2'b00	2'b00: I²S left channel data 2'b01: I²S right channel data 2'b10:1/2 * (right + left) 2'b11: Data = 0
	1:0	N/A	R	2'd0	Reserved

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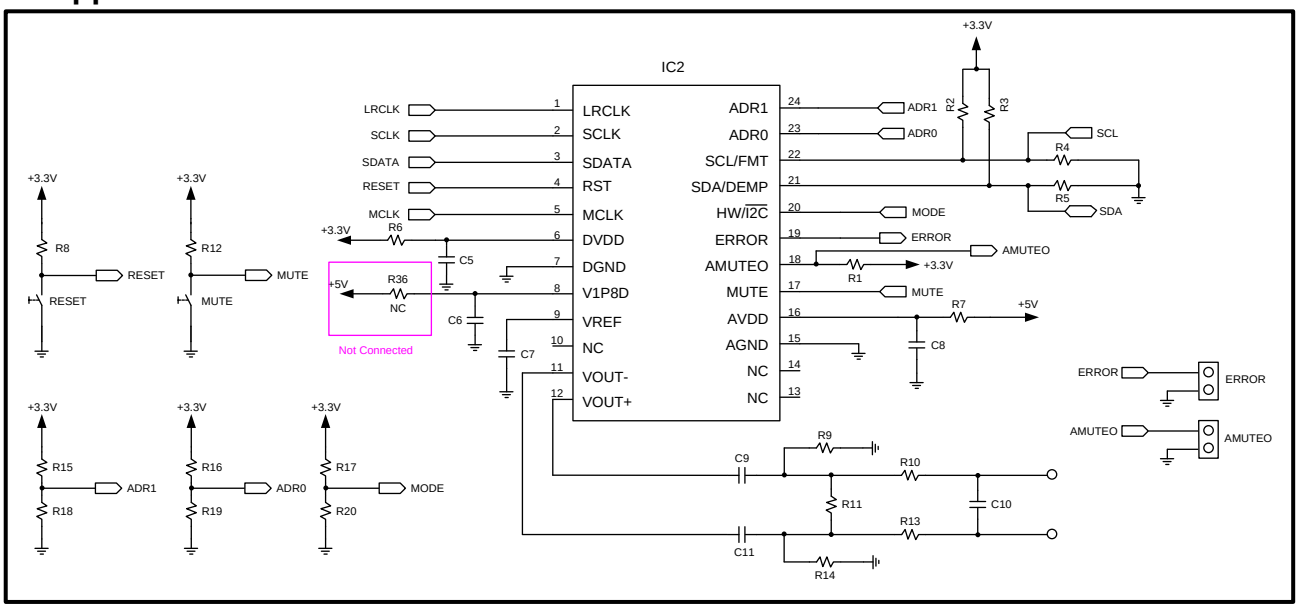
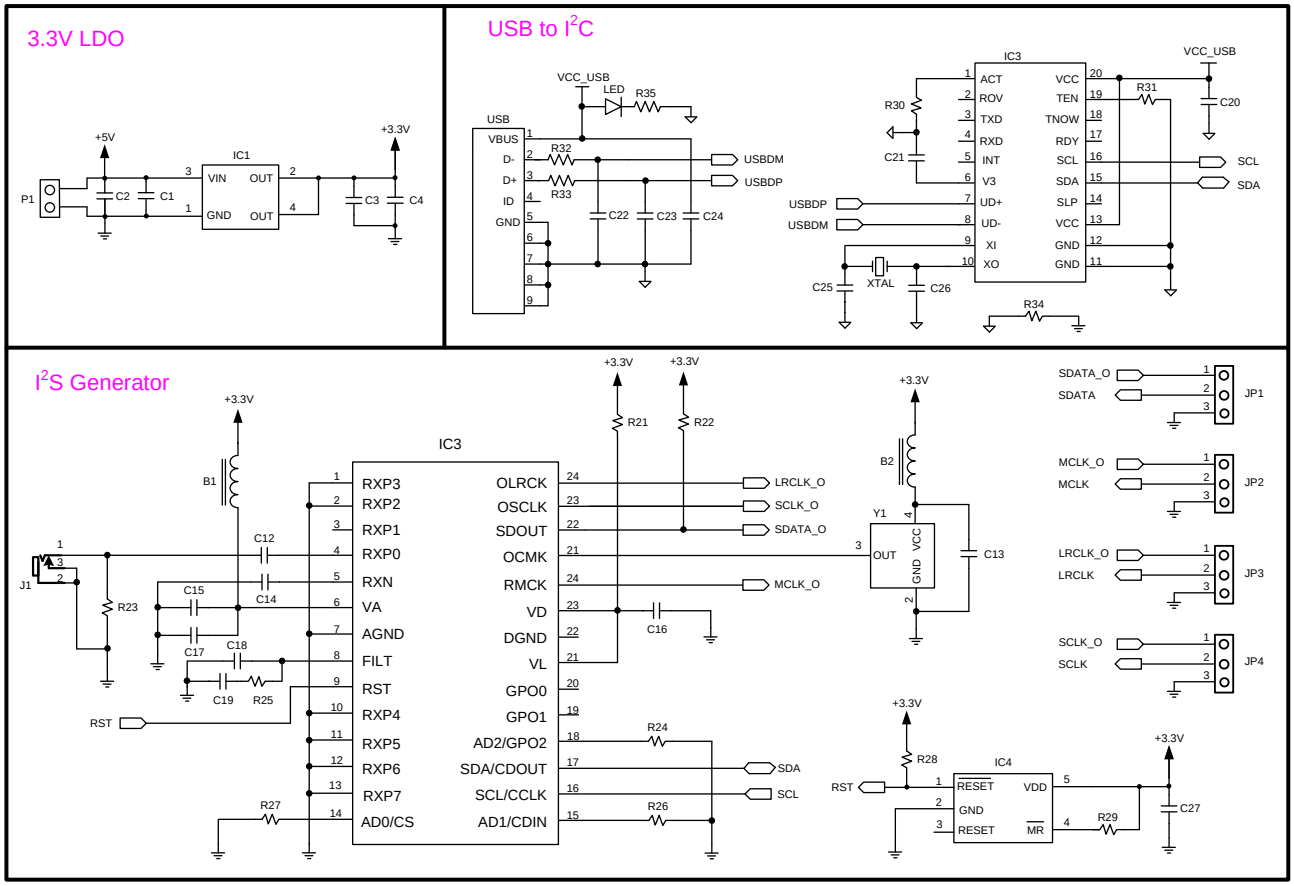
Schematic, BOM, and Layout

Typical Application Schematic



(a) SY2A54560 Application Schematic



(b) Other Peripherals (Optional)

Figure 21.SY2A54560 EVM Schematic

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BOM

Designator	Description	Part Number	Manufacturer
IC2	Mono Audio Digital to Analog Converter, TSSOP24	SY2A54560HNP	Silergy
C22, C23, C25, C26	33pF/16V, X7R, 0603		Murata
C10	2.2nF/16V, X7R, 0603		Murata
C12, C13, C14, C16, C17, C18, C19	10nF/16V, X7R, 0603		Murata
C1, C3, C20, C21, C27	100nF/16V, X7R, 0603		Murata
C5, C6, C7, C8, C9, C11	1uF/16V, X7R, 0603		Murata
C2, C4, C15, C24	10uF/16V, X7R, 0603		Murata
R6, R7, R21, R31, R34	0, ±10%, 0603		
R36	NC (0), ±10%, 0603		
R32, R33	10, ±10%, 0603		
R23	75, ±10%, 0603		
R35	470, ±10%, 0603		
R10, R13	560, ±10%, 0603		
R25	3k, ±10%, 0603		
R2, R3, R18, R19, R20, R28, R29, R30	4.7k, ±10%, 0603		
R4, R5, R15, R16, R17	NC (4k7), ±10%, 0603		
R8, R12	10k, ±10%, 0603		
R1	NC (10k), ±10%,0603		
R11	20k, ±10%, 0603		
R22, R24, R26, R27	47k, ±10%, 0603		
B1, B2	3.3, ±10%, 0805		
MUTE, RESET	Light Touch Switches, SMD,2.9x3.5mm-4P	EVPAA202K	Panasonic
Y1	OSC-HALF-5X7, SMD, 5X3.2mm-4P	ASFL1-12.288MHZ-L-T	
XTAL	12MHz		
USB	Mini USB		
IC5	USB bus convert chip, SSOP20	CH341T	
IC3	Digital Audio Interface Receiver, TSSOP28	CS8416	
IC4	Voltage Monitor with Watchdog Timer, SOT-23(5)	TPS3825	
IC1	3.3V Voltage Regulator, SOT-223	LM1117	
LED	LED, 0805		
J1	RCA connector	PJRAN1X1U02X	

PCB Layout Guidelines

To obtain optimal EMC and audio performance of the SY2A54560, PCB layout must follow the following guidelines:

- A short and thick power wire is recommended to reduce voltage drop.
- A ground plane is recommended for a good ground connection.
- To reduce parasitic inductance and resistance, high-frequency ceramic capacitors with low ESR should be placed as close to the power pins (such as DVDD, AVDD, V1P8D and VREF pin) as possible. These capacitors should be connected to the ground plane using vias.

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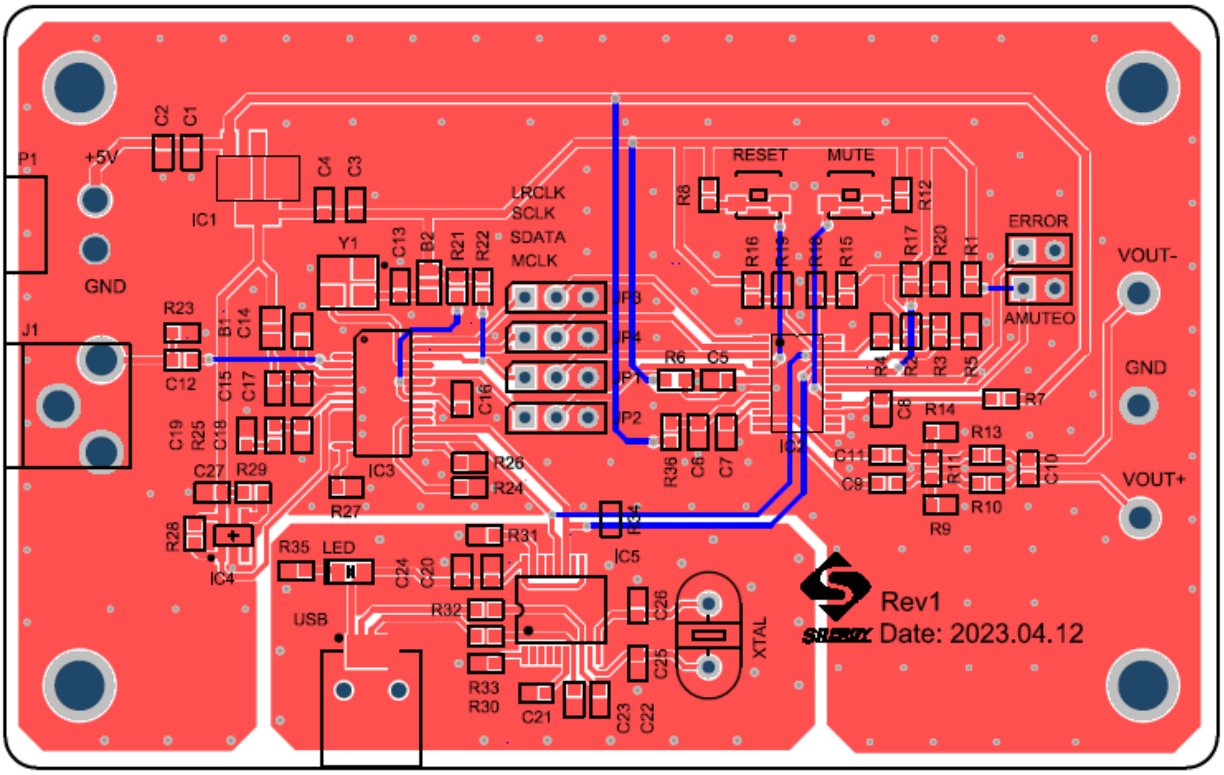

Figure 22.SY2A54560 EVM Layout

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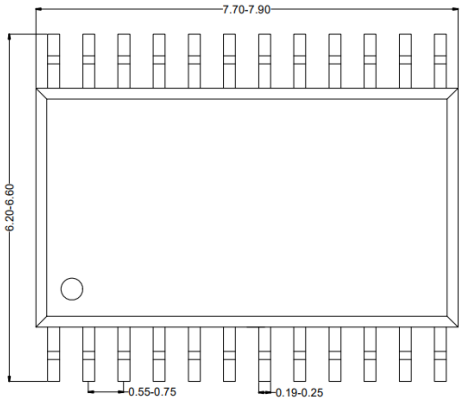
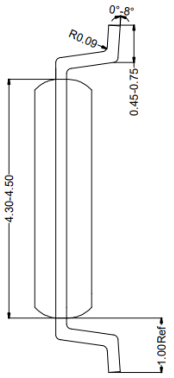
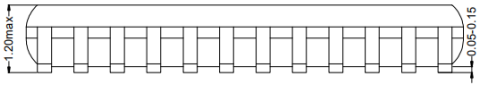
TSSOP24 Package Outline



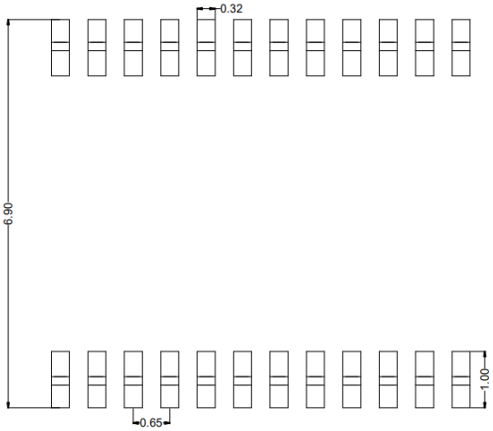
Top View



Side View



Front View



Recommended PCB Layout (Reference Only)

Note: All dimensions are in millimeters and exclude mold flash and metal burr.

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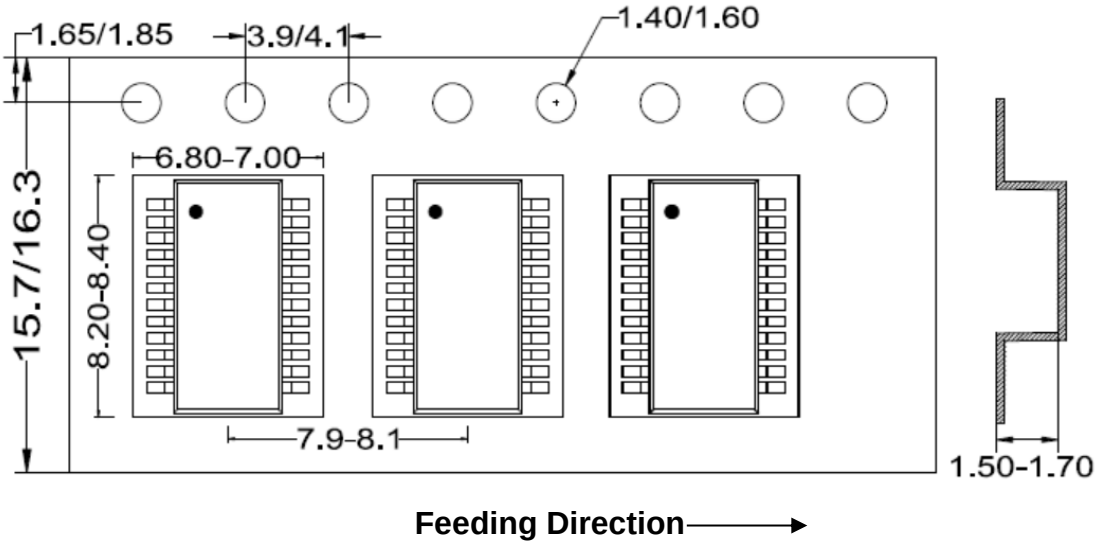
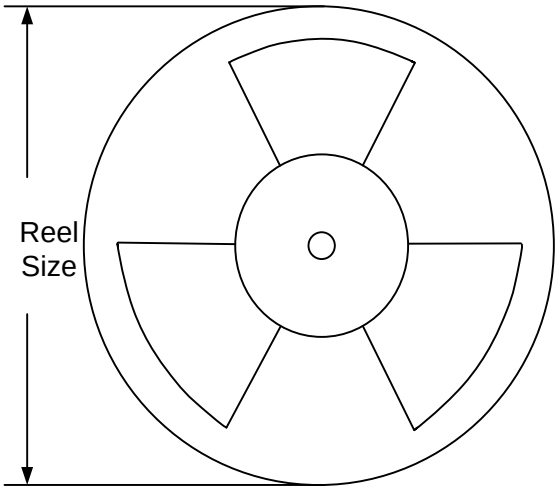
Tape and Reel Information

Tape Dimensions and Pin 1 Orientation



Reel Dimensions



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Trailer Length(mm)	Leader Length (mm)	Qty per Reel (pcs)
TSSOP24	16	8	13"	400	400	3000

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Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, not warrantied. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
0.9	Oct. 27, 2023	Initial Release	
1.0	Jan. 21, 2025	Language Improvement for clarity	

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