SA89851/ SA89853

8- and 16-Channel 12-Bit, 1MSPS, Single-Ended Automotive Analog-to-Digital Converter

General Description

The SA89851/3 is a 12-bit multi-channel analog-to-digital converter (ADC) featuring a successive approximation register (SAR) architecture with a built-in sample and hold circuit. The device supports a wide analog supply range of 2.7V to 5.25V. The low power consumption makes this device ideal for battery-powered and isolated power supply applications.

The device features two software-selectable input ranges (0V to VREF and 0V to 2xVREF), individually configurable general-purpose input/outputs (GPIOs), and two programmable alarm thresholds per channel. It also includes a power-down feature to conserve energy when operating at reduced conversion speeds.

Features

- 8- and 16-Channel, 12-Bit ADC
- Analog Supply Range: 2.7V to 5.25V
- I/O Supply Range: 1.7V to 5.25V
- 1MHz Sample-Rate Device
- Qualified for Automotive Applications
- Two Software or Hardware Selectable Unipolar Input Ranges: 0V to 2.5V or 0V to 5V
- Auto and Manual Channel Selection Modes
- Two Programmable Alarm Levels per Channel
- Individually Configurable GPIOs
- Low Power Dissipation
- Power-Down Feature
- 20MHz SPI-Compatible Serial Interface
- 30-Pin and 38-Pin TSSOP Packages
- AEC-Q100 Grade 1: -40°C to 125°C Ambient Operating Temperature Range

Applications

- Battery-Powered Systems
- Power Supply Monitoring
- Driver Assistance Applications
- HV Traction Inverter Voltage/Temp Monitoring

Typical Application

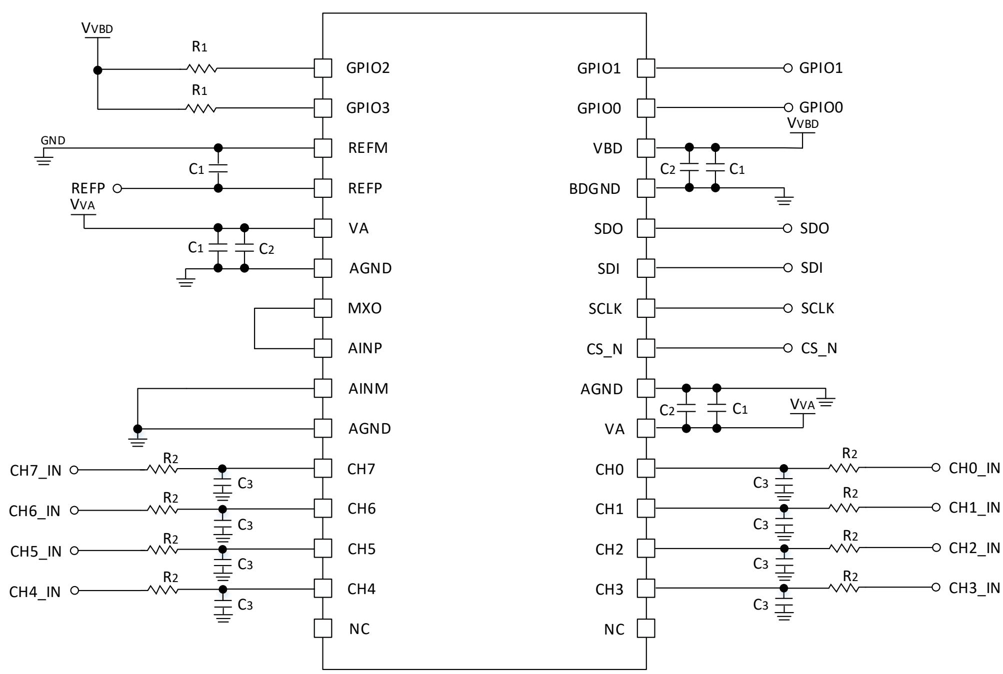

Figure 1. Typical Application (SA89851)

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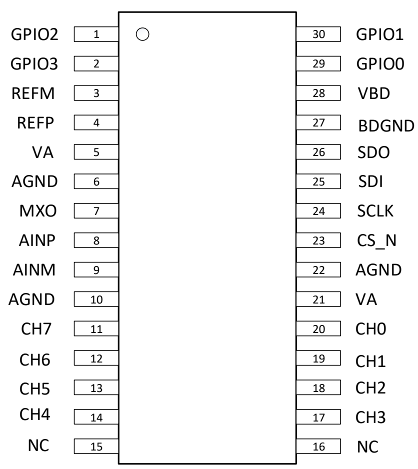
Ordering Information

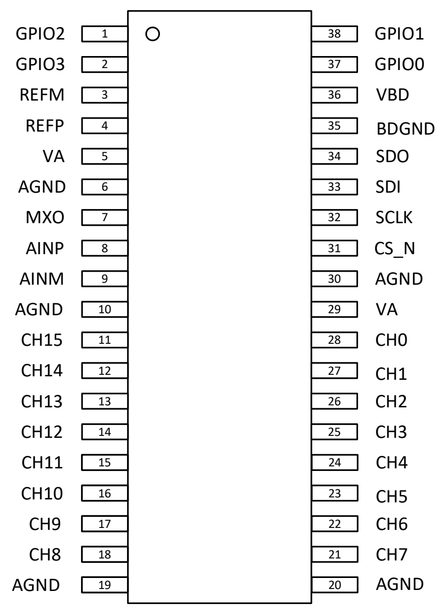
Ordering Part Number	Package Type	Description	Top Mark
SA89851HLP	TSSOP30	8-Channel ADC	**FQT*xyz***
SA89853HUP	TSSOP38	16-Channel ADC	**FQWxyz**

Device code: FQT, FQW
x=year code, y=week code, z=lot number code
* Future product. Specifications subject to change.

Pinout (Top View)



(TSSOP30)



(TSSOP38)

Pin Description

Pin No.		Pin Name	Pin Description
TSSOP30	TSSOP38		
1	1	GPIO2	The pin can be configured as general-purpose input or output.
		Range	The pin can be configured for range selection. A high level selects the 0V to 2xVREF range; a low level selects a 0V to VREF range.
2	2	GPIO3	The pin can be configured as general-purpose input or output.
		PD_N	The pin can be configured as active low power-down input.
3	3	REFM	Ground for reference.
4	4	REFP	Input pin for reference.
5	5	VA	Analog supply power.
6	6	AGND	Ground for analog circuitry.
7	7	MXO	The output from the multiplexer.
8	8	AINP	ADC input signal.
9	9	AINM	The ground for ADC input.
10	10	AGND	Ground for analog circuitry.

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/	11	CH15	The input channel 15 of the multiplexer.
/	12	CH14	The input channel 14 of the multiplexer.
/	13	CH13	The input channel 13 of the multiplexer.
/	14	CH12	The input channel 12 of the multiplexer.
/	15	CH11	The input channel 11 of the multiplexer.
/	16	CH10	The input channel 10 of the multiplexer.
/	17	CH9	The input channel 9 of the multiplexer.
/	18	CH8	The input channel 8 of the multiplexer.
/	19	AGND	Ground for analog circuitry.
/	20	AGND	Ground for analog circuitry.
11	21	CH7	The input channel 7 of the multiplexer.
12	22	CH6	The input channel 6 of the multiplexer.
13	23	CH5	The input channel 5 of the multiplexer.
14	24	CH4	The input channel 4 of the multiplexer.
15	/	NC	Not connect.
16	/	NC	Not connect.
17	25	CH3	The input channel 3 of the multiplexer.
18	26	CH2	The input channel 2 of the multiplexer.
19	27	CH1	The input channel 1 of the multiplexer.
20	28	CH0	The input channel 0 of the multiplexer.
21	29	VA	Analog power supply.
22	30	AGND	Ground for analog circuitry.
23	31	CS_N	Active-low serial data enable.
24	32	SCLK	Serial interface clock.
25	33	SDI	Serial interface data input.
26	34	SDO	Serial interface data output.
27	35	BDGND	Ground for digital circuitry.
28	36	VBD	Digital I/O supply voltage.
29	37	GPIO0	The pin can be configured as general-purpose input or output.
		Low_High_Alarm	The pin can be configured as an active high output indicator for high or low threshold alarm, depending on the programming.
30	38	GPIO1	The pin can be configured as general-purpose input or output.
		Low_Alarm	The pin can be configured as an active high output indicator for low threshold alarm.

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Block Diagram

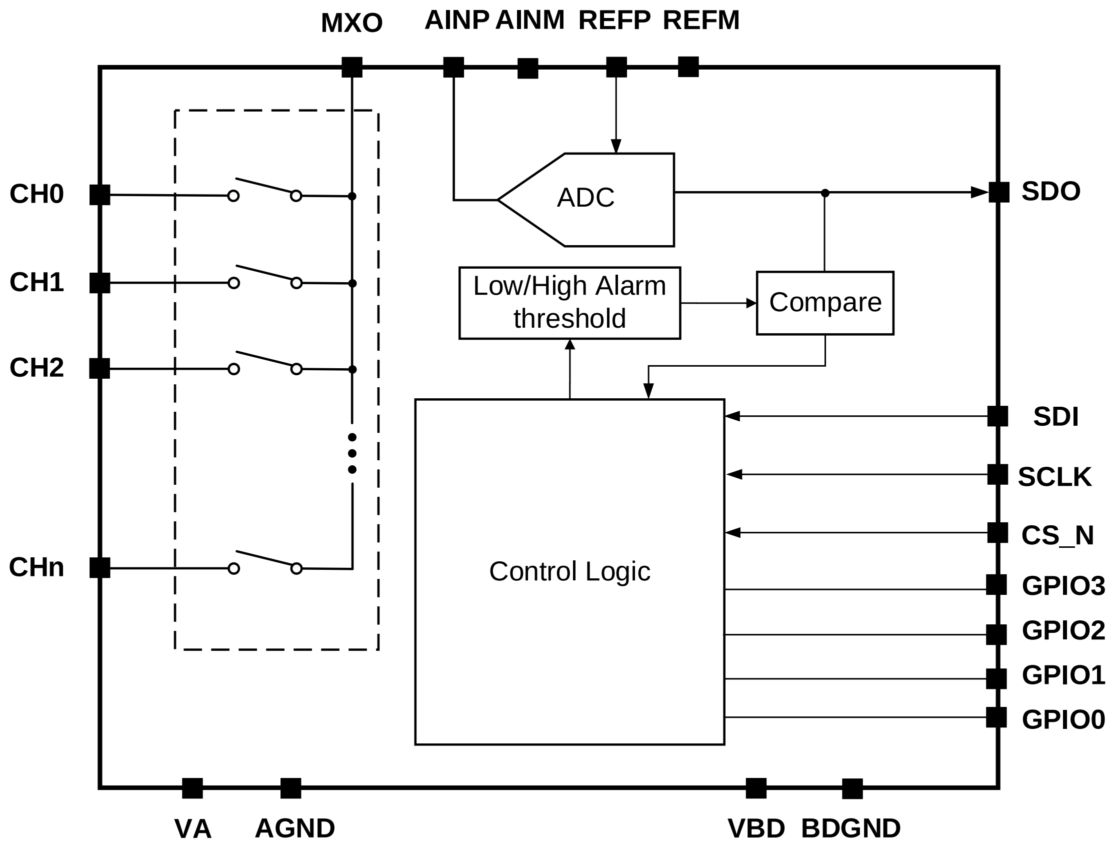

Figure 2. Block Diagram

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Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VA, VBD	-0.3	6.5	V
AINP, MXO, REFP, CH0-CHn	-0.3	V_{VA}+0.3	
CS_N, SCLK, SDI, SDO	-0.3	V_{VBD}+0.3	
GPIO0-GPIO3	-0.3	V_{VBD}+0.3	
Junction Temperature	-40	150	°C
Storage Temperature	-55	150	
ESD: HBM (Human Body Model)	± 2000		V
ESD: CDM (Charged Device Model)	± 750		V

Thermal Information

Parameter (Note 2)	TSSOP38	TSSOP30	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	122.73	156.63	°C/W
θ_{JC} Junction-to-Case (Top) Thermal Resistance	10.5	21.3	
θ_{JB} Junction-to-Board Thermal Resistance	57.42	82.5	

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VA	2.7	5.25	V
VBD	1.7	V_{VA}	V
AINP, MXO, CH0-CHn	0	V_{VA}	V
REFP	2	3	V
CS_N, SCLK, SDI, SDO, GPIO0-GPIO3	0	V_{VBD}	V
Operation Ambient Temperature Range	-40	125	°C

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Electrical Characteristics: SA89851

V_{VA} = 2.7V to 5.25V, V_{VBD} = 1.7V to V_{VA}, V_{REF} = 2.5V ± 0.1V, T_A = –40°C to 125°C, f_{sample} = 1MHz, Range 1: 0-V_{REF}, Range 2 while 2xV_{REF}≤V_{VA}: 0-2xV_{REF}, typical values are T_A = 25°C, unless otherwise noted (**Note 4**).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Analog Input						
Full-Scale Input Span		Range 1	0		V_{REF}	V
		Range 2 while 2xV_{REF}≤V_{VA}	0		2×V_{REF}	V
Absolute Input Range		Range 1	-0.2		V_{REF} +0.2	V
		Range 2 while 2xV_{REF}≤V_{VA}	-0.2		2×V_{REF} +0.2	V
Input Capacitance (Note 5)				16		pF
Input Leakage Current		T_A = 125°C		50		nA
Sampling Dynamics (Note 5)						
Conversion Time		20MHz SCLK			800	ns
Acquisition Time			325			ns
Maximum Throughput Rate		20MHz SCLK			1	MHz
Aperture Delay				5		ns
Step Response				150		ns
Over Voltage Recovery				150		ns
Static Performance						
Resolution				12		Bits
No Missing Codes			11			Bits
Integral Linearity	INL		-3.6	± 1.2	3.6	LSB
Differential Linearity	DNL		-2	± 0.85	1.8	LSB
Offset Error		Range 1	-5	± 1	5	LSB
		Range 2	-4	± 1	4	LSB
Gain Error		Range 1	-4	± 0.8	2.5	LSB
		Range 2	-5.5	± 0.8	4	LSB
Total Unadjusted Error	TUE			± 3		LSB
Dynamic Characteristics (Note 5)						
Total Harmonic Distortion	THD	100kHz		-72		dB
Signal-to-Noise Ratio	SNR	100kHz, V_{VBD}⩽3.3V		69		dB
		100kHz, V_{VBD}⩾5V		64		dB
Signal-to-Noise +Distortion	SINAD	100kHz, V_{VBD}⩽3.3V		67.2		dB
		100kHz, V_{VBD}⩾5V		63.3		dB
Spurious-Free Dynamic Range	SFDR	100kHz		75		dB
Small Signal Bandwidth		At -3dB		47		MHz
Channel-to-Channel Crosstalk		Any off-channel with 100 kHz. Full-scale input to channel being sampled with DC input (isolation crosstalk).		-92		dB
		From previously sampled to channel with 100 kHz. Full-scale input to channel being sampled with DC input (memory crosstalk).		-83		dB

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External Reference Input						
Reference Voltage at REFP	V_{REF}		2	2.5	3	V
Reference Resistance	R_{REF}			31		kΩ
Power Supply Requirements						
Analog Power-Supply Voltage	V_{VA}		2.7	3.3	5.25	V
Digital I/O-Supply Voltage	V_{VBD}		1.7	3.3	V_{VA}	V
Supply Current (Normal Mode)	I_{VA}	At V_{VA} = 2.7V to 3.6V and 1MHz throughput		2.1	2.4	mA
		At V_{VA} = 2.7V to 3.6V static state		1	1.25	mA
		At V_{VA} = 4.7V to 5.25V and 1MHz throughput		2.8	3.2	mA
		At V_{VA} = 4.7V to 5.25V static state		1.2	1.45	mA
Power-Down State Supply Current				0.7		μA
Digital I/O-Supply Current	I_{VBD}	V_{VA} = 5.25V, f_{sample} = 1 MHz		1.1		mA
Power-up Time				200		us
Invalid Conversion after Power up or Reset					1	cycle
Latch-up				JESD78 Class I		
Temperature Range						
Specified Performance			-40		125	℃
Alarm Setting						
Higher Threshold Range			0		FFC	Hex
Lower Threshold Range			0		FFC	Hex
Digital Input / Output (CMOS Logic Family)						
High Logic-Level Input Voltage	V_{IH}		0.75 x V_{VBD}			V
Low Logic-Level Input Voltage	V_{IL}	V_{VA} = 5V			0.8	V
		V_{VA} = 3V			0.4	V
High Logic-Level Output Voltage	V_{OH}	At source current (I_S) = 200μA	V_{VBD} - 0.2			V
Low Logic-Level Output Voltage	V_{OL}	At I_{sink} = 200μA	0.4			V
Data Format MSB First				MSB first		
Timing Requirements (Note 5)						
Conversion Time	t_c	V_{VBD} = 1.8V			16	SCLK
		V_{VBD} = 3V			16	SCLK
		V_{VBD} = 5V			16	SCLK
Minimum Quiet Sampling Time Needed from Bus Tri-State to Start of Next Conversion	t_q	V_{VBD} = 1.8V	40			ns
		V_{VBD} = 3V	40			ns
		V_{VBD} = 5V	40			ns
Delay Time, CS_N Low to First Data (DO–15) out	t_{d1}	V_{VBD} = 1.8V			38	ns
		V_{VBD} = 3V			27	ns
		V_{VBD} = 5V			17	ns
Setup Time, CS_N Low to First Rising Edge of SCLK	t_{su1}	V_{VBD} = 1.8V	8			ns
		V_{VBD} = 3V	6			ns
		V_{VBD} = 5V	4			ns
	t_{d2}	V_{VBD} = 1.8V			35	ns

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Delay Time, SCLK Falling to SDO Next Data Bit Valid		V_{VBD} = 3V			27	ns
		V_{VBD} = 5V			17	ns
Hold Time, SCLK Falling to SDO Data Bit Valid	t_{h1}	V_{VBD} = 1.8V	7			ns
		V_{VBD} = 3V	5			ns
		V_{VBD} = 5V	3			ns
Delay Time, 16th SCLK Falling Edge to SDO 3-state	t_{d3}	V_{VBD} = 1.8V			26	ns
		V_{VBD} = 3V			22	ns
		V_{VBD} = 5V			13	ns
Setup Time, SDI Valid to Rising Edge of SCLK	t_{su2}	V_{VBD} = 1.8V	2			ns
		V_{VBD} = 3V	3			ns
		V_{VBD} = 5V	4			ns
Hold Time, Rising Edge of SCLK to SDI Valid	t_{h2}	V_{VBD} = 1.8V	12			ns
		V_{VBD} = 3V	10			ns
		V_{VBD} = 5V	6			ns
Pulse Duration CS_N High	t_{w1}	V_{VBD} = 1.8V	20			ns
		V_{VBD} = 3V	20			ns
		V_{VBD} = 5V	20			ns
Delay time 16th SCLK falling edge to CS_N high	t_{d4}	V_{VBD} = 1.8V	7			ns
		V_{VBD} = 3V	6			ns
		V_{VBD} = 5V	5			ns
Pulse Duration SCLK High	t_{wH}	V_{VBD} = 1.8V	20			ns
		V_{VBD} = 3V	20			ns
		V_{VBD} = 5V	20			ns
Pulse Duration SCLK Low	t_{wL}	V_{VBD} = 1.8V	20			ns
		V_{VBD} = 3V	20			ns
		V_{VBD} = 5V	20			ns
Frequency SCLK	$f_{(SCLK)}$	V_{VBD} = 1.8V			20	MHz
		V_{VBD} = 3V			20	MHz
		V_{VBD} = 5V			20	MHz

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Electrical Characteristics: SA89853

V_{VA} = 2.7V to 5.25V, V_{VBD} = 1.7V to V_{VA}, V_{REF} = 2.5V ± 0.1V, T_A = –40°C to 125°C, f_{sample} = 1MHz, Range 1: 0-V_{REF}, Range 2 while 2xV_{REF}≤V_{VA}: 0-2xV_{REF}, typical values are T_A = 25°C, unless otherwise noted (**Note 4**).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Analog Input						
Full-Scale Input Span		Range 1	0		V_{REF}	V
		Range 2 while 2xV_{REF}≤V_{VA}	0		2×V_{REF}	V
Absolute Input Range		Range 1	-0.2		V_{REF} +0.2	V
		Range 2 while 2xV_{REF}≤V_{VA}	-0.2		2×V_{REF} +0.2	V
Input Capacitance (Note 5)				16		pF
Input Leakage Current		T_A = 125°C		50		nA
Sampling Dynamics (Note 5)						
Conversion Time		20MHz SCLK			800	ns
Acquisition Time			325			ns
Maximum Throughput Rate		20MHz SCLK			1	MHz
Aperture Delay				5		ns
Step Response				150		ns
Over Voltage Recovery				150		ns
Static Performance						
Resolution				12		Bits
No Missing Codes			11			Bits
Integral Linearity	INL		-3.6	± 1.2	4	LSB
Differential Linearity	DNL		-2	± 0.85	1.8	LSB
Offset Error		Range 1	-5	± 1	5	LSB
		Range 2	-4	± 1	4	LSB
Gain Error		Range 1	-4	± 0.8	2.5	LSB
		Range 2	-5.5	± 0.8	4	LSB
Total Unadjusted Error	TUE			± 3		LSB
Dynamic Characteristics (Note 5)						
Total Harmonic Distortion	THD	100kHz		-72		dB
Signal-to-Noise Ratio	SNR	100kHz, V_{VBD}⩽3.3V		69		dB
		100kHz, V_{VBD}⩾5V		64		dB
Signal-to-Noise +Distortion	SINAD	100kHz, V_{VBD}⩽3.3V		67.2		dB
		100kHz, V_{VBD}⩾5V		63.3		dB
Spurious-Free Dynamic Range	SFDR	100kHz		75		dB
Small Signal Bandwidth		At -3dB		47		MHz
Channel-to-Channel Crosstalk		Any off-channel with 100 kHz. Full-scale input to channel being sampled with DC input (isolation crosstalk).		-92		dB
		From previously sampled to channel with 100 kHz. Full-scale input to channel being sampled with DC input (memory crosstalk).		-83		dB

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External Reference Input						
Reference Voltage at REFP	V_{REF}		2	2.5	3	V
Reference Resistance	R_{REF}			31		kΩ
Power Supply Requirements						
Analog Power-Supply Voltage	V_{VA}		2.7	3.3	5.25	V
Digital I/O-Supply Voltage	V_{VBD}		1.7	3.3	V_{VA}	V
Supply Current (Normal Mode)	I_{VA}	At V_{VA} = 2.7V to 3.6V and 1MHz throughput		2.1	2.4	mA
		At V_{VA} = 2.7V to 3.6V static state		1	1.25	mA
		At V_{VA} = 4.7V to 5.25V and 1MHz throughput		2.8	3.2	mA
		At V_{VA} = 4.7V to 5.25V static state		1.2	1.45	mA
Power-Down State Supply Current				0.7		μA
Digital I/O-Supply Current	I_{VBD}	V_{VA} = 5.25V, f_{sample} = 1MHz		1.1		mA
Power-up Time				200		us
Invalid Conversion after Power up or Reset					1	cycle
Latch-up			JESD78 Class I			
Temperature Range						
Specified Performance			-40		125	℃
Alarm Setting						
Higher Threshold Range			0		FFC	Hex
Lower Threshold Range			0		FFC	Hex
Digital Input / Output (CMOS Logic Family)						
High Logic-Level Input Voltage	V_{IH}		0.75 x V_{VBD}			V
Low Logic-Level Input Voltage	V_{IL}	V_{VA} = 5V			0.8	V
		V_{VA} = 3V			0.4	V
High Logic-Level Output Voltage	V_{OH}	At source current (I_S) = 200μA	V_{VBD} - 0.2			V
Low Logic-Level Output Voltage	V_{OL}	At I_{sink} = 200μA			0.4	V
Data Format MSB First			MSB first			
Timing Requirements (Note 5)						
Conversion Time	t_c	V_{VBD} = 1.8V			16	SCLK
		V_{VBD} = 3V			16	SCLK
		V_{VBD} = 5V			16	SCLK
Minimum Quiet Sampling Time Needed from Bus Tri-State to Start of Next Conversion	t_q	V_{VBD} = 1.8V	40			ns
		V_{VBD} = 3V	40			ns
		V_{VBD} = 5V	40			ns
Delay Time, CS_N Low to First Data (DO–15) out	t_{d1}	V_{VBD} = 1.8V			38	ns
		V_{VBD} = 3V			27	ns
		V_{VBD} = 5V			17	ns
Setup Time, CS_N Low to First Rising Edge of SCLK	t_{su1}	V_{VBD} = 1.8V	8			ns
		V_{VBD} = 3V	6			ns
		V_{VBD} = 5V	4			ns
	t_{d2}	V_{VBD} = 1.8V			35	ns

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Delay Time, SCLK Falling to SDO Next Data Bit Valid		V_{VBD} = 3V			27	ns
		V_{VBD} = 5V			17	ns
Hold Time, SCLK Falling to SDO Data Bit Valid	t_{h1}	V_{VBD} = 1.8V	7			ns
		V_{VBD} = 3V	5			ns
		V_{VBD} = 5V	3			ns
Delay Time, 16th SCLK Falling Edge to SDO 3-state	t_{d3}	V_{VBD} = 1.8V			26	ns
		V_{VBD} = 3V			22	ns
		V_{VBD} = 5V			13	ns
Setup Time, SDI Valid to Rising Edge of SCLK	t_{su2}	V_{VBD} = 1.8V	2			ns
		V_{VBD} = 3V	3			ns
		V_{VBD} = 5V	4			ns
Hold Time, Rising Edge of SCLK to SDI Valid	t_{h2}	V_{VBD} = 1.8V	12			ns
		V_{VBD} = 3V	10			ns
		V_{VBD} = 5V	6			ns
Pulse Duration CS_N High	t_{w1}	V_{VBD} = 1.8V	20			ns
		V_{VBD} = 3V	20			ns
		V_{VBD} = 5V	20			ns
Delay time 16th SCLK falling edge to CS_N high	t_{d4}	V_{VBD} = 1.8V	7			ns
		V_{VBD} = 3V	6			ns
		V_{VBD} = 5V	5			ns
Pulse Duration SCLK High	t_{wH}	V_{VBD} = 1.8V	20			ns
		V_{VBD} = 3V	20			ns
		V_{VBD} = 5V	20			ns
Pulse Duration SCLK Low	t_{wL}	V_{VBD} = 1.8V	20			ns
		V_{VBD} = 3V	20			ns
		V_{VBD} = 5V	20			ns
Frequency SCLK	$f_{(SCLK)}$	V_{VBD} = 1.8V			20	MHz
		V_{VBD} = 3V			20	MHz
		V_{VBD} = 5V			20	MHz

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Tested under natural convection and chip mounted on low effective single-layer PCB in accordance with JESD5-3.

Note 3: The device is not guaranteed to function outside its recommended operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J = 25℃$. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design or statistical correlation and not production tested.

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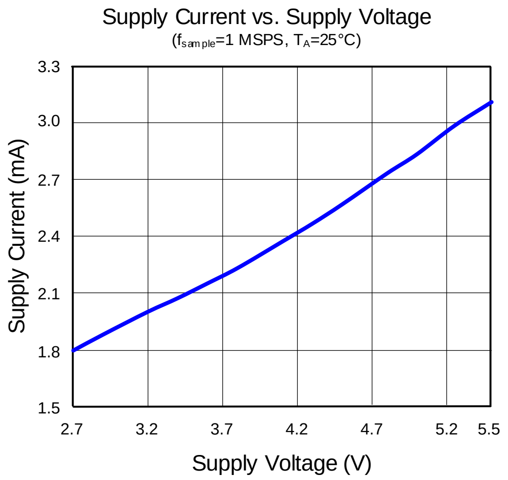
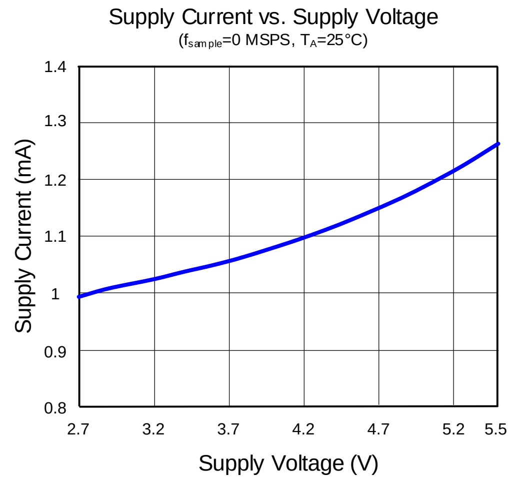
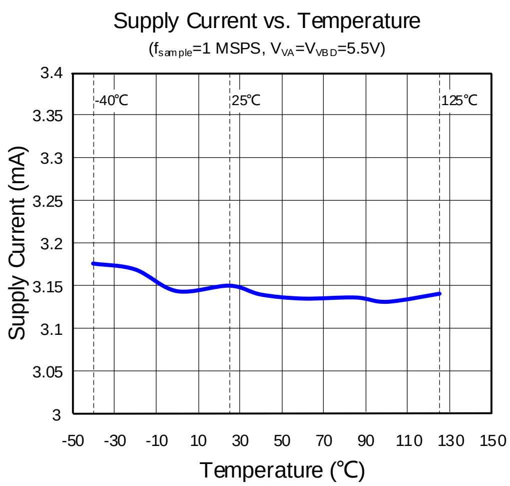
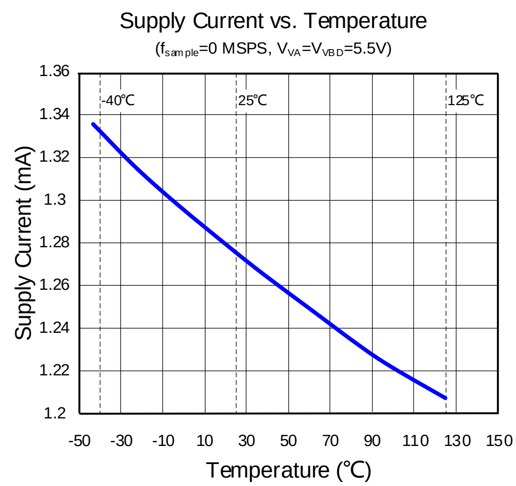
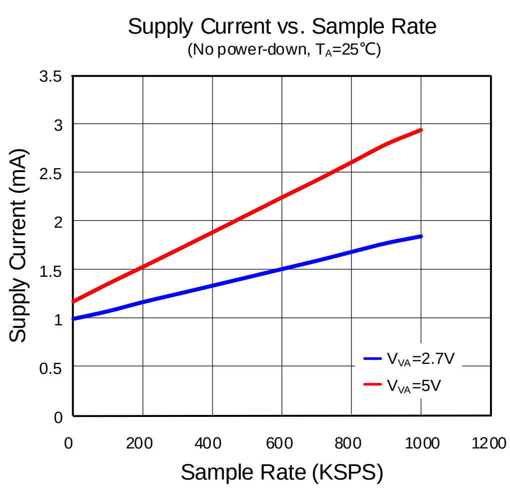
Typical Performance Characteristics

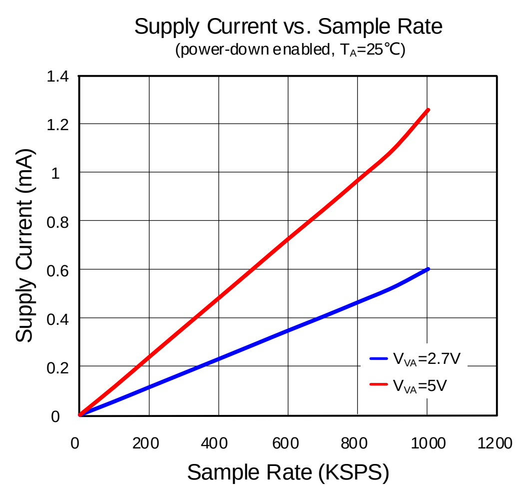












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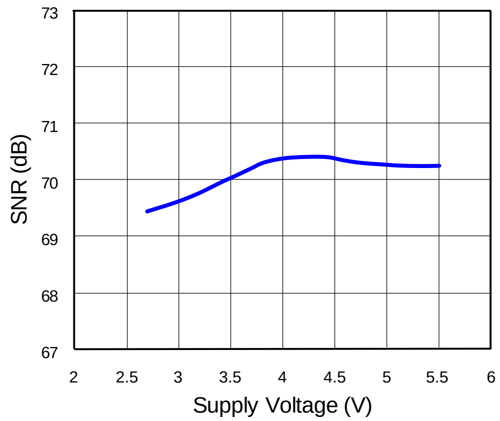
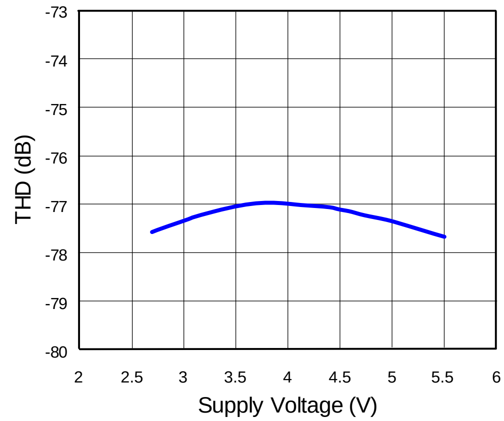
SNR vs. Supply Voltage
(f_{sample}=1MSPS, f_{input}=100kHz, T_A=25°C, V_{VBD}=3V)



THD vs. Supply Voltage
(f_{sample}=1MSPS, f_{input}=100kHz, T_A=25°C, V_{VBD}=3V)



SINAD vs. Supply Voltage
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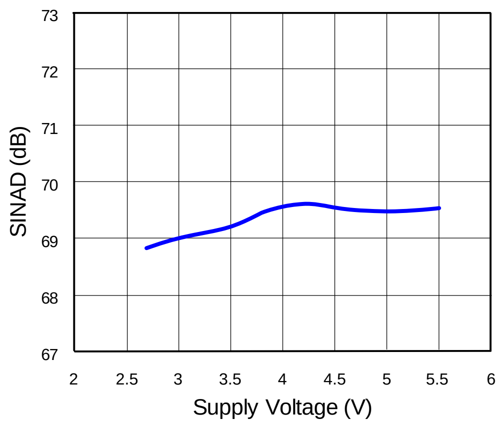

SFDR vs. Supply Voltage
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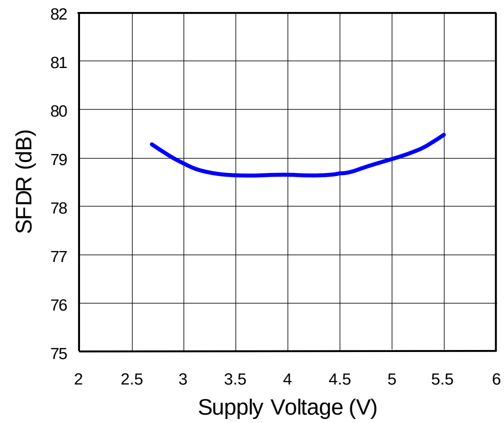
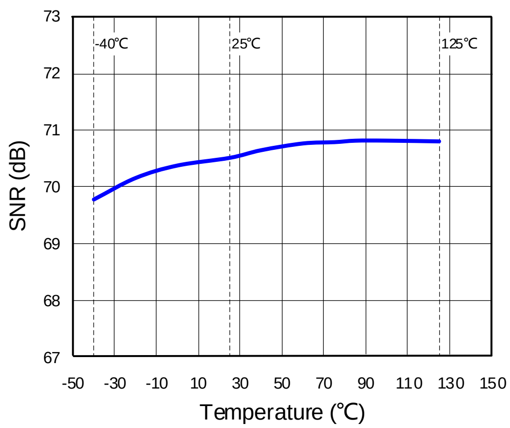
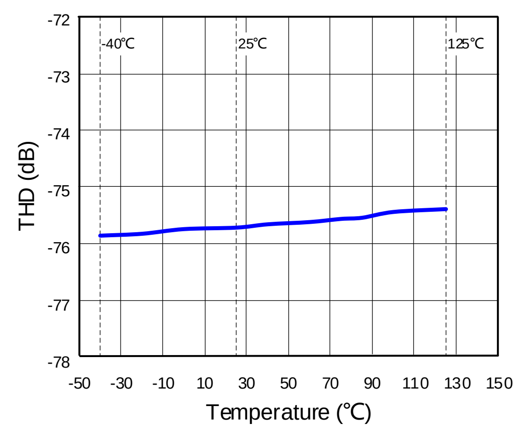


SNR vs. Temperature
(f_{sample}=1MSPS, f_{input}=100kHz, V_{VA}=5V, V_{VBD}=3V)



THD vs. Temperature
(f_{sample}=1MSPS, f_{input}=100kHz, V_{VA}=5V, V_{VBD}=3V)



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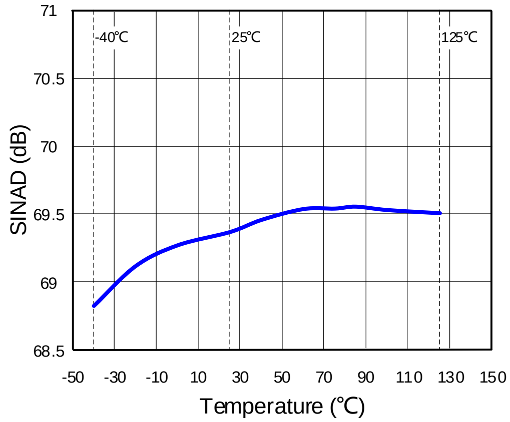
SINAD vs. Temperature
(f_{sample}=1MSPS, f_{input}=100kHz, V_{VA}=5V, V_{VBD}=3V)



SFDR vs. Temperature
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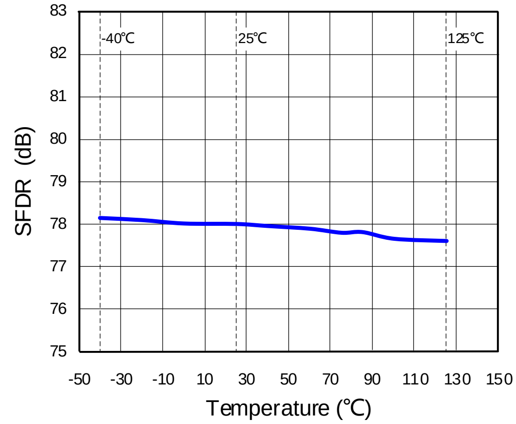
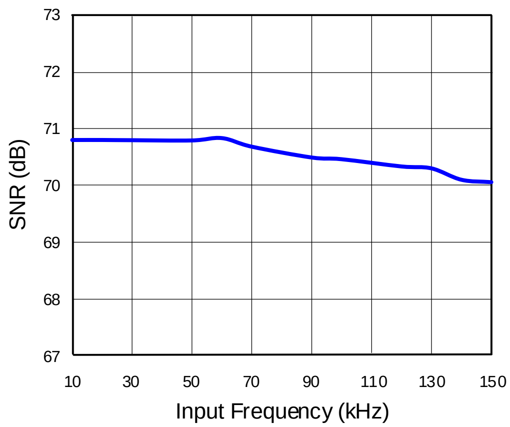
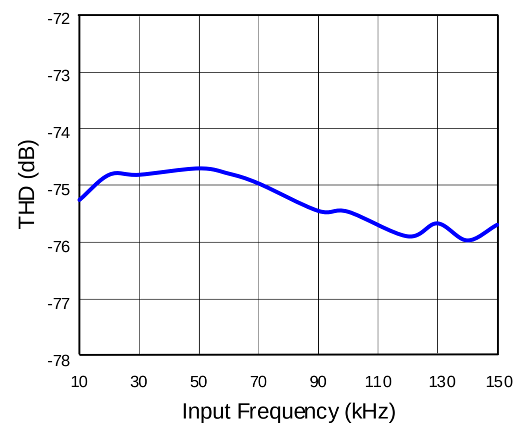


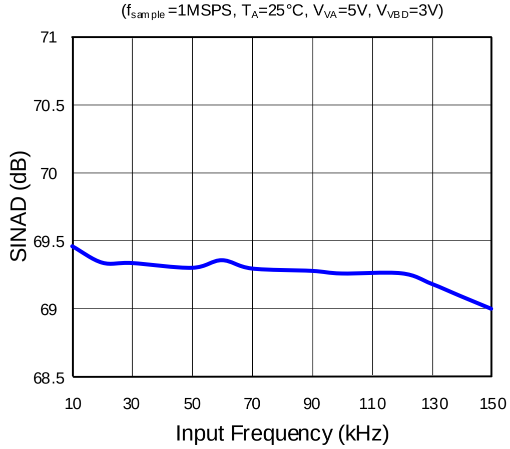
SNR vs. Input Frequency
(f_{sample}=1MSPS, T_A=25°C, V_{VA}=5V, V_{VBD}=3V)



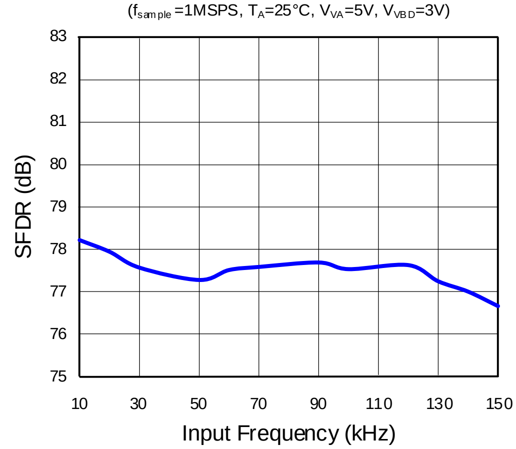
THD vs. Input Frequency
(f_{sample}=1MSPS, T_A=25°C, V_{VA}=5V, V_{VBD}=3V)



SINAD vs. Input Frequency
(f_{sample}=1MSPS, T_A=25°C, V_{VA}=5V, V_{VBD}=3V)



SFDR vs. Input Frequency
(f_{sample}=1MSPS, T_A=25°C, V_{VA}=5V, V_{VBD}=3V)



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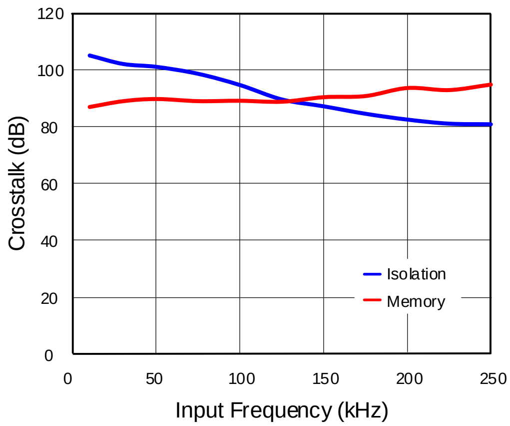
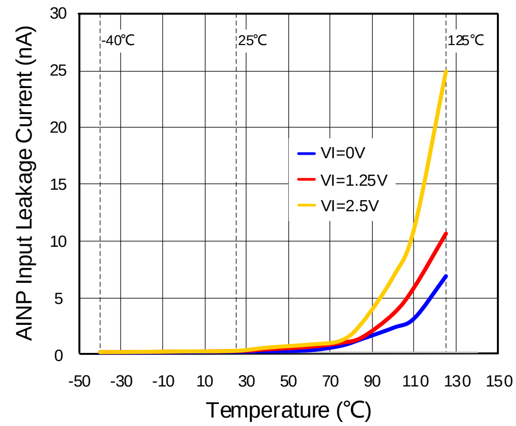
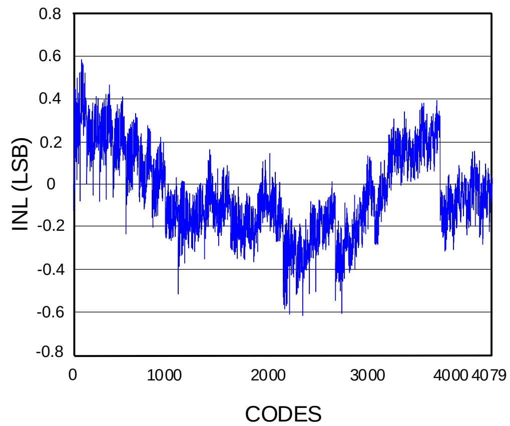
Crosstalk vs. Input Frequency
(f_{sample}=1MSPS, V_{VA}=5V, V_{VBD}=5V, CH0 and CH1)



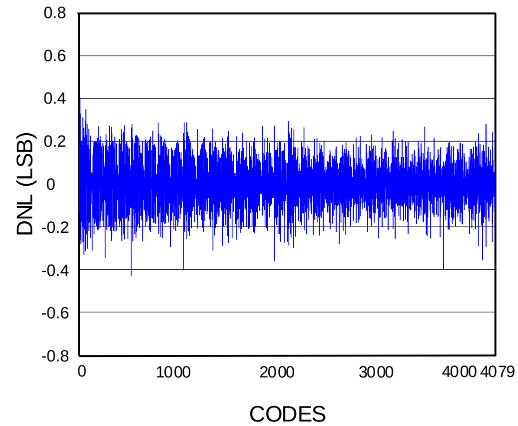
AINP Input Leakage current vs. Temperature
(V_{VA}=5V, V_{VBD}=5V)



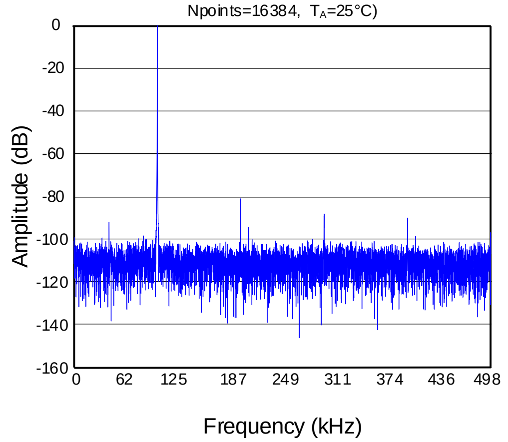
INL Error
(f_{sample} = 1MSPS, V_{VA} = 5V, V_{VBD} = 5V, T_A=25°C)



DNL Error
(f_{sample} = 1MSPS, V_{VA} = 5V, V_{VBD} = 5V, T_A=25°C)



Power Spectrum
(V_{VA}=5V, V_{VBD}=5V, f_{input}=100kHz, f_{sample}=1MSPS,
Npoints=16384, T_A=25°C)



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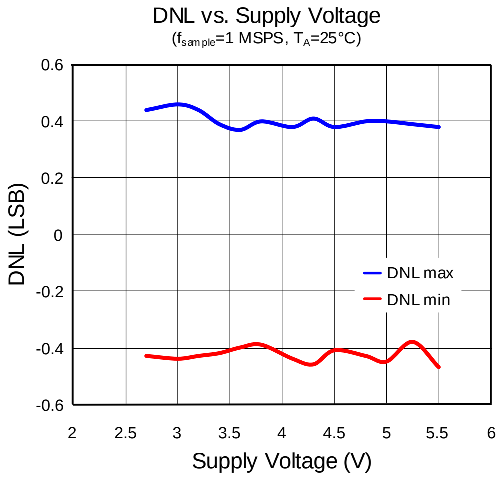
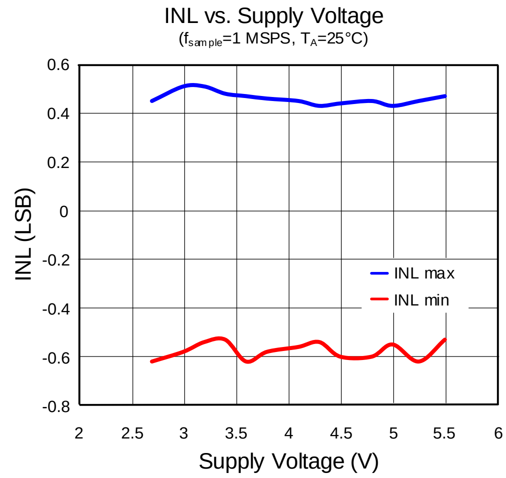
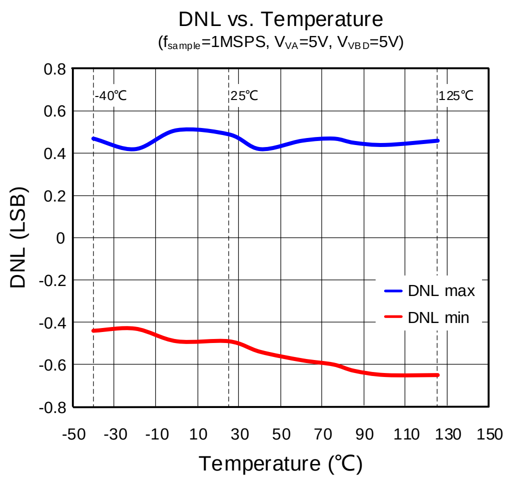
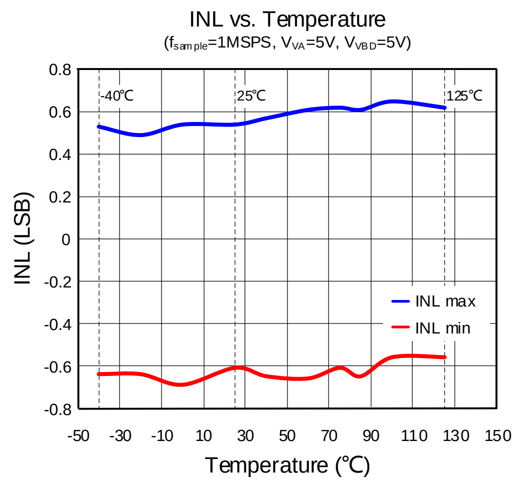
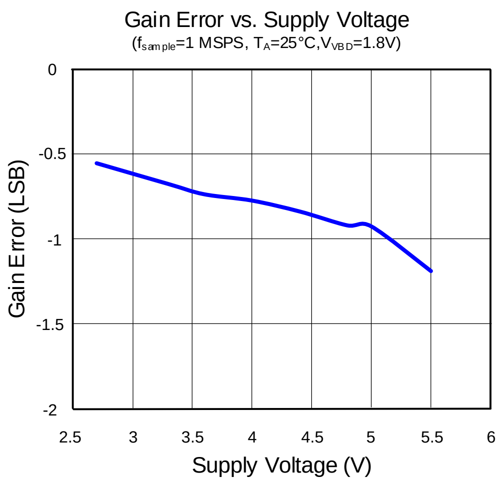
SA89851 12-Bit 8-Channel

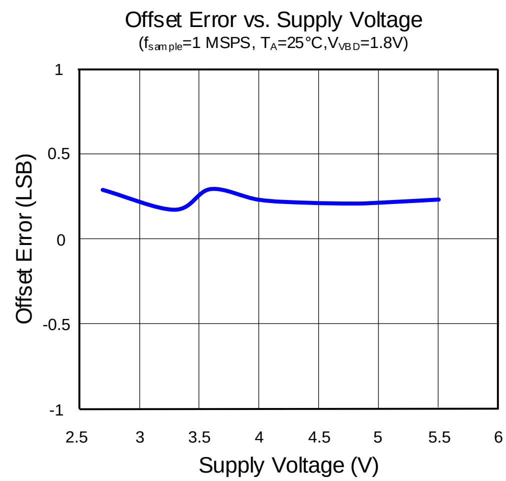












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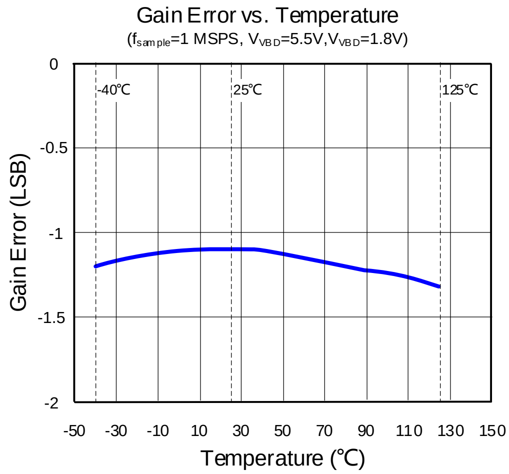

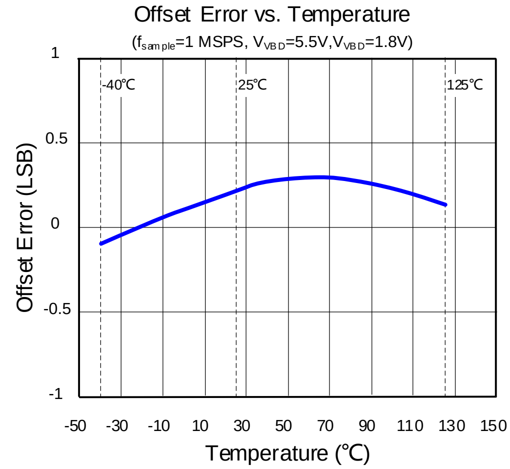

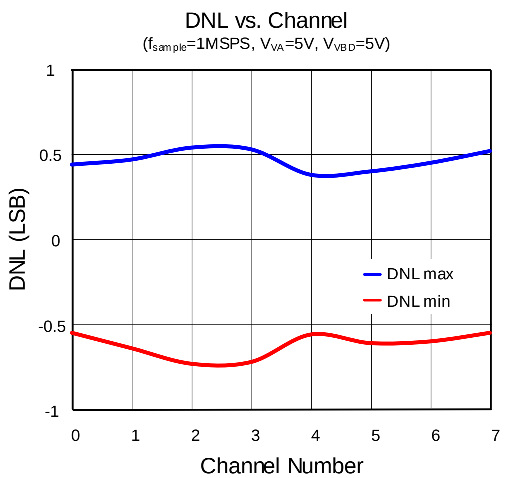

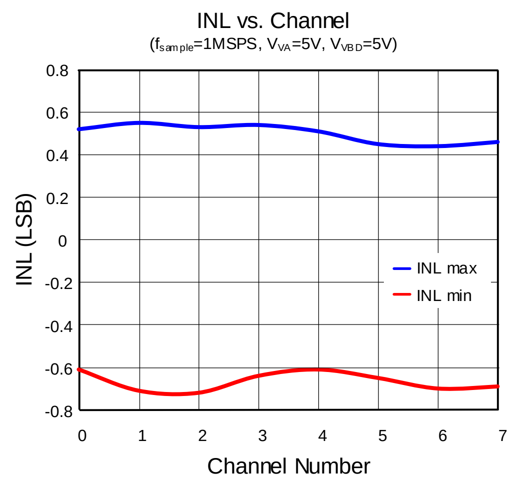

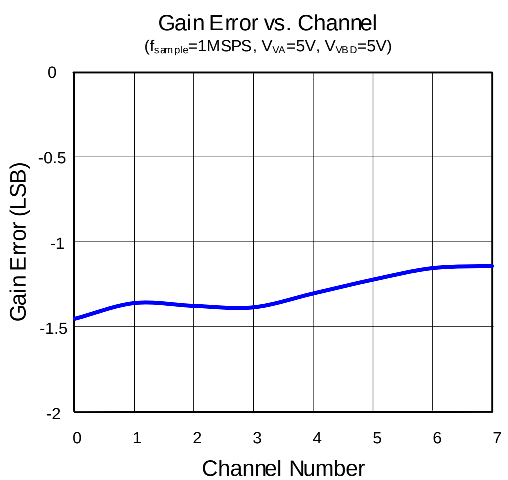

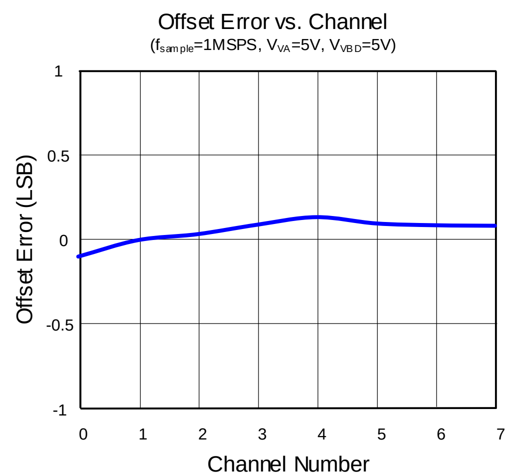

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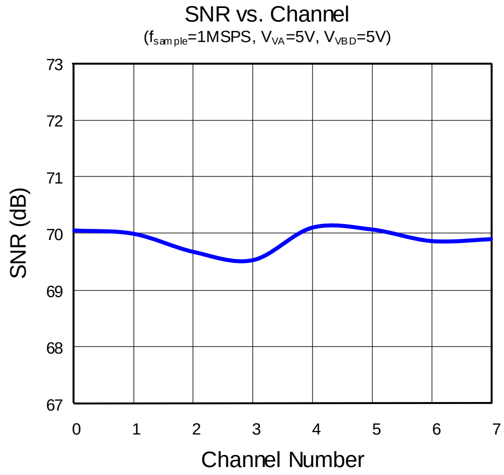

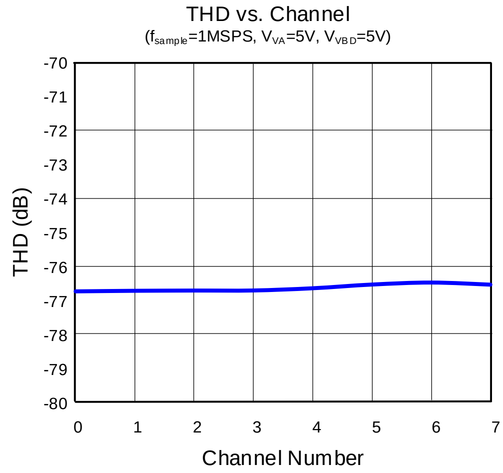

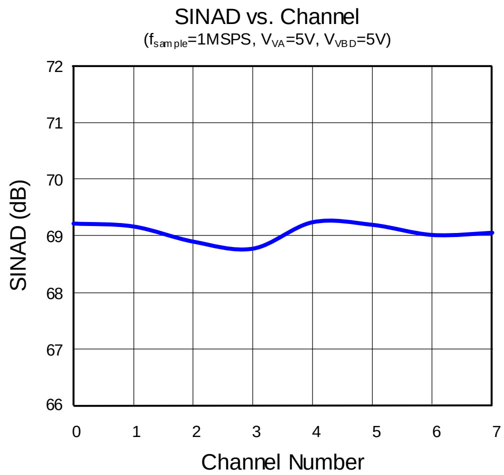

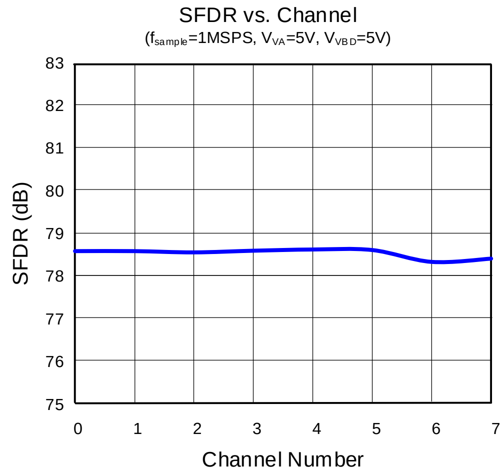

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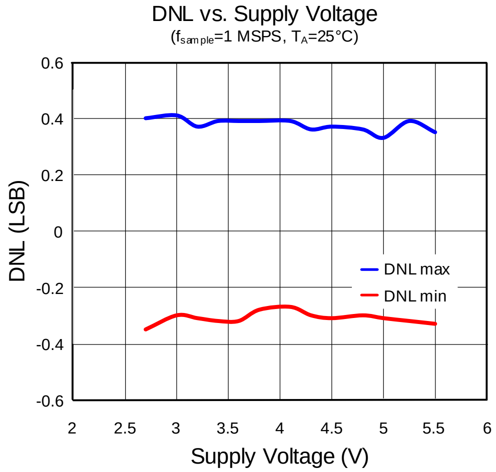
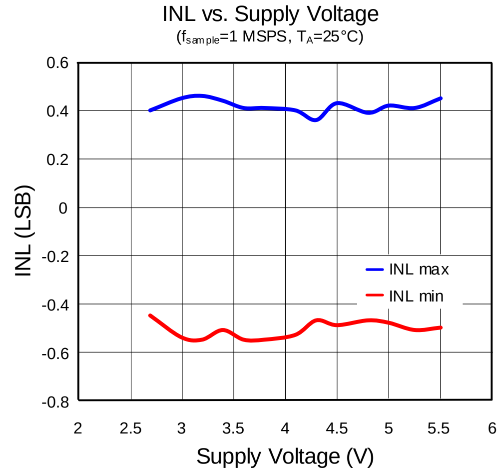
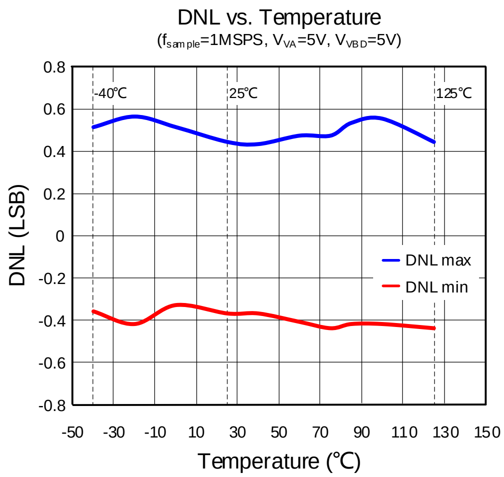
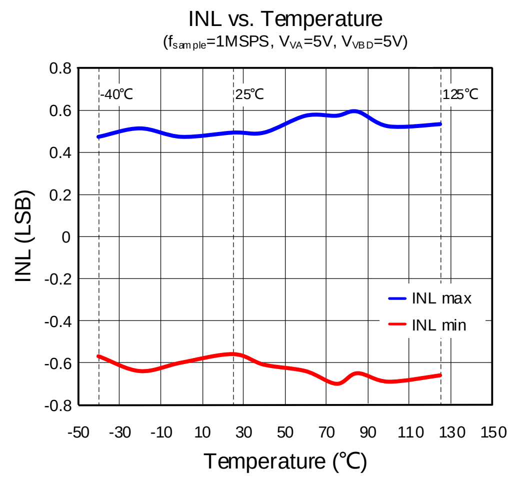
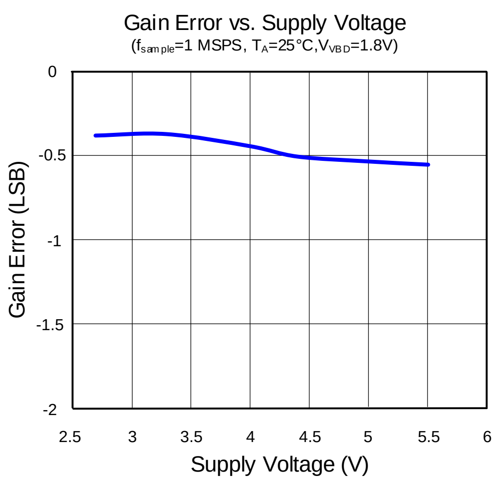
SA89853 12-Bit 16-Channel

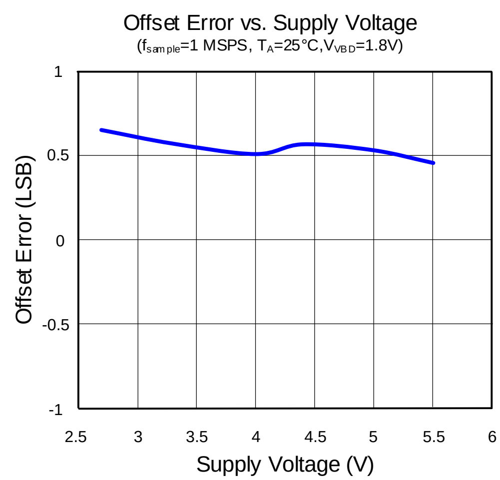












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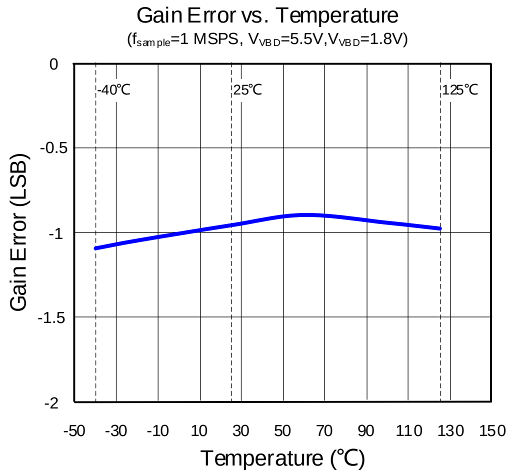

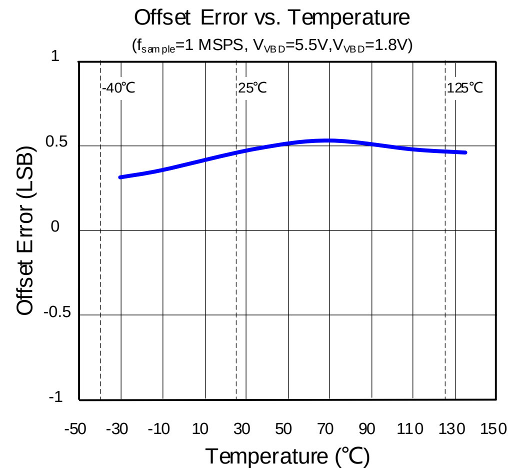

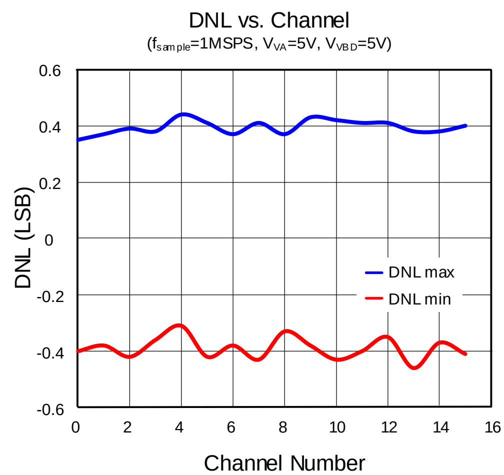

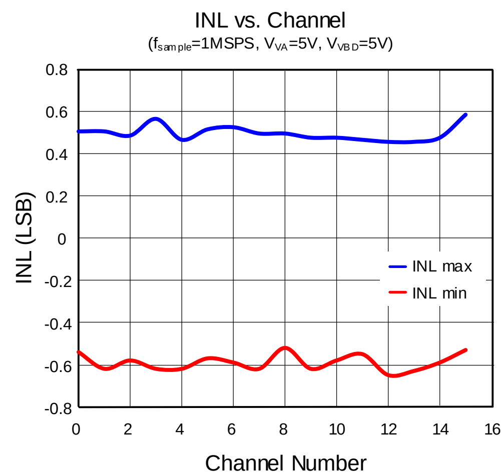

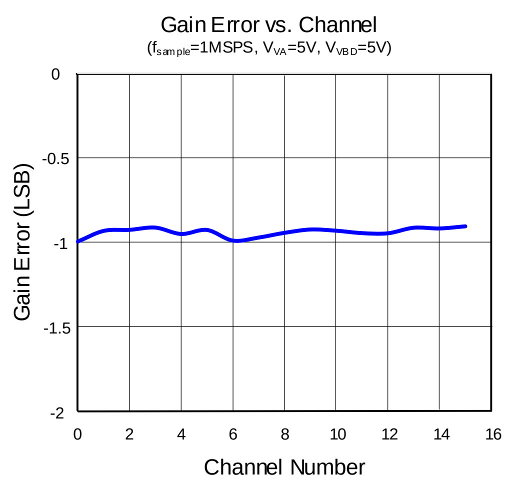

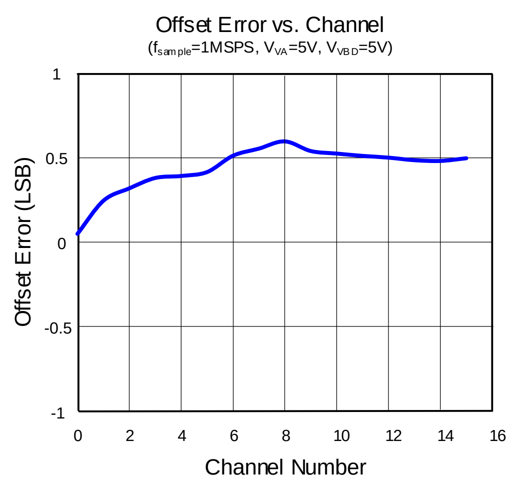

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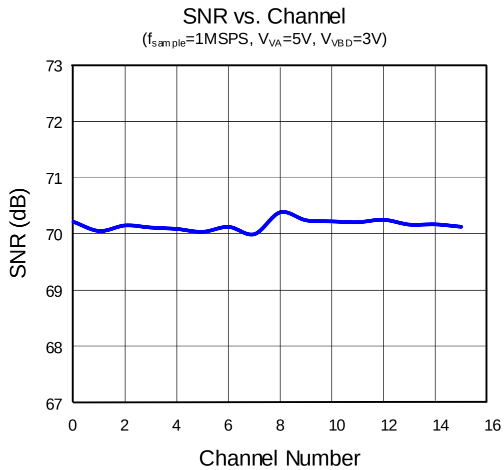

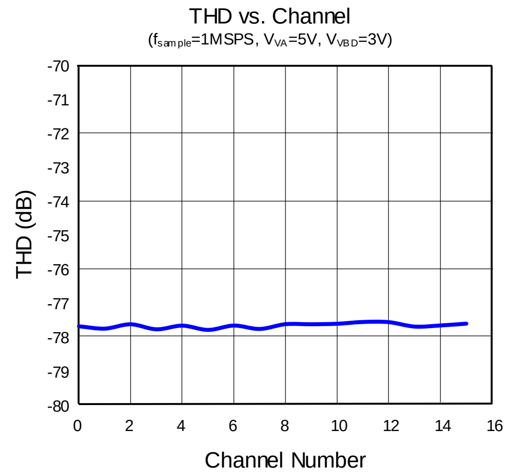

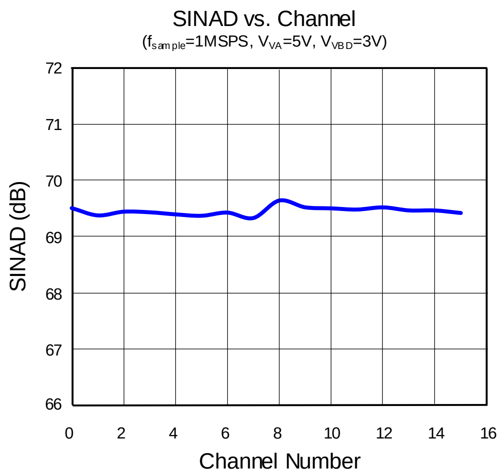

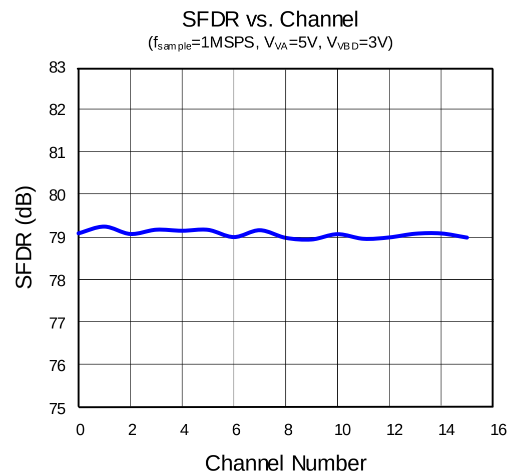

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Definitions

Total Harmonic Distortion (THD)

The total harmonic distortion, measured in decibels, quantifies the deviations between the attenuated input waveform of an ADC and an ideal sine wave reference. THD serves as an indicator of the harmonic components that are present in the ADC input signal.

Signal-to-Noise Ratio (SNR)

The signal-to-noise ratio, measured in decibels, defines the ratio of signal power to noise power. A high SNR means the signal is clear and easy to detect or interpret.

Signal-to-Noise + Distortion (SINAD)

The signal-to-noise ratio + distortion, measured in decibels, defines the ratio of signal power to noise-plus-distortion power. SINAD combines the effect of noise and distortion power, which indicates the ADC sensitivity performance.

Spurious-Free Dynamic Range (SFDR)

The spurious-free dynamic range, measured in decibels, quantifies the strength ratio of the fundamental signal to the strongest spurious signal in the input. SFDR serves as an indicator of the effective signal range.

Channel-to-Channel Crosstalk

The channel-to-channel crosstalk, measured in decibels, quantifies the effect of the full-scale input signal from one channel to another.

Isolation crosstalk is the effect of any off-channel with full-scale input to the other sampled channel.

Memory crosstalk is the effect of the previous sampled channel with full-scale input to the current sampled channel.

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Functional Description

Overview

The SA89851/3 device is a 12-bit high-speed multi-channel SAR A/D converter, which uses an external reference and serial clock to run the conversion. The sample rate can be controlled by setting the CS_N period.

The input channel is selected through the multiplexer, and then the output can be shorted directly to the AINP pin or be connected through a buffer to the AINP pin. The differential input between the AINP and AINM pins is sampled during the conversion. The ADC code can be read back through SPI communication.

The device offers two input ranges (0V to VREF and 0V to 2xVREF), selectable through the mode control register or GPIO2 pin. It features a power-down function to conserve power when inactive. Additionally, the device has four general-purpose input and output (GPIO) pins, which support the alarm function for high and low thresholds on each channel.

Device Operation Timing

Figures 3 and 4 illustrate the operation timing of the device. The device's functionality is configured through the CS_N, SCLK, and SDI pins, while the conversion data is output from the SDO pin.

On the falling edge of the CS_N pin, the device samples the input signal from the chosen channel, initiating the conversion process. The conversion process ends on the sixteenth falling edge of the SCLK pin. The 16-bit output data on the SDO pin includes a 4-bit channel address or GPIO status (see **Table 1**, **Table 2**, and **Table 5**), followed by the 12-bit ADC conversion data. At the same time, a new channel is selected through the multiplexer on the second falling edge of the SCLK pin, with the acquisition time for this newly selected channel starting on the fourteenth rising edge of the SCLK and ending on the next falling edge of CS_N pin.

The device is equipped with four individually configurable GPIOs, which can be configured as either GPI or GPO. GPI data is latched on the falling edge of the CS_N pin and mapped onto bits DO15-12 when the DI04 bit is set to 1 in the previous frame. GPO data can be set through the SDI pin and updated on the falling edge of the CS_N pin.

The 16-bit data input on the SDI pin is clocked in on each rising edge of the SCLK pin. The DO15 bit is clocked out on the SDO pin on the falling edge of the CS_N pin, and the remaining 15 bits are clocked out on each falling edge of the SCLK pin.

GPIO0 and GPIO1 can be configured to serve as low or high alarms, signaling when the input signal crosses the predefined alarm thresholds. The alarm is activated on the twelfth falling edge of the SCLK pin within the same frame and is reset on the tenth falling edge of the SCLK pin in the next frame.

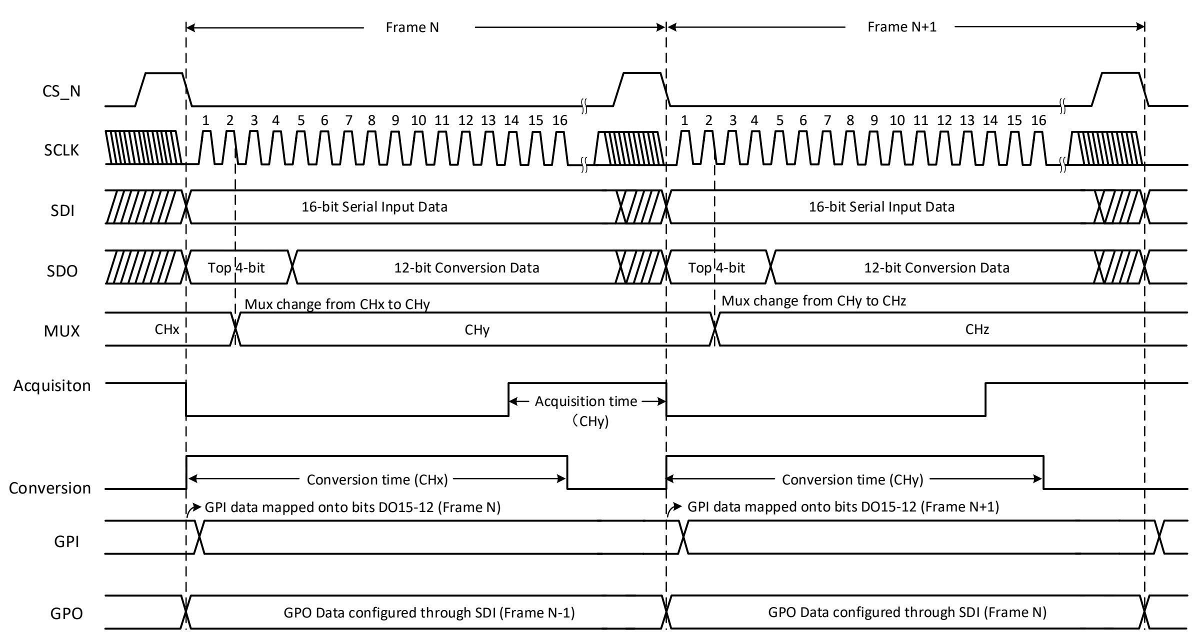

Figure 3. Device Operation Timing

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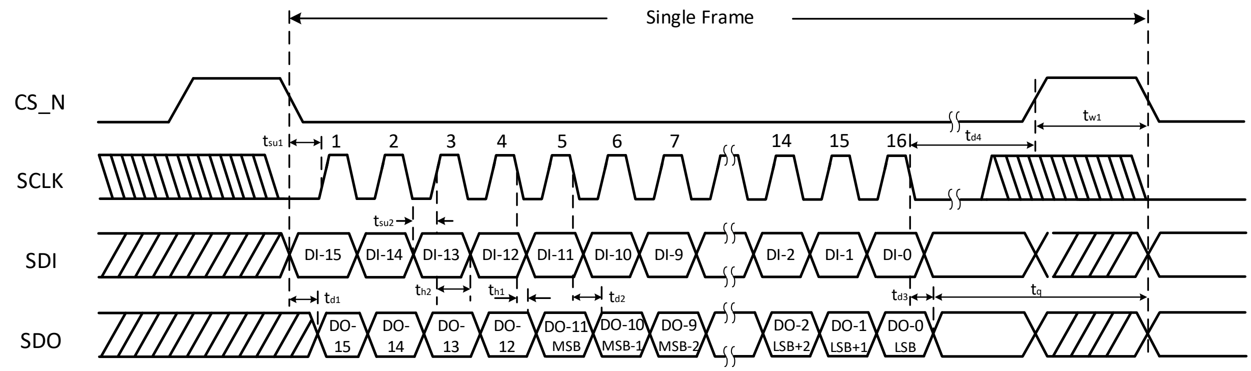

Figure 4. SPI Timing Diagram

Initialization Setup

Figure 5 shows the initialization setup. Following a power-up or reset, the device starts in manual mode on channel 0. The user should program the registers to configure GPIOs, set the low/high alarms, and determine the channel sequence for automatic operation. Once those settings are configured, the device can operate in various channel sequencing modes, including manual, auto-1, and auto-2 modes.

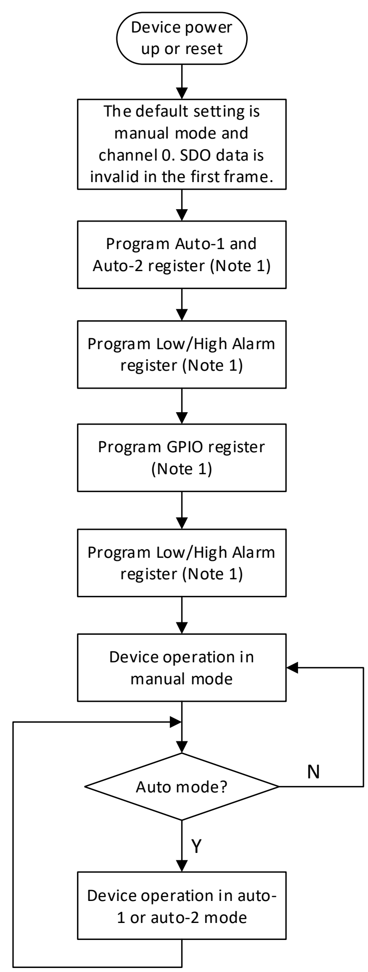

Figure 5. Device Initialization Setup

Note 1: Throughout the programming setup, the device remains in manual mode and on channel 0, providing valid conversion data. During this setup phase, channel and range selection or GPIO configuration can be performed. Any programming step can be bypassed if not required.

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Analog Input

Figure 6 illustrates the equivalent circuit for the multiplexer and ADC input. The multiplexer is switched to the selected channel, and the internal capacitors of MXO/AINP are charged. Then, the voltage difference between the AINP and AINM pin is sampled on the internal capacitor array, and the device outputs conversion data in the next frame.

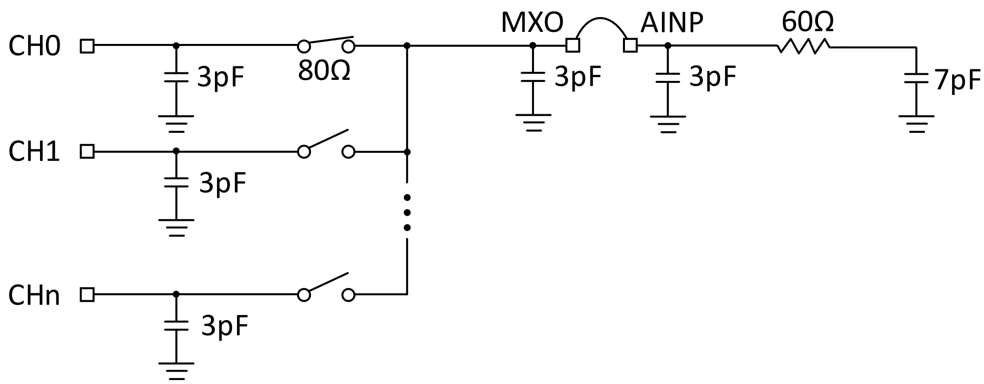

Figure 6. Multiplexer and ADC Input Equivalent Circuit

Device Operating Modes

The device can be set to either manually select a channel (manual mode) or automatically cycle through chosen channels (auto-1, auto-2 modes). In manual mode, the channel is specified in each frame, and the device will select this channel for the next frame. Upon power-up or following a reset, the device defaults to manual mode and channel-0.

Manual Mode

Figure 7 shows the device operation timing diagram in manual mode, which selects channels CH2, CH4, and CH6 in sequence. **Table 1** lists the settings of the mode control register for manual mode. Prior register programming is not required for manual mode operation.

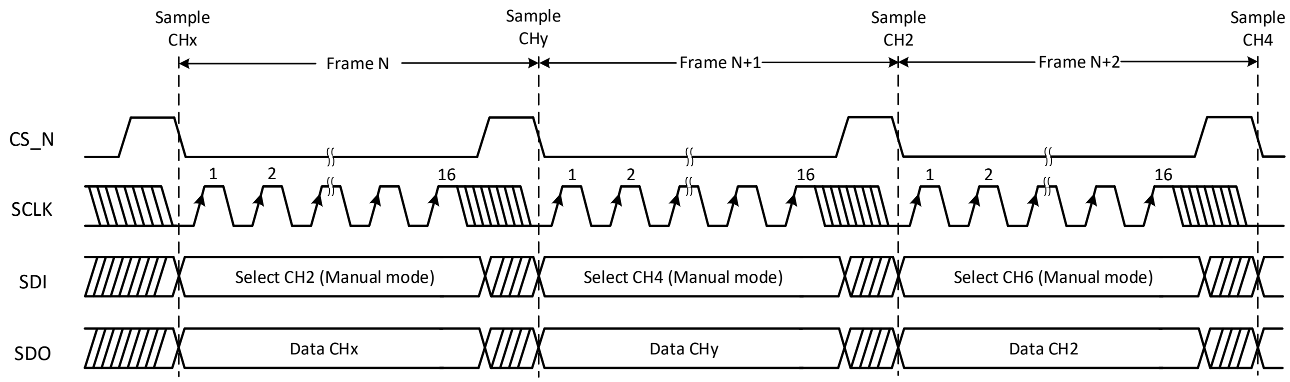

Figure 7. Device Operation Timing Diagram for Manual Mode

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Table 1. Mode Control Register Setting for Manual Mode

<table>
<tr><th>Bits</th><th>Reset State</th><th>Logic State</th><th colspan="4">Description</th></tr>
<tr><td>DI15-12</td><td>0001</td><td>0001</td><td colspan="4">Selects manual mode.</td></tr>
<tr><td rowspan="2">DI11</td><td rowspan="2">0</td><td>1</td><td colspan="4">Enables programming of bits DI [06:00].</td></tr>
<tr><td>0</td><td colspan="4">The device retains values of bits DI [06:00] from the previous frame.</td></tr>
<tr><td>DI10-07</td><td>0000</td><td>-</td><td colspan="4">This 4-bit data represents the address of the next channel to be selected in the next frame. DI10 = MSB and DI07 = LSB. For example, 0000 represents channel-0, 0001 represents channel-1, and so on.</td></tr>
<tr><td rowspan="2">DI06</td><td rowspan="2">0</td><td>0</td><td colspan="4">Selects 0 to VREF input range (range 1).</td></tr>
<tr><td>1</td><td colspan="4">Selects 0 to 2xVREF input range (range 2).</td></tr>
<tr><td rowspan="2">DI05</td><td rowspan="2">0</td><td>0</td><td colspan="4">Normal operation (no power down).</td></tr>
<tr><td>1</td><td colspan="4">Powers down on the 16th SCLK falling edge.</td></tr>
<tr><td rowspan="4">DI04</td><td rowspan="4">0</td><td>0</td><td colspan="4">The 16-bit SDO output data is the current channel address on DO [15:12], and a 12-bit conversion data on bits DO [11:00].</td></tr>
<tr><td rowspan="3">1</td><td colspan="4">The GPIO3-GPIO0 data (both input and output) is mapped onto DO [15:12] in the below order. The remaining 12-bit data DO [11:00] represents the 12-bit conversion data of the current channel.</td></tr>
<tr><td>DO15</td><td>DO14</td><td>DO13</td><td>DO12</td></tr>
<tr><td>GPIO3</td><td>GPIO2</td><td>GPIO1</td><td>GPIO0</td></tr>
<tr><td rowspan="3">DI03-00</td><td rowspan="3">0000</td><td rowspan="3">-</td><td colspan="4">The GPIO data configured as output will output the corresponding bit setting, and data configured as input will be ignored. The SDI bit and corresponding GPIO information is shown below.</td></tr>
<tr><td>DI03</td><td>DI02</td><td>DI01</td><td>DI00</td></tr>
<tr><td>GPIO3</td><td>GPIO2</td><td>GPIO1</td><td>GPIO0</td></tr>
</table>

Auto-1 Mode

Figure 8 shows the device operation timing diagram for auto-1 mode. The device scans all selected channels in sequence (CH1, CH3, CH5, CH7 are selected in this example).

Table 2 lists the settings of mode control register settings for auto-1 mode.

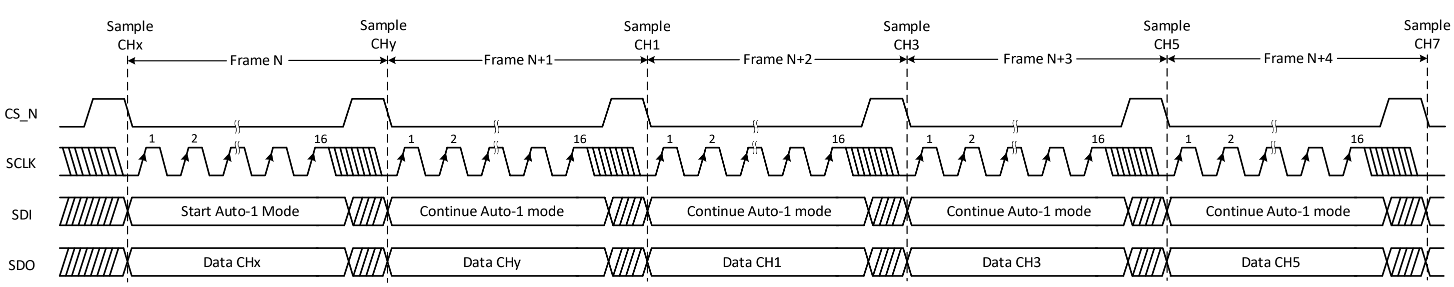

Figure 8. Device Operation Timing Diagram for Auto-1 Mode

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Table 2. Mode Control Register Setting for Auto-1 Mode

<table>
<tr><th>Bits</th><th>Reset State</th><th>Logic State</th><th colspan="4">Description</th></tr>
<tr><td>DI15-12</td><td>0001</td><td>0010</td><td colspan="4">Selects auto-1 mode.</td></tr>
<tr><td rowspan="2">DI11</td><td rowspan="2">0</td><td>1</td><td colspan="4">Enables programming of bits DI [10:00].</td></tr>
<tr><td>0</td><td colspan="4">The device retains values of bits DI [10:00] from the previous frame.</td></tr>
<tr><td rowspan="2">DI10</td><td rowspan="2">0</td><td>1</td><td colspan="4">The channel is reset to the lowest programmed channel in the auto-1 program register.</td></tr>
<tr><td>0</td><td colspan="4">The channel counter increments with each conversion (no reset).</td></tr>
<tr><td>DI09-07</td><td>000</td><td>-</td><td colspan="4">Do not care.</td></tr>
<tr><td rowspan="2">DI06</td><td rowspan="2">0</td><td>0</td><td colspan="4">Selects 0 to VREF input range (range 1).</td></tr>
<tr><td>1</td><td colspan="4">Selects 0 to 2xVREF input range (range 2).</td></tr>
<tr><td rowspan="2">DI05</td><td rowspan="2">0</td><td>0</td><td colspan="4">Normal operation (no power down).</td></tr>
<tr><td>1</td><td colspan="4">Powers down on the 16th SCLK falling edge.</td></tr>
<tr><td rowspan="4">DI04</td><td rowspan="4">0</td><td>0</td><td colspan="4">The 16-bit SDO output data is the current channel address on DO [15:12], and a 12-bit conversion data on bits DO [11:00].</td></tr>
<tr><td rowspan="3">1</td><td colspan="4">The GPIO3-GPIO0 data (both input and output) is mapped onto DO [15:12] in the below order. The remaining 12-bit data DO [11:00] represents the 12-bit conversion data of the current channel.</td></tr>
<tr><td>DO15</td><td>DO14</td><td>DO13</td><td>DO12</td></tr>
<tr><td>GPIO3</td><td>GPIO2</td><td>GPIO1</td><td>GPIO0</td></tr>
<tr><td rowspan="3">DI03-00</td><td rowspan="3">0000</td><td rowspan="3">-</td><td colspan="4">The GPIO data configured as output will output the corresponding bit setting, and data configured as input will be ignored. The SDI bit and corresponding GPIO information is shown below.</td></tr>
<tr><td>DI03</td><td>DI02</td><td>DI01</td><td>DI00</td></tr>
<tr><td>GPIO3</td><td>GPIO2</td><td>GPIO1</td><td>GPIO0</td></tr>
</table>

The auto-1 program register is programmed to select the channels for the auto-1 sequence on power up or reset, shown in *Figure 9*. In the first frame, the device enters auto-1 register programming sequence, and in the second frame, the device programs the preselected channels. See Tables 3 and 4 for the program registers setting in auto-1 mode.

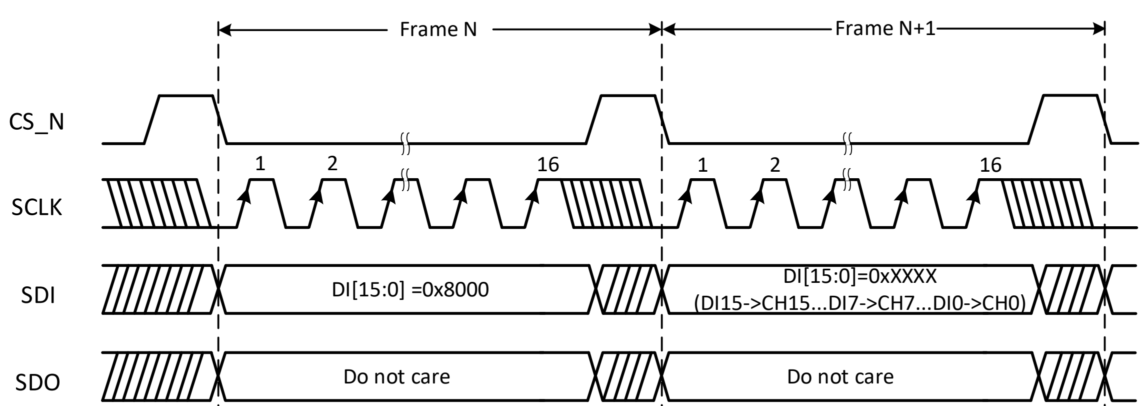

Figure 9. Program Auto-1 Mode Register

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Table 3. Program Registers Setting for Auto-1 Mode

Bits	Reset State	Logic State	Description
Frame 1			
DI15-12	NA	1000	Enter auto-1 program sequence.
DI11-00	NA	-	Do not care.
Frame 2			
DI15-00	All 1's	0 (individual bit)	A particular channel is programmed to be skipped in the auto-1 sequence. The channel numbers are one-to-one associated with SDI bits. For example, DI15 corresponds to CH15...DI7 corresponds to CH7…DI0 corresponds to CH0.
		1 (individual bit)	A particular channel is programmed to be preselected in the auto-1 sequence. The channel numbers are one-to-one associated with SDI bits. For example, DI15 corresponds to CH15...DI7 corresponds to CH7…DI0 corresponds to CH0.

Table 4. Mapping of Channels to SDI Bits in Auto-1 Mode

Device (Note 2)	SDI Bits															
	DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
8 Channels	-	-	-	-	-	-	-	-	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
16 Channels	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

Note 2: For 16 channels version, if channel 15 is preselected in auto-1 mode program, preselect at least one channel in channel 12-14.

Auto-2 Mode

Figure 10 shows the device operation timing diagram for auto-2 mode. The device scans from channel 0 to the last channel. **Table 5** lists the mode control register settings for auto-2 mode.

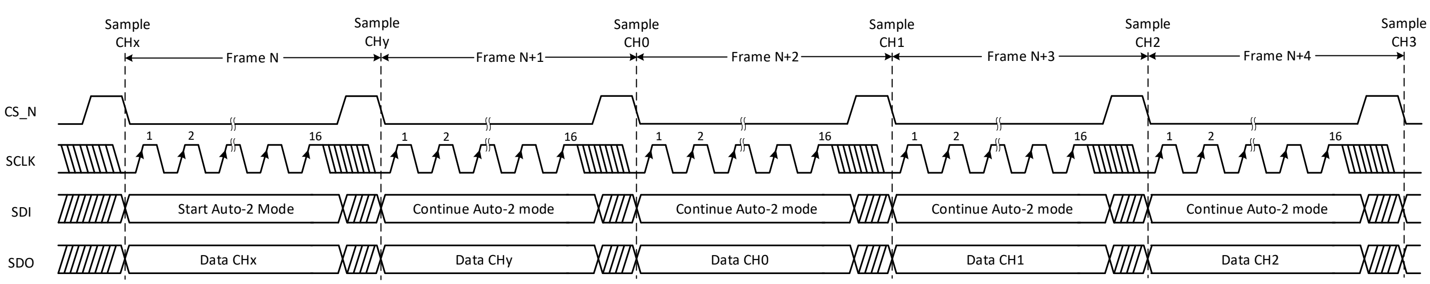

Figure 10. Device Operation Timing Diagram for Auto-2 Mode

Table 5. Mode Control Register Setting for Auto-2 Mode

Bits	Reset State	Logic State	Description
DI15-12	0001	0011	Selects auto-2 mode.

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<table>
<tr><td rowspan="2">DI11</td><td rowspan="2">0</td><td>1</td><td colspan="4">Enables programming of bits DI [10:00].</td></tr>
<tr><td>0</td><td colspan="4">The device retains values of bits DI [10:00] from the previous frame.</td></tr>
<tr><td rowspan="2">DI10</td><td rowspan="2">0</td><td>1</td><td colspan="4">The channel is reset to channel 0.</td></tr>
<tr><td>0</td><td colspan="4">The channel counter increments every conversion (no reset).</td></tr>
<tr><td>DI9-07</td><td>000</td><td>-</td><td colspan="4">Do not care.</td></tr>
<tr><td rowspan="2">DI06</td><td rowspan="2">0</td><td>0</td><td colspan="4">Selects 0 to VREF input range (range 1).</td></tr>
<tr><td>1</td><td colspan="4">Selects 0 to 2xVREF input range (range 2).</td></tr>
<tr><td rowspan="2">DI05</td><td rowspan="2">0</td><td>0</td><td colspan="4">Normal operation (no power down).</td></tr>
<tr><td>1</td><td colspan="4">Powers down on the 16th SCLK falling edge.</td></tr>
<tr><td rowspan="4">DI04</td><td rowspan="4">0</td><td>0</td><td colspan="4">The 16-bit SDO output data is the current channel address on DO [15:12] and the 12-bit conversion data on bits DO [11:00].</td></tr>
<tr><td rowspan="3">1</td><td colspan="4">The GPIO3-GPIO0 data (both input and output) is mapped onto DO [15:12] in the below order. The remaining 12-bit data DO [11:00] represents the 12-bit conversion data of the current channel.</td></tr>
<tr><td>DO15</td><td>DO14</td><td>DO13</td><td>DO12</td></tr>
<tr><td>GPIO3</td><td>GPIO2</td><td>GPIO1</td><td>GPIO0</td></tr>
<tr><td rowspan="3">DI03-00</td><td rowspan="3">0000</td><td rowspan="3">-</td><td colspan="4">The GPIO data configured as output will output the corresponding bit setting, and data configured as input will be ignored. The SDI bit and corresponding GPIO information is shown below.</td></tr>
<tr><td>DI03</td><td>DI02</td><td>DI01</td><td>DI00</td></tr>
<tr><td>GPIO3</td><td>GPIO2</td><td>GPIO1</td><td>GPIO0</td></tr>
</table>

The auto-2 program register is programmed to select the last channel for the auto-2 sequence on power up or reset, as shown in *Figure 11*. The device enters the auto-2 programming sequence and completes programming in only one frame. See **Table 6** for the program registers setting in auto-2 mode.

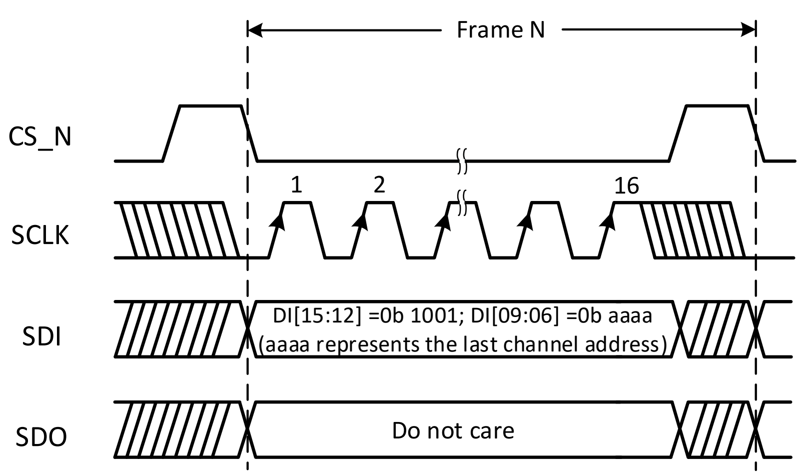

Figure 11. Program Auto-2 Mode Register

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Table 6. Program Registers Setting for Auto-2 Mode

Bits	Reset State	Logic State	Description
DI15-12	NA	1001	Enter auto-2 program sequence.
DI11-10	NA	-	Do not care.
DI09-06	NA	aaaa	This 4-bit data denotes the address of the last channel for auto-2 mode. When in auto-2 mode, the channel counter begins at channel 0 and increments every frame until the counter equals ‘aaaa’. The channel counter rolls over to channel 0 in the next frame.
DI05-00	NA	-	Do not care.

Continuous Operation in a Selected Mode

When the device operates in one of the modes described above, the device can continue in the same mode using the register settings below.

Table 7. Continued Operation in a Selected Mode

Bits	Reset State	Logic State	Description
DI15-12	0001	0000	The chip maintains its operation in the current mode. In auto-1 and auto-2 modes, the channel counter automatically increments, while in manual mode, the device keeps the previously selected channel. Data on DI [11:0] should be disregarded, and operations will proceed with the prior settings. The SDI can be kept low when there are no updates to the mode control register.
DI11-10	All 0	-	These bits are ignored when DI [15:12] bits are set to 0000.

Digital Output

The digital output can be read back using the SPI interface. **Table 8** shows the output codes corresponding to the different analog input voltages.

Table 8. Ideal Analog Input Voltages and Output Codes

Description	Analog Value		Digital Output (Binary Code)
Full-Scale Range	Range 1	Range 2	-
Least Significant Bit (LSB)	VREF/4096	2VREF/4096	-
Full-Scale	VREF - 1LSB	2VREF - 1LSB	1111 1111 1111
Midscale	VREF/2	VREF	1000 0000 0000
Midscale - 1LSB	VREF/2 - 1LSB	VREF - 1LSB	0111 1111 1111
Zero	0V	0V	0000 0000 0000

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GPIO Registers

The device has four general-purpose input and output pins, which can be independently programmed as general-purpose input (GPI) or general-purpose output (GPO). The GPO data can be written into the device through the SDI line and refreshed on every CS_N falling edge. See *Figure 12* and **Table 9** for the GPIO operation timing diagram and register settings.

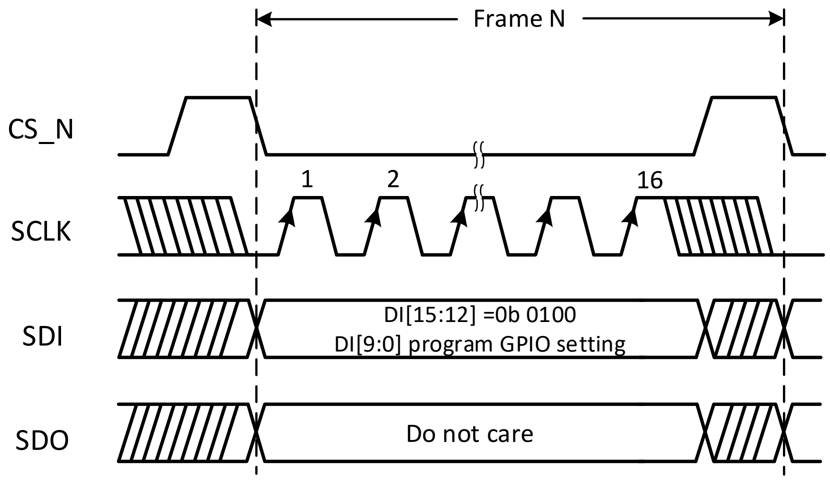

Figure 12. Program GPIO Register

Table 9. GPIO Program Registers Setting

Bits	Reset State	Logic State	Description
DI15-12	NA	0100	Enter the GPIO program sequence.
DI11-10	00	00	Reserved, must be set to 00.
DI09	0	1	Resets all registers in the next CS_N frame to the reset state shown in the corresponding tables (the device also resets itself).
		0	Normal operation.
DI08	0	1	Configures the GPIO3 pin as the device power-down input.
		0	The GPIO3 pin remains a general-purpose input or output.
DI07	0	1	Configures the GPIO2 pin as a device-range input.
		0	The GPIO2 pin remains a general-purpose input or output.
DI06-04	000	000	The GPIO1 and GPIO0 pins remain a general-purpose input or output.
		xx1	Configures the GPIO0 pin as a high-alarm or low-alarm output with an active high output. GPIO1 remains a general-purpose input or output.
		010	Configures GPIO0 as a high-alarm output with an active high output. The GPIO1 pin remains a general-purpose input or output.
		100	Configures GPIO1 as a low-alarm output with an active high output. The GPIO0 pin remains a general-purpose input or output.

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		110	Configures GPIO1 as a low-alarm output and the GPIO0 pin as a high-alarm output. These are both active high outputs.
DI03 (Note 3)	0	1	The GPIO3 pin is configured as general-purpose output.
		0	The GPIO3 pin is configured as general-purpose input.
DI02 (Note 3)	0	1	The GPIO2 pin is configured as general-purpose output.
		0	The GPIO2 pin is configured as general-purpose input.
DI01 (Note 3)	0	1	The GPIO1 pin is configured as general-purpose output.
		0	The GPIO1 pin is configured as general-purpose input.
DI00 (Note 3)	0	1	The GPIO0 pin is configured as general-purpose output.
		0	The GPIO0 pin is configured as general-purpose input.

Note 3: The following settings are valid for the GPIO pins that are not assigned a specific function through DI [08:04].

Alarm Thresholds for GPIO Pins

Each channel has a separate low alarm and high alarm threshold. For simplified programming, the sixteen channels are divided into four groups and the eight channels are divided into two groups. In the first frame, the device programs the group number, and in the second frame, the device programs the channel number, low/high alarm selection, and alarm threshold. This process is shown in *Figure 13*. See **Table 10** and **11** for Alarm Groups and Alarm Program Register settings.

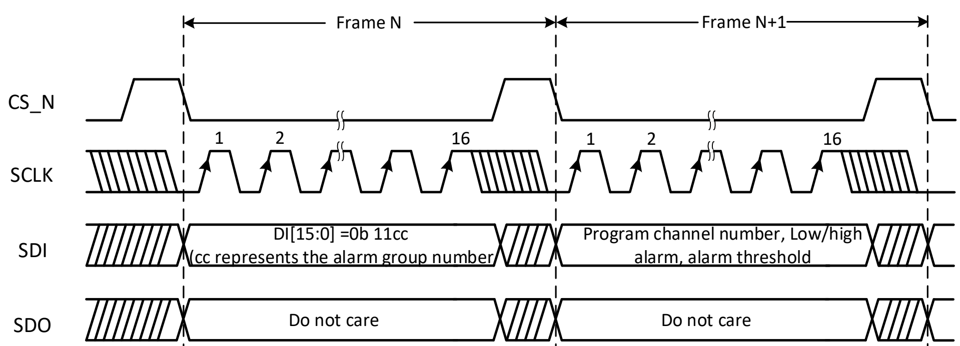

Figure 13. Program Alarm Register

Table 10. Alarm Program Registers Groups

Group	Registers	Alarm Program Register DI [15:12] (Frame 1)
0	High and low alarm for channels 0, 1, 2, and 3.	1100
1	High and low alarm for channels 4, 5, 6, and 7.	1101
2	High and low alarm for channels 8, 9, 10, and 11.	1110
3	High and low alarm for channels 12, 13, 14, and 15.	1111

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Table 11. Alarm Program Registers Settings

Bits	Reset State	Logic State	Description
Frame 1			
DI15-12 (Note 4)	NA	1100	Alarm programming sequence for group 0.
		1101	Alarm programming sequence for group 1.
		1110	Alarm programming sequence for group 2.
		1111	Alarm programming sequence for group 3.
DI11-00	NA	-	Do not care.
Frame 2			
DI15-14	NA	dd	Where 'dd' means the lower two bits of the channel number in binary format. The device programs the alarm for the channel represented by the binary number 'ccdd'. Note that 'cc' is programmed in the first frame.
DI13	NA	1	High-alarm register selection.
		0	Low-alarm register selection.
DI12	NA	1	Exit alarm programming in the next frame. To exit the alarm programming sequence, the bit must be set to one.
		0	Continue the alarm programming sequence in the next frame.
DI11-10	NA	-	Do not care.
DI09-00	High alarm: all ones Low alarm: all zeros	-	The 10-bit alarm threshold is compared against the upper 10 bits of the 12-bit conversion result stored in the alarm register.

Note 4: DI [15:12] =11cc is the alarm programming request for group cc. 'cc' refers to the group number in binary format.

Reference

The SA89851/3 device require an external reference voltage of 2~3V for optimal operation. To achieve the best performance from the ADC converter, a stable and low-noise reference voltage is necessary between the REFP and REFM pins. A 10-μF ceramic decoupling capacitor should be connected between these pins and positioned as close to them as possible.

Power Saving

The SA89851/3 device provides a power-down function to achieve low-power dissipation when not in use. There are two ways to implement this function. One is to set the DI05 bit to 1 in the mode control register (refer to Table 1, Table 2, and Table 5); the device powers down on the 16^{th} falling edge of the SCLK pin in the next frame. Another is to assign the GPIO3 pin as a power-down input (refer to Table 9), which is active-low input, causing the device to power down immediately after the GPIO3 pin is driven low.

Power Supply Recommendations

The device supports a wide analog supply range of 2.7V to 5.25V and a digital supply range of 1.7V to 5.25V. The analog supply voltage must always be higher than the digital supply voltage. To guarantee optimal performance, well-regulated power supplies are critical, necessitating the use of decoupling capacitors at each supply power pin. These capacitors should be positioned as close to the pins as possible.

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Application Information

The SA89851/3 device is commonly used in battery-powered systems for voltage monitoring, as depicted in Figure 14. It features a 20MHz SPI-compatible interface for high-speed data capture and transmission. A clean and low-noise band-gap reference (such as the SA89550) should be used as the external reference between the REFP and REFM pins to achieve accurate performance. The low power consumption and power-down feature of the device conserve power whether the device is in active use or not.

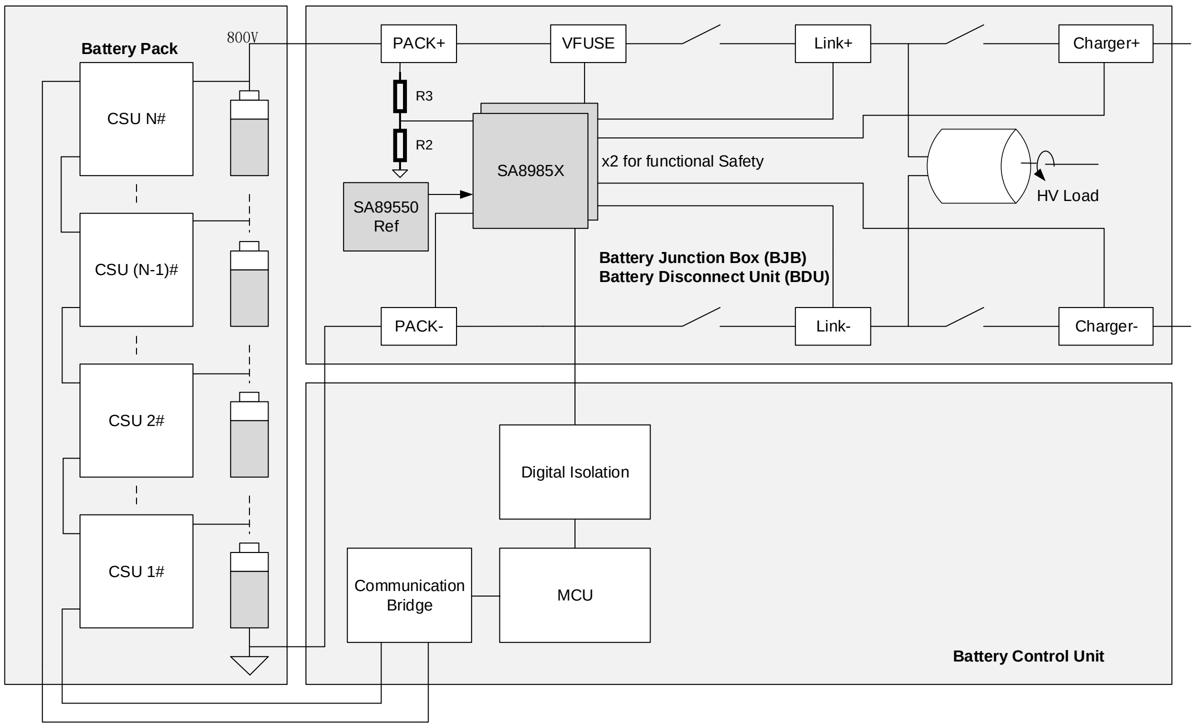

Figure 14. Application Example

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Application Schematic

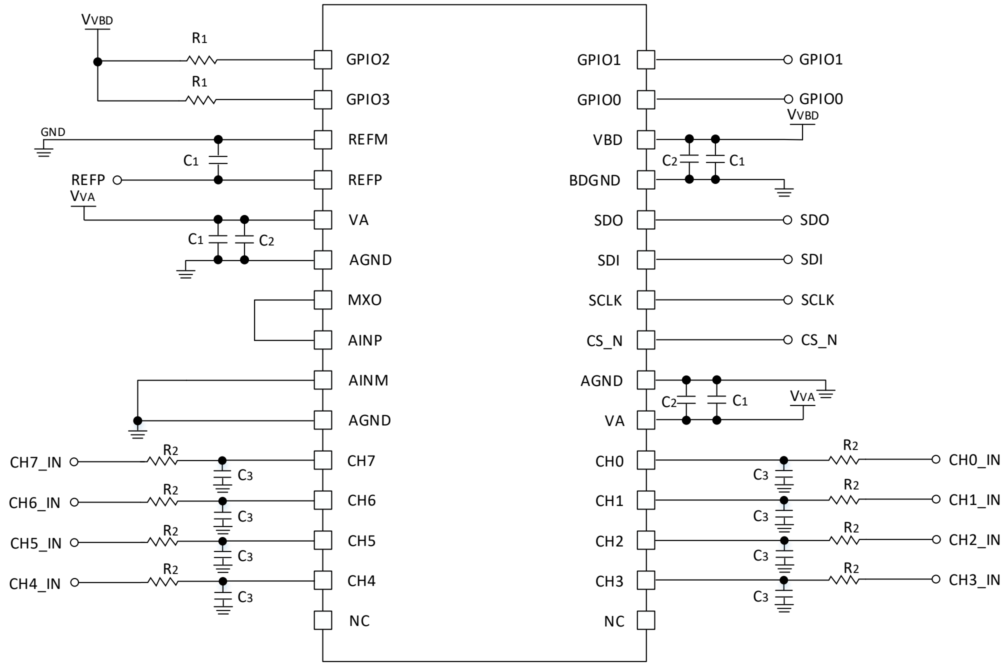

Figure 15. Schematic Diagram (SA89851)

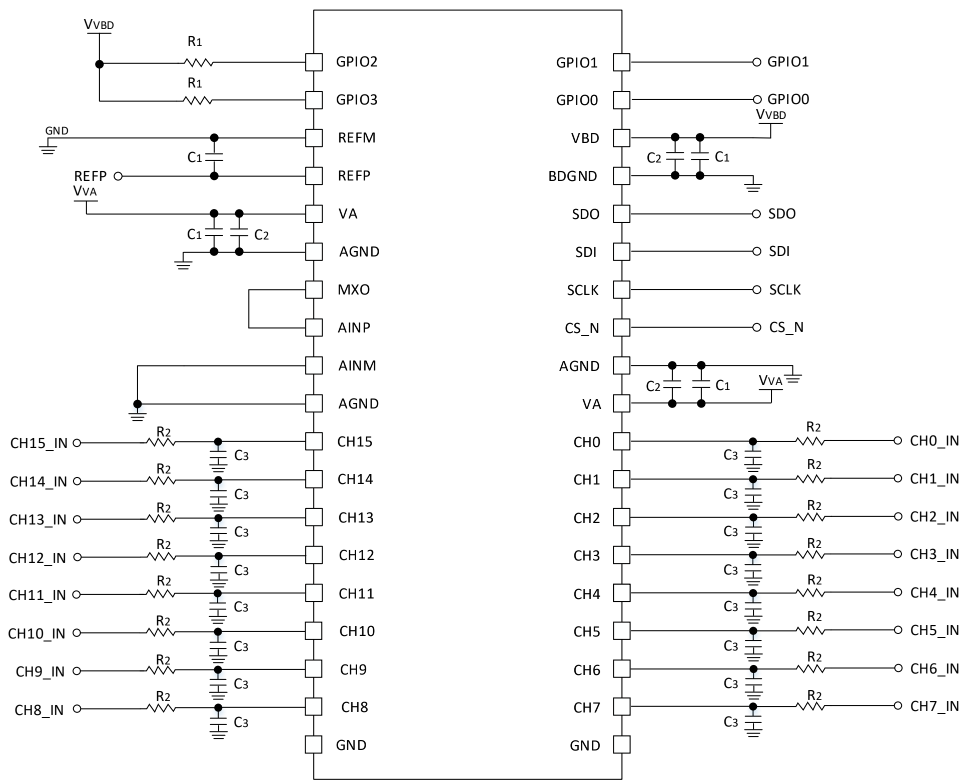

Figure 16. Schematic Diagram (SA89853)

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BOM List

Designator	Description	Part Number	MFR
C1	10μF/16V, 10%, 0805	MuRata	GRM21BC71C106KE11L
C2	0.1μF/16V, 10%, 0603	MuRata	GRM033C71C104KE14D
C3	270pF/50V, 5%, 0603	Yageo	CC0603JRNP09BN271
R1	47kΩ, 1%, 100mW, 0603	Yageo	RC0603FR-0747KL
R2	33Ω, 1%, 100mW, 0603	Uni-Royal	0603WAF330JT5E

PCB Layout Guide

For the best performance of the ADC converter, the following guidelines should be followed:

1. **Decoupling Capacitor C1:** A minimum of a 10-μF ceramic decoupling capacitor is required between the REFP and REFM pins, positioned as closely as possible to these pins.
2. **Decoupling Capacitors C2:** Add the decoupling capacitors at each supply pin and place them as close as possible to the power and ground pins.
3. **Decoupling Capacitor C3:** Decoupling capacitors are necessary at the channel inputs to charge the internal capacitor during the sampling period, ensuring accurate sampling.
4. Depending on the PCB layout, parasitic inductance may be present on the SDO pin. To minimize the ringing of SPI output, place a small resistor in series with the SDO pins to slow down the signal edges, and place it close to the ADC.
5. When using a high drive capability SPI interface for the host, using series termination for the SCLK and SDI lines is recommended, as it can help reduce ringing and noise. The low value series resistors should be placed close to the driver (MCU or FPGA).

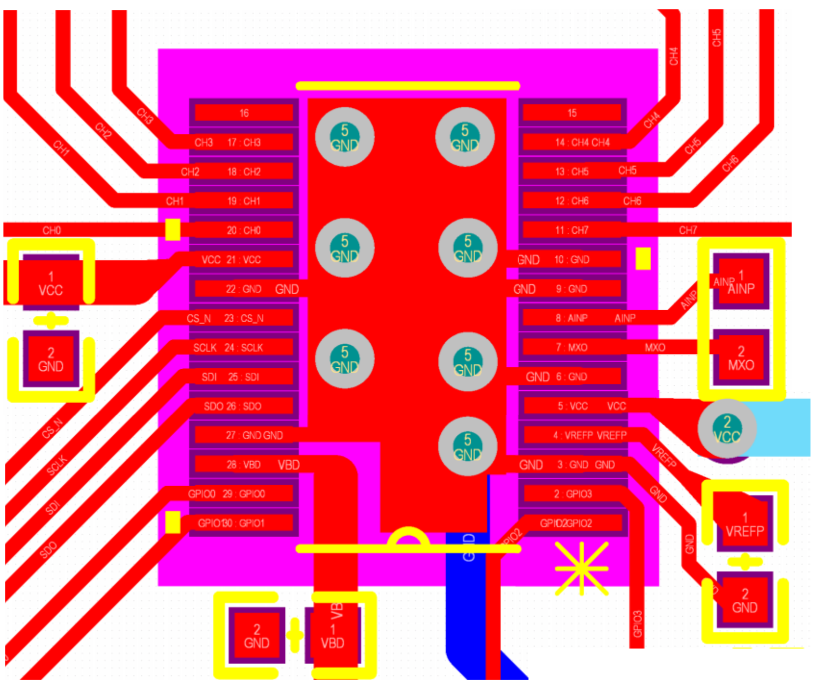

Figure 17. SA89851 Layout Recommendation

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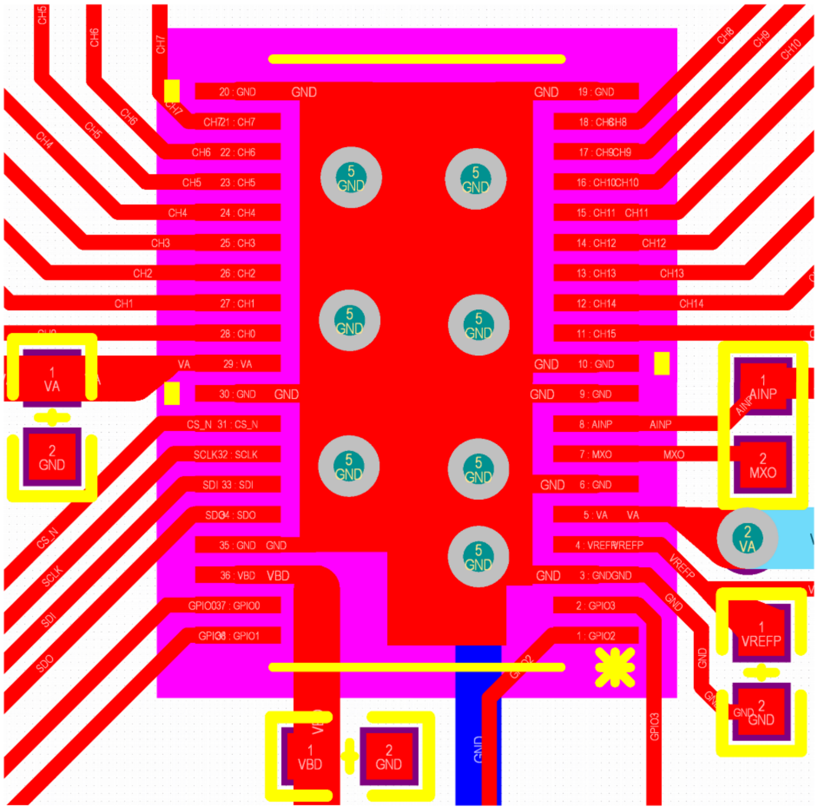

Figure 18. SA89853 Layout Recommendation

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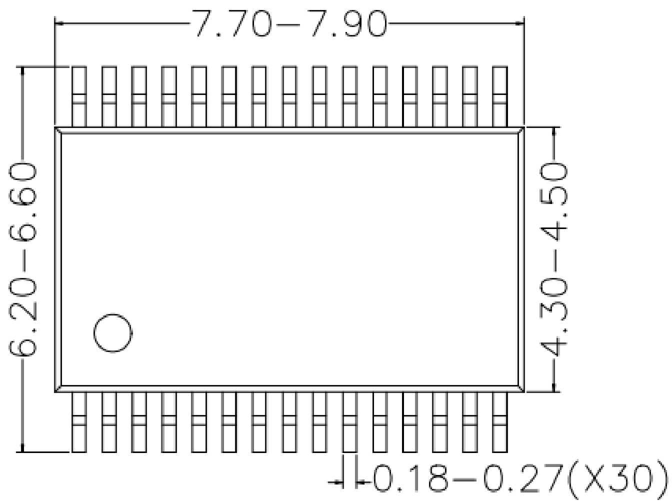
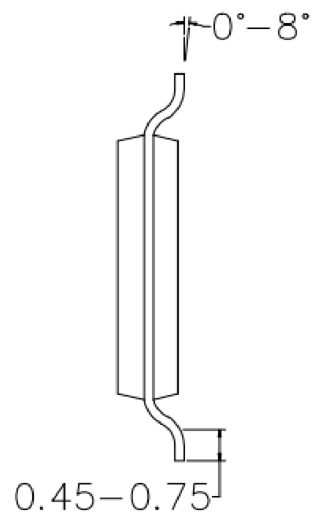
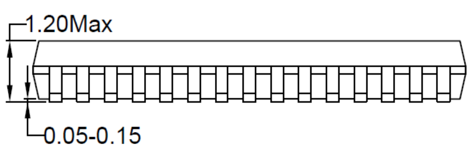
TSSOP30 Package Outline Drawing



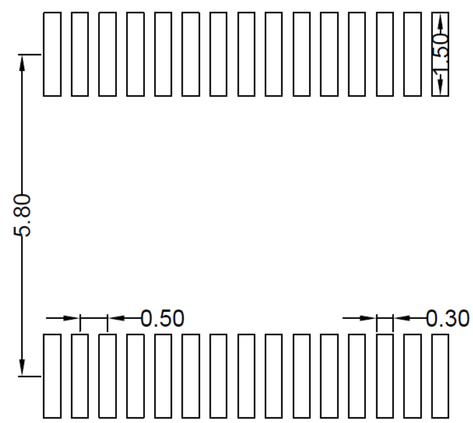
Top View



Side View



Front View



Recommended PCB layout (Reference only)

Note: All dimensions are in millimeters and exclude mold flash and metal burr.

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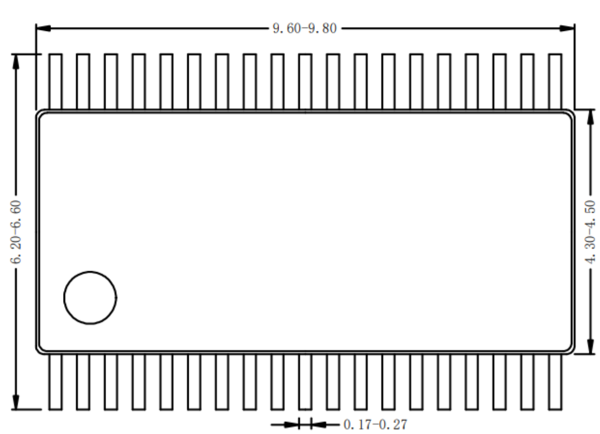
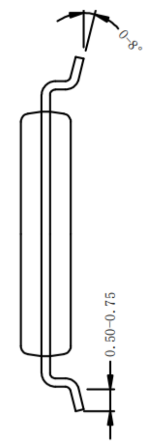
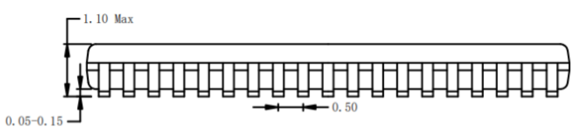
TSSOP38 Package Outline and PCB Footprint



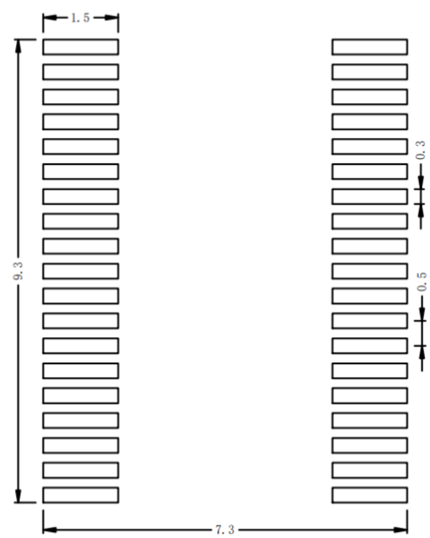
Top View



Side View



Front View



Recommended PCB Footprint

(Reference Only)

Note: All dimensions are in millimeters and exclude mold flash and metal burr.

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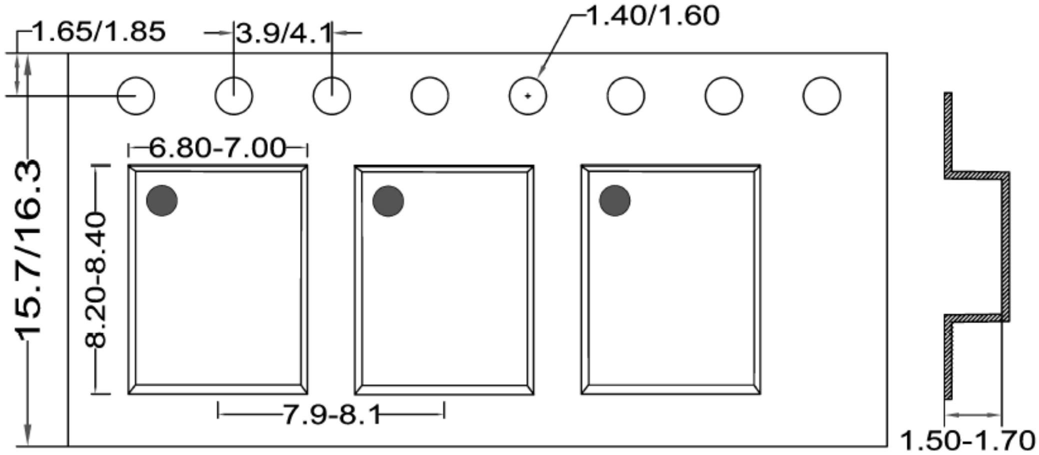
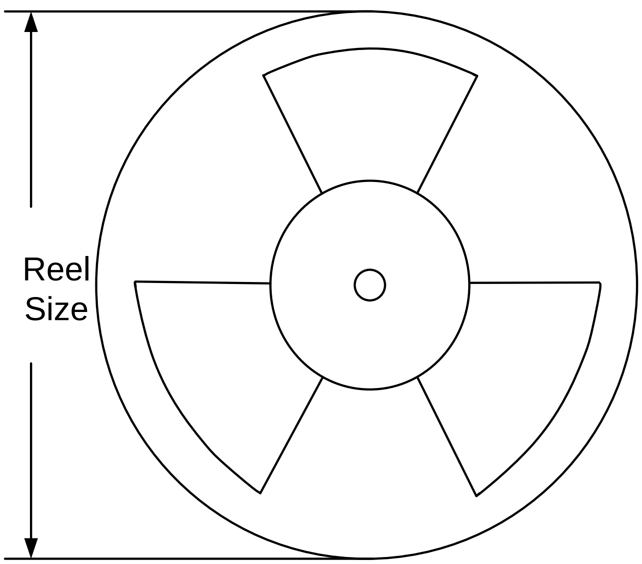
Tape and Reel Information TSSOP30

1. Tape Dimensions and Pin 1 Orientation



Direction of Feed

2. Reel Dimensions



Package type	Tape width (mm)	Pocket pitch (mm)	Reel size (Inch)	Trailer * length (mm)	Leader * length (mm)	Qty per reel (pcs)
TSSOP30(WB)	16	8	13"	400	400	4000

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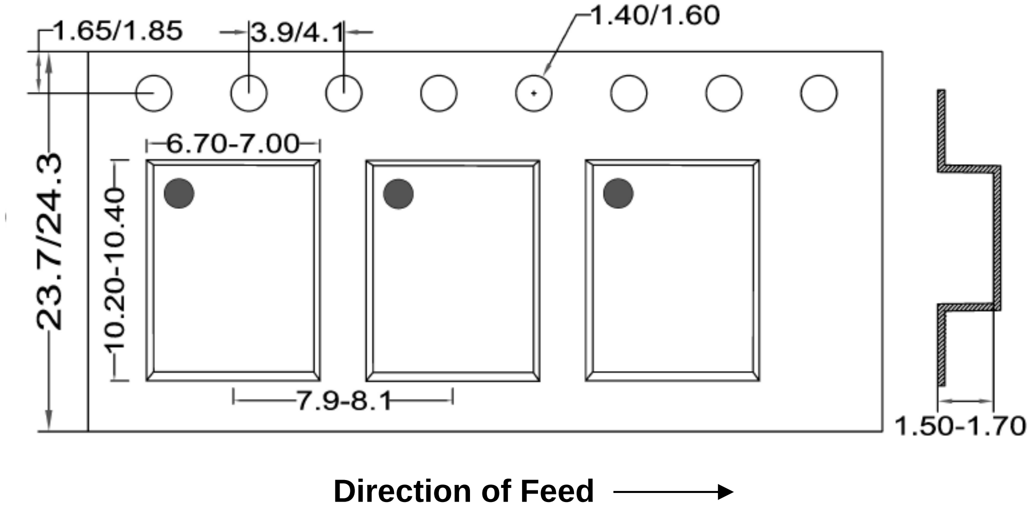
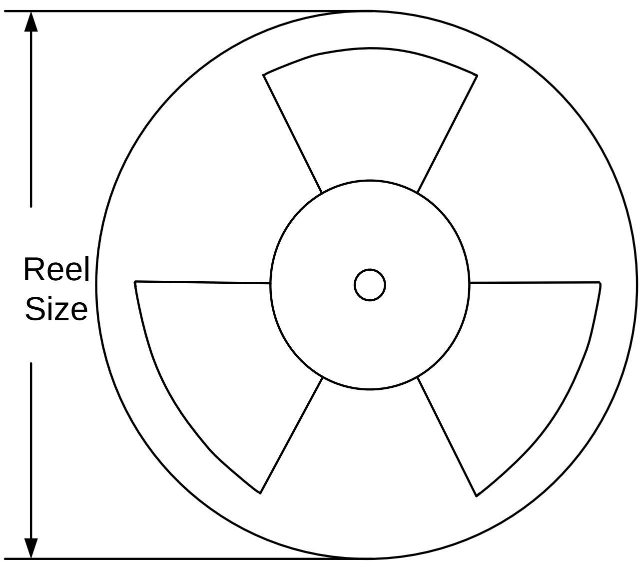
Tape and Reel Information TSSOP38

1. Tape Dimensions and Pin 1 Orientation



2. Reel Dimensions



Package Type	Tape width (mm)	Pocket pitch (mm)	Reel size (Inch)	Trailer * length (mm)	Leader * length (mm)	Qty per reel (pcs)
TSSOP38	24	8	13"	400	400	2500

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Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
Apr. 30, 2024	Revision 1.0	Initial Release
June 30,2024	Revision 1.0	SA89853 related information added

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