General Description

The SY2A54055 is a 22W, efficient Class-D audio power amplifier for driving a bridged-tied mono speaker for automotive emergency call (eCall), telematics, instrument cluster and infotainment applications. An adjustable power limiter allows the user to set a virtual voltage rail lower than the chip supply to limit the amount of current through the speaker. The DC detection circuit measures the frequency and amplitude of the PWM signal and shuts off the output stage if the input capacitors are damaged or shorts exist on the inputs.

The SY2A54055 can drive a mono speaker as low as 2Ω. The high efficiency of the device, eliminates the need for an external heat sink when playing music.

Fully short protections include output short to GND, PVDD, and output-to-output. The short-circuit protection and thermal protection includes an auto-recovery feature. The device also incorporates load diagnostic circuitry designed for detecting and determining the status of output connections at start. It supports the following diagnostics: short to GND, short to PVDD, short load, open load. The device reports the presence of any of the short or open conditions to the system via I^2C.

Ordering Information

SY2A54055 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY2A54055HFA	TSSOP16E	

Features

- 22W into a 4Ω Load at <10% THD+N from a 14.4V Supply
- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3
- Highly Efficient Class-D Operation Eliminating Need for Heat Sink
- Operates from 4.5V to 18V
- Thermal and Over-Circuit Protection with Auto Recovery
- Load Diagnostic Functions:
  Open and Shorted Output Load
  Output-to-Ground and Output-to-PVDD Shorts
- Comprehensive Click and Pop Suppression
- Space-Saving Surface Mount TSSOP16E Package

Applications

- Noise Generation for HEV/EV
- Emergency Call Systems (e Call)
- Cluster
- AVAS
- Linear Motor Driver

Typical Application

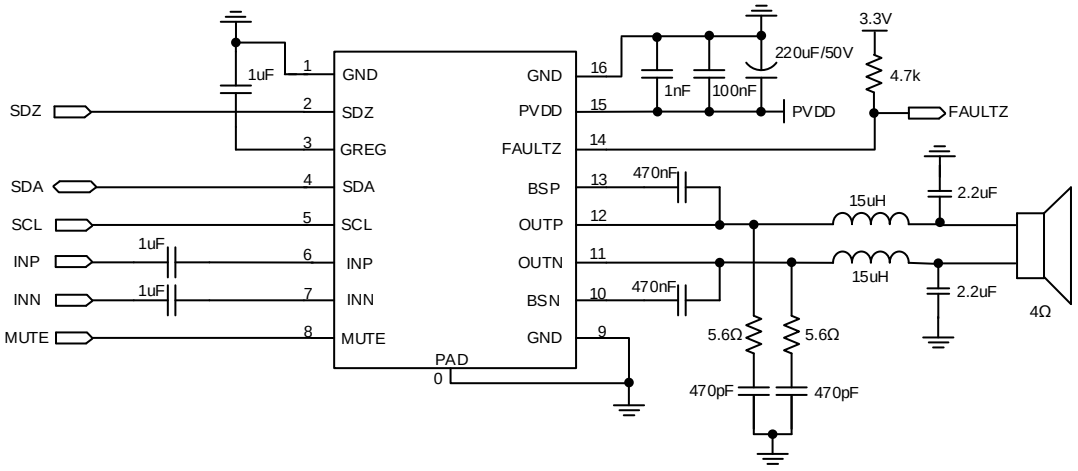
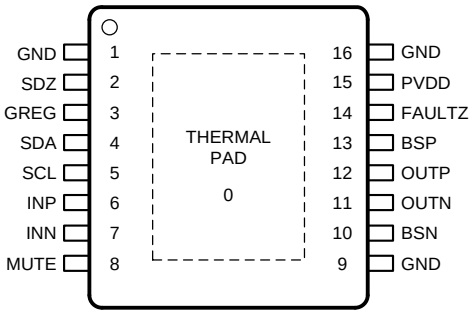


Figure1. Typical Application Circuit

Pin out (Top View)



(TSSOP-16E)

Top Mark: CDH*xyz* (device code: CDH, ***x=year code, y=week code, z= lot number code)***

Pin Name	Pin No.	Pin Description
SDZ	2	Shutdown signal for IC (low = output HiZ, high = operational). TTL logic levels with compliance to PVDD.
FAULTZ	14	Open drain output used to display fault status. Voltage compliant to PVDD.
GREG	3	Internal regulator output for gate driver. Nominal voltage is 3.4V.
INP	6	Positive audio input. Biased at 2.4V.
INN	7	Negative audio input. Biased at 2.4V.
MUTE	8	Mute input, active high.
PVDD	15	Power supply for H-bridge.
BSP	13	Bootstrap I/O for positive high-side FET.
OUTP	12	Class-D H-bridge positive output.
GND	1,9,16	Power ground for PVDD.
BSN	10	Bootstrap I/O for negative high-side FET.
OUTN	11	Class-D H-bridge negative output.
SDA	4	I^2C data.
SCL	5	I^2C clock.
Thermal Pad	0	Connect to GND. Thermal pad should be soldered down on all applications to secure the device property to the printed wiring board.

Block Diagram

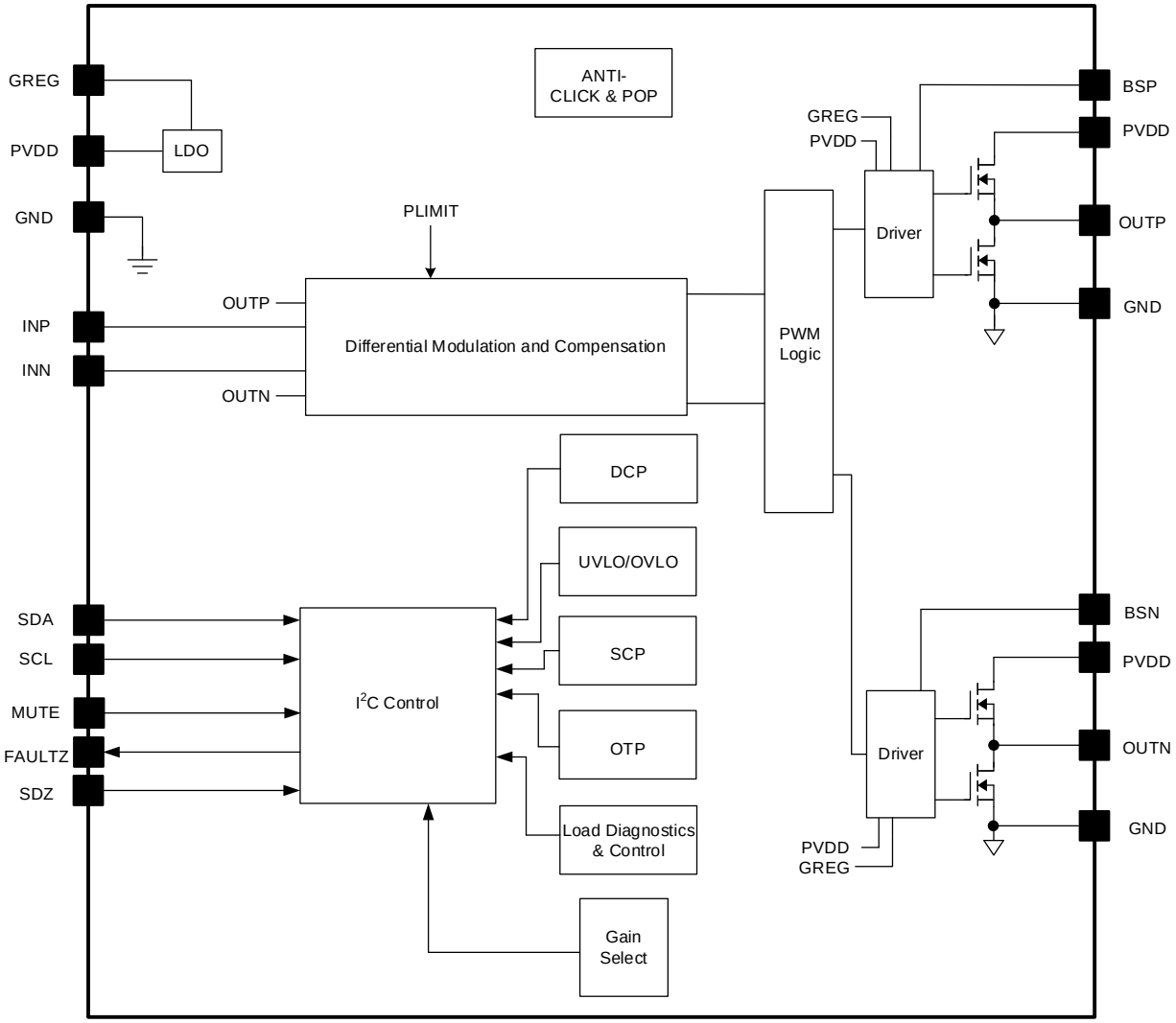


Figure2. SY2A54055 Block Diagram

Absolute Maximum Ratings (Note 1)

V_{DD}, Supply Voltage
PVDD ---------- -0.3V to 21V
V_I, Interface Pin Voltage
SDZ, MUTE, FAULTZ---------- -0.3V to (PVDD +0.3) V
INP, INN ---------- -0.3V to 3.6V
SDA, SCL ---------- -0.3V to (GREG +0.3) V
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 28.4°C/W
θ_{JC} (top) ---------- 20°C/W
θ_{JC} (bottom) ---------- 2.6°C/W
θ_{JB} ----------15.3°C/W
ψ_{JT}---------- 0.3°C/W
T_J, Operating Junction Temperature ---------- -40°C to 150°C
T_{stg}, Operating Storage Temperature ---------- -65°C to 150°C

Recommended Operating Conditions

V_{DD}, Supply Voltage PVDD ---------- 4.5V to 18V
V_{IH}, High-Level Input Voltage SDZ, MUTE ---------- 1.2V to 3.3V
V_{IL}, Low-Level Input Voltage SDZ, MUTE ---------- 0V to 0.6V
R_L, Minimum Load Resistance Output Configuration ---------- ≥1.9Ω
T_A, Operating Free-air Temperature ---------- -40°C to 125°C

Electrical Characteristics

(T_A = -40°C to 125°C, PVDD=12V, R_L=4Ω, default I^2C setting, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
DC Characteristics						
PVDD	V_{DD}		4.5		18	V
V_{DD} Under Voltage Lockout Voltage	V_{UVLO_RISE}	V_{DD} Rising to exit UVLO		3.9	4.3	V
	V_{UVLO_FALL}	V_{DD} Falling to enter UVLO	3.2	3.6		V
V_{DD} Over Voltage Lockout Voltage	V_{OVLO_RISE}	V_{DD} Rising to enter OVLO		22.7	23.8	V
	V_{OVLO_FALL}	V_{DD} Falling to exit OVLO	20.3	21.5		V
Quiescent Supply Current	I_Q	SDZ=12V, no load, no snubber		12		mA
		SDZ=0V, no load, no snubber		5		μA
High-Level Input Voltage	V_{IH}	SDZ, MUTE	1.2			V
Low-Level Input Voltage	V_{IL}	SDZ, MUTE			0.6	V
Low-Level Output Voltage	V_{OL}	FAULTZ, $R_{PULL-UP}$=100kΩ			0.6	V
High-Level Input Current	I_{IH}	V_I=12V, V_{DD}=12V			1	μA
Low-Level Input Current	I_{IL}	V_I= 0V, V_{DD}=12V			1	μA
Drain-Source on-State Resistance	R_{DSON}	T_J=25°C, including metal and bonding wire		185		mΩ
Gain	G	No load	19	20	21	dB
			25	26	27	
			31	32	33	
			35	36	37	
Turn-on Time (Note 3)	t_{ON}	From SDZ high to PWM on		296		ms
Turn-off Time (Note 3)	t_{OFF}	From SDZ low to PWM off		48		ms
Class-D Output Offset Voltage (Measured Differentially)	$\|V_{OS}\|$	T_J=25°C,V_I=0V, Gain=26dB		1.5	10	mV
Gate Drive Supply	GREG	SDZ=12V, V_I=0V	3.2	3.4	3.6	V
DC Detection Time (Note 3)	t_{DCDET}			600		ms
DC Detection Threshold (Output Differential Duty-cycle) (Note 3)				15		%
PWM Frequency	f_{PWM}	Selectable for AM avoidance		400		kHz
				500		
AC Characteristics (Note 3)						
Power Supply Ripple Rejection	PSRR	V_{ripple}=200mV_{PP}, Gain=20dB, 1kHz, inputs AC-coupled to GND		65		dB
Output Power	P_O	PVDD=6V, R_L=2Ω, f=1kHz, <=1%THD+N		4.5		W
		PVDD=9V, R_L=2Ω, f=1kHz, <=1%THD+N		9.7		

		f=1kHz, <=1%THD+N		12.6		
		PVDD=14.4V, R_L=4Ω, f=1kHz, <=10%THD+N		22		
		PVDD=16V, R_L=4Ω, f=1kHz, <=1%THD+N		21.2		
		PVDD=12V, R_L=8Ω, f=1kHz, <=10%THD+N		9.6		
		PVDD=18V, R_L=8Ω, f=1kHz, <=1%THD+N		17.5		
Total Harmonic Distortion + Noise	THD+N	f=1 kHz, Po=5W		0.048		%
Output Integrated Noise Floor	V_n	T_J=25°C,20Hz to 22kHz, A-weighted filter, Gain=20dB		57		μV
Signal to Noise Ratio	SNR	Max output at THD+N<1%, f=1kHz, Gain=20dB, A-weighted, PVDD=12V		102		dB
Protection (Note 3)						
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C
Over Current Protection	I_{OC}			5		A
Load Diagnostics						
Voltage to Detect a Short from OUT pin(s) to PVDD			5.5		19	V
Resistance to Detect a Short from OUT Pin(s) to Ground					50	Ω
Open Load Detection Threshold		Including speaker wires	95	130	190	Ω
Short Load Detection Threshold		T_A=25°C, Including speaker wires	0.7	1.3	1.7	Ω
		Including speaker wires	0.5	1.3	1.9	
I²C						
SDA/SCL High-level Input Voltage			1.3			V
SDA/SCL Low-level Input Voltage					0.5	V
SDA High-level Output Voltage		$R_{PULL-UP}$=100kΩ to 3.3V	3			V
SDA Low-level Output Voltage		3mA sink current			0.3	V

Note 1: Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective four layer thermal conductivity test board of JEDEC 51-7.

Note 3: Typical test value on demonstration board, guarantee by design.

I²C Timing Requirements for Control Port

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCL}	SCL frequency	No wait states		400	kHz
t_r	SCL and SDA rise time			300	ns
t_f	SCL and SDA fall time			300	ns
t_{WH}	SCL high duration time		0.6		us
t_{WL}	SCL low duration time		1.3		us
t_{S1}	SDA to SCL setup time		250		ns
t_{h1}(Note1)	SCL to SDA hold time		0		ns
t_{buf}	Free time between stop and start condition		1.3		us
t_{S2}	SCL to start condition		0.6		us
t_{h2}	Start condition to SCL hold time		0.6		us
t_{S3}	SCL to stop condition		0.6		us

Note 1: A device must internally provide a hold time of at least t_f for the SDA signal to bridge the undefined region of the falling edge of SCL.

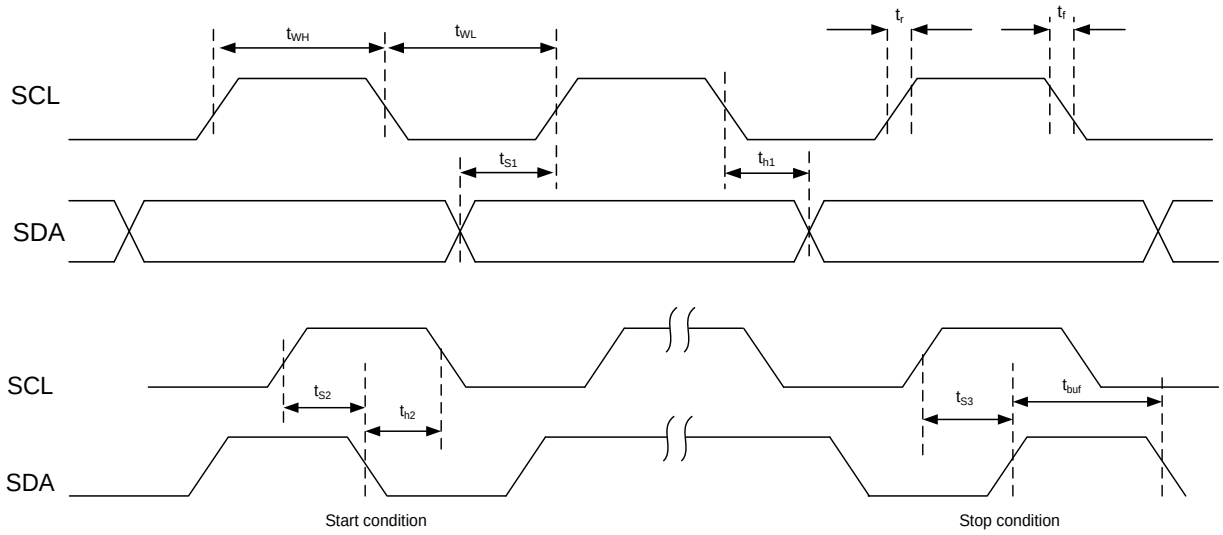
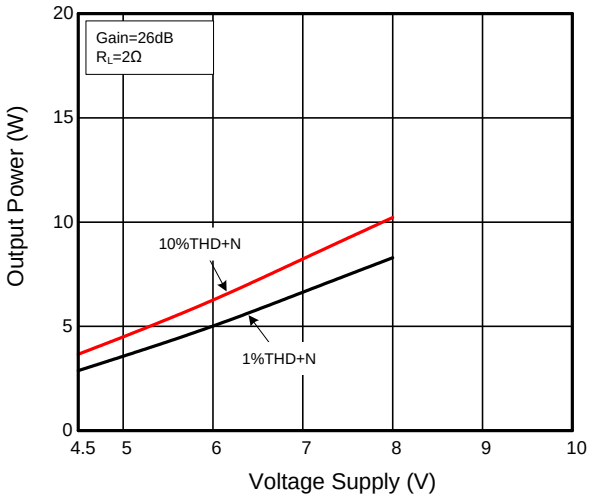


Figure 3. I²C Timing Diagram

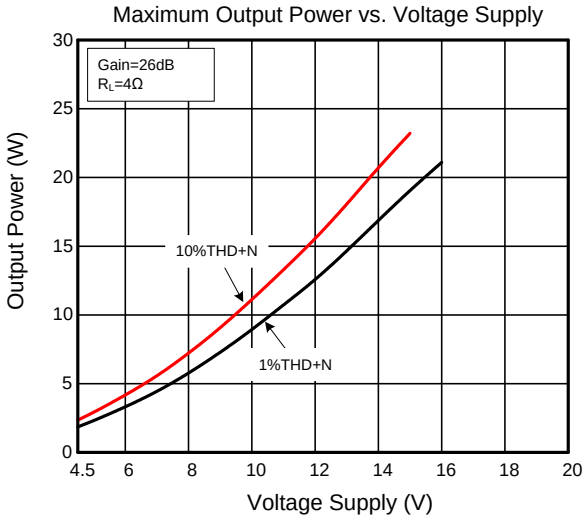
Typical Performance Characteristics

(All measurements taken at 1 kHz, unless otherwise noted)

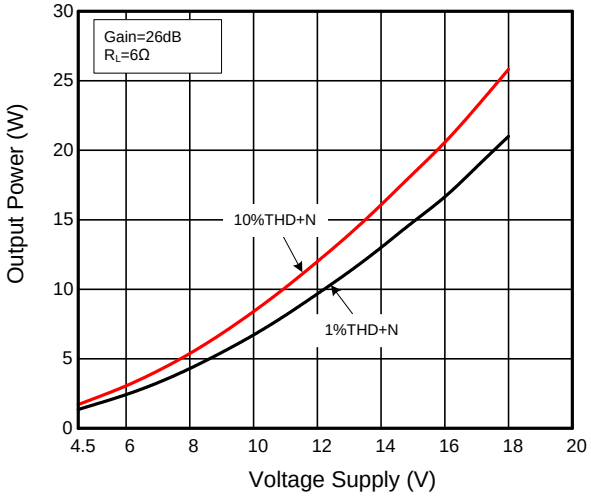
Maximum Output Power vs. Voltage Supply



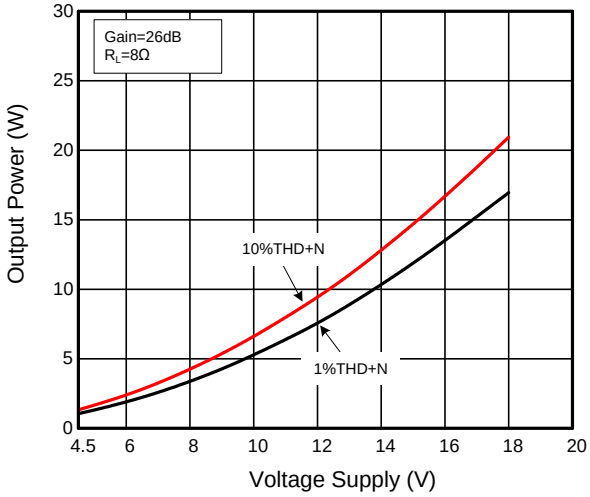
Maximum Output Power vs. Voltage Supply



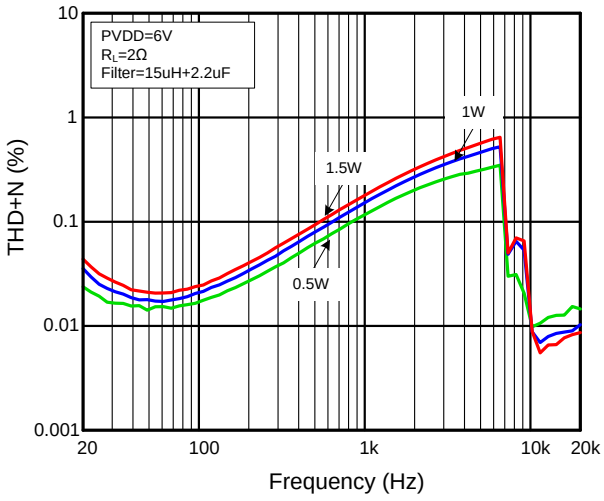
Maximum Output Power vs. Voltage Supply



Maximum Output Power vs. Voltage Supply



THD+N vs. Frequency



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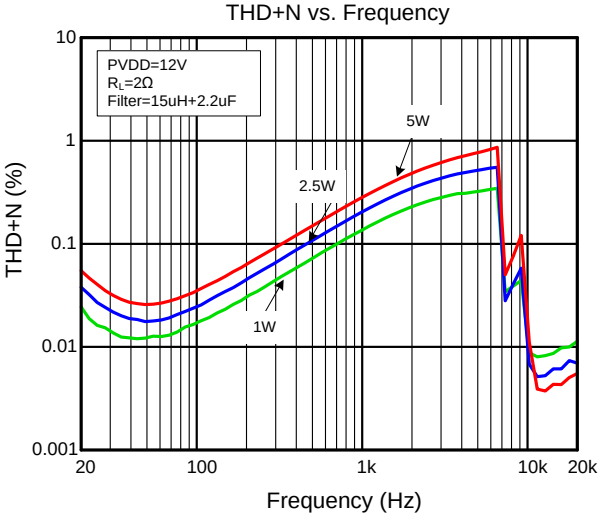

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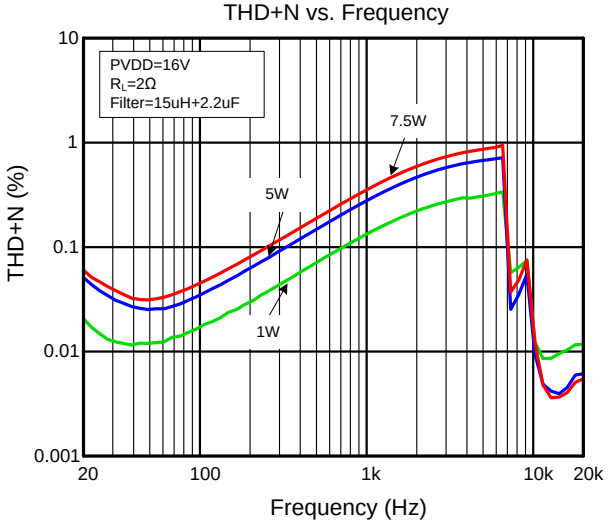

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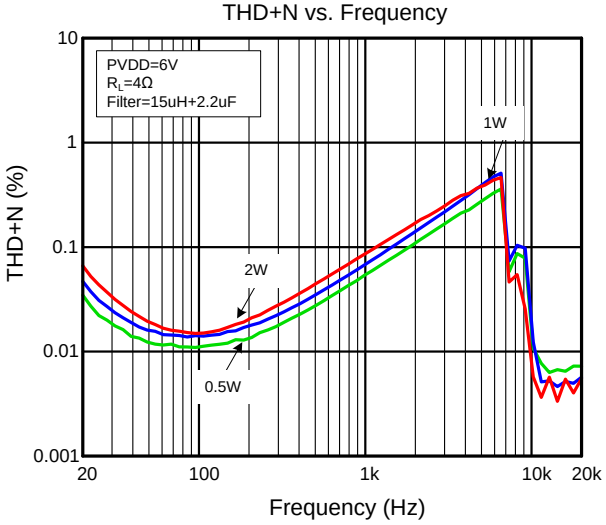

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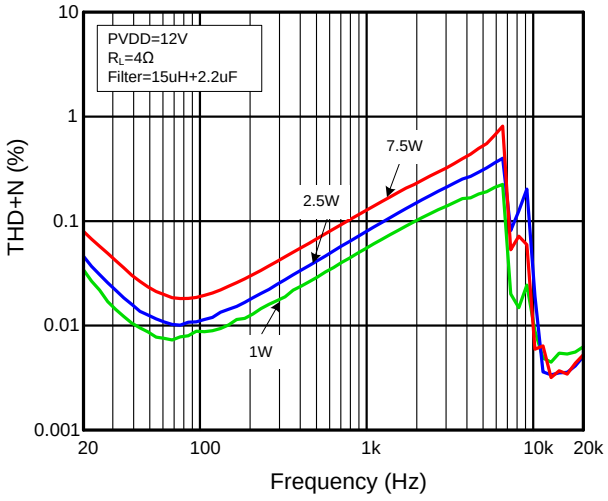
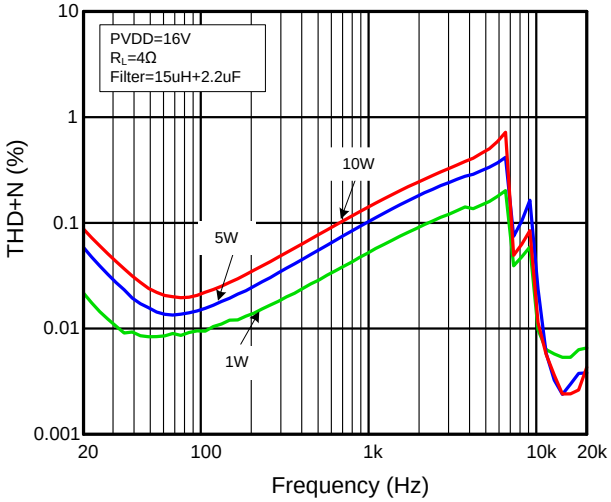
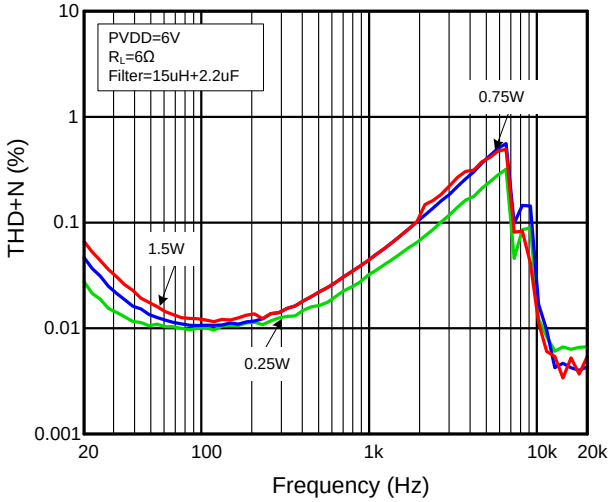


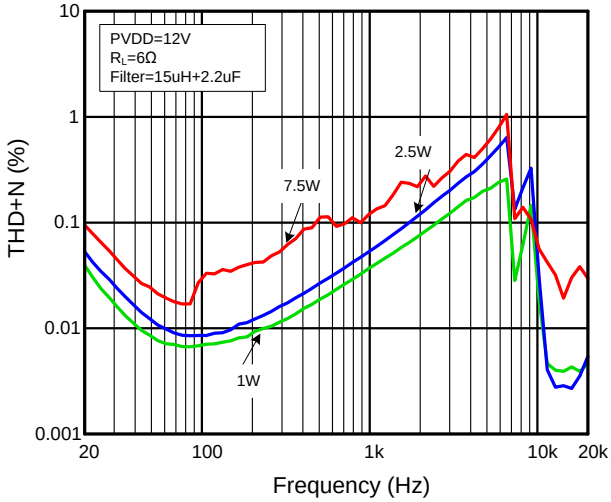
THD+N vs. Frequency



THD+N vs. Frequency



THD+N vs. Frequency



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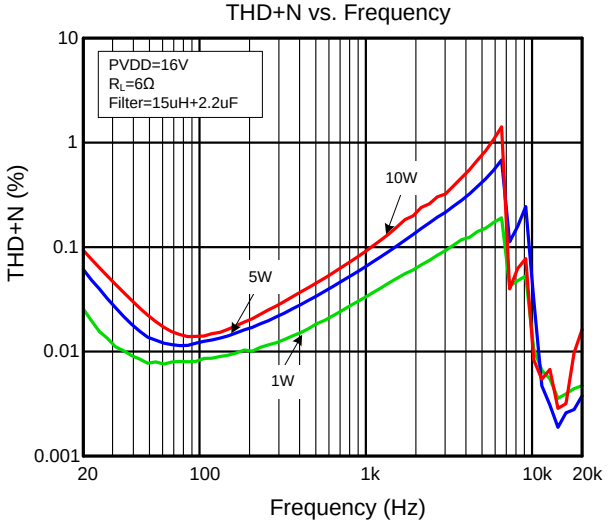

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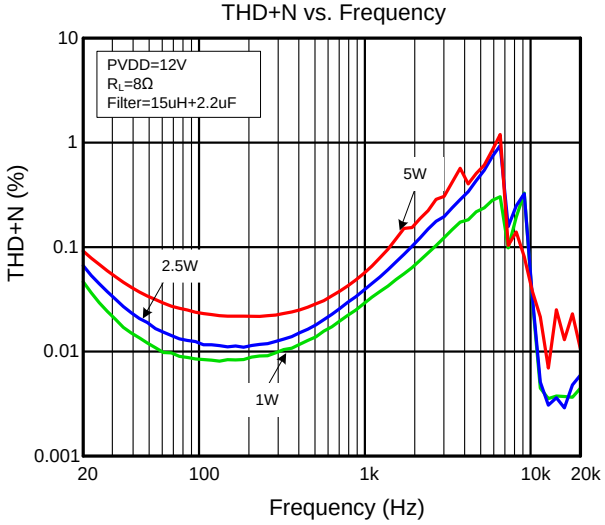
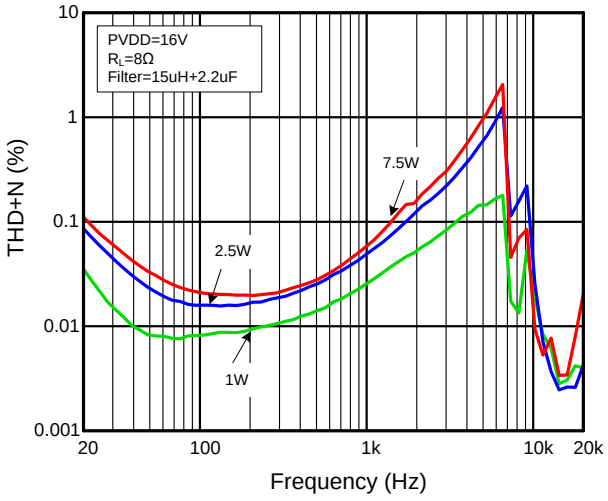
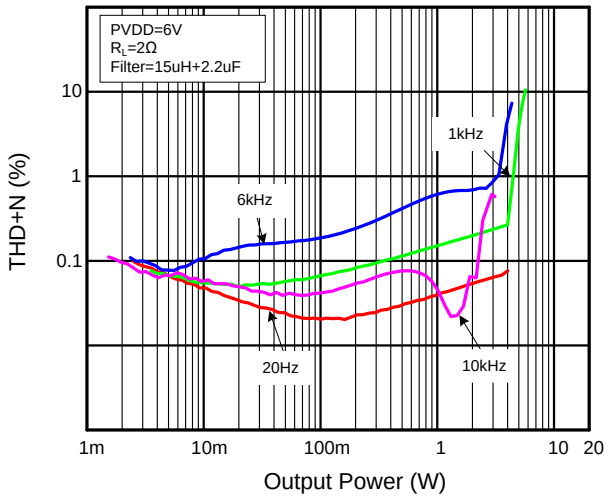


THD+N vs. Frequency



THD vs. Output Power



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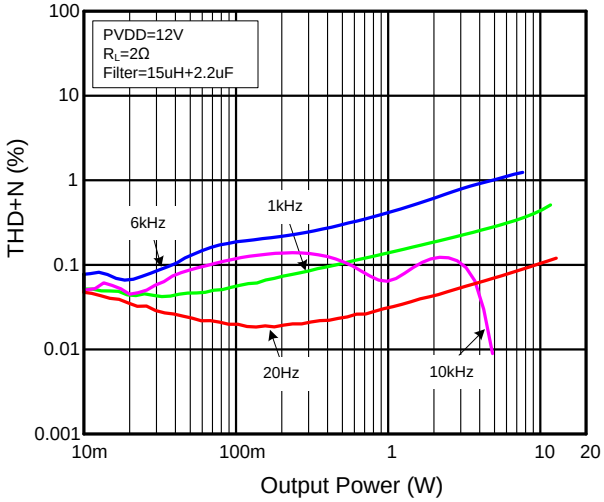

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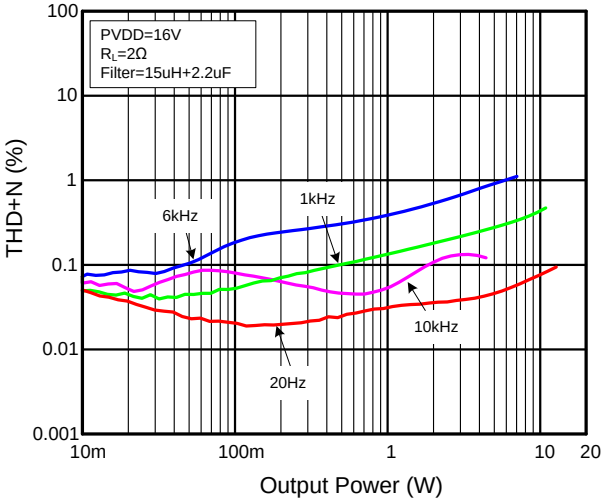

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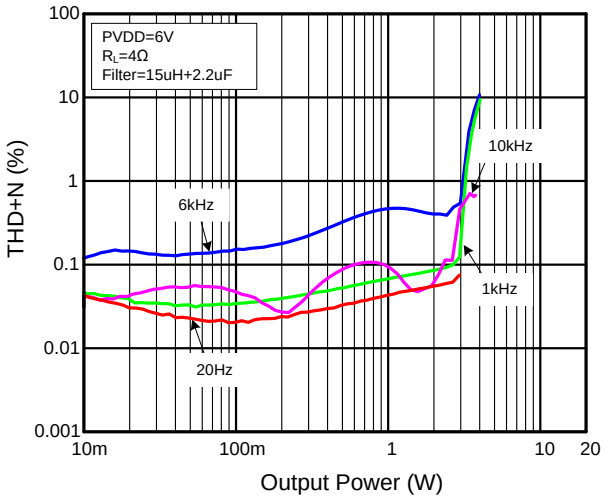
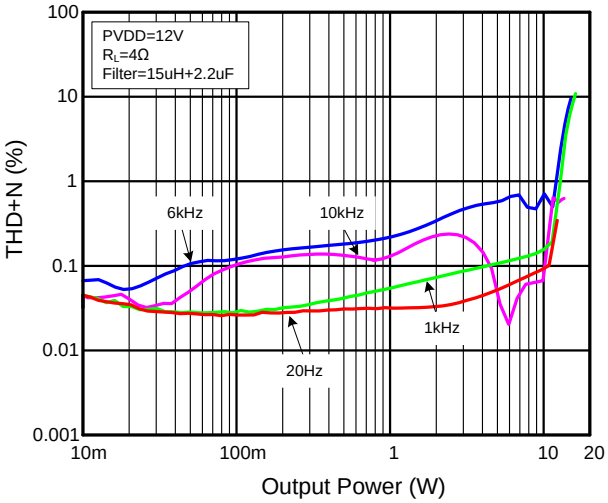
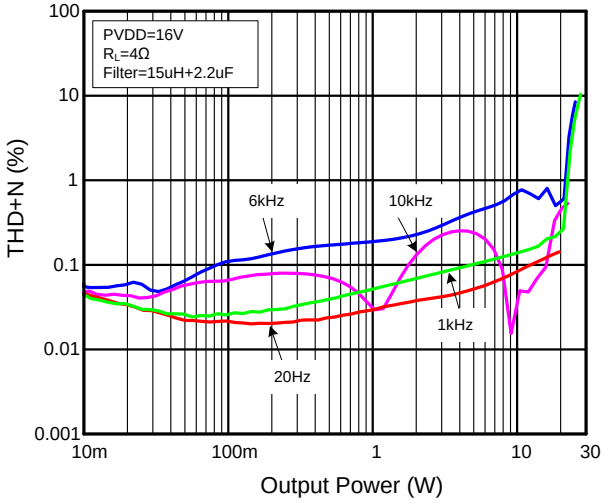


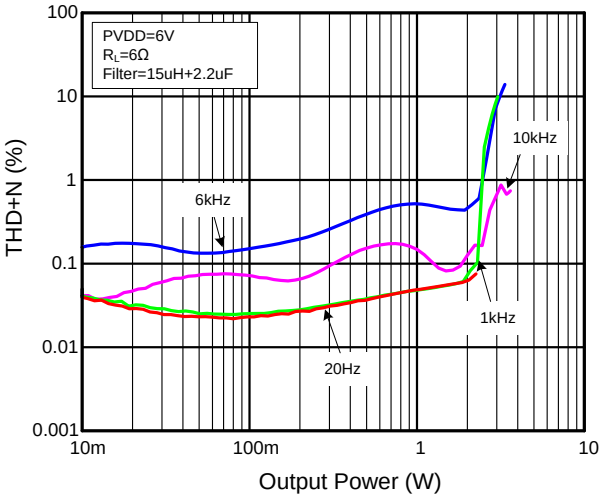
THD vs. Output Power



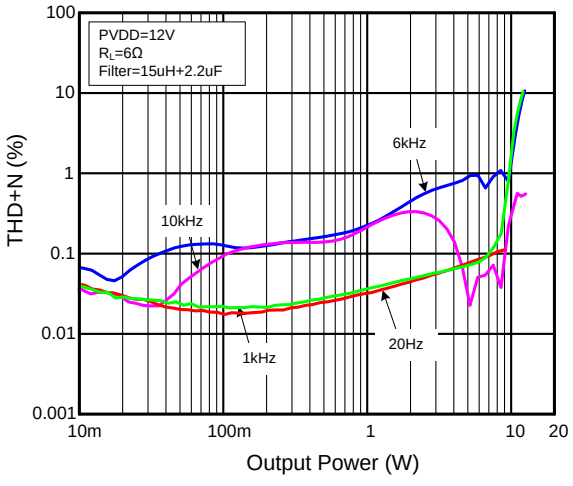
THD vs. Output Power



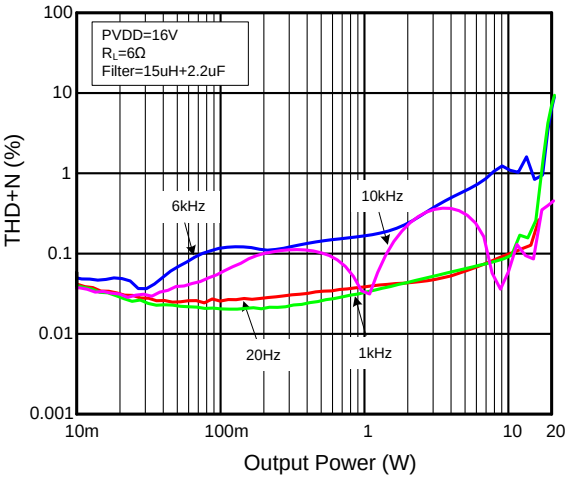
THD vs. Output Power



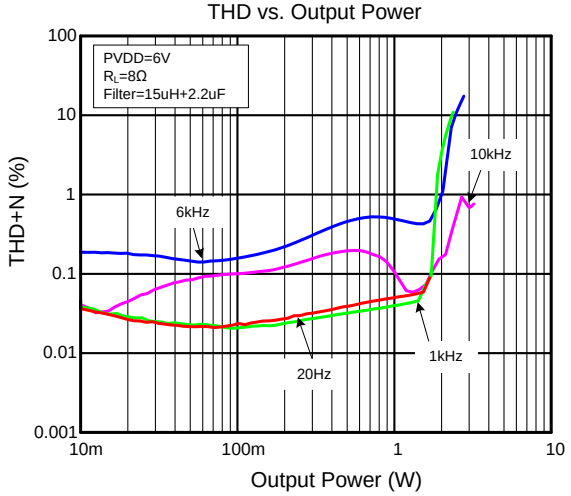
THD vs. Output Power



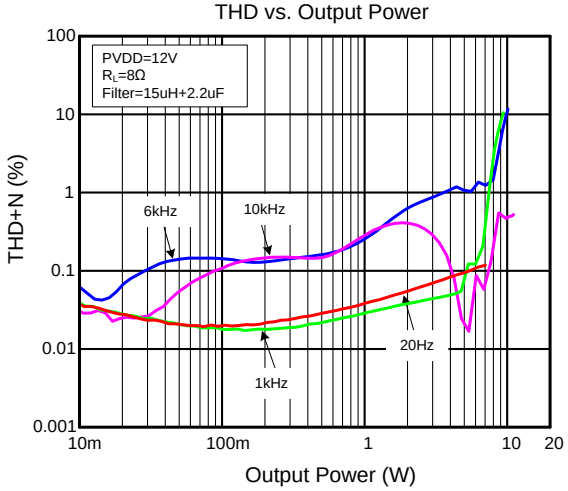
THD vs. Output Power



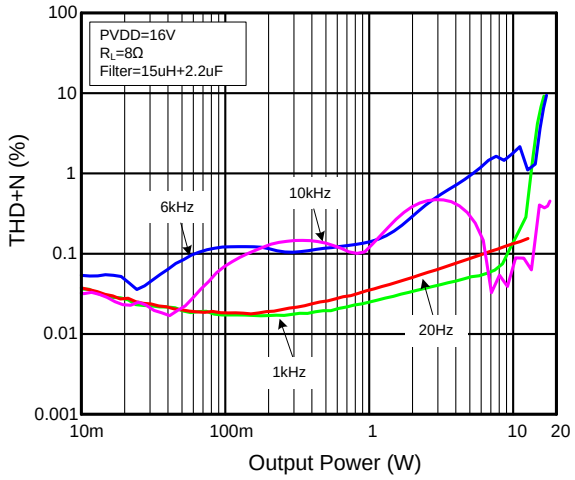
THD vs. Output Power



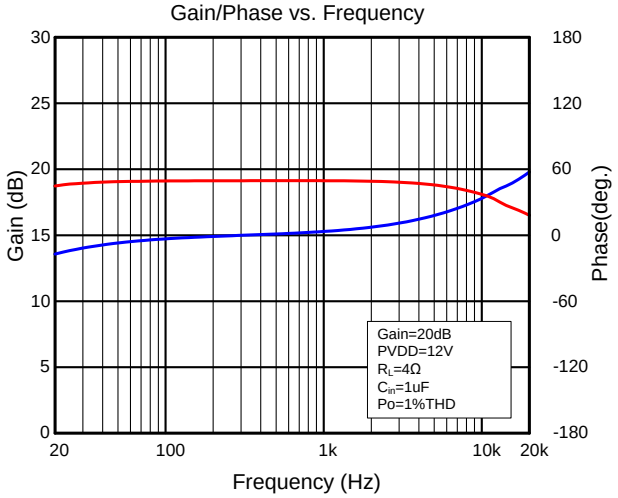
THD vs. Output Power



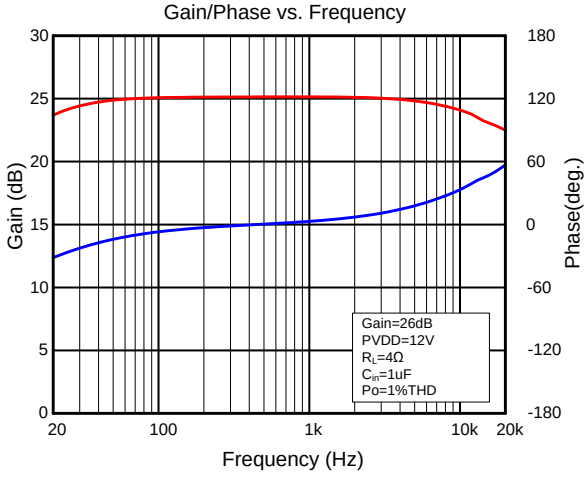
THD vs. Output Power



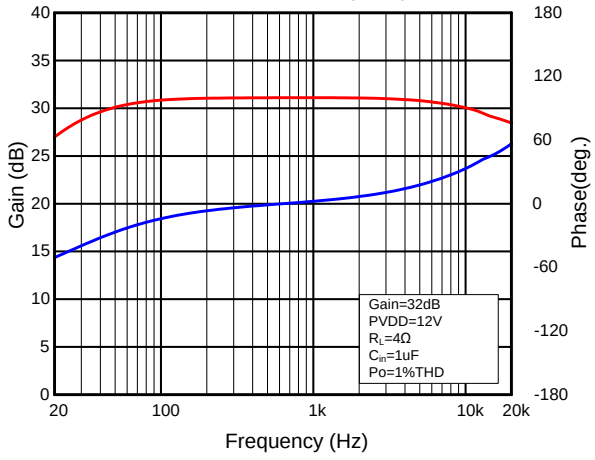
Gain/Phase vs. Frequency



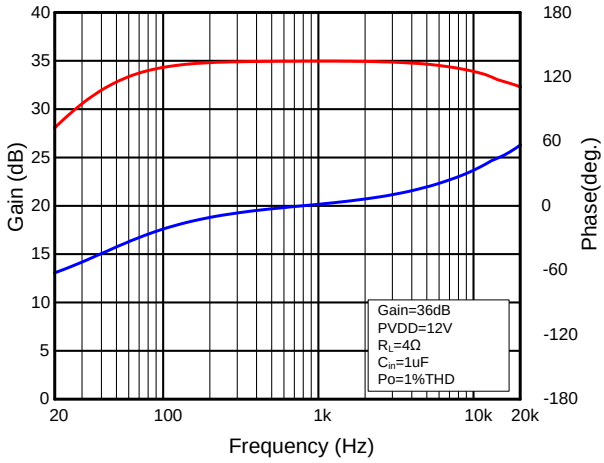
Gain/Phase vs. Frequency



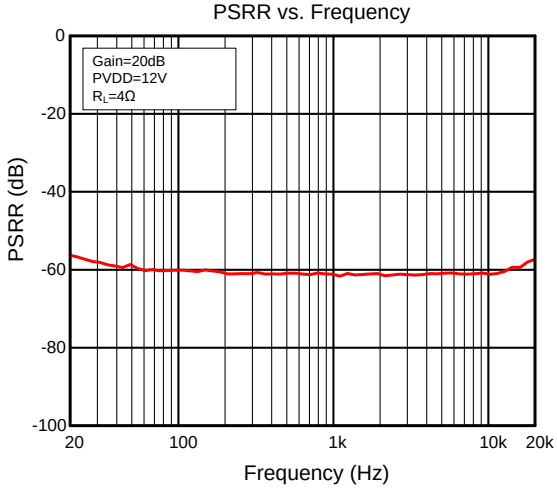
Gain/Phase vs. Frequency



Gain/Phase vs. Frequency



PSRR vs. Frequency



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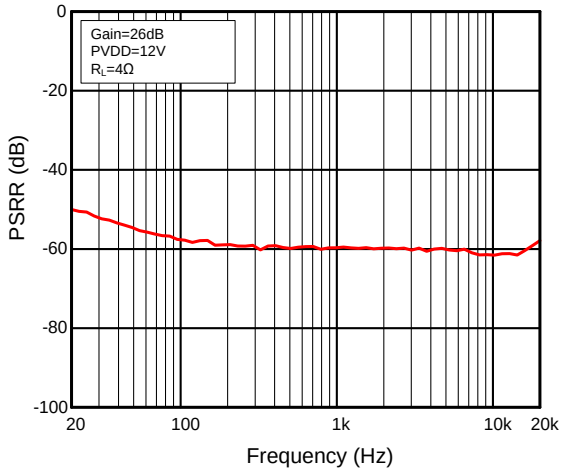
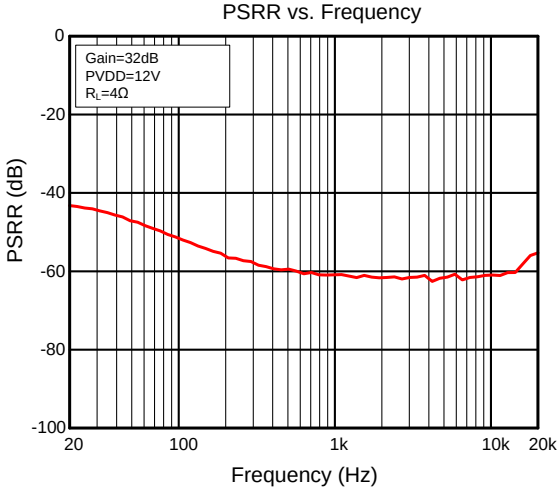
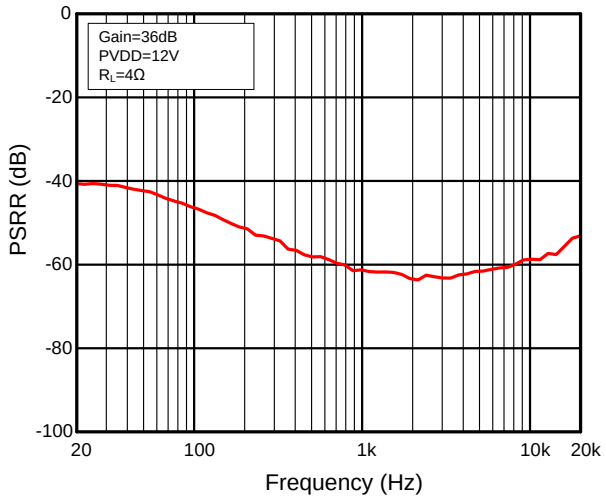


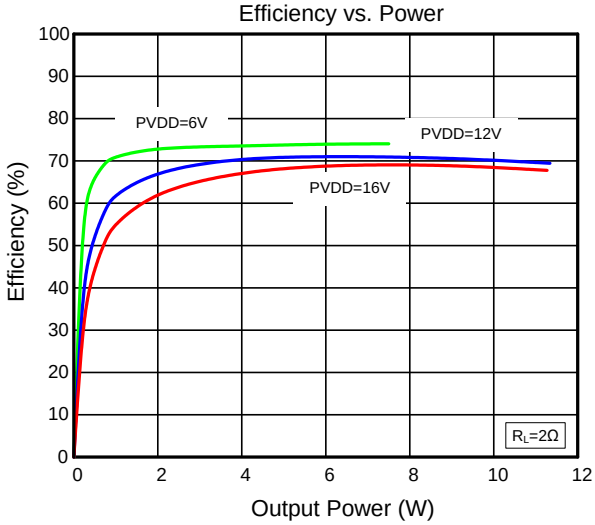
PSRR vs. Frequency

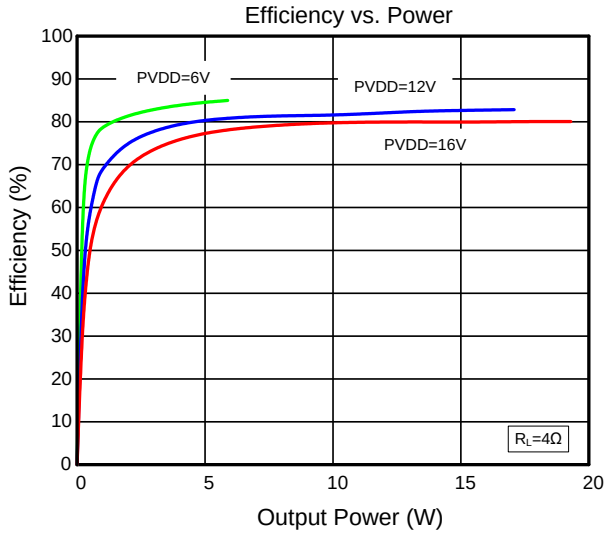


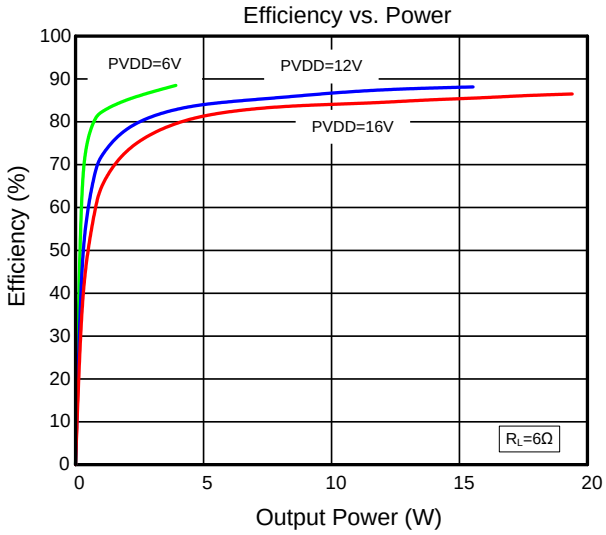
PSRR vs. Frequency

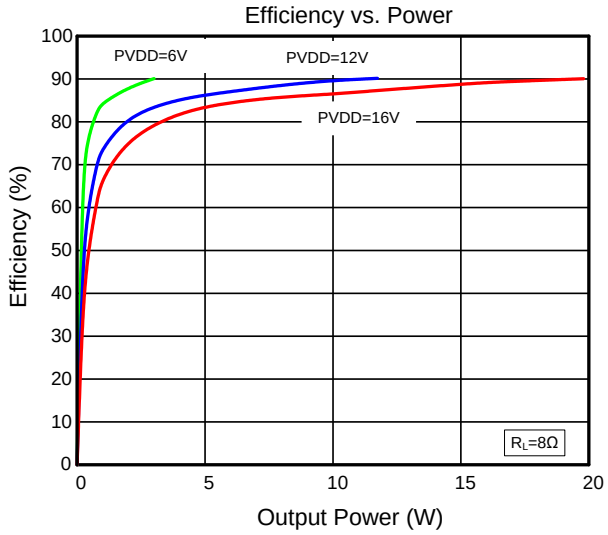


Efficiency vs. Power









Function Description

The SY2A54055 is a mono analog-input audio amplifier for use in the automotive environment which is AEC-Q100 qualified with temperature grade1 (-40°C to 125°C), HBM ESD classification level H2, and CDM ESD classification level C3 per AEC-Q100-011 revD.

The function operations of SY2A54055 are as follows:

Gain Setting

The gain of the SY2A54055 is set by bit7 and bit6 of Control register(0x03). The programmable gains listed in Table 1 are realized by changing the taps on the input resistors inside the amplifier which causes the input impedance (Z_i) to be dependent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the gain variation from part-to-part is small. However, the input impedance from part-to-part at the same gain may shift by ±10% because of shifts in the actual resistance of the input resistors.

For design purposes, the input network should be designed assuming an input impedance of 4.1 kΩ, which is the absolute minimum input impedance of SY2A54055. At the lower gain settings, the input impedance could increase as high as 33 kΩ.

Table1. Gain and Input Impedance

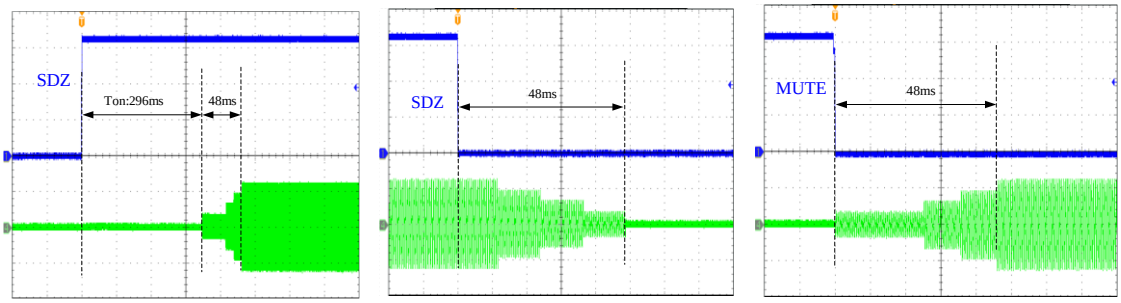
Amplifier Gain (dB)	Input impedance (kΩ)
20	30
26	15
32	7.5
36	4.6

SDZ and Mute Operation

The SY2A54055 employs a shutdown mode of operation designed to reduce supply current during periods of nonuse for power conservation. Pull down the SDZ pin, the amplifier will enter shutdown mode, then the internal 3.3V LDO (For AVDD and MOSFET gate driver) is disabled, MOSFET stay in Hi-Z state for low power dissipation, and the slave I^2C device can't be visited. Pull high SDZ pin, the amplifier will exit shutdown mode, perform load diagnostics and drive speaker for music.

The SY2A54055 has a mute mode to make the amplifier output silent, which is active high on MUTE pin. Pull down MUTE pin to return to normal play mode.

The SY2A54055 has the fade feature that the amplifier gain is changed step by step when entering operation mode or shutdown mode, with which the listener will be comfortable with the smooth sound status switching in psychoacoustics. There are three cases behaving with fade feature, amplifier exit shutdown, enter shutdown and exit mute. The typical fade period is about 48ms.



(a) exit shutdown (b) enter shutdown (c) exit mute

Figure 4. Fade Feature

Modulation Scheme

The SY2A54055 uses BD mode modulation scheme, see as Figure 5. Each output is switching from 0V to the supply voltage. The OUTP and OUTN are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTP is greater than 50% and OUTN is less than 50% for positive output voltages. The duty cycle of OUTP is less than 50% and OUTN is greater than 50% for negative output voltages. The voltage across

the load sits at 0V throughout most of the switching period, greatly reducing the switching current, which reduces any I^2R losses in the load.

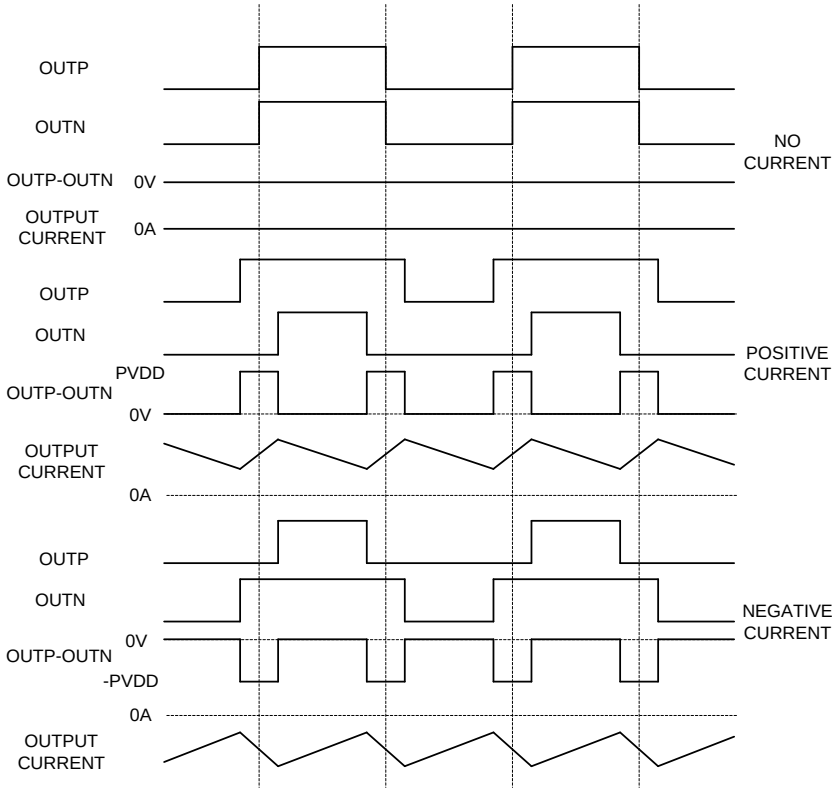


Figure 5. BD Mode Modulation

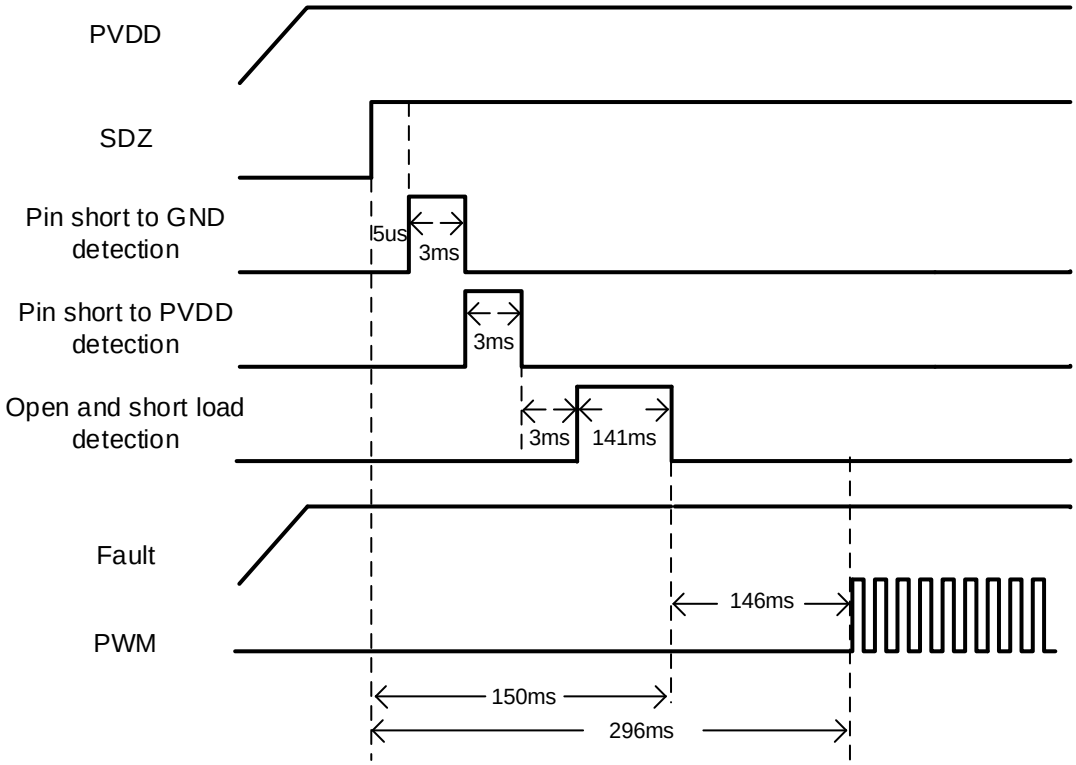
Load Diagnostics and Timing

The SY2A54055 incorporates load diagnostic circuitry designed for detecting and determining the status of output connections. It supports the following diagnostics:

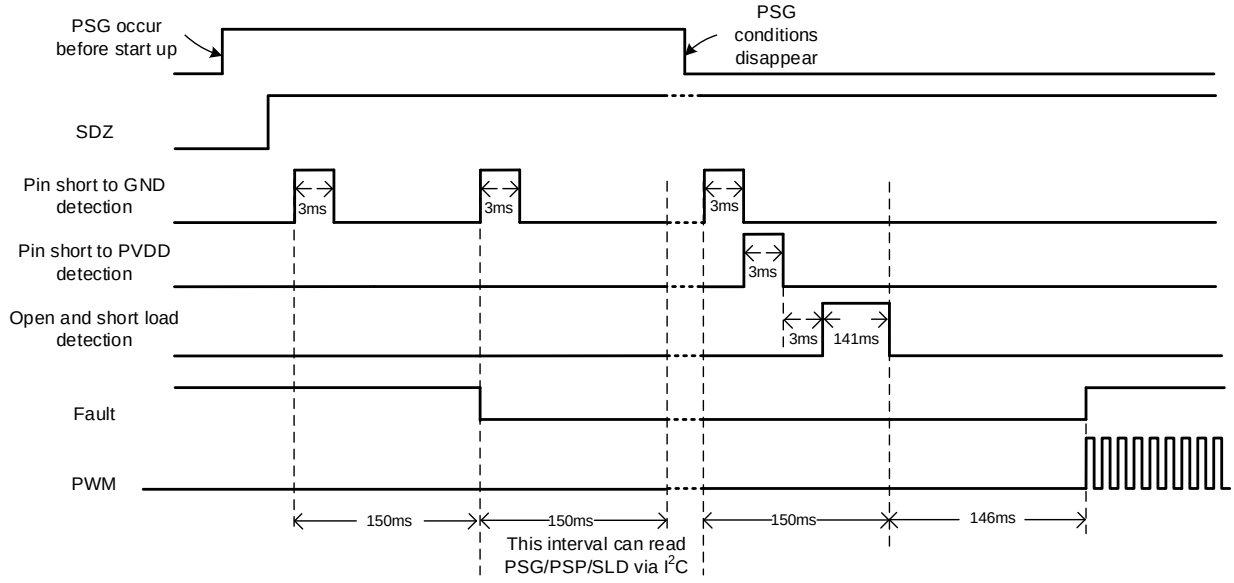
- Short to GND
- Short to PVDD
- Short load
- Open load

The SY2A54055 reports the presence of any of the short or open conditions to the system by Fault register(0x01) and Status and Load Diagnostic register(0x02). The load diagnostic function runs after SDZ low to high. During this test, the outputs are in a Hi-Z state. The device determines whether the output is a short to GND, short to PVDD, open load, or shorted load. The load diagnostic biases the output, which therefore requires limiting the capacitance value for proper functioning. The load diagnostic test takes approximately 150ms (typical) to detect the four load status, and then wait 146ms (typical) for control system acquiring LD result. On detection of an open load, the output still operates. On detection of any other fault condition, the output goes into a Hi-Z state and the device checks the load continuously with 150ms interval until removal of the fault condition. After detection of a normal output condition, the audio output starts.

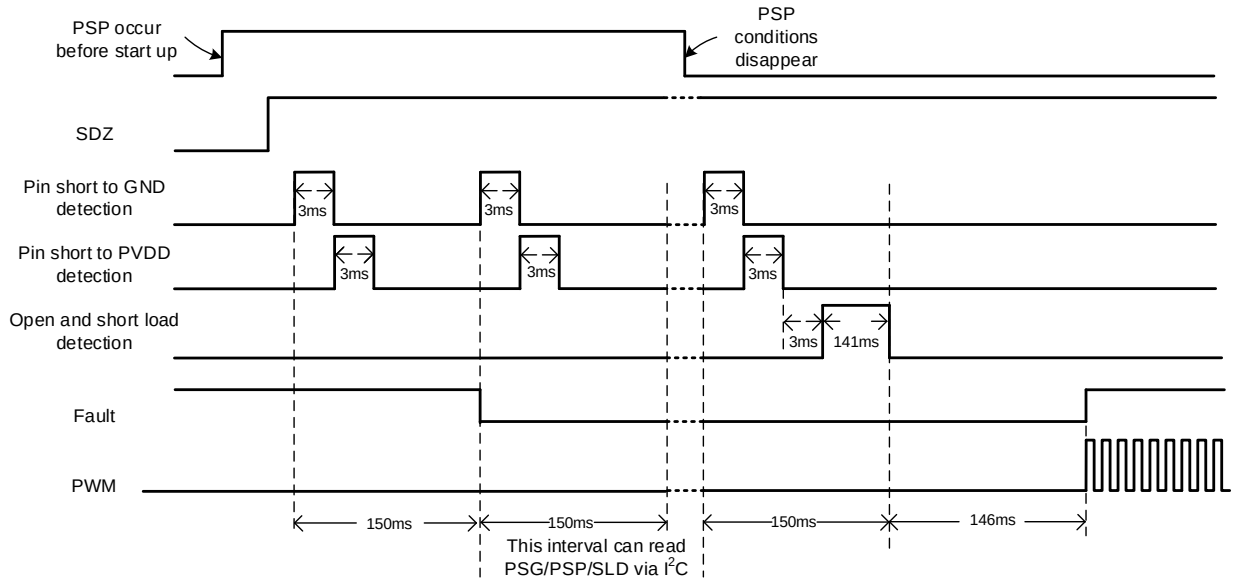
The SY2A54055 performs load diagnostic tests as shown in Figure 6.



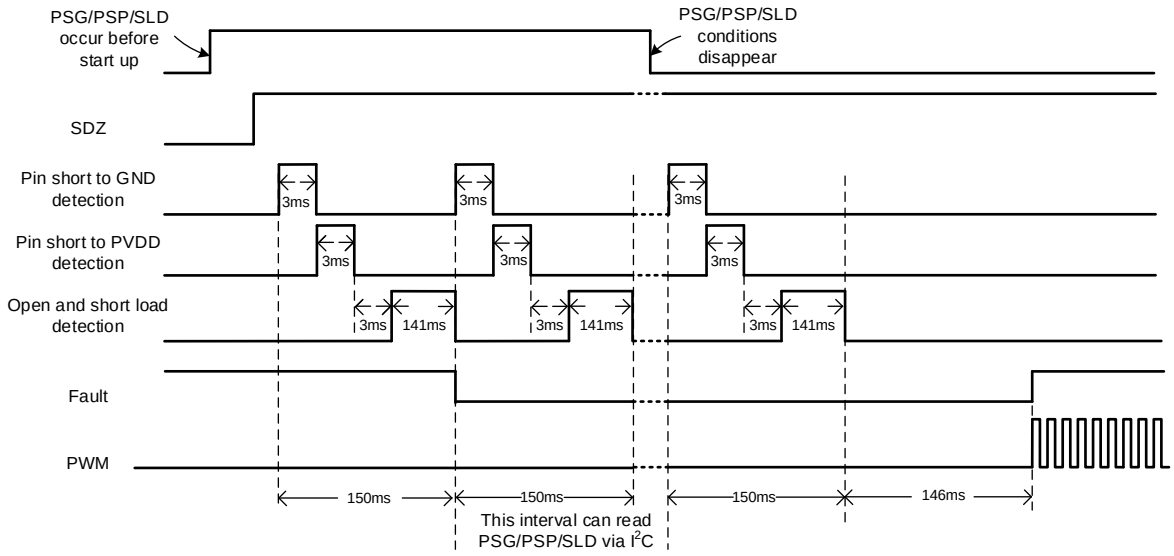
(a) Normal or OLD



(b) PSG detect continuously



(c) PSP detect continuously



(d) SLD detect continuously

Figure 6. Load Diagnostics Timing

In addition, if SY2A54055 is used in eCall system, where will do load diagnostic all the time unless an emergency happens, because of the timing variation, the recommended SDZ pull down time is at 215ms±15ms after SDZ pull up, which is appropriate to avoid entering play mode.

PLIMIT

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the duty cycle to a fixed maximum value. This limit can be thought of as a "virtual" voltage rail which is lower than the supply connected to PVDD. The limited output voltage can be set by bit3-bit5 of Control register(0x03). There are 7 selectable output voltage. This output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

The output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance, shown as Equation (1).

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L} \text{ for unclipped power} \qquad (1)$$

Where

- R_S is the total series resistance including $R_{DS(ON)}$, and any resistance in the output filter.
- R_L is the load resistance.
- V_P is the peak amplitude set in register 0x03.
- P_{OUT}(10% THD+N) =1.25 × P_{OUT}(unclipped).

I²C Serial Control Interface

The device communicates with the system processor via the I²C serial communication bus as an I²C slave-only device. The processor can poll the device via I²C to determine the operating status. All reports of fault conditions and detections are via I²C. The system can also set numerous features and operating conditions via I²C. The I²C interface is active approximately 1ms after the SDZ pin is high.

The I²C interface controls the following device features:

- Changing gain setting to 20dB, 26dB, 32dB, or 36dB.
- Controlling PLIMIT peak voltage value.
- Reporting load diagnostic results.
- Changing of switching frequency for AM radio avoidance.

The device has a bidirectional I²C interface that compatible with the I²C bus protocol and supports both 100kHz and 400kHz data transfer rates for single and multiple byte write and read operations. The device does not support a multi-master bus or wait state insertion. The I²C control is used to program the registers of the device and to read device status. The device performs all I²C operations without I²C wait cycles. The device address of SY2A54055 is 0xD8.

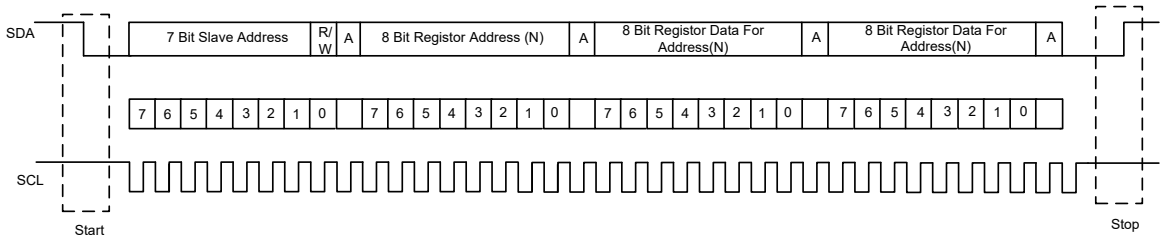


Figure 7. Typical I²C Sequence

Single and Multiple Byte Transfers

The I²C serial control interface supports both single byte and multiple read/write operations for sub addresses 0x00 to 0x03.

During multiple byte read operations, the device responds with data, a byte at a time, starting at the sub address assigned, as long as the master device continues to response with acknowledges. If a particular sub address does not contain 8*N bits, the unused bits are read as logic 0.

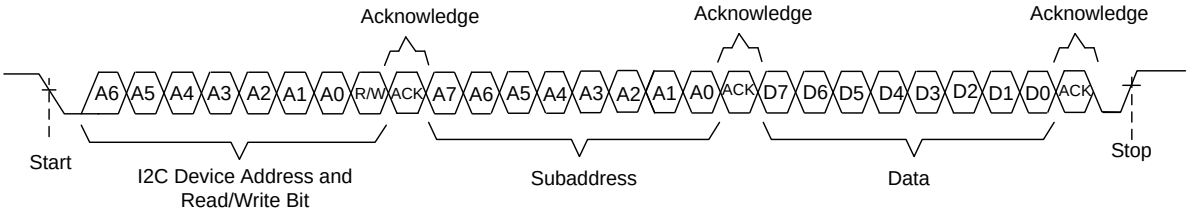


Figure 8. Single Byte Write Transfer

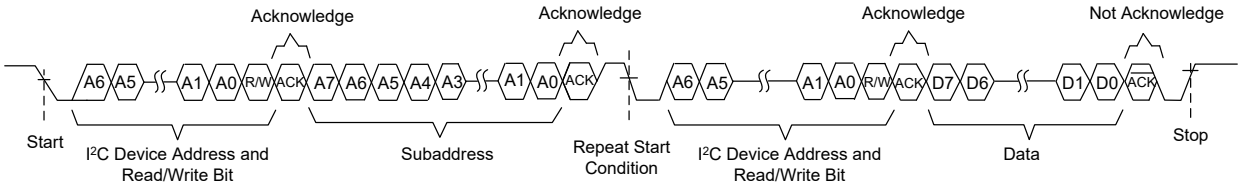


Figure 9. Single Byte Read Transfer

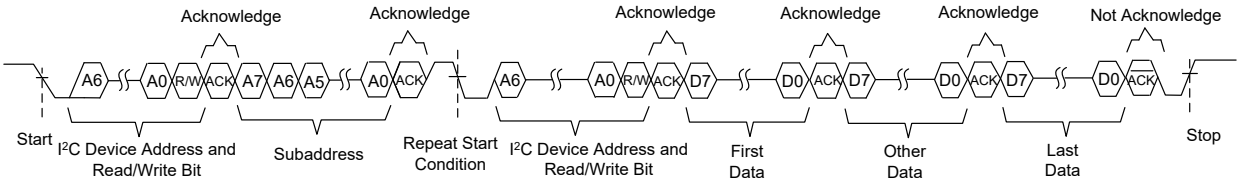


Figure 10. Multiple-Byte Read Transfer

Input Resistance

Changing the gain setting can vary the input resistance of the amplifier from the smallest value, 4.6 kΩ ±10%, to the largest value, 30 kΩ ±10%. As a result, if a single capacitor is used in the input high-pass filter, the –3 dB or cutoff frequency may change when changing gain steps.

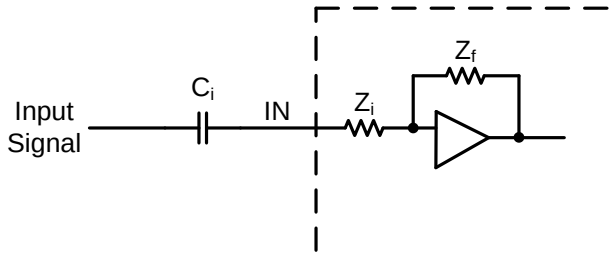


Figure 11. Input Impedance

Use Equation 2 to calculate the –3dB frequency. Use the values listed in Table 1 for R_i.

$$f_c = \frac{1}{2\pi \cdot R_i \cdot C_i} \quad (2)$$

Input Capacitor, C_i

In the typical application, input capacitor C_i is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case C_i and the input impedance of the amplifier (R_i) from a high-pass filter with the corner frequency are determined in Equation 2.

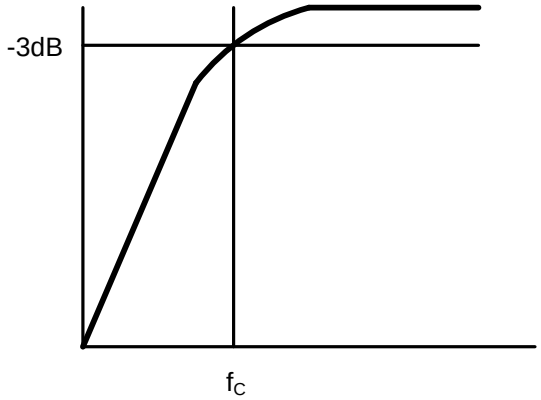


Figure12. -3dB frequency of HPF

The value of C_i is important, as it directly affects the bass (low-frequency) performance of the circuit. The input resistance of the SY2A54055 value is fixed at 30kΩ±20%, Consider the specification calls for a flat bass response down to 20Hz. Equation 2 is reconfigured as Equation 3.

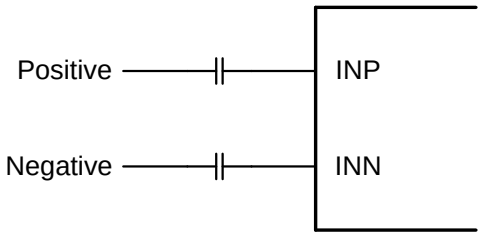
$$C_i = \frac{1}{2\pi \cdot R_i \cdot f_c} \qquad (3)$$

In this example, C_I is 0.26μF; so, one would likely choose a value of 0.47μF as this value is commonly used. A further consideration for this capacitor is the leakage path from the input source through the input network, C_I, and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at 2.4V, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application. Additionally, lead-frame solder can create dc offset voltages, and it is important to ensure that boards are cleaned properly.

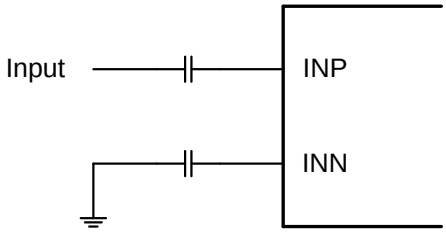
Differential Input

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the SY2A54055 with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the SY2A54055 with a single-ended source, AC-ground the INP or INN input through a capacitor equal in value to the input capacitor on INN or INP and apply the audio source to either input. In a single-ended input application, the unused input should be AC-grounded at the audio source instead of at the device input for best noise performance. For good transient performance, the impedance seen at each of the two differential inputs should be the same. The input signal connection is shown as Figure 13.

The impedance seen at the inputs should be limited to an RC time constant to allow the input dc blocking capacitors to become completely charged during the 100ms power-up time. If the input capacitors are not allowed to completely charge, there will be some additional sensitivity to component matching which can result in pop if the input components are not well matched.



(a) Differential Input



(b) Single-ended Input

Figure 13. Input Signal Connection

BSN and BSP

The half H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 470nF ceramic capacitor, rated for at least 16V, must be connected from

each output to its corresponding bootstrap input. Specifically, one 470nF capacitor must be connected from OUTP to BSP, and one 470nF capacitor must be connected from OUTN to BSN.
The bootstrap capacitors connected between the BSx pins and their corresponding outputs function as a floating power supply for the high-side N-channel power MOSFET gate-drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

GREG Supply

The GREG supply powers the gates of the output full bridge transistors. Add a 1μF capacitor to ground at this pin.

Efficiency: LC Filter Required with the Traditional Class-D Modulation Scheme

The main reason that the traditional Class-D amplifier needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme, because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is $2 \times V_{DD}$, and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The SY2A54055 modulation scheme has little loss in the load without a filter because the pulses are short and the change in voltage is V_{DD} instead of $2 \times V_{DD}$. As the output power increases, the pulses widen, making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed.

An LC filter with a cutoff frequency less than the Class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance but higher impedance at the switching frequency than the speaker, which results in less power dissipation, therefore increasing efficiency. Figure 14 is the typical LC filter structure.

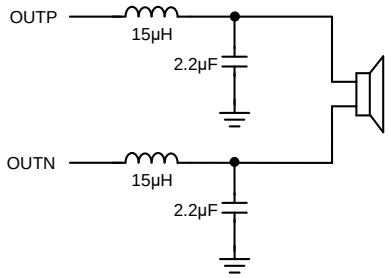


Figure 14. Typical LC output filter, Cutoff Frequency is 27 kHz, Speaker Impedance = 4Ω

Ferrite Bead Filter Consideration

When SY2A54055 is used in low output power application it is possible to design a high efficiency Class-D audio amplifier while minimizing interference to surrounding circuits. It is also possible to accomplish this with only a low-cost ferrite bead filter. In this case it is necessary to carefully select the ferrite bead used in the filter.

One important aspect of the ferrite bead selection is the type of material used in the ferrite bead. Not all ferrite material is alike, so it is important to select a material that is effective in the 10 to 100 MHz range which is the key to the operation of the Class D amplifier. Many of the specifications regulating consumer electronics have emissions limits as low as 30MHz. It is important to use the ferrite bead filter to block radiation in the 30 MHz and above range from appearing on the speaker wires and the power supply lines which are good antennas for these signals. The impedance of the ferrite bead can be used along with a small capacitor with a value in the range of 1000 pF to reduce the frequency spectrum of the signal to an acceptable level. For best performance, the resonant frequency of the ferrite bead/capacitor filter should be less than 10MHz.

Also, it is important that the ferrite bead is large enough to maintain its impedance at the peak currents expected for the amplifier. Some ferrite bead manufacturers specify the bead impedance at a variety of current levels. In this case

it is possible to make sure the ferrite bead maintains an adequate amount of impedance at the peak current the amplifier will see. If these specifications are not available, it is also possible to estimate the bead current handling capability by measuring the resonant frequency of the filter output at very low power and at maximum power. A change of resonant frequency of less than fifty percent under this condition is desirable.

A high quality ceramic capacitor is also needed for the ferrite bead filter. A low ESR capacitor with good temperature and voltage characteristics will work best.

Additional EMC improvements may be obtained by adding snubber networks from each of the class D outputs to ground. Suggested values for a simple RC series snubber network would be 10Ω in series with a 470pF capacitor although design of the snubber network is specific to every application and must be designed taking into account the parasitic reactance of the printed circuit board as well as the audio amp. Take care to evaluate the stress on the component in the snubber network especially if the amp is running at high PVDD. Also, make sure the layout of the snubber network is tight and returns directly to the PGND. The typical ferrite bead filter is shown as Figure 15.

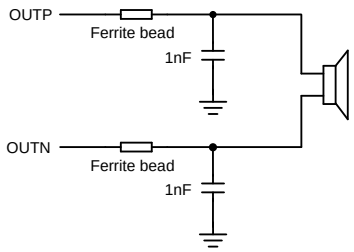


Figure 15. Typical Ferrite Bead EMI Filter

Output Filter Using Consideration for EMI Suppression

There may be a few circuit instances where it is necessary to add a complete LC reconstruction filter. These circumstances might occur if there are nearby circuits which are very sensitive to noise. In these cases, a classic second order Butterworth filter similar to those shown in the figures above can be used.

Some systems have little power supply decoupling from the AC line but are also subject to line conducted interference (LCI) regulations. These include systems powered by "wall warts" and "power bricks." In these cases, it LC reconstruction filters can be the lowest cost means to pass LCI tests. Common mode chokes using low frequency ferrite material can also be effective at preventing line conducted interference.

Protection Circuits

The device is fully protected against short circuit, over temperature, DC-detect, over voltage and under voltage.

Over-Current Protection (OCP)

The SY2A540554 has protection from over-current conditions caused by a short circuit on the output stage. The short circuit protection fault is reported on the FAULTZ pin as a low state. The amplifier outputs are switched to a Hi-Z state when the short circuit protection latch is engaged. The latch will be cleared after 775ms and the device will auto-recovery.

Under Voltage Lockout (UVLO) and Over Voltage Lockout (OVLO)

If at any time the voltage on the PVDD pin falls below the under voltage or rises above over voltage lockout threshold voltage, all circuitry in the device is disabled and internal logic is reset. The UVLO and OVLO can be reported on the FAULT pin and Fault Register. Operation resumes when PVDD rises above the UVLO threshold with hysteresis or falls below OVLO threshold with hysteresis.

Over Temperature Protection (OTP)

Thermal protection on the SY2A540554 prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of die is reduced by 15°C.

DC Detection

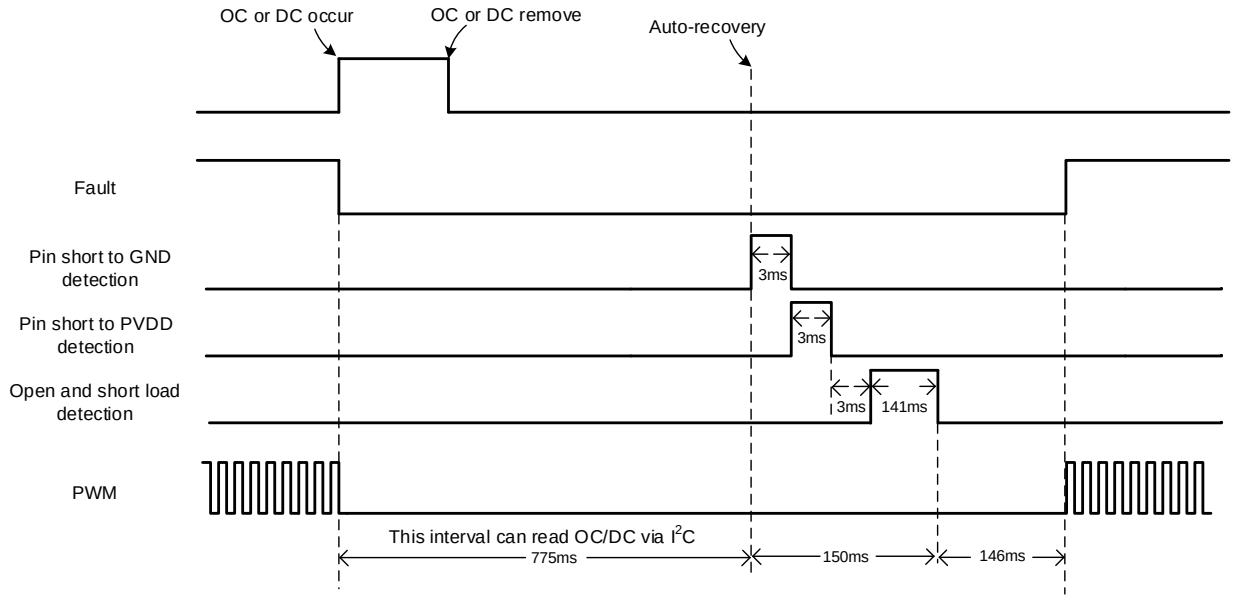
The SY2A540554 circuitry protects the speakers from DC current which might occur because of defective capacitors on the input or shorts on the printed circuit board at the inputs. A DC-detect fault is reported on the FAULT pin as a low state. The DC-detect fault also causes the amplifier to shut down by changing the state of the outputs to Hi-Z. The device will auto-recovery after DC protect 775ms.

A DC-detect fault is issued when the output differential duty-cycle exceeds 15% (for example, 58%, –42%) for more than 600ms at the same polarity. This feature helps protect the speaker from large DC currents or AC currents less than 1 Hz. To avoid nuisance faults because of the DC detect circuit, hold the SDZ pin low at power-up until the signals at the inputs are stable. Also, match the impedance at the positive and negative input to avoid nuisance DC-detect faults.

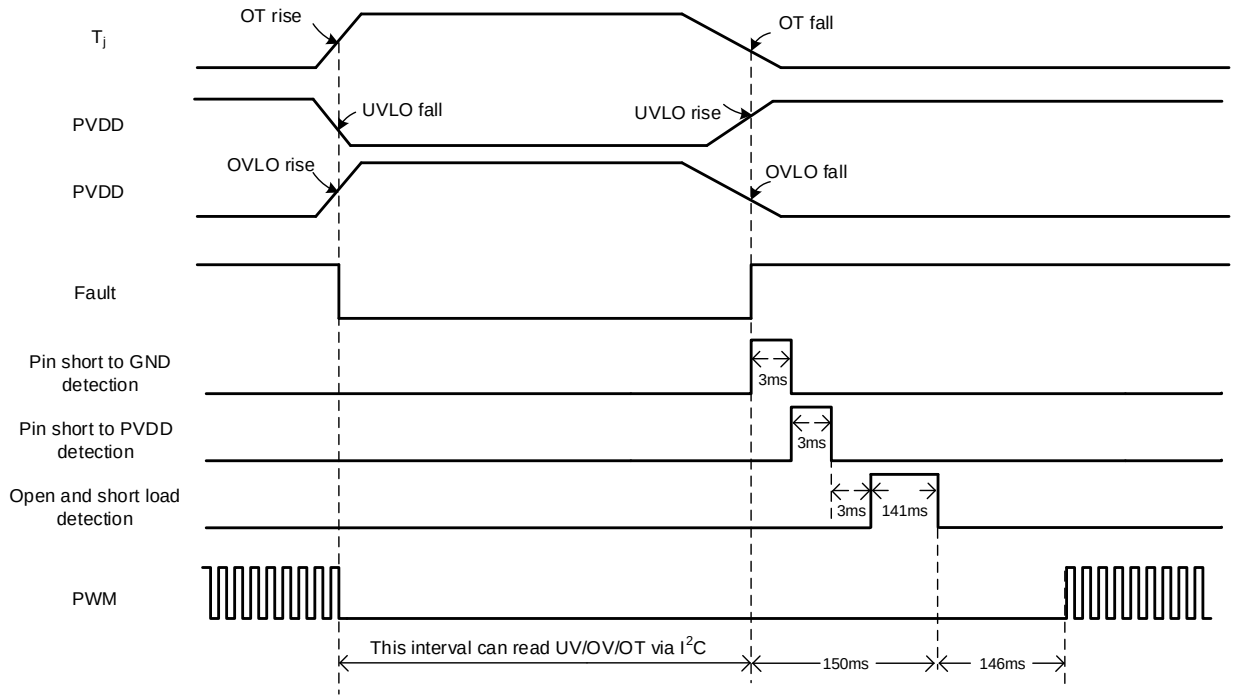
Fault and Actions

The following tables list fault and actions.

Fault Event	Fault Event Category	Monitoring States	Reporting Method	Action Result	Clearing
UV	Voltage fault	Except shutdown	I^2C + FAULTZ pin	Hi-Z	Self-recovery when fault conditions disappear
OV					
OTP	Thermal				
OC fault	Output channel fault	Play			Auto recovery after 775ms and repeat load diagnostic until pass, then PWM out after 146ms
DC detect					
PSG PSP SLD	Diagnostic	Perform on start up or auto-recovery			Repeat load diagnostic until pass
OLD			I^2C	Normal output	Cycle power or pull down SDZ



(a) Auto-recovery from OCP/DCP



(b) Auto-recovery from OTP/UVLO/OVLO

Figure 16. Auto-recovery Feature

Power Supply Recommendations

The power supply requirements for the SY2A540554 consist of one higher-voltage supply to power the output stage of the speaker amplifier. Several on-chip regulators are included on the SY2A540554 to generate the voltages necessary for the internal circuitry of the audio path. It is important to note that the voltage regulators which have been integrated are sized only to provide the current necessary to power the internal circuitry. The external pins are provided only as a connection point for off-chip bypass capacitors to filter the supply. Connecting external circuitry to these regulator outputs may result in reduced performance and damage to the device. The high voltage supply, between 4.5 V and 18 V, supplies the power stage (PVDD).

The SY2A54055 is a high-performance CMOS audio amplifier that requires adequate power-supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power-supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power-supply leads. For higher-frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (SER) ceramic capacitor, typically 0.1μF to 1μF, placed as close as possible to the device V_{DD} lead works best. For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 220μF or greater placed near the audio power amplifier is recommended. The 220μF capacitor also serves as local storage capacitor for supplying current during large signal transients on the amplifier outputs. The PVDD terminals provide the power to the output transistors, so a 220μF or larger capacitor should be placed on each PVDD terminal.

Printed Circuit Board (PCB) Layout

The SY2A54055 can be used with a small, inexpensive ferrite bead output filter for most applications. However, since the Class-D switching edges are fast, it is necessary to take care when planning the layout of the printed circuit board. The following suggestions will help to meet EMC requirements.

- Decoupling capacitors—The high-frequency decoupling capacitors should be placed as close to the PVDD terminals as possible. Large (220μF or greater) bulk power supply decoupling capacitors should be placed near the SY2A54055 on the PVDD supplies. Local, high-frequency bypass capacitors should be placed as close to the PVDD pins as possible. These caps can be connected to the thermal pad directly for an excellent ground

connection. Consider adding a small, good quality low ESR ceramic capacitor between 220pF and 1000pF and a larger mid-frequency cap of value between 0.1μF and 1μF also of good quality to the PVDD connections at each end of the chip.

- Keep the current loop from each of the outputs through the ferrite bead and the small filter cap and back to PGND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.
- Grounding—The PVDD decoupling capacitors should connect to GND. Analog ground and power ground should be connected at the thermal pad, which should be used as a central ground connection or star ground for the SY2A54055.
- Output filter—The ferrite EMI filter should be placed as close to the output terminals as possible for the best EMI performance. The LC filter should be placed close to the outputs. The capacitors used in both the ferrite and LC filters should be grounded to power ground.
- Thermal pad—The thermal pad must be soldered to the PCB for proper thermal performance and optimal reliability. The dimensions of the thermal pad and thermal land should be as large as possible. Solid vias should be equally spaced underneath the thermal land. The vias should connect to a solid copper plane, either on an internal layer or on the bottom layer of the PCB.

Register Maps

Table 1. I²C Address

Description	Fixed Address							Read/Write Bit	I2C Address
	MSB	6	5	4	3	2	1	LSB	
I2C Write	1	1	0	1	1	0	0	0	0xD8
I2C Read	1	1	0	1	1	0	0	1	0xD9

Table 2. I²C Address Register Summary

Description	R/W	Register Description
0x01	R	Latched Fault Register
0x02	R	Status and Load Diagnostic Register
0x03	R/W	Control Register

Table 3. Fault Register (0x01)

D7	D6	D5	D4	D3	D2	D1	D0	Function Description
0	0	0	0	0	0	0	0	No faults, default value
-	-	-	-	-	-	-	1	Reserved
-	-	-	-	-	-	1	-	Reserved
-	-	-	-	-	1	-	-	A load-diagnostics faults has occurred
-	-	-	-	1	-	-	-	Over current shutdown has occurred
-	-	-	1	-	-	-	-	PVDD under-voltage has occurred
-	-	1	-	-	-	-	-	PVDD over-voltage has occurred
-	1	-	-	-	-	-	-	DC offset protection has occurred
1	-	-	-	-	-	-	-	Over-temperature shutdown has occurred

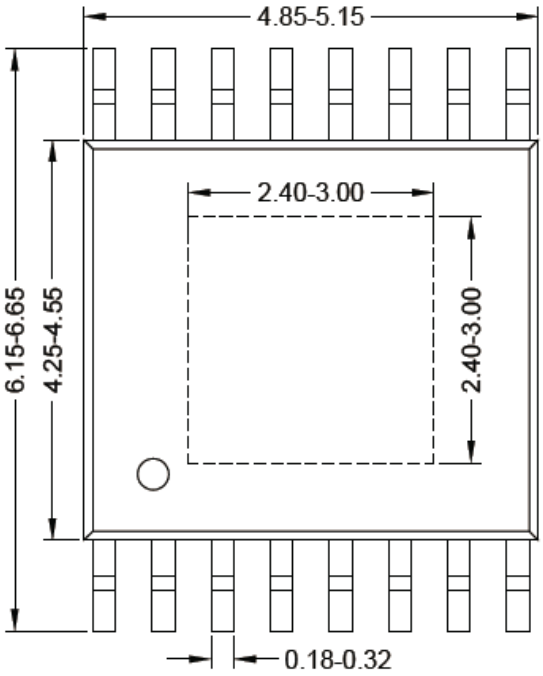
Table 4. Status and Load Diagnostic Register (0x02)

D7	D6	D5	D4	D3	D2	D1	D0	Function Description
0	0	0	0	0	0	0	0	No diagnostic faults, default value
-	-	-	-	-	-	-	1	Output short to PVDD
-	-	-	-	-	-	1	-	Output short to Ground
-	-	-	-	-	1	-	-	Open load
-	-	-	-	1	-	-	-	Shorted load
-	-	-	1	-	-	-	-	Load diagnostic error occurred
-	-	1	-	-	-	-	-	State reset or doing load diagnostic
-	1	-	-	-	-	-	-	In mute mode
1	-	-	-	-	-	-	-	In play mode

Table 5. Control Register (0x03)

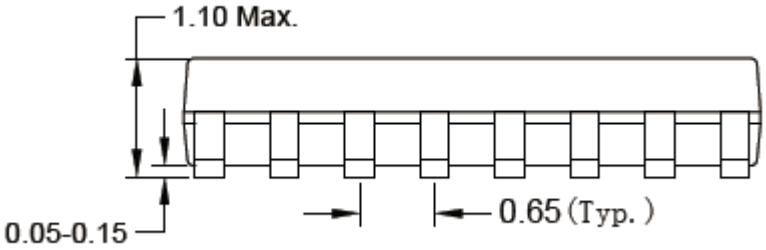
D7	D6	D5	D4	D3	D2	D1	D0	Function Description
0	1	1	1	1	0	0	0	Default value. 26dB gain, switching frequency is 400kHz. Power limit function disable
0	0	-	-	-	-	-	-	20dB gain
0	1	-	-	-	-	-	-	26dB gain
1	0	-	-	-	-	-	-	30dB gain
1	1	-	-	-	-	-	-	36dB gain
-	-	1	1	1	-	-	-	Power limit function disable
-	-	1	1	0	-	-	-	Power limit to 11.5V peak output
-	-	1	0	1	-	-	-	Power limit to 9.6V peak output
-	-	1	0	0	-	-	-	Power limit to 7.5V peak output
-	-	0	1	1	-	-	-	Power limit to 6.1V peak output
-	-	0	1	0	-	-	-	Power limit to 4.9V peak output
-	-	0	0	1	-	-	-	Power limit to 4.2V peak output
-	-	0	0	0	-	-	-	Power limit to 3.4V peak output
-	-	-	-	-	-	-	1	Switching frequency set to 500kHz
-	-	-	-	-	1	1	-	reserved

TSSOP16E Package Outline Drawing

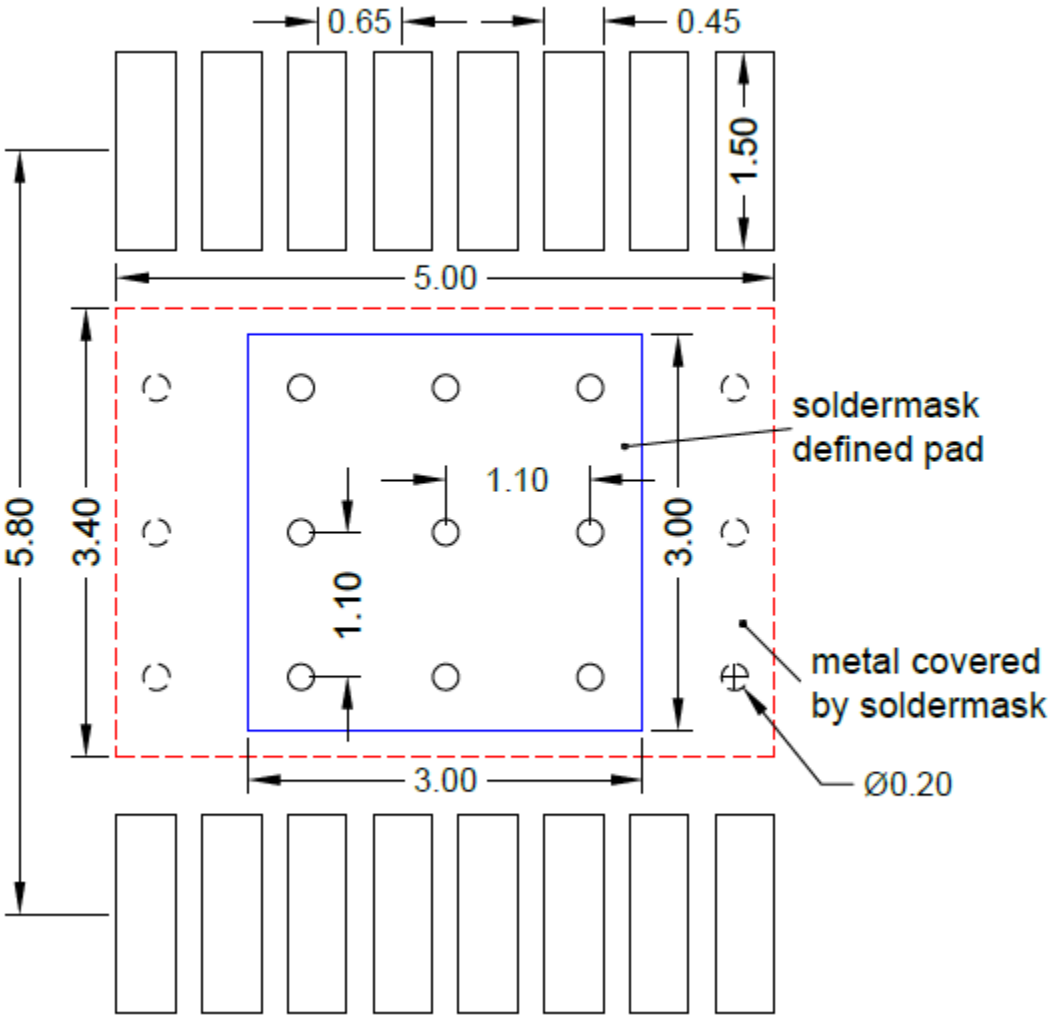


Top view

Side view A



Side view B

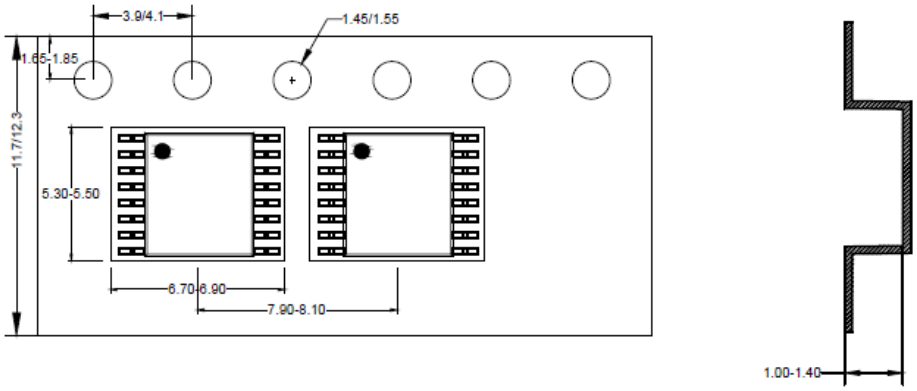


Recommended PCB layout
(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

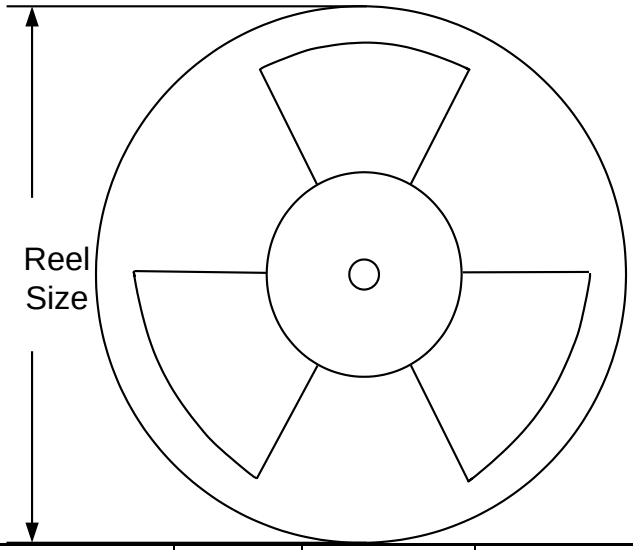
Taping & Reel Specification

1. TSSOP16E taping orientation



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
TSSOP16E	12	8	400	400	3000

3. Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, not warrantied. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
0.9	Dec.16, 2022	Initial Release	
1.0	Dec. 16, 2023	Production Release	

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