

General Description

The SY205259DWC is a low-capacitance transient voltage suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for data interfaces. With a typical capacitance of 160pF, the SY205259DWC is designed to protect systems against overvoltage and overcurrent transient events. It complies with IEC 61000-4-2 (ESD, $\pm 30\text{kV}$ air, $\pm 30\text{kV}$ contact discharge), IEC 61000-4-5 (Surge, 22A, 8/20 μs), etc.

Each SY205259DWC device can protect one data line. It offers system designers flexibility to protect single data line where space is a premium concern.

Features

- Transient Protection for Data Lines
 - IEC 61000-4-2 (ESD) $\pm 30\text{kV}$ (Air) $\pm 30\text{kV}$ (Contact)
 - IEC 61000-4-5 (Surge) 22A (8/20 μs)
- Package Optimized for Data Lines
- Ultra-small Package: DFN1.0x0.6-2L
- Protects One Data, Control or Power Line
- Capacitance: 160pF (Typical)
- Low Leakage Current: 0.1 μA @ V_{RWM} (Max.)
- Low Clamping Voltage

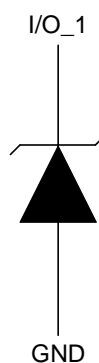
Applications

- Portable Electronics
- Desktops, Servers and Notebooks
- Cellular Phones
- MP3 Ports
- Digital Camera Ports

Mechanical Characteristics

- Package: DFN1.0x0.6-2L
- Marking: Device Code, Date Code
- Packaging: Tape and Reel

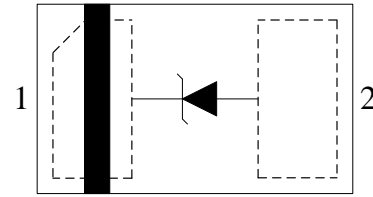
Circuit Diagram



Ordering Information

Part Number	Package Type	Top Mark
SY205259DWC	DFN1.0x0.6-2L RoHS Compliant and Halogen Free	BM

Pinout (Top View)



Marking Codes



Note 1: “B” is device code, fixed.

Note 2: “M” is date code.

Absolute Maximum Rating (1)				
Parameter	Symbol	Min	Max	Unit
Maximum Peak Pulse Current (8/20μs)	I_{PP}		22	A
Maximum Peak Pulse Power (8/20μs)	P_{PK}		220	W
ESD per IEC 61000-4-2 (Air)	V_{ESD}	-30	30	kV
ESD per IEC 61000-4-2 (Contact)				
Operating Temperature	T_{OPT}	-40	+125	°C
Storage Temperature	T_{STG}	-55	+150	°C

Electrical Characteristics $T_A = 25^\circ\text{C}$ (4)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal Reverse Working Voltage	V_{RWM}				5.0	V
Reverse Leakage Current @ V_{RWM}	I_R	$V_{RWM} = 5\text{V}, T = 25^\circ\text{C}$		0.01	0.1	μA
Reverse Breakdown Voltage @ I_T	V_{BR}	$I_T = 1\text{mA}$	5.6		8	V
Clamping Voltage @ $I_{PP} (5)$	V_C	$I_{PP} = 22\text{A}, t_p = 8/20\mu\text{s}$		10		V
Clamping Voltage @ $I_{PP} (5)$	V_C	$I_{PP} = 16\text{A}, t_p = 10/100\text{ns}$		7.8		V
Dynamic Resistance(2,5)	R_{DYN}	$t_p = 10/100\text{ns}$		0.06		Ω
Parasitic Capacitance (5)	C_{ESD}	$V_R = 0\text{V}, f = 1\text{MHz}$		160	180	pF

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: R_{DYN} calculated based on $I_{PP}=8\text{A}$ to $I_{PP}=16\text{A}$, $t_p = 10/100\text{ns}$.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested at $T_A \approx T_J = -40$ to 125°C . Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design or statistical correlation and not production tested.

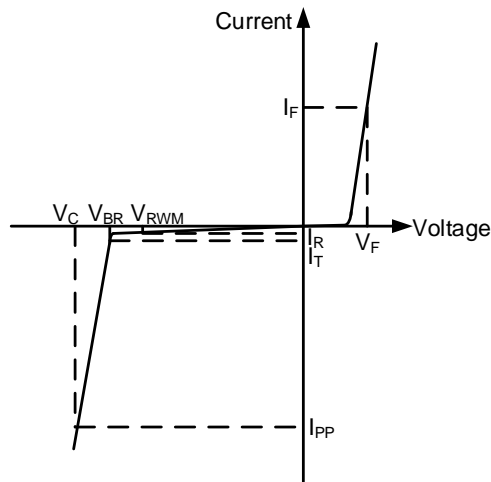
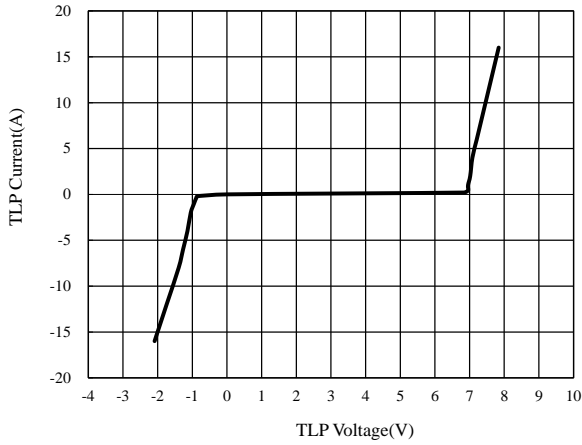


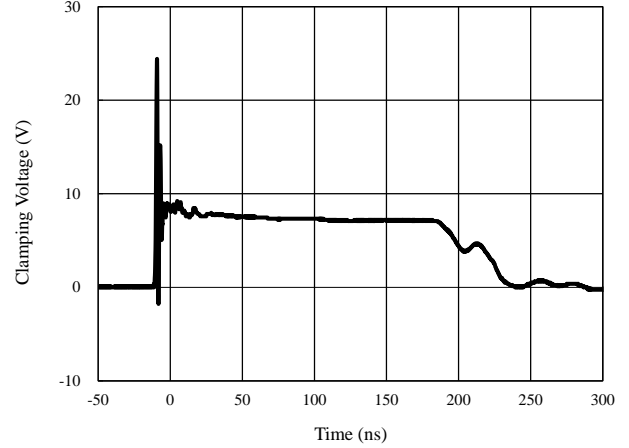
Figure 1. Uni- directional TVS

Typical Characteristics

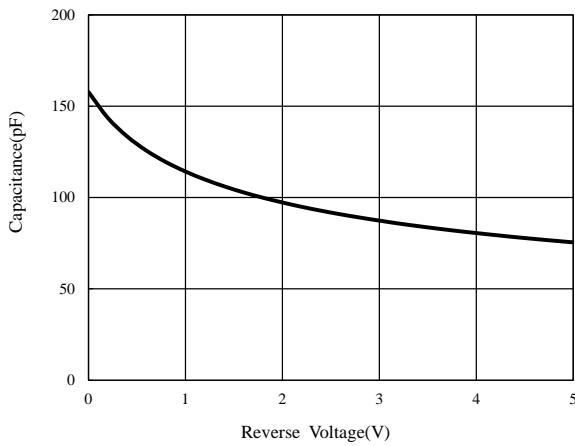
TLP testing of I/O to GND



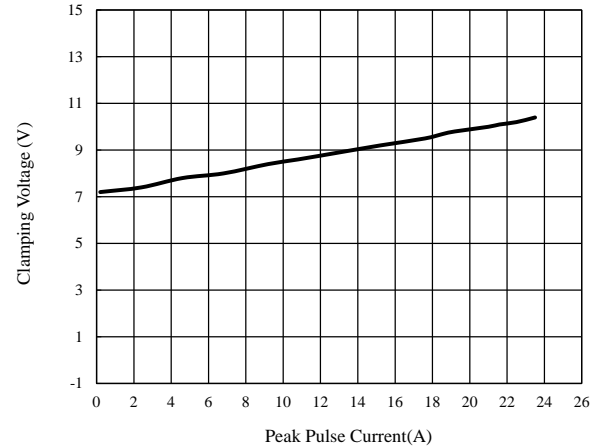
ESD Clamping of I/O to GND (+8kV Contact per IEC 61000-4-2)



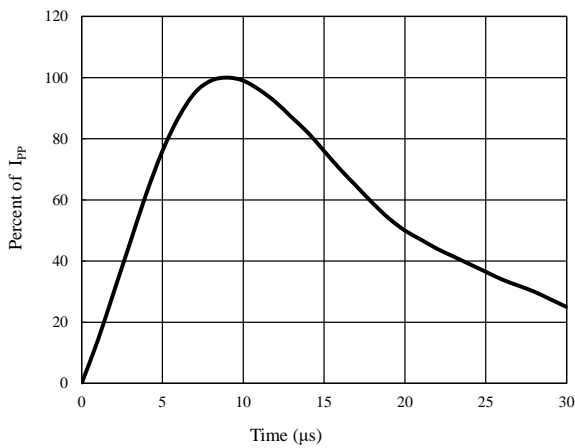
Capacitance vs. Reverse Voltage



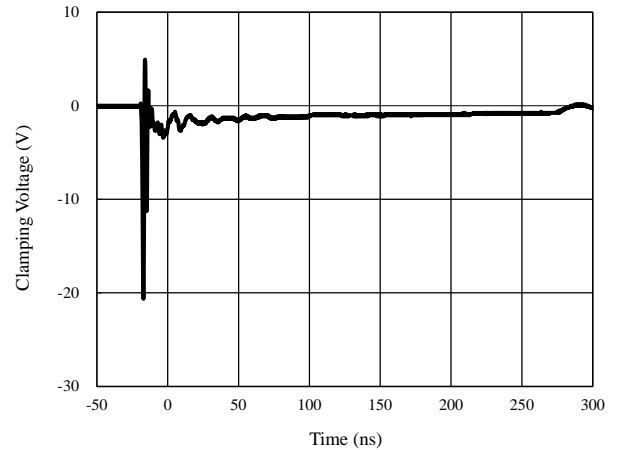
Clamping Voltage vs. Peak Pulse Current



8/20μs Pulse Waveform



ESD Clamping of I/O to GND (-8kV Contact per IEC 61000-4-2)



Application Information

Pin Connection in PCB

The SY205259DWC is designed to protect one Uni-directional data line against overvoltage and overcurrent transient events by clamping it to an acceptable reference.

The connection of the SY205259DWC pins is shown in Figure 2 below. The protected line is connected at Pin 1. Pin 2 is the GND, which should connect to a ground plane on the PCB board. All traces connected to the SY205259DWC pins should be as short as possible to minimize the parasitic inductance.

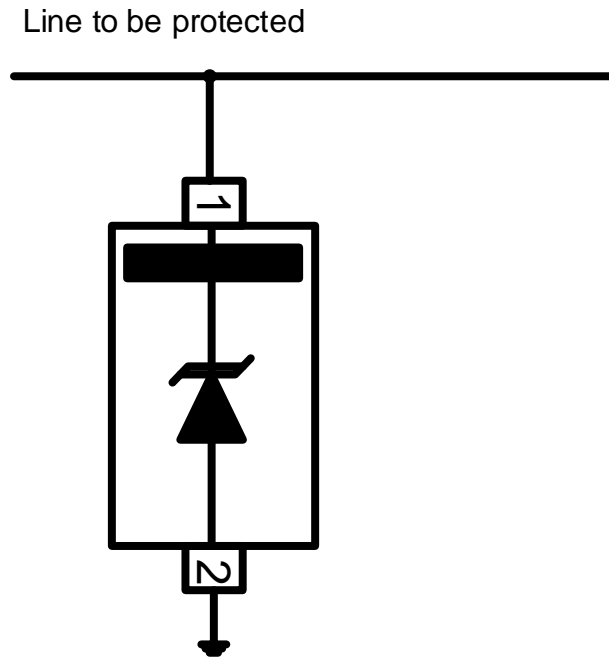


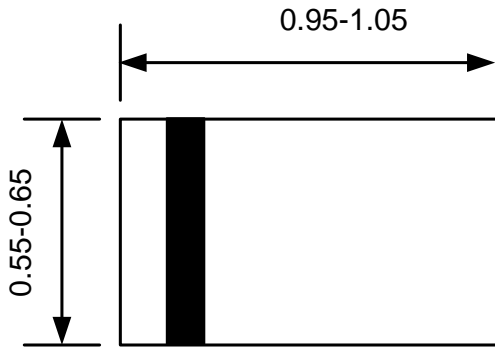
Figure 2. ESD/Surge Protection Circuit

PCB Layout Guidelines

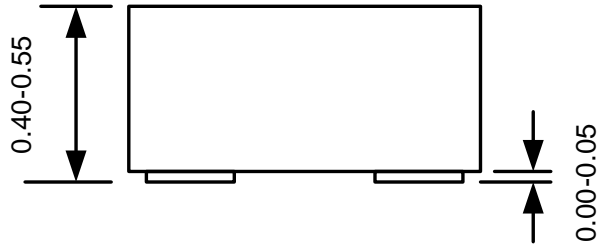
In order to obtain good ESD protection, a good circuit design is necessary. Thus the following circuit board guidelines are recommended.

- Place the SY205259DWC as close to the connectors or terminals port as possible.
- The vias should be wide, which connect SY205259DWC to the ground of board.
- Avoid running signals near board edges
- The SY205259DWC should be placed near the protected lines.
- SY205259DWC ground pin to the board ground rail path should be as short as possible. It could reduce the ESD transient return path to ground.

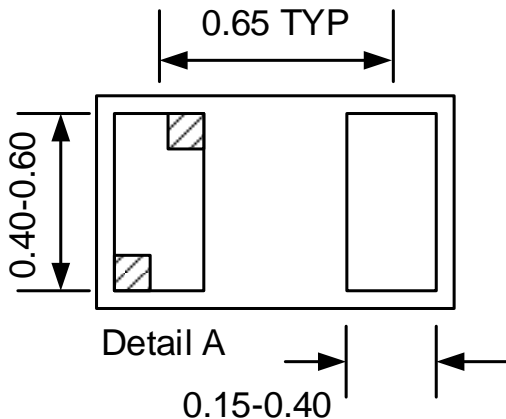
DFN1.0x0.6-2L Package Outline Drawing



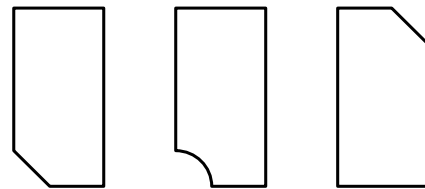
Top View



Side View

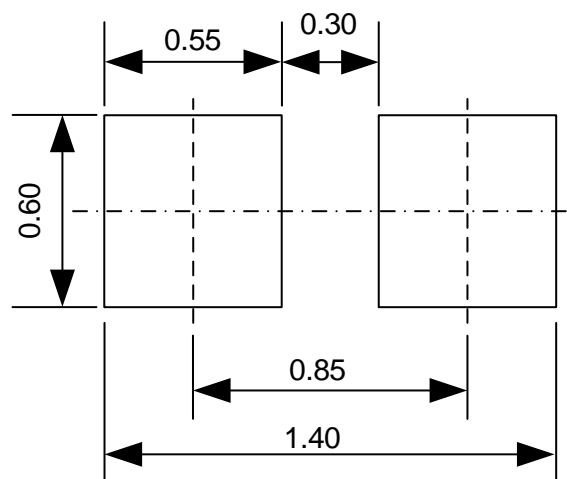


Bottom View



Pin1 Identifier: 3 options

Detail A

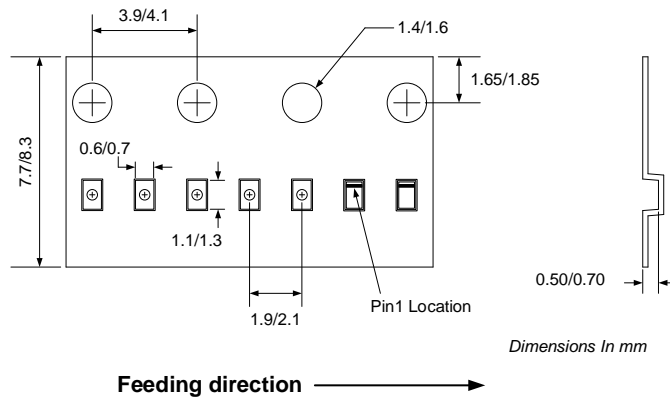


Recommended PCB Layout
(Reference only)

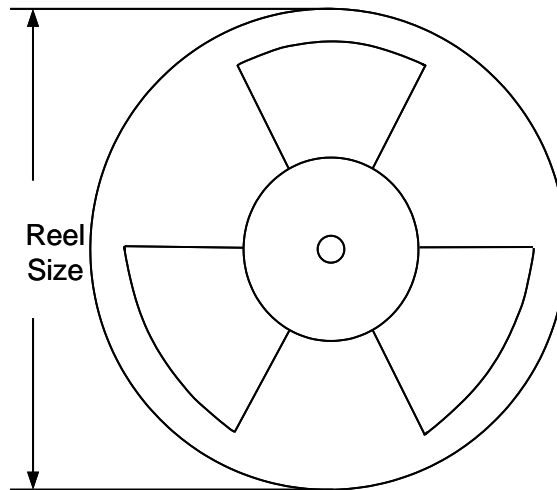
Note: All dimensions are in millimeters and exclude mold flash and metal burr.

Tape and Reel Specification

Tape Dimensions and Pin 1 Orientation



Reel Dimensions



Package Type	Tape Width (mm)	Pocket pitch(mm)	Leader Length (mm)	Qty per Reel(pcs)
DFN1.0x0.6-2L	8	2	400	10000



Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
0.9	August 29, 2023	Initial Release	
1.0	February 6, 2025	Production Release. Language Improvement for clarity.	

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