

General Description

The SY205270DWC is a single-line, uni-directional transient voltage suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for various applications.

The device protects sensitive electronic components from ESD and other transient overcurrent events. It complies with IEC 61000-4-2 (ESD) standards (\pm 30kV air, \pm 30kV contact discharge) and IEC 61000-4-5 (surge) standards (12A, 8/20µs).

The SY205270DWC is available in a DFN1.0×0.6-2L package with an operating voltage of 20V.

Features

- Operating Voltage: 20V and Below
- Transient Protection for a Single Line
 - IEC61000-4-2(ESD) ±30kV (Air) ±30kV (Contact)
 - IEC61000-4-5(Surge) 12A (8/20µs)
- Protects One Data, Control or Power Line
- Capacitance: 85pF(Typical)
- Low Leakage Current: 0.01µA@V_{RWM}(Typical)
- Low Clamping Voltage

Applications

- USB VBUS Lines Protection
- Desktops, Servers, and Notebooks
- Smart Phones
- Microprocessor Based Equipment
- Portable Instrumentation

Mechanical Characteristics

- DFN1.0×0.6-2L Package
- Marking: Device Code, Date Code
- Packaging: Tape and Reel

Circuit Diagram



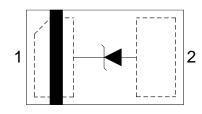


SY205270DWC

Ordering Information

Part Number	Package type	Top Mark
SY205270DWC	DFN1.0×0.6-2L	aM

Pinout (Top View)



Marking Codes



Note: "a" is device code, fixed.

"M" is date code.

Absolute Maximum Rating(Note 1)					
Parameter	Symbol	Min	Мах	Unit	
Peak Pulse Current (8/20µs)	I _{PP}		12	А	
Peak Pulse Power (8/20µs)	Ррк		450	W	
ESD per IEC 61000-4-2 (Air)	Vesd	-30	30	k)/	
ESD per IEC 61000-4-2 (Contact)	VESD	-30	30	kV	
Junction Temperature	TJ	-40	+125	°C	
Storage Temperature	Tstg	-55	+150	°C	

Electrical Characteristics (IO referenced to GND, $T_A = 25^{\circ}C$ (Note 2))						
Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Nominal Reverse Operating Voltage	Vrwm				20	V
Reverse Leakage Current at V _{RWM}	I _R	$V_{RWM} = 20V$			0.1	μA
Reverse Breakdown Voltage at I_T	V_{BR}	l⊤ = 1mA	22		28	V
Forward Voltage at IF	VF	I _F =1mA	0.4		1.2	V
Clamping Voltage at IPP (Note 3)	Vc	I _{PP} = 12Α, t _p = 8/20μs		33		V
Clamping Voltage at IPP (Note 3)	Vc	$I_{PP} = 16A, t_p = 10/100ns$		26		V
Dynamic Resistance (Notes 3, 4)	Rdyn	t _p = 10/100ns		0.08		Ω
Parasitic Capacitance (Note 3)	CESD	$V_R = 0V$, f = 1MHz		85	110	pF

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J = 25^{\circ}$ C. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 3: Guaranteed by design or statistical correlation and not production tested.

Note 4: R_{DYN} calculated based on I_{PP} =8A to I_{PP} =16A, $t_p = 10/100$ ns.



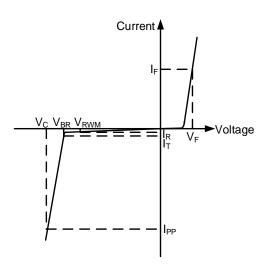
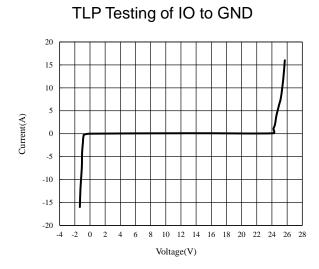


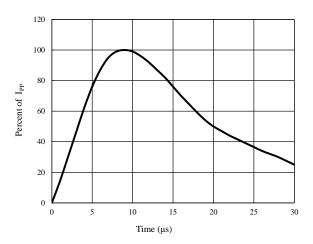
Figure 1. Uni-directional TVS



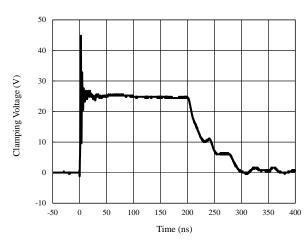
Typical Characteristics, IO Referenced to GND



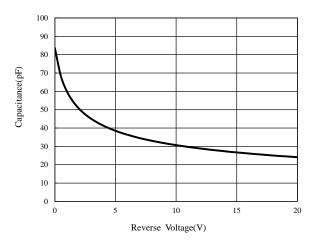
8/20µs Pulse Waveform



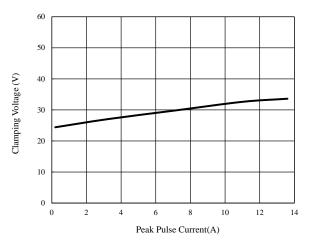
ESD Clamping of IO to GND (+8kV Contact per IEC 61000-4-2)



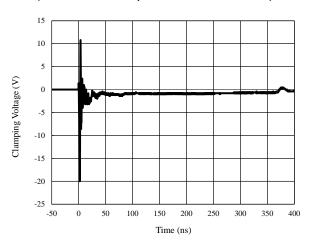
Capacitance vs. Reverse Voltage



Clamping Voltage vs. Peak Pulse Current



ESD Clamping of IO to GND (-8kV Contact per IEC 61000-4-2)





Application Information

PCB Pin Connections

The SY205270DWC protects one directional data line against overvoltage and overcurrent transient events by clamping it to an acceptable reference.

The SY205270DWC pin connections are shown in Figure 2. The protected line connects to Pin 1, while Pin 2 connects to GND, which should be tied to a ground plane on the board. All path lengths connected to the pins of the SY205270DWC should be as short as possible to minimize parasitic inductance.

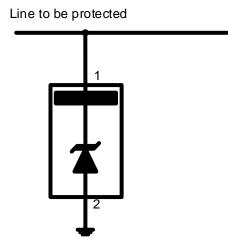


Figure 2. ESD/Surge Protection Circuit

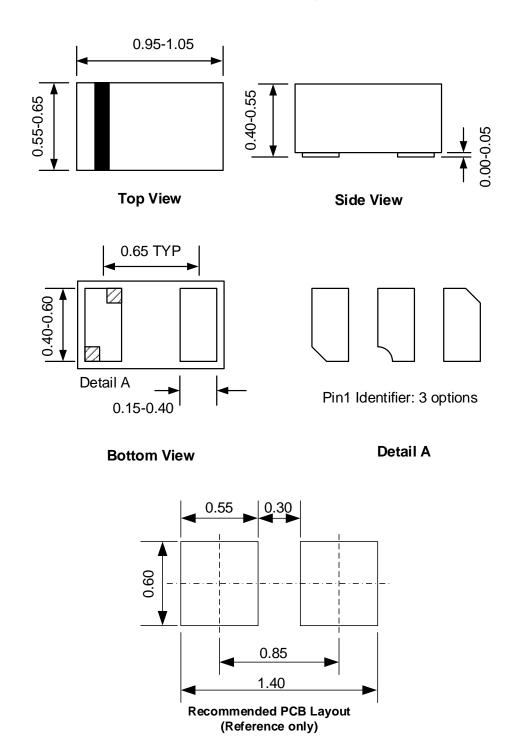
PCB Layout Guidelines

For optimum ESD protection and circuit performance, the following PCB layout guidelines are recommended:

- Place SY205270DWC as close to the connector or terminal ports as possible.
- Use a large via to connect the SY205270DWC pin to the ground.
- Avoid running signals near board edges.
- The SY205270DWC should be placed near the protected line.
- The distance between the SY205270DWC ground pin and the GND reference path should be as short as possible.





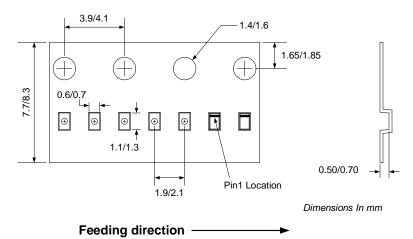


Notes: All dimensions are in millimeters and exclude mold flash and metal burr.

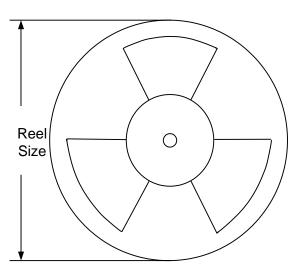


Tape and Reel Information

Tape Dimensions and Pin 1 Orientation



Reel Dimensions



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Qty per Reel (pcs)
DFN1.0×0.6-2L	8	2	7"	10000



Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, not warrantied. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
1.0	Jun. 05, 2024	Initial Release	



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