SY205271DWD

Low Capacitance TVS Protection

General Description

The SY205271DWD is a low-capacitance, bi-directional transient voltage suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for data, control, or power lines.

With a typical capacitance of 18pF, the device is designed to protect parasitic-sensitive systems against overvoltage and overcurrent transient events. It complies with IEC 61000-4-2 (ESD), (±30kV air, ±30kV contact discharge), and IEC 61000-4-5 (Surge) (6A, 8/20μs) standards.

Each SY205271DWD device can protect one line. It is available in a compact DFN1.0×0.6-2 package.

Features

- Transient Protection for Data Lines
  - IEC61000-4-2(ESD) ±30kV (Air) ±30kV (Contact)
  - IEC61000-4-5(Surge) 6A (8/20μs)
- Low Capacitance:18pF(Typical)
- Low Leakage Current: 0.01μA@V_{RWM}(Typical)
- Low Clamping Voltage

Applications

- Desktops, Servers and Notebooks
- Digital Camera Ports
- Smart Phones

Mechanical Characteristics

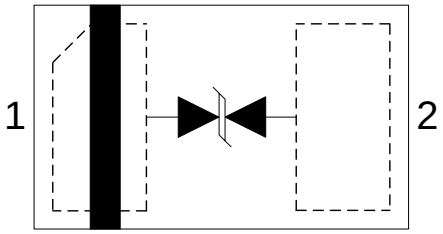
- DFN1.0×0.6-2 Package
- Marking: Device Code, Date Code
- Packaging: Tape and Reel

Circuit Diagram

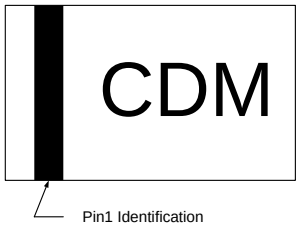
Ordering Information

Part Number	Package type	Top Mark
SY205271DWD	DFN1.0×0.6-2	CDM

Pinout (Top View)



Marking Codes



Note: "CD" is device code, fixed. M" is date code.

Absolute Maximum Ratings (Note 1)				
Parameter	**Symbol**	**Min**	**Max**	**Unit**
Peak Pulse Current (8/20μs)	I_{PP}		6	A
Peak Pulse Power (8/20μs)	P_{PK}		180	W
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	-30 -30	30 30	kV
Junction Temperature	T_J	-40	+125	°C
Storage Temperature	T_{STG}	-55	+150	°C

Electrical Characteristics (Between IO1 and IO2, T_A = 25°C)						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
Nominal Reverse Working Voltage	V_{RWM}				15	V
Reverse Leakage Current at V_{RWM}	I_R	V_{RWM} = 15V, T_A = 25°C		0.01	0.1	μA
Reverse Breakdown Voltage at I_T	V_{BR}	I_T = 1mA	16.6		23	V
Dynamic Resistance (Notes 3, 4)	R_{DYN}	t_p = 10/100ns		0.17		Ω
Clamping Voltage at I_{PP} (Note 3)	V_C	I_{PP} =6A, t_p = 8/20μs		28	30	V
Clamping Voltage at I_{PP} (Note 3)	V_C	I_{PP} = 16A, t_p = 10/100ns		25		V
Parasitic Capacitance (Note 3)	C_{ESD}	V_R = 0V, f = 1MHz		18	22	pF

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$ = 25℃. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 3: Guaranteed by design or statistical correlation and not production tested.

Note 4: R_{DYN} calculated based on I_{PP}=8A to I_{PP}=16A, t_p = 10/100ns

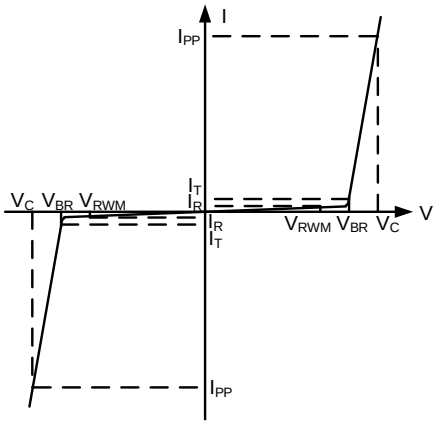
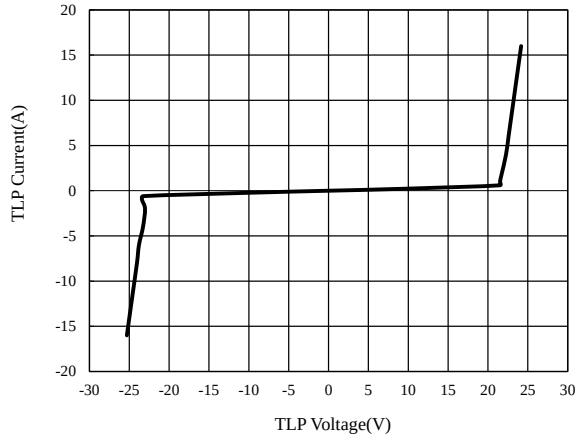


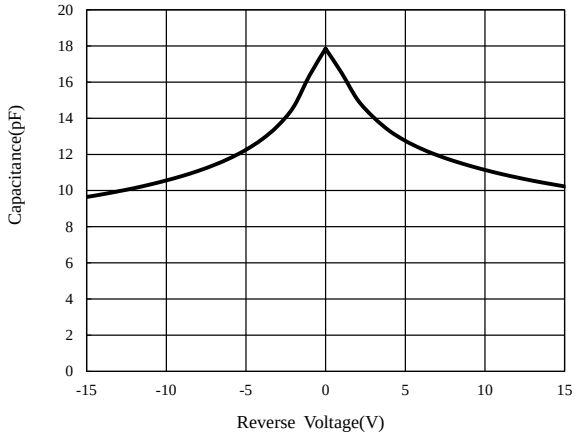
Figure 1. Bi-directional TVS

Typical Performance Characteristics, Between IO1 and IO2

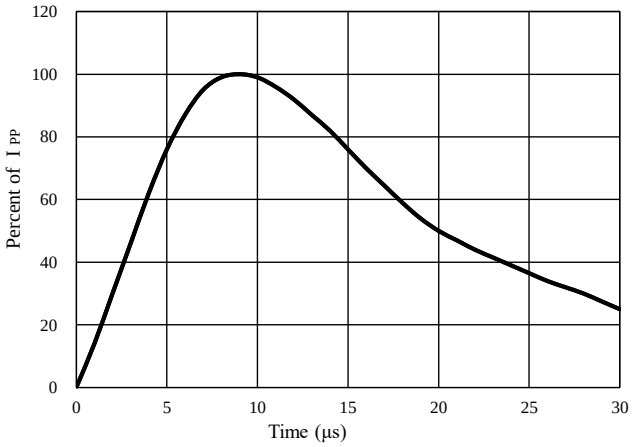
TLP Testing of IO1 to IO2



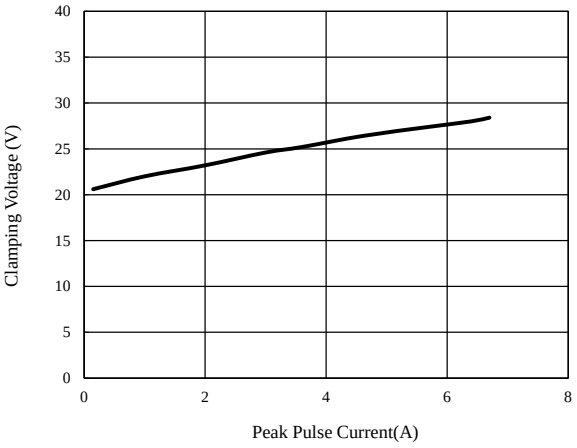
Capacitance vs. Voltage



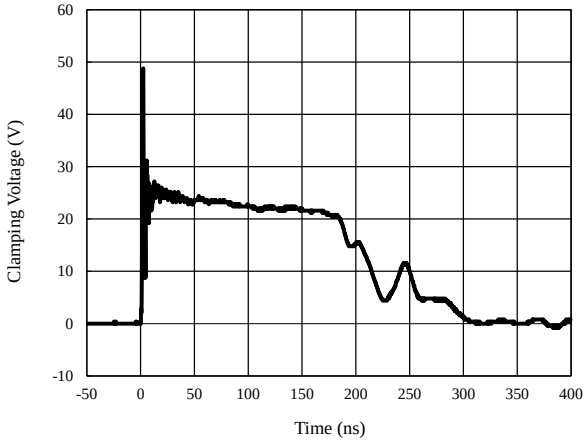
Pulse Waveform



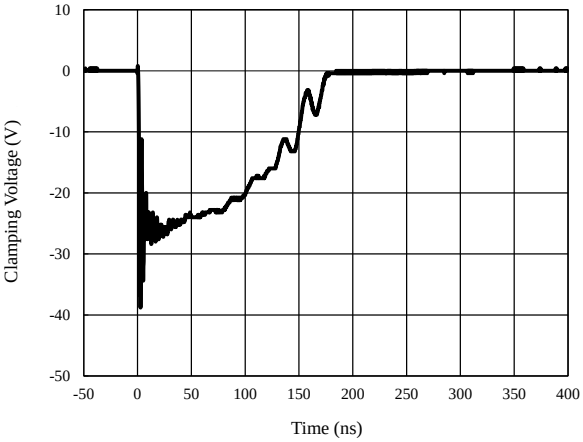
Clamping Voltage vs. Peak Pulse Current



ESD Clamping of IO1 to IO2
(+8kV Contact per IEC 61000-4-2)



ESD Clamping of IO1 to IO2
(-8kV Contact per IEC 61000-4-2)



Application Information

PCB Pin Connections

The SY205271DWD protects one bidirectional data line against overvoltage and overcurrent transient events by clamping it to an acceptable reference.

The SY205271DWD pin connections are shown in Figure 2. The protected line connects to one of the pins, while the other can connect to GND, which should connect to a ground plane on the board. All path lengths connected to the pins of the SY205271DWD should be as short as possible to minimize parasitic inductance

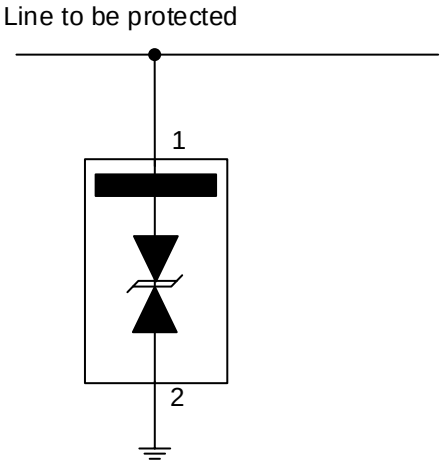


Figure 2. ESD/Surge Protection Circuit

PCB Layout Guidelines

For optimum ESD protection and circuit performance, the following PCB layout guidelines are recommended:

- Place SY205271DWD as close to the connector or terminal ports as possible.
- Use a large via to connect the SY205271DWD pin to the ground.
- Avoid running signals near board edges.
- The SY205271DWD should be placed near the protected line.
- The distance between the SY205271DWD ground pin and the GND reference path should be as short as possible.

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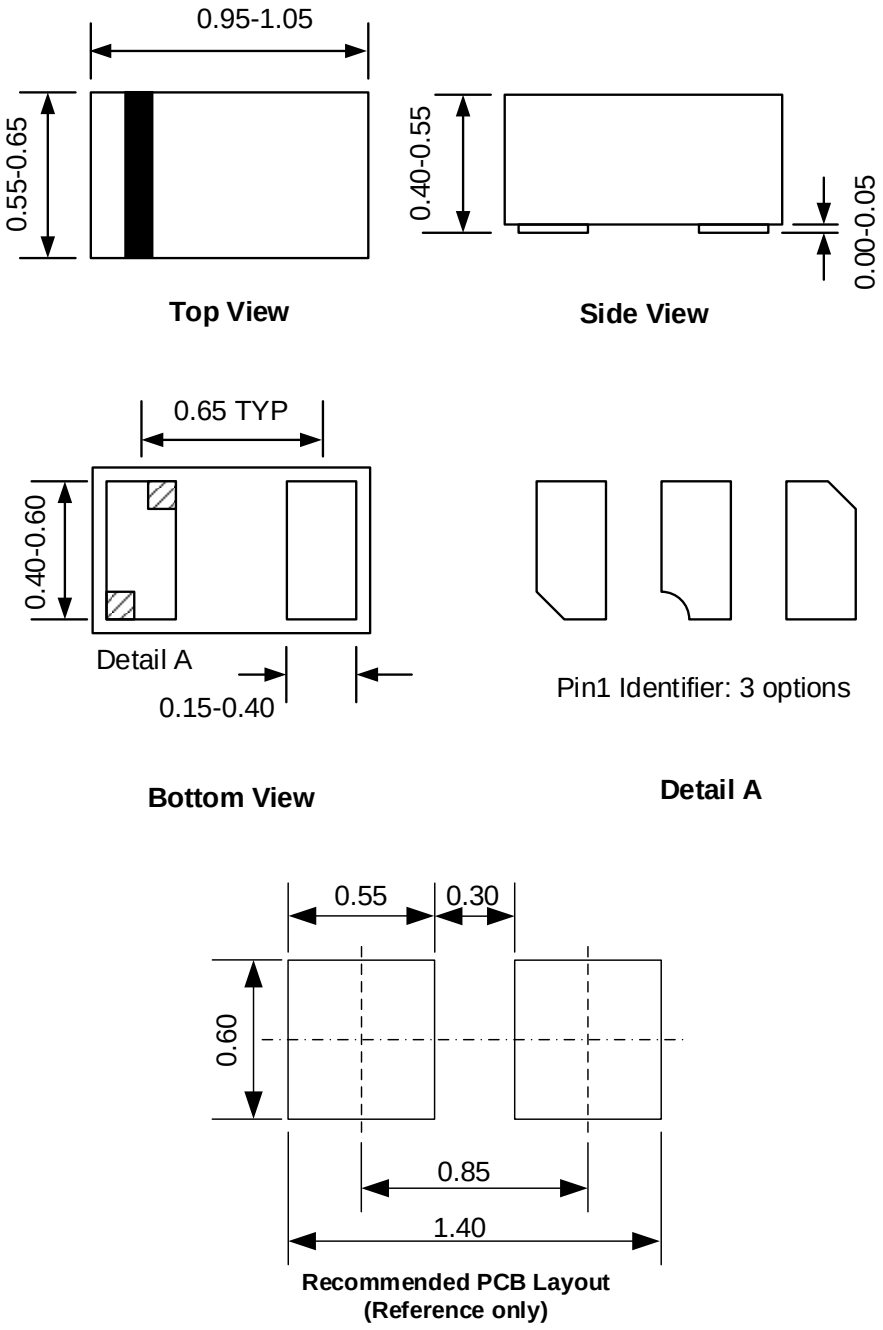
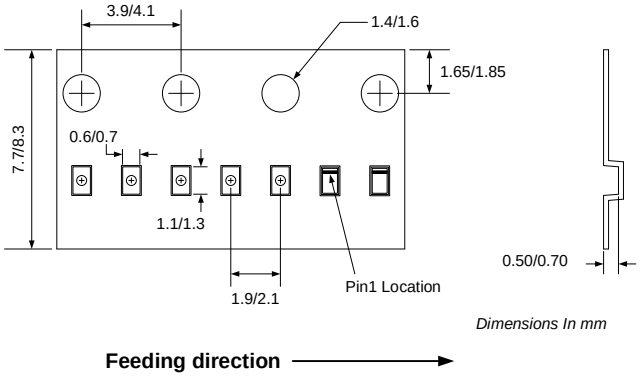
DFN1.0×0.6-2 Package Outline



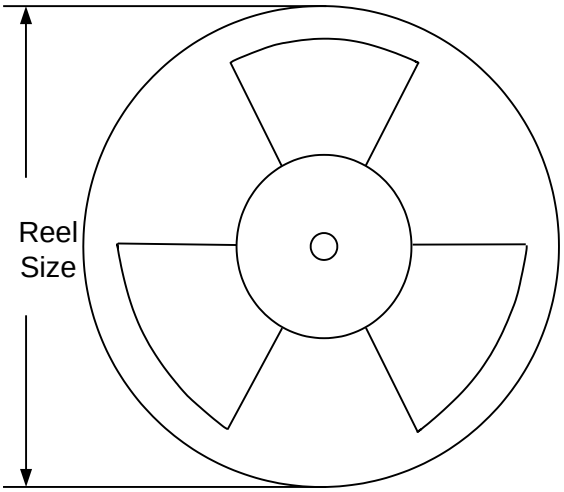
Notes: All dimensions are in millimeters and exclude mold flash and metal burr.

Tape and Reel Information

Tape Dimensions and Pin 1 Orientation



Reel Dimensions



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Qty per Reel (pcs)
DFN1.0×0.6-2L	8	2	7"	10000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, not warrantied. Please make sure that you have the latest revision..

Revision Number	Revision Date	Description	Pages changed
1.0	Jun.05, 2024	Initial Release	

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