

General Description

The SY205276DWD is an ultra-low capacitance uni-directional transient voltage suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces.

With a typical capacitance of 0.85pF, the device is designed to protect parasitic-sensitive systems against overvoltage and overcurrent transient events. It complies with IEC 61000-4-2 (ESD), ($\pm 30\text{kV}$ air, $\pm 30\text{kV}$ contact discharge), and IEC 61000-4-5 (Surge) (14A, 8/20 μs) standards.

The SY205276DWD can protect one high-speed data line. Its ultra-low capacitance, ultra-small size, and high ESD robustness make the SY205276DWD ideal for high-speed data ports and high-frequency line applications. The low clamping voltage of the SY205276DWD guarantees minimum stress on the protected device.

Features

- Operating Voltage: 5V and Below
- Transient Protection for High-speed Data Lines
 - IEC61000-4-2 (ESD) $\pm 30\text{kV}$ (Air) $\pm 30\text{kV}$ (Contact)
 - IEC61000-4-5 (Surge) 14A (8/20 μs)
- Ultra Low Capacitance: 0.85pF (Typical)
- Protects One High-Speed Data Line
- Low Clamping Voltage

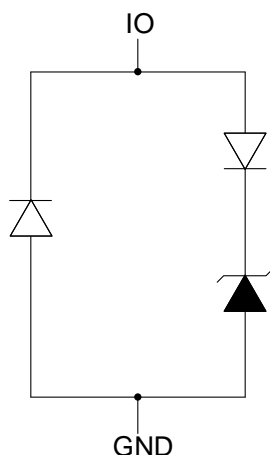
Applications

- Desktops, Servers and Notebooks
- USB2.0

Mechanical Characteristics

- DFN1.0x0.6-2 Package
- Marking: Device Code, Date Code
- Packaging: Tape and Reel

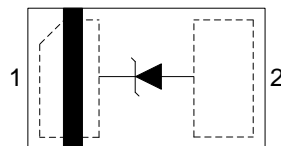
Circuit Diagram



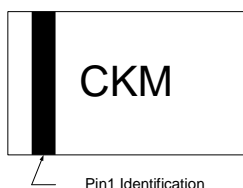
Ordering Information

Pinout (Top View)

Part Number	Package Type	Top Mark
SY205276DWD	DFN1.0x0.6-2	CKM



Marking Codes



Notes: “CK” is device code, fixed.

“M” is date code.

Pin Descriptions

Device Pins	Name	Description
1	Input/Output	IO
2	GND	GND

Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Min	Max	Unit
ESD per IEC 61000-4-2 (Air)	V_{ESD}	-30	30	kV
ESD per IEC 61000-4-2 (Contact)		-30	30	
Junction Temperature	T_J	-40	+125	°C
Storage Temperature	T_{STG}	-55	+150	°C

Electrical Characteristics (IO Referenced to GND, $T_A = 25^\circ\text{C}$, Note 4)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal Reverse Working Voltage	V_{RWM}				5.0	V
Reverse Leakage Current at V_{RWM}	I_R	$V_{RWM} = 5\text{V}$, $T_A = 25^\circ\text{C}$		0.01	0.1	μA
Reverse Triggering Voltage at I_{t1}	V_{BR}	$I_{t1} = 1\text{mA}$, Pin1 to Pin2	5.6		10	V
Forward Voltage	V_f	$I_F = 1\text{mA}$, Pin2 to Pin1	0.4		1.2	V
Dynamic Resistance (Notes 2, 5)	R_{DYN}	$t_p = 10/100\text{ns}$		0.22		Ω
Clamping Voltage at I_{PP} (Note 5)	V_C	$I_{PP} = 16\text{A}$, $t_p = 10/100\text{ns}$		4.5		V
Clamping Voltage at I_{PP} (Note 5)	V_C	$I_{PP} = 14\text{A}$, $t_p = 8/20\mu\text{s}$		5	7	V
Parasitic Capacitance (Note 5)	C_{ESD}	$V_R = 1\text{V}$, $f = 1\text{MHz}$		0.85	1.2	pF

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: R_{DYN} calculated based on $I_{PP}=8\text{A}$ to $I_{PP}=16\text{A}$, $t_p = 10/100\text{ns}$

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J = 25^\circ\text{C}$. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design or statistical correlation and not production tested.

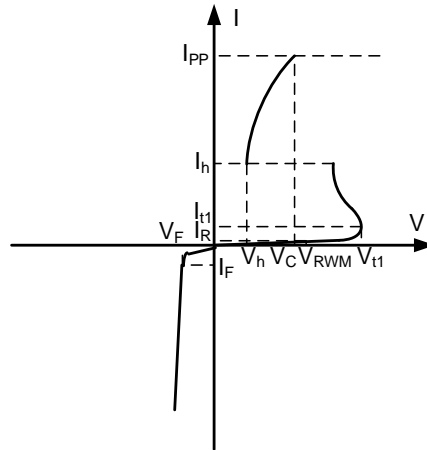
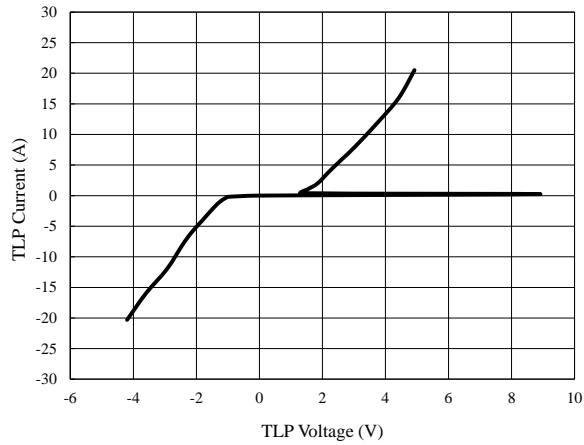


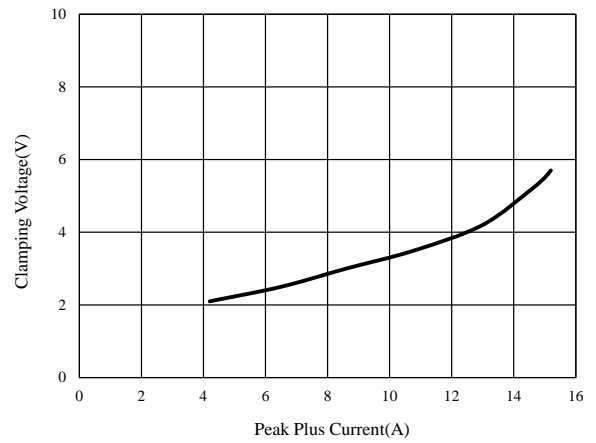
Figure 1. Unii-Directional TVS

Typical Performance Characteristics, IO Referenced to GND

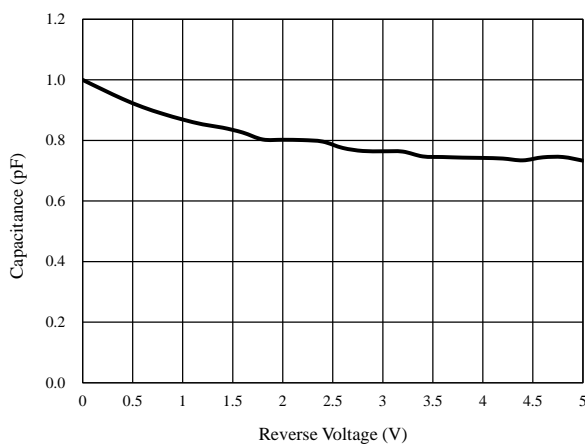
TLP Testing



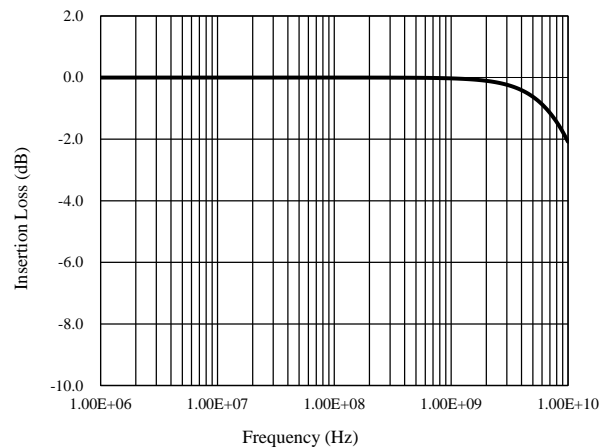
Clamping Voltage vs. Peak Pulse Current (8/20 μ s)



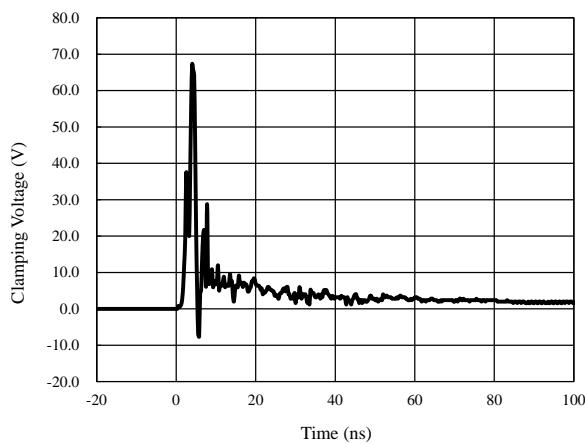
Capacitance vs. Voltage



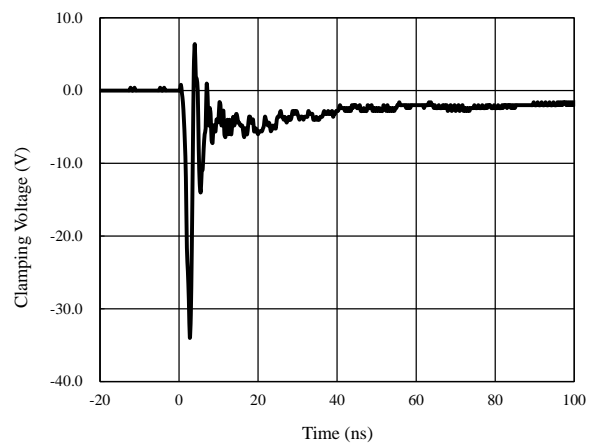
Insertion Loss S21



ESD Clamping (+8kV Contact per IEC 61000-4-2)



ESD Clamping (-8kV Contact per IEC 61000-4-2)



Application Information

The SY205276DWD provides ESD and surge protection for high-speed lines, such as USB 2.0. The device has a low clamping voltage of 4.5V at a TLP current of 16A, offering excellent ESD protection performance. Additionally, the surge IPP is 14A, with a surge clamping voltage of only 5V. It provides surge protection levels higher than 30V, ensuring robust surge protection performance.

PCB Pin Connections

Figure 2 shows the typical application for the USB 2.0. An SY205276DWD device can protect one high-speed line by connecting pin 1 to the high-speed line and pin 2 to the ground.

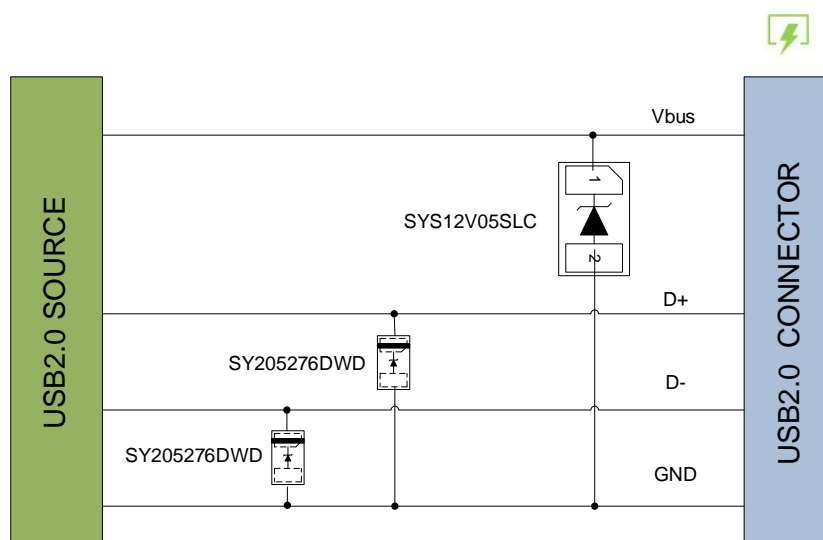


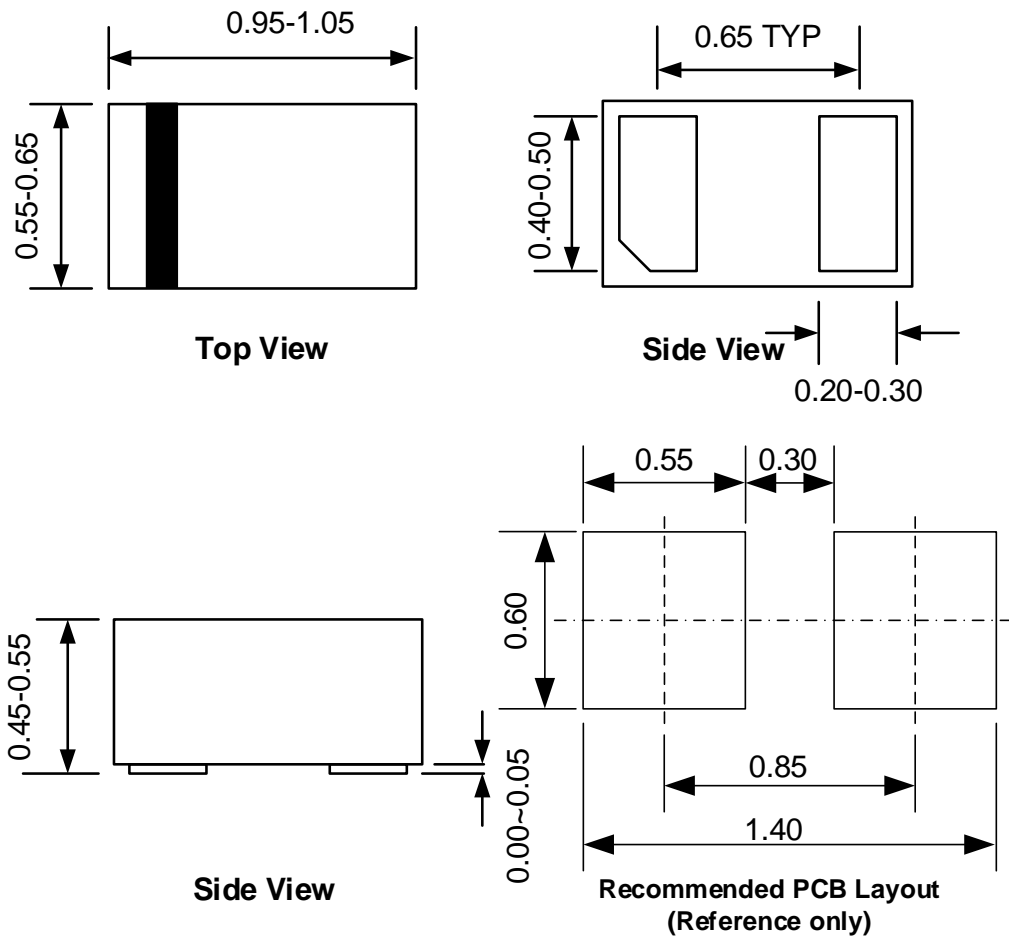
Figure 2. SY205276DWD Application for USB2.0

PCB Layout Guidelines

For optimum ESD protection and circuit performance, the following PCB layout guidelines are recommended:

- The SY205276DWD GND pin to the PCB GND rail path should be as short as possible to reduce the ESD transient return path to GND.
- The vias connecting the SY205276DWD GND pins to the PCB GND should be wide.
- Place SY205276DWD as close to the connector port as possible to reduce parasitic inductance and restrict ESD coupling into adjacent traces.
- Avoid running critical signals near board edges

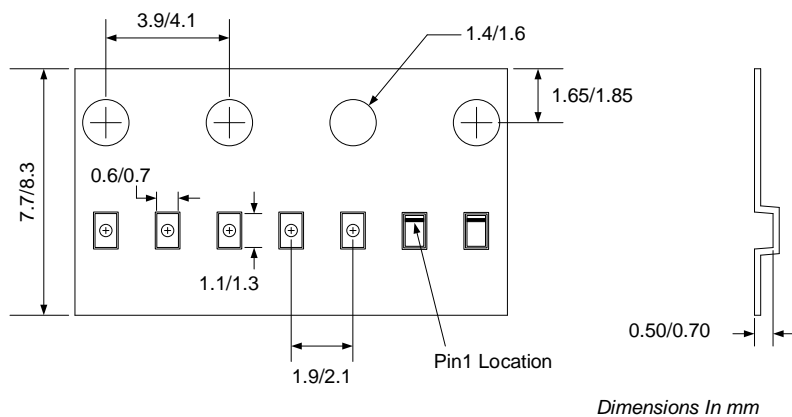
DFN1.0x0.6-2 Package Outline



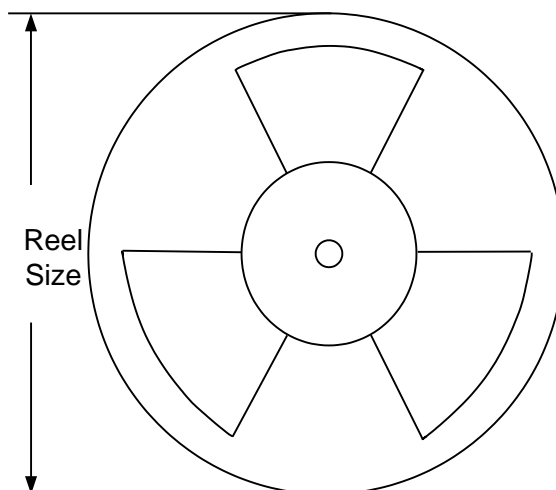
Note: All dimensions are in millimeters and exclude mold flash and metal burr.

Tape and Reel Information

Tape Dimensions and Pin 1 Orientation



Reel Dimensions



Package Type	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Qty per Reel (pcs)
DFN1.0x0.6-2	8	2	7"	10000



Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, not warranted. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
1.0	Jul.23, 2024	Initial Release	

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